CLASS : S.E. COMP

SUBJECT : DEL

EXPT. NO.: 7

DATE:

TITLE : Flip Flop Conversion

OBJECTIVE : To design and realize flip flop conversion

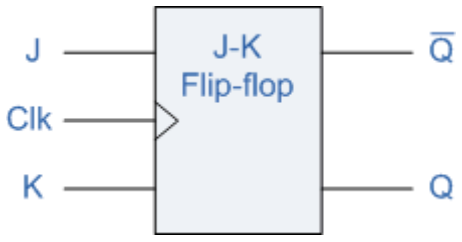
APPARATUS:

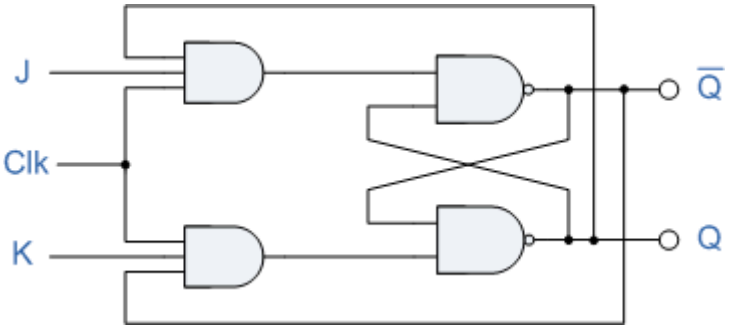
Digital-Board, IC 7476(Dual JK), 7408 (AND-gate), 7432 (OR-gate), D Flip flop

Theory:

JK Flip-Flop:

The JK Flip-Flop is basically a Gated SR Flip-Flop with the addition of clock input circuitry that prevents the il egal or invalid output that can occur when both input S equal's logic level "1" and input R equals logic level "1". The symbol for a JK Flip-flop is similar to that of an SR Bi stable as seen in the previous tutorial except for the addition of a clock input.

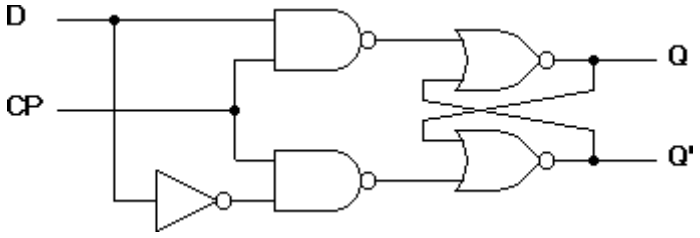




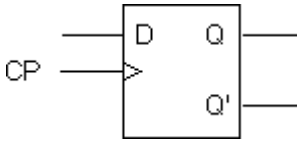
The Truth Table for the JK Function

J	K	Q	Q	
0	0	0	0	same as for the SR Latch
0	0	1	1	
0	1	0	0	
0	1	1	0	
1	0	0	1	
1	0	1	1	
1	1	0	1	toggle action
1	1	1	0	

D Flip-Flop:

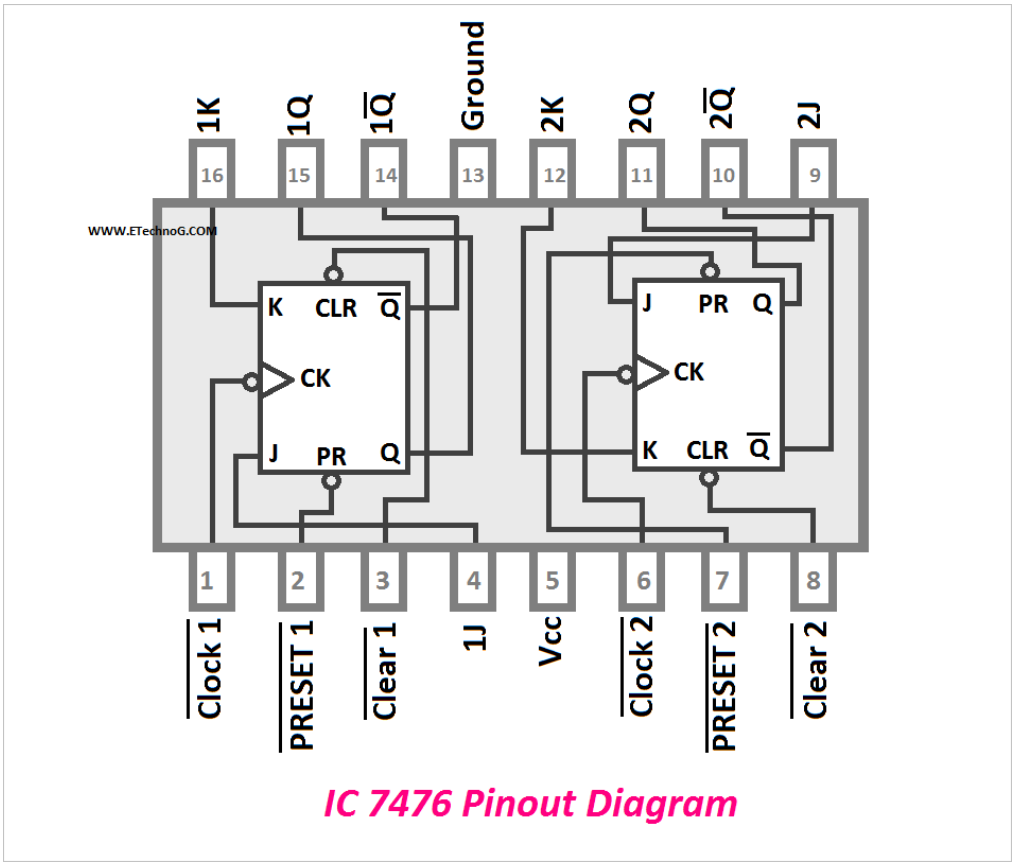


It has only one input, D-input or data input. From the truth table it is clear that output Q_{n+1} at the end of clock pulse equals the input Dn before the clock pulse. It means input appears at the output at the end of the clock pulse. The output is delayed and hence the name is D Flip-flop.



Input D_n	Output Q_{n+1}
0	0
1	1

Pin Diagram



IC 7476 Pinout Diagram

PROCEDURE:

1] Make connections as per the logic circuit for D flip flop to SR Flip flop and verify the truth table.

Conversion of D Flip Flop to SR Flip Flop

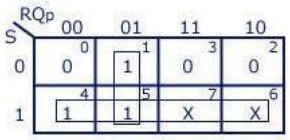
D is the actual input of the flip flop and S and R are the external inputs. Eight possible combinations are achieved from the external inputs S, R and Qp. But, since the combination of S=1 and R=1 are invalid, the values of Qp+1 and D are considered as "don't cares". The logic diagram showing the conversion from D to SR, and the K-map for D in terms of S, R and Qp are shown below.

D Flip Flop to S-R Flip Flop

Conversion Table

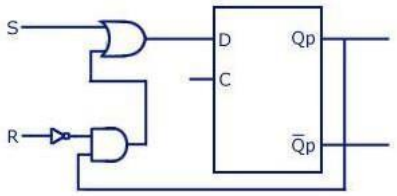
S-R Inputs S	R	Outputs Qp	Qp+1	D Input
0	0	0	0	0
0	0	1	1	1
0	1	0	0	0
0	1	1	0	0
1	0	0	1	1
1	0	1	1	1
1	1	Invalid		Dont care
1	1	Invalid		Dont care

K-map



$D = S+\bar{R}Q_n$

Logic Diagram



2] Make connections as per the logic circuit for JK flip flop to T Flip flop and verify the truth table.

JK Flip Flop to T Flip Flop

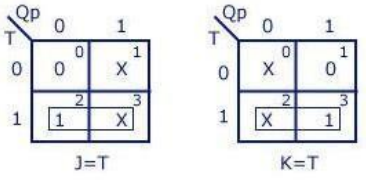
J and K are the actual inputs of the flip flop and T is taken as the external input for conversion. Four combinations are produced with T and Qp. J and K are expressed in terms of T and Qp. The conversion table, K-maps, and the logic diagram are given below.

J-K Flip Flop to T Flip Flop

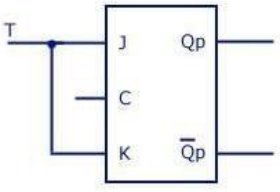
Conversion Table

T Input	Outputs Qp	Qp+1	J-K Inputs J	K
0	0	0	0	X
0	1	1	X	0
1	0	1	1	X
1	1	0	X	1

K-maps



Logic Diagram



Logic Gates / MSI Device required for Implementation:

Sr.No.	Title	Name of the IC	Number of Gates required	IC Required
01	**Conversion of D Flip Flop to SR Flip Flop**			
02	**JK Flip Flop to T Flip Flop**			

Conclusion:

REFFRENCE:

1. **R.P.Jain "Modern Digital Electronics" TMH 4th Edition**
2. **D.Leach,Malvino,Saha,"Digital Principles and Applications",TMH**

Subject teacher
Sign with Date Remark