CLASS : S.E. COMP

SUBJECT : DEL

EXPT. NO.: 7 **DATE :**

TITLE **:** Mod N asynchronous and synchronous counter (IC 7490)

OBJECTIVE:

- To design and implement mod - 10, mod - 7 BCD counter using IC 7490.

APPARATUS:

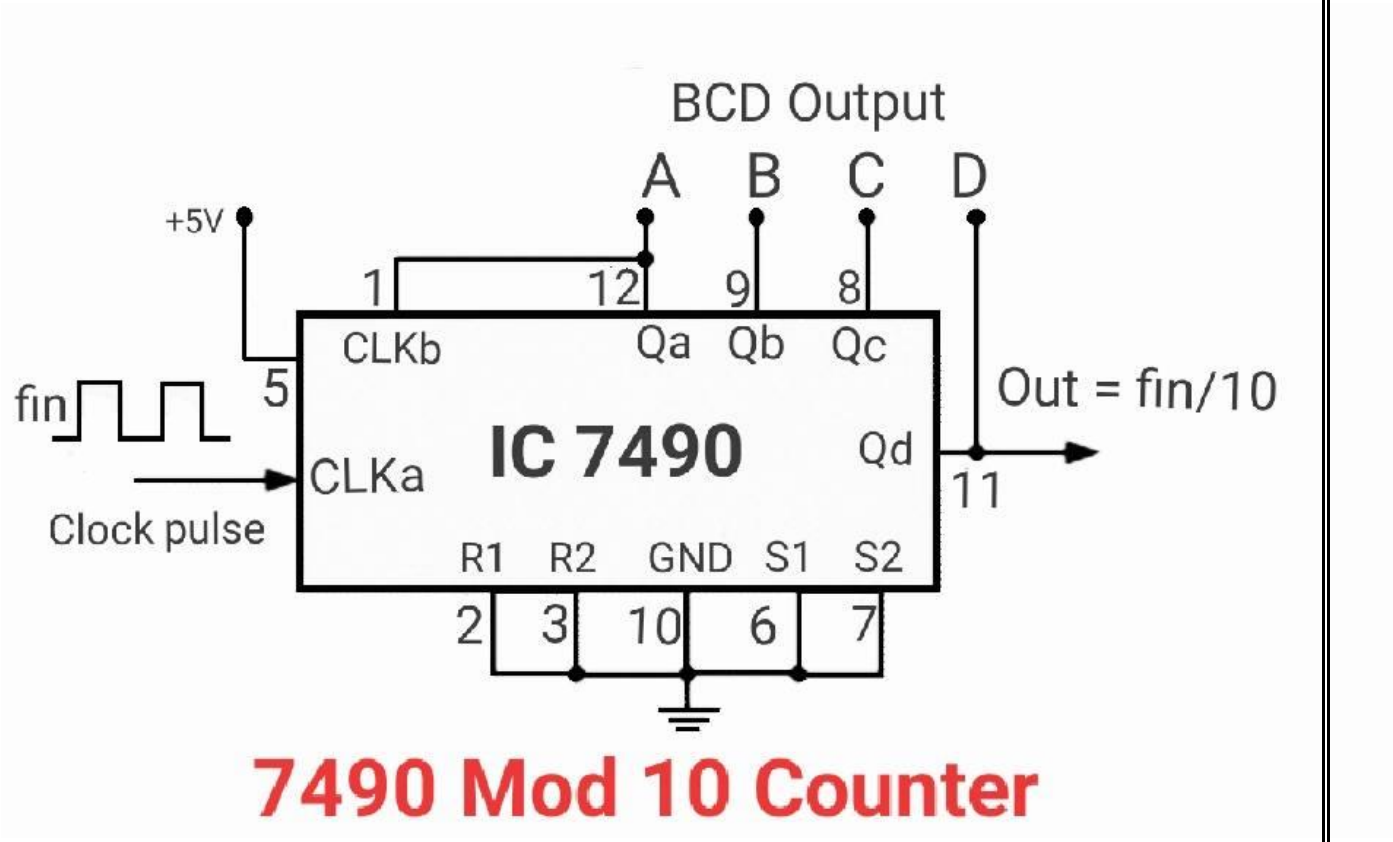
Digital-Board, IC 7490, IC 74191, basic gates.

THEORY:

IC 7490 is a TTL MSI (medium scale integration) decade counter. It contains 4 master slave flip flops internally connected to provide MOD-2 i.e. divide by 2 and MOD-5 i.e. divide by 5 counters. MOD-2 and Mod-5 counters can be used independently or in cascading.

It is a 4-bit ripple type decade counter. The device consists of 4-master slave flip flops internally connected to provide a divide by two and divide by 5 sections. Each section has a separate clock i/p to initiate state changes of the counter on the high to low clock transition n.

Pin Diagram of IC 7490:



Procedure:

1] Make connections for the logic circuit Mod 10 Counter.

Design of MOD-10 counter using IC 7490:

- The QA o/p the first flip flop is connected to the i/p B which is clock i/p of internal MOD-5 ripple counter. Due to cascading of Mod-2 and Mod-5 counters, the overall configuration the decade counters count from 0000 to 1001. After 1001 mod-5 resets to 0000 and next count after 1001 is 0000.
- When QA o/p is connected to B i/p, we have the Mod-2 counter followed by Mod-5 counter. The count sequence obtained is shown in the table.
- It may be noted that QA changes from 0 to 1 the state of Mod-5 counter doesn't change, whereas when QA changes from 1 to 0 the Mod-5 counter goes to the next state.

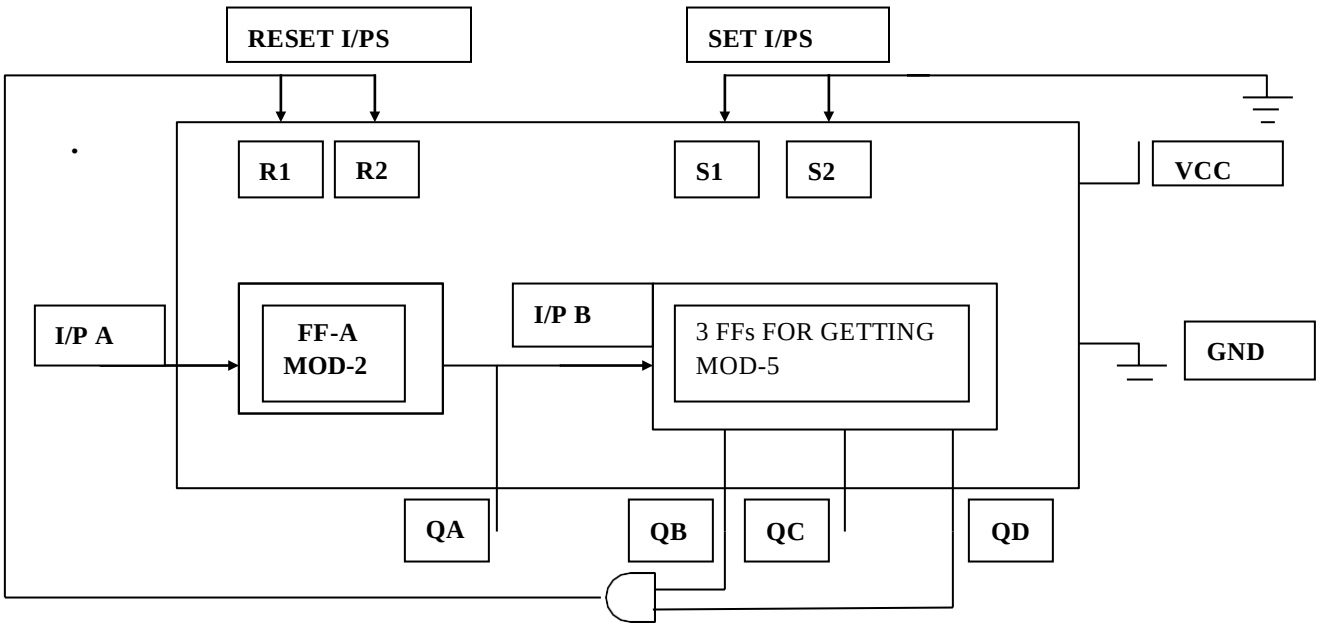
Function Table of MOD-2 counter:

Input A clock	Output	Count
↓	0	0
↓	1	1

Function Table of MOD-5 counter:

Input B clock	Output			Count
	QD	**QC**	**QB**	
↓	**0**	**0**	**0**	**0**
↓	**0**	**0**	**1**	**1**
↓	**0**	**1**	**0**	**2**
↓	**0**	**1**	**1**	**3**
↓	**1**	**0**	**0**	**4**

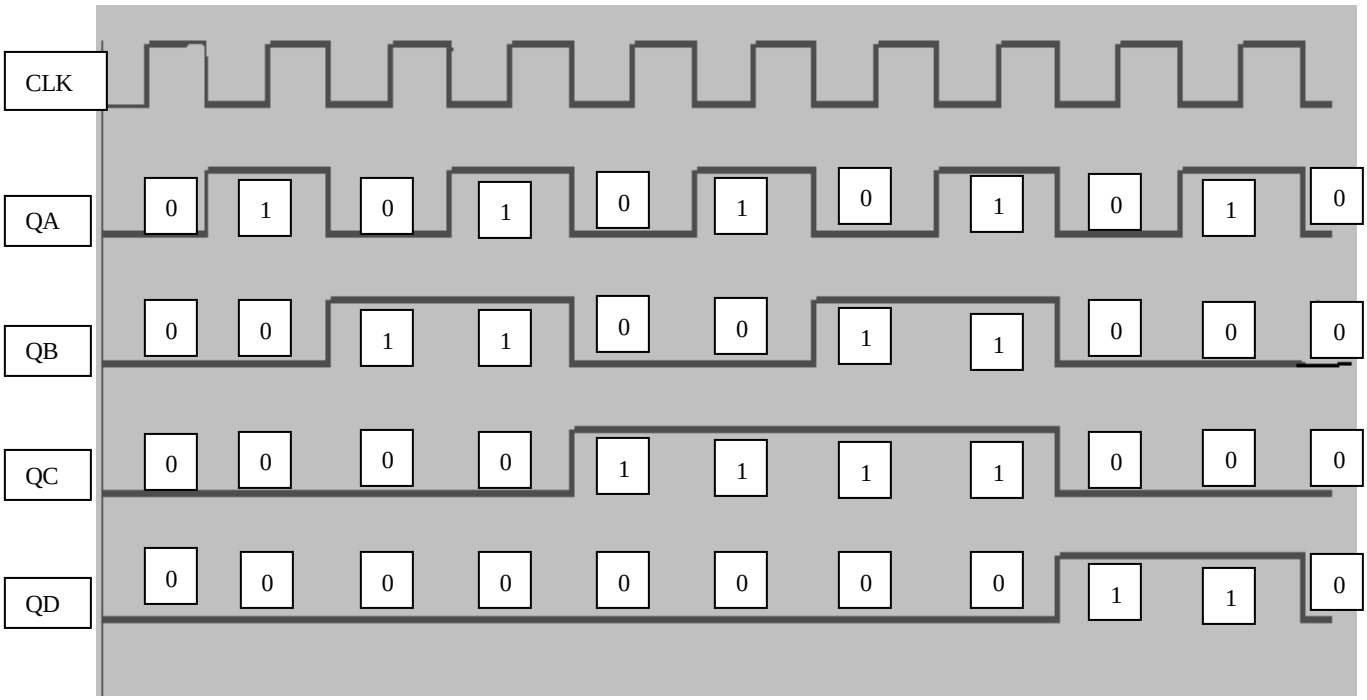
Diagram



Function table:

I/p clock	Output				Count
	QD	QC	QB	QA	
↓	0	0	0	0	0
↓	0	0	0	1	1
↓	0	0	1	0	2
↓	0	0	1	1	3
↓	0	1	0	0	4
↓	0	1	0	1	5
↓	0	1	1	0	6
↓	0	1	1	1	7
↓	1	0	0	0	8
↓	1	0	0	1	9

Timing diagram of mod10:



2] Make connections for the logic circuit Mod-7 Counter.

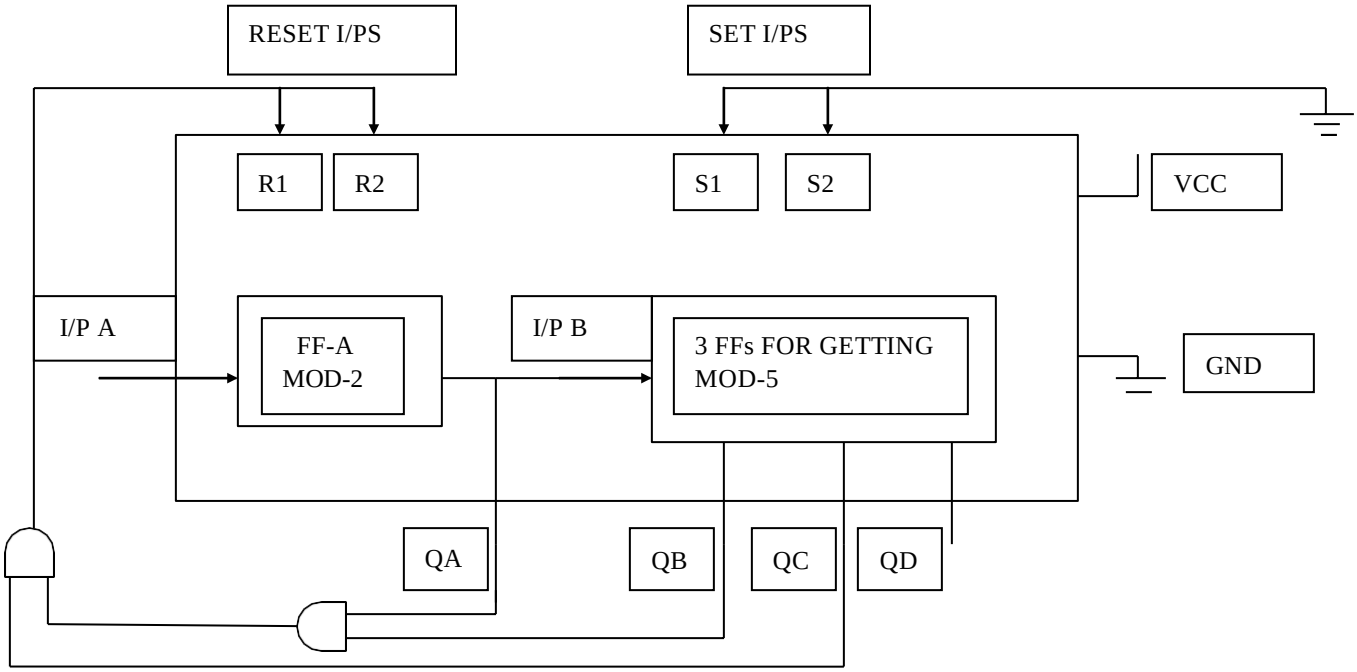
Design of Mod-7 Counter using IC 7490:

- Mod-7 counter counts through seven states from 0 to 6 counters and it should reset as soon as the count becomes 7.
- The o/p of reset logic should be 1 corresponding to invalid states. The reset logic o/p should be applied to pin 2 and 3.

Truth Table of Reset Logic:

QD	QC	QB	QA	Y
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	1
1	0	0	1	1

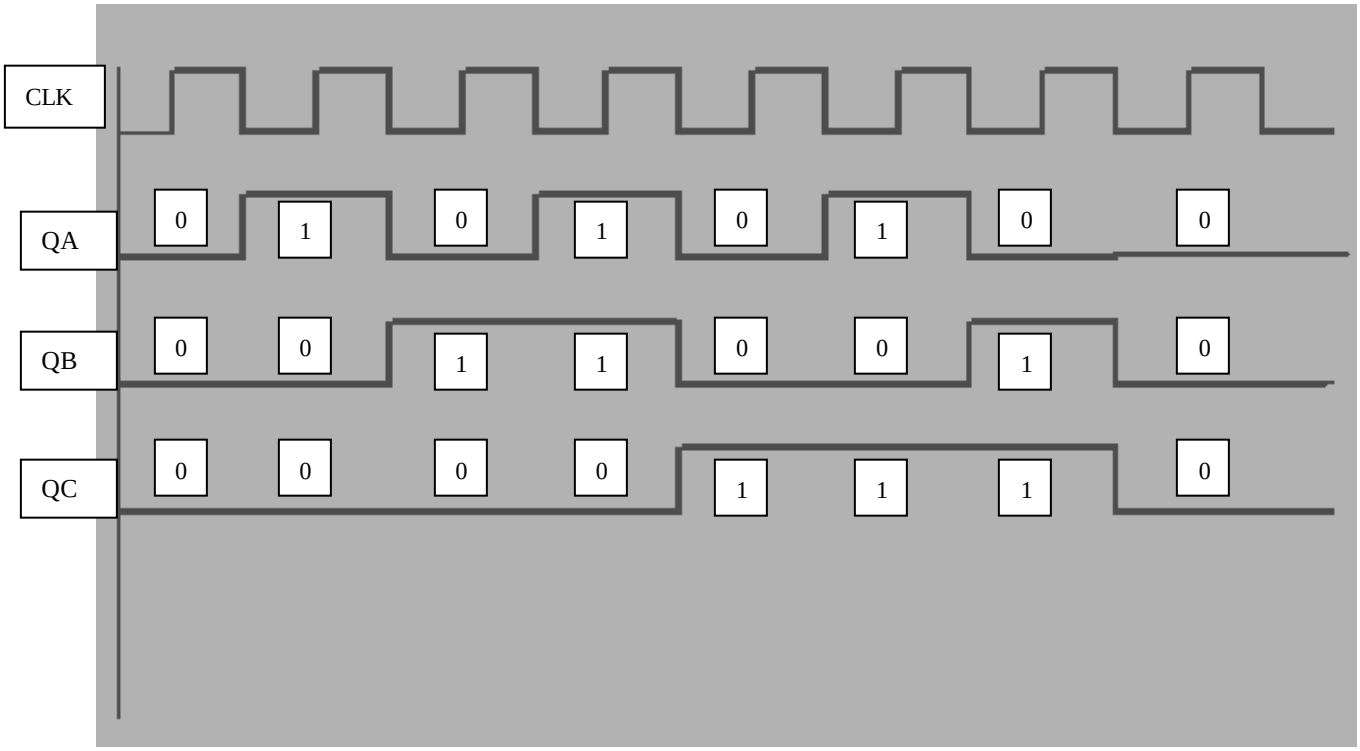
Diagram:



Function table:

I/p clock	Output				Count
	QD	**QC**	**QB**	**QA**	
↓	**0**	**0**	**0**	**0**	**0**
↓	**0**	**0**	**0**	**1**	**1**
↓	**0**	**0**	**1**	**0**	**2**
↓	**0**	**0**	**1**	**1**	**3**
↓	**0**	**1**	**0**	**0**	**4**
↓	**0**	**1**	**0**	**1**	**5**
↓	**0**	**1**	**1**	**0**	**6**

Timing diagram of mod7:



Logic Gates / MSI Device required for Implementation:

Sr.No.	Title	Name of the IC	Number of Gates required	IC Required
01				
02				

Conclusion:

REFFRENCE:

1. **R.P.Jain "Modern Digital Electronics" TMH 4th Edition**
2. **D.Leach,Malvino,Saha,"Digital Principles and Applications",TMH**

Subject teacher
Sign with Date Remark