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| **LAB EXPT.**  **NO** | **PROBLEM STATEMENT** | **LAST DATE FOR COMPLETION** |
|  | **Group A** |  |
| **1** | To Realize Full Adder/ Subtractor using a) Basic Gates and b) Universal Gates | 3rd week of Aug 2023 |
| **2** | Design and implement Code Converters-Binary to Gray and BCD to Excess-3 | 4th week of Aug 2023 |
| **3** | Design BCD Adder and Binary Adder using 4-bit Binary Adder (IC 7483) and Realization of Binary Adder using IC 7483. | 1st week of Sep 2023 |
| **4** | Realization of Boolean Expression for suitable combination logic using MUX 74151 /74153, DMUX 74154/74138 | 2nd week of Sep 2023 |
| **5** | To Verify the truth table of two-bit comparators using logic gates. | 3rd week of Sep 2023 |
| **6** | Design and Implement Parity Generator and checker using EX-OR. | 3rd Week of Sep 2023 |
|  | **Group B** |  |
| **7** | Design and Realization: Flip Flop conversion | 4th week of Sep 2023 |
| **8** | Design of 2 bit and 3-bit Ripple Counter using MS JK flip-flop. | 1st week of Oct 2023 |
| **9** | Design of Synchronous 4 bit Up and Down Counter using IC 74191. | 2nd week of Oct 2023 |
| **10** | Realization of Mod -N counter using (Decade Counter IC 7490). | 3rd week of Oct 2023 |
| **11** | Design and implement Sequence generator (for Prime Number/odd and even) using MS JK flip-flop. | 2st week of Nov 2023 |
| **12** | Design and implement Sequence detector using MS JK flip-flop. | 4th week of Nov 2023 |
|  | **Group C** |  |
| **13** | Study of Shift Registers (SISO, SIPO, PISO, PIPO) | Last week of Nov 2023 |
| **14** | Design of ASM chart using MUX controller Method. | Last week of Nov 2023 |

SCHEDULE OF LAB EXPERIMENTS

DEPARTMENT: Computer Engineering CLASS: S.E

ACADEMIC YEAR: 2023-24 SEMESTER: I

SUBJECT: DIGITAL ELECTRONICS LABORATORY

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Subject Coordinator Head of Department

Mrs. A. D. Bundele Dr. G V Kale