1cm² Sensor Designs

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Outline

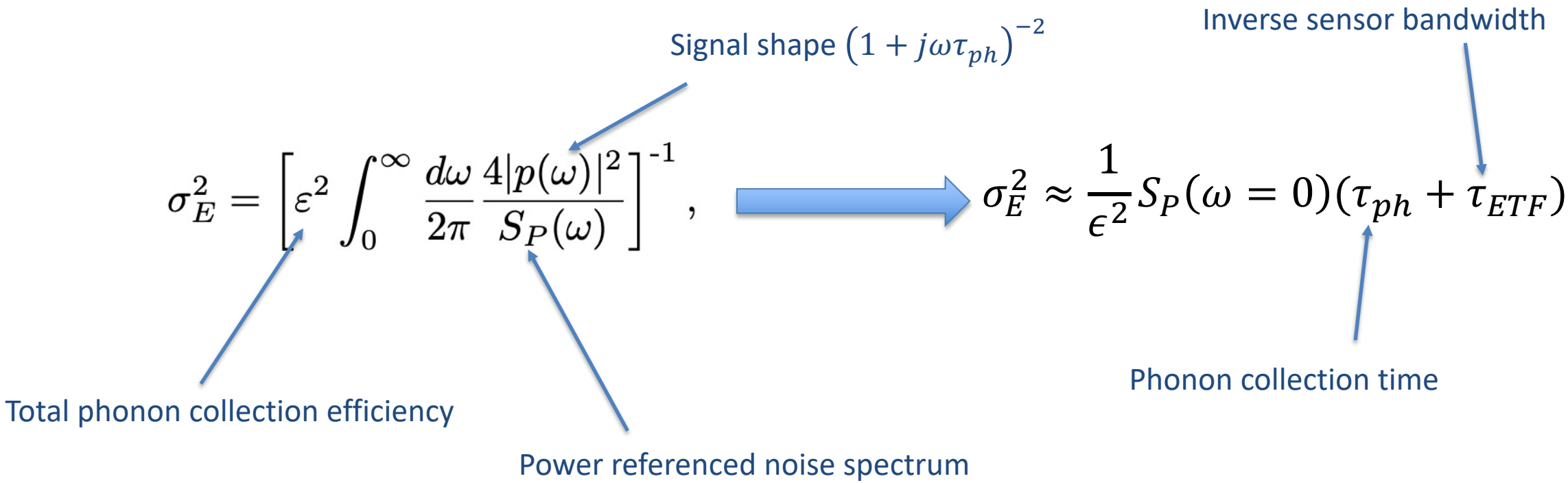
- QET Design Considerations
  - How does Energy resolution scale with Tc and Al Surface Coverage
- Optimization of low coverage QET devices
  - 4,1,0.25
- Detector mask designs

Low Coverage Design Considerations

The following arguments are using toy models for illustrative purposes

Goal: Energy Sensitivity

The absolute most important design driver is energy sensitivity!

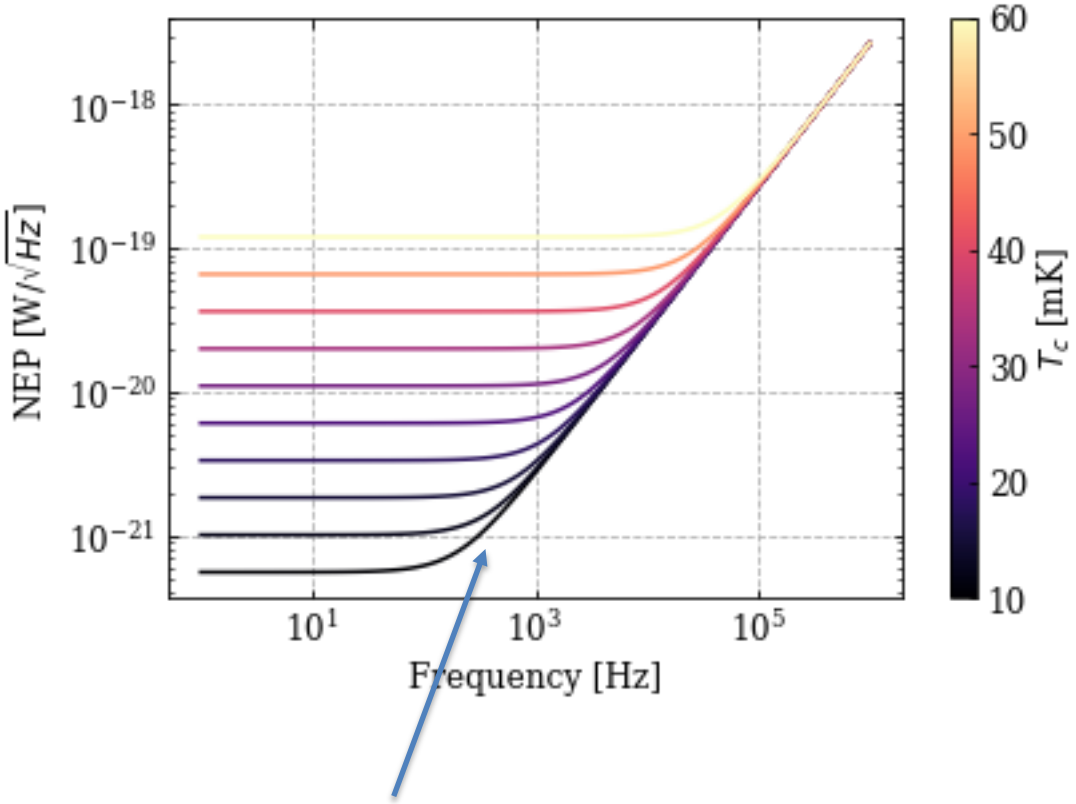


Breaking Down the Noise

Considering only the thermal fluctuation noise between the sensor and the bath (TFN), the power noise (NEP^2) is given by

$$S_P(\omega) \approx 4nk_B F \Sigma_{ep} N_{TES} V_{TES} T_c^{n+1}(1+\omega^2\tau_{ETF}^2)$$

$$\tau_{ETF} \approx \sqrt{\frac{2}{n}\frac{f_{sc}\gamma}{\alpha\Sigma_{ep}}}\,T_c^{2-n}$$ (ignoring contributions from resistance, etc)



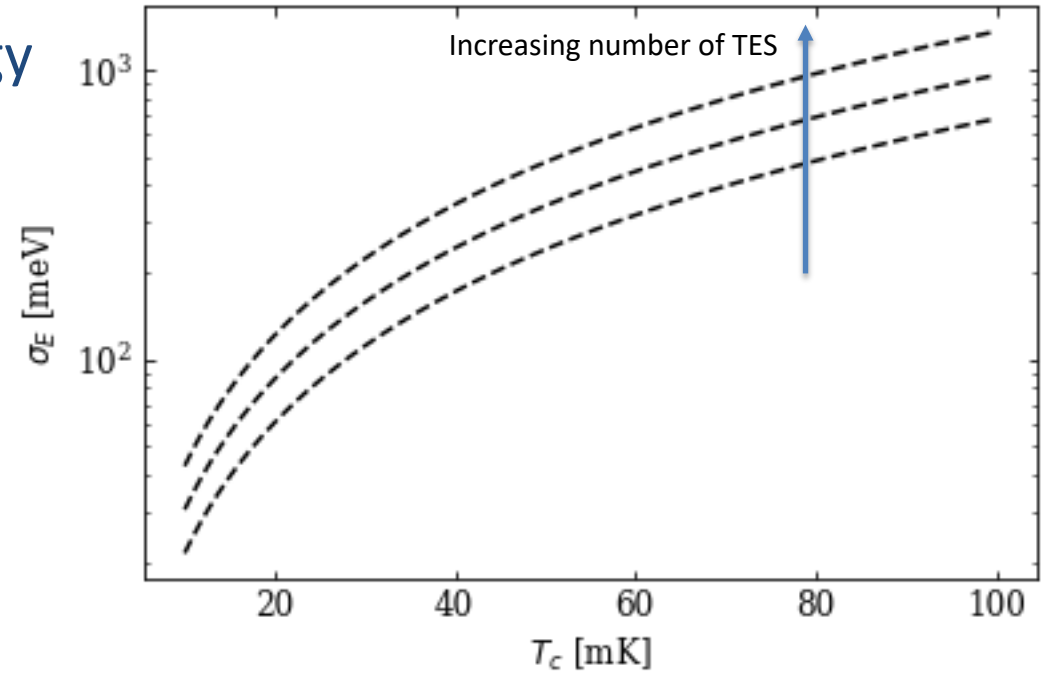
In-band noise decreases faster with Tc than bandwidth

Ignoring the Phonons…

In the limit that $\tau_{ph} \ll \tau_{ETF}$, the TES energy resolution scales as

$$\sigma_E^2 \approx \frac{1}{\epsilon^2} S_P(\omega = 0)\tau_{ETF}$$

$$\sigma_E^2 \propto N_{TES} V_{TES} T_c^3$$



Decreasing volume/number of TES and Tc has huge benefits

Phonon Collection Time

What if we don't ignore the phonon collection time? Taking the opposite limit, consider only the phonon collection time (ie $\tau_{ph} \gg \tau_{ETF}$)

$$\sigma_E^2 \approx \frac{1}{\epsilon^2} S_P(\omega = 0)\tau_{ph}$$

$$\tau_{ph} \propto \frac{V_{detector}}{N_{TES}A_{QET}}$$

$$\sigma_E^2 \propto \frac{1}{\epsilon^2}\Sigma_{ep}V_{TES}V_{detector}T_c^{n+1}$$

In this limit, the Tc dependence is even stronger!

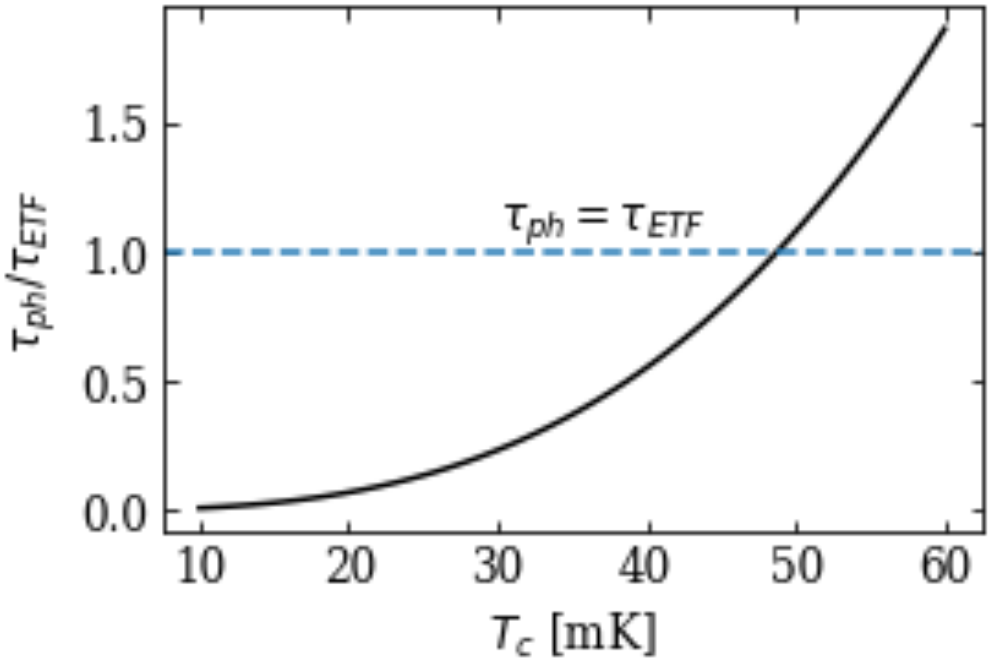
Note: Once we are in this limit, there is no longer a strong dependence on the number of TESs

How do we stay in the limit that $\tau_{ph} > \tau_{ETF}$?

As we decrease the Tc, the sensor bandwidth gets smaller, ie τ_{ETF} gets bigger

We need to decrease the number of TESs and/or decrease the size of the QETs (decrease surface coverage)

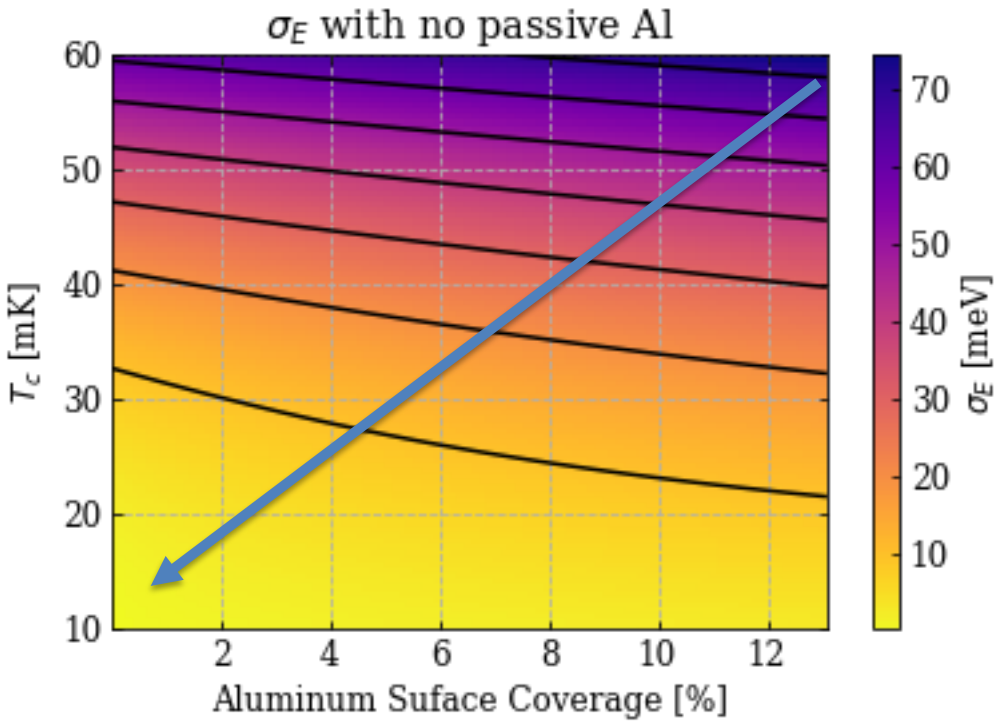
$$\tau_{ph} \propto \frac{V_{detector}}{N_{TES} A_{QET}}$$

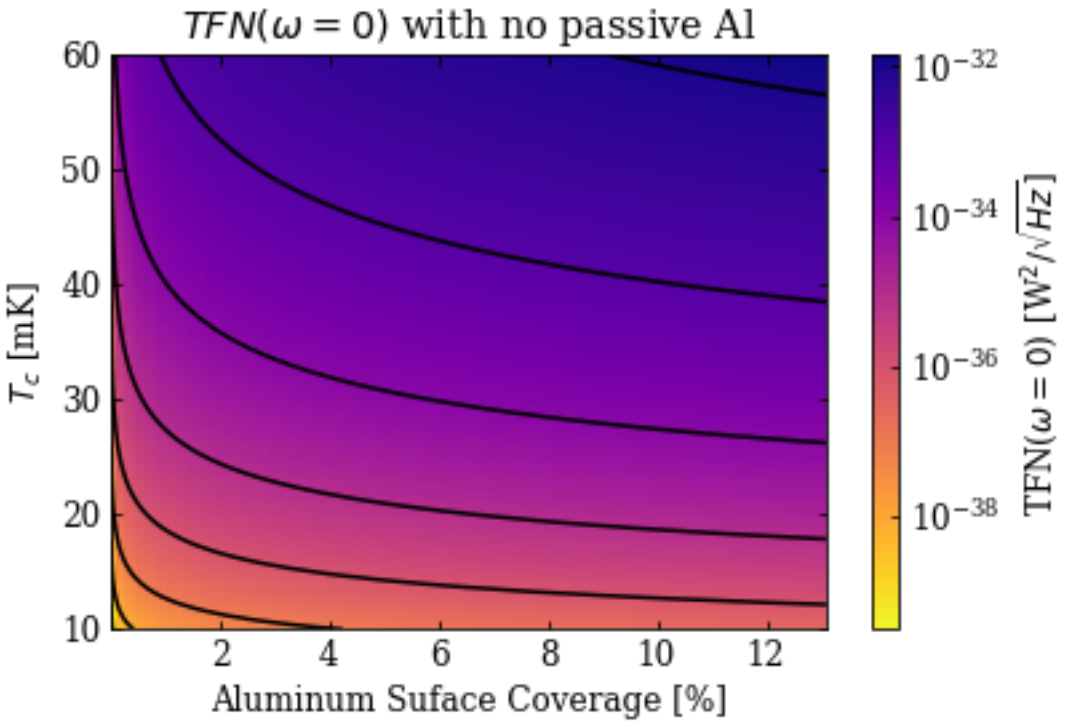


A good way to think about this: As the sensor slows down by decreasing Tc, you need to give it more time to collect all the phonons

Combining Tc and Surface Coverage

Ignoring the effects of passive Aluminum, the optimum design is always towards lower Tc and lower surface coverage



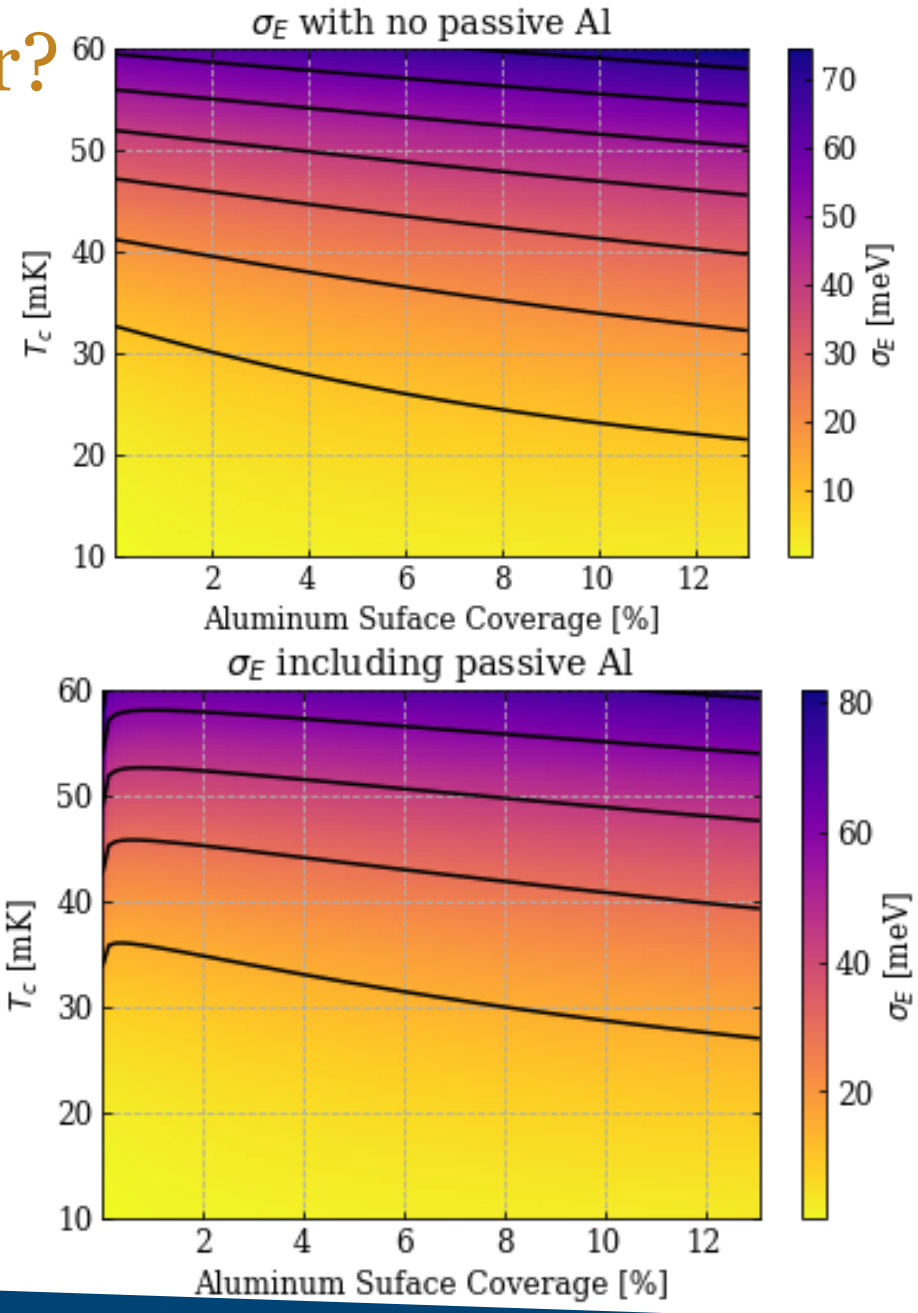


Is Lower Surface Coverage Always Better?

Until now, we have ignored the phonon collection efficiency. Keeping all other QET design factors the same, this scales as

$$\epsilon \propto \frac{Active\ Al\ area}{(Active + Passive)\ Al\ area}$$

Even though the noise improves for lower coverage designs, the signal efficiency eventually gets killed by the passive aluminum.

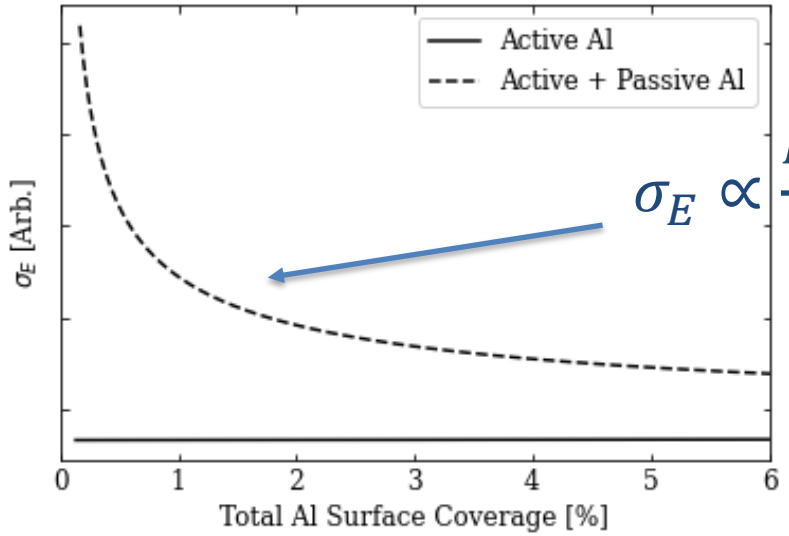


Passive Surface Area

For low coverage devices, the passive Aluminum is VERY important!

For fixed surface coverage: High Tc

$\tau_{ph} \gg \tau_{ETF}$

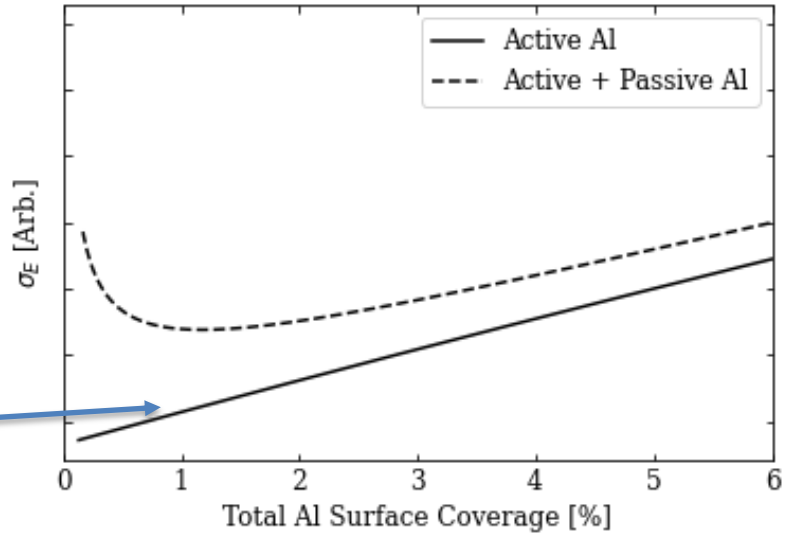


$$\sigma_E \propto \frac{N_{TES}+1}{N_{TES}}$$

$$\sigma_E \propto N_{TES}$$

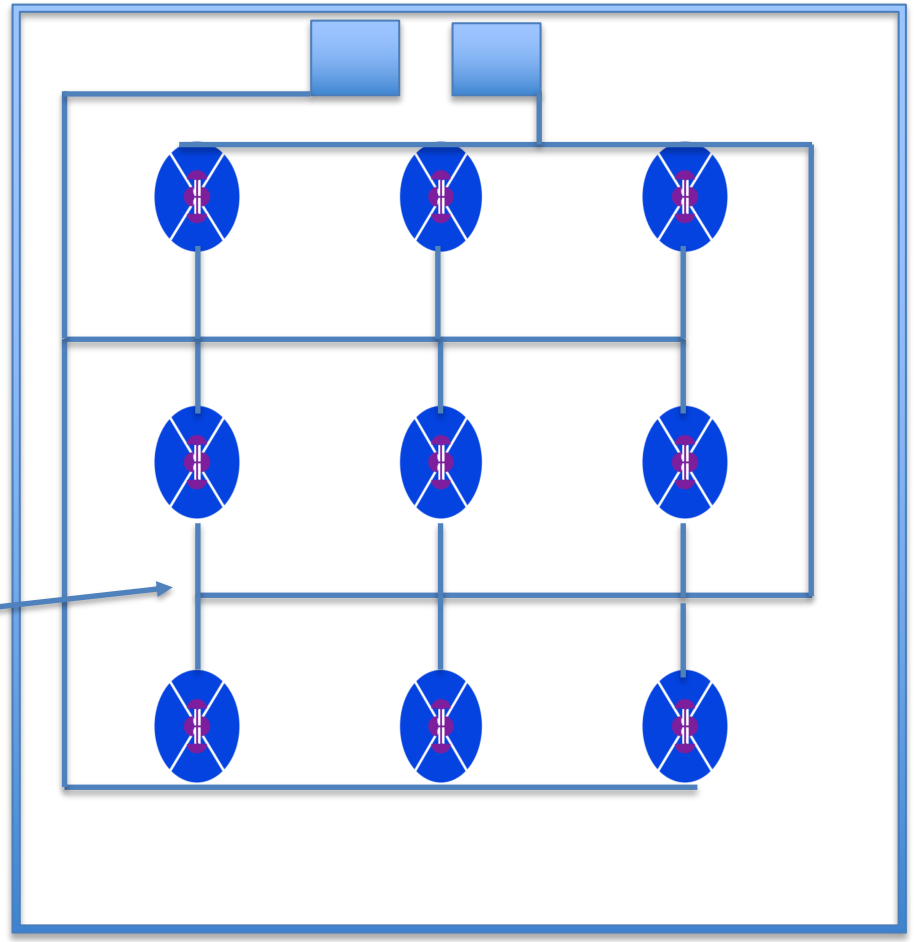
For fixed surface coverage: Low Tc

$\tau_{ph} \sim \tau_{ETF}$



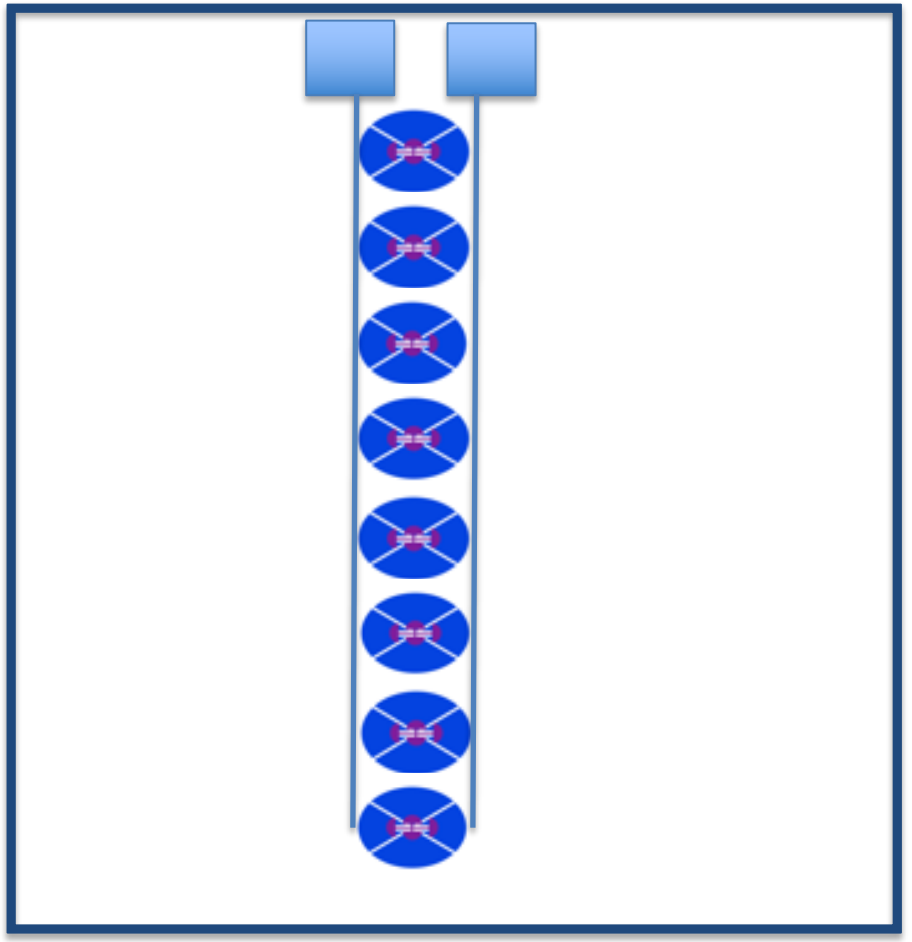
Where Does the Passive Area Come From?

- Contributions to passive area are:
  - Alignment Marks
    - Can be placed on different chips since this is fabricated on a full wafer
  - Bonding pads
    - Small area ~size of a few QETs
  - Au thermalization pad
    - Small area ~size of a few QETs
  - Bias Rails
    - Biggest offender!



Close Packed Design

- Reduce passive Al by ‘close packing’ the design.
- Greatly improve energy resolution
- Comes at the cost of introducing position dependance



Dependence on Rn

- We don't get to change the TES parameters and number of TES's for free

$$N_{TES} = \frac{\rho_W}{R_N} \frac{\ell_{TES}}{w_{TES} h_{TES}}$$

$$SA \propto \ell_{fin}^2 N_{TES} \propto \frac{\ell_{fin}^2 \ell_{TES}}{R_N}$$

- Since QET's are in parallel, larger normal resistance means fewer QETs. Fewer QET's means lower surface coverage
- Ntes is set by requirements on the normal resistance
- Choose normal resistance such that $R_0 \approx 30\% R_N$ is >>5-10x R_ℓ, but not too large that the SQUID noise is significant

Wafer Layout - Devices

- High coverage device for Dan McKinsey
  - 50% Al coverage
- Low coverage devices for SPICE
  - 4%, 1%, 0.25% Al coverage devices for very low energy resolution and to study phonon collection time
  - Primarily single channel, but a few 2 channel devices for studying thermal conductance(s)
- TES/QET test structures
  - A few chips for noise and QET dynamics studies
    - Likely very similar to original QP devices

QET Optimization

- For real optimization, consider all intrinsic noise sources + model the phonon/quasi-particle collection efficiencies in the overlap regions
- To keep the surface coverage fixed, we use the following objective function

$$\mathcal{L} = \frac{1}{\epsilon^2 \int_0^\infty \frac{dw}{2\pi} \frac{4|p(\omega)|^2}{S_P(\omega)}} [1 + |SA_{actual} - SA_{target}|]$$

- Grid search over number of fins [2-6], and Rn:
  - Allowing TES length, Al fin length, W/Al overlap length to vary
- Optimize assuming a W/Al effective volume factor of both 0.13% (expected) and 0.45% (measured). Choose average of optimum parameters between the two cases
- Code: https://github.com/ucbpylegroup/DarkOpt

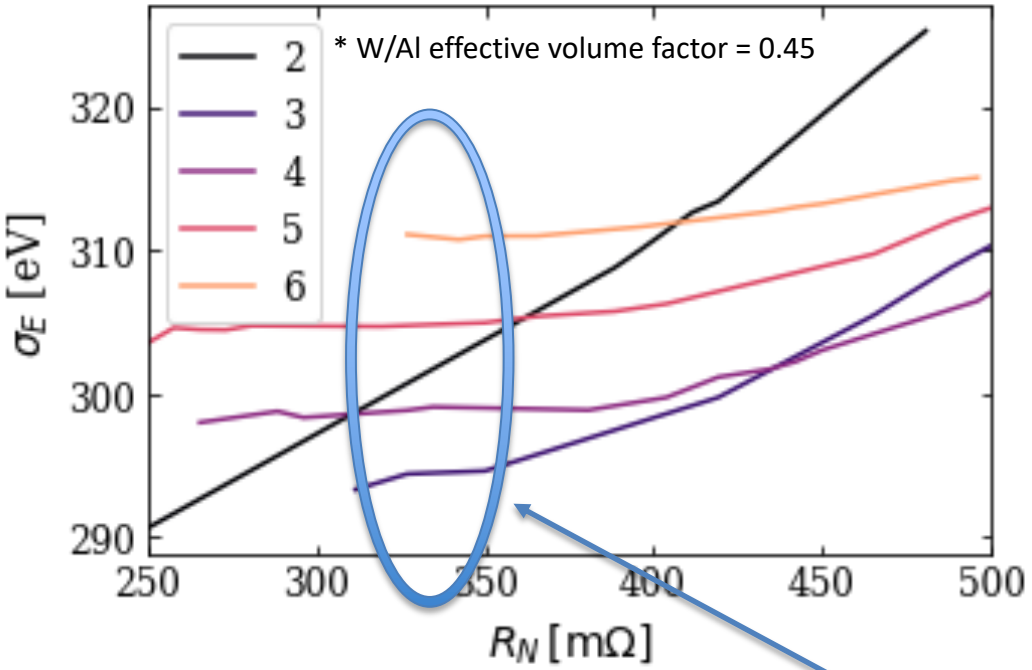
Low Coverage Devices

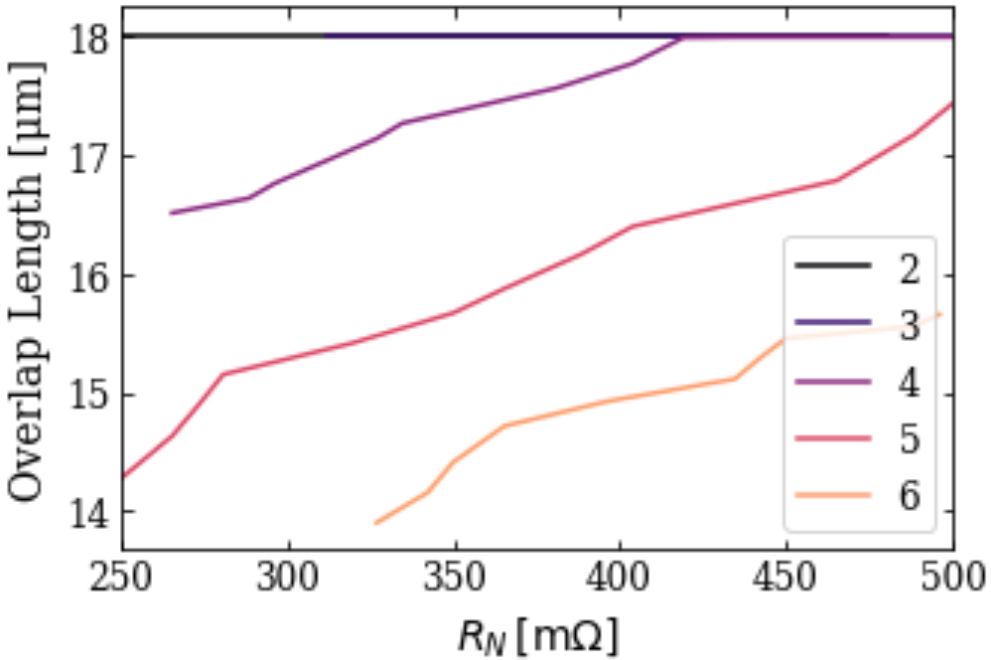
Devices are optimized assuming Tc is 40mK. However, the lower coverage designs will only become beneficial for much lower Tc's

4% Coverage Device

- Optimize for normal resistance
  - Keep surface coverage fixed and optimize free QET params as a function of Rn

Smaller number of fins forces the overlap region to be large. We don't yet have a good understanding of large overlap lengths. We should exclude the 2 and 3 fin designs for this device





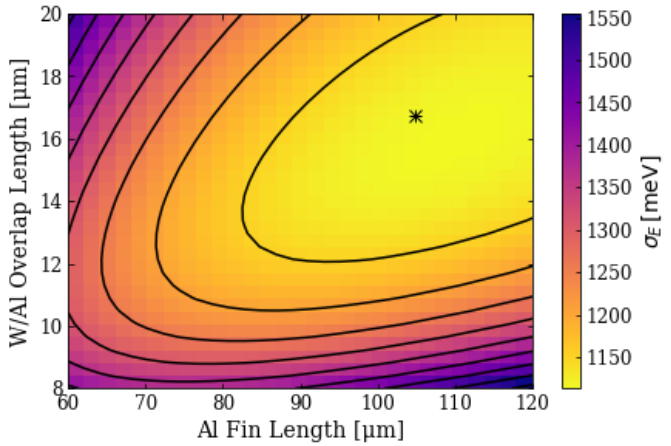
Choose Rn around 300-350, and 5 fin design

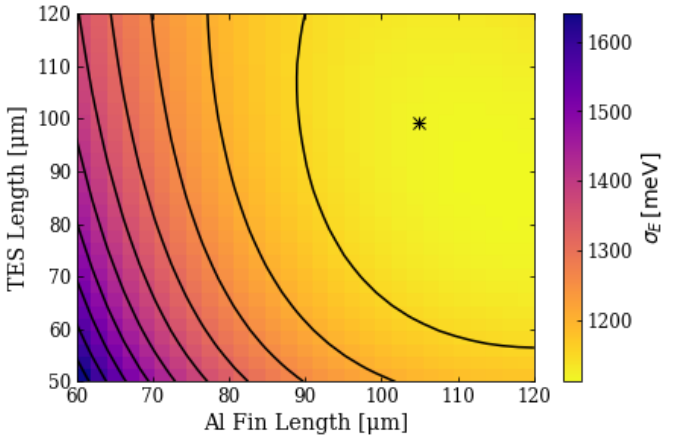
4% Coverage Device

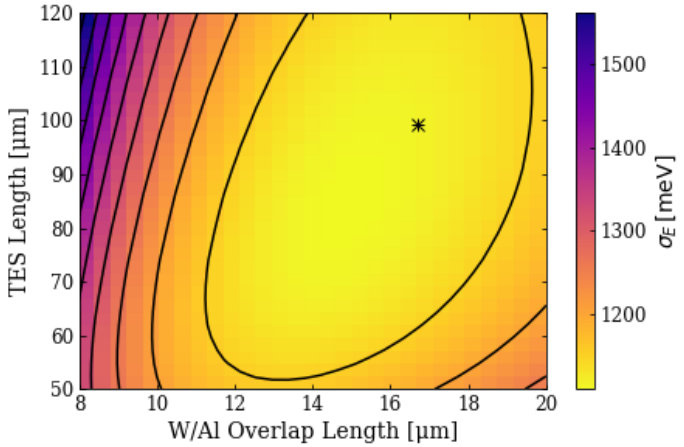
σ_E	303 [meV] (Tc=40mK) 1117.5 [meV] (Tc=70mK)
TES Length	99.1 [μm]
TES Width	2.5 [μm]
TES Thickness	40 [nm]
Al Fin Length	104.8 [μm]
Al Fin Thickness	600 [nm]
Number of Fins	5
W/Al Overlap Length	16.7 [μm]
Total Al Surface Coverage	4.060 [%]
Active Al	3.705 [%]
Passive Al	0.356 [%]
τ_{ETF}	55 [μs] (Tc=40mK) 15 [μs] (Tc=70mK)
τ_{ph}	24.04 [μs]
Absolute Phonon Collection Efficiency	23.79 [%]
Number of TESs	293
R_N	325.0 [mΩ]

Vary Parameters but fixed Number of TESs (fixed Rn)

Plots shown at bandwidth matched Tc of 70mK

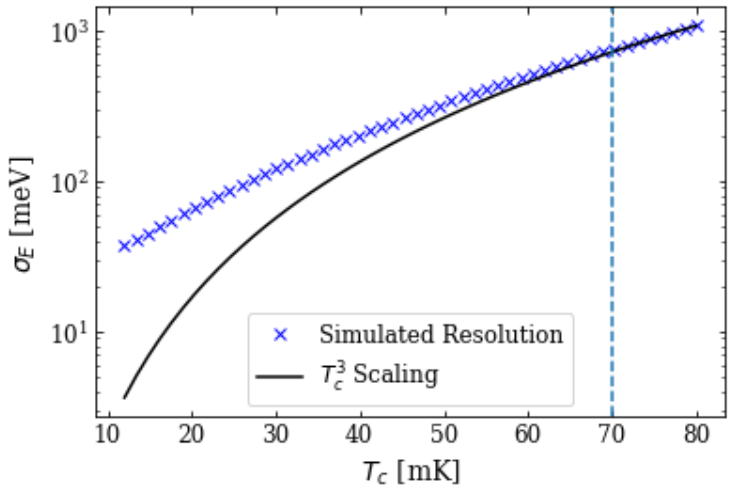






Note: plots are not always at optimum because the parameters are the average of two different Fin volume efficiencies

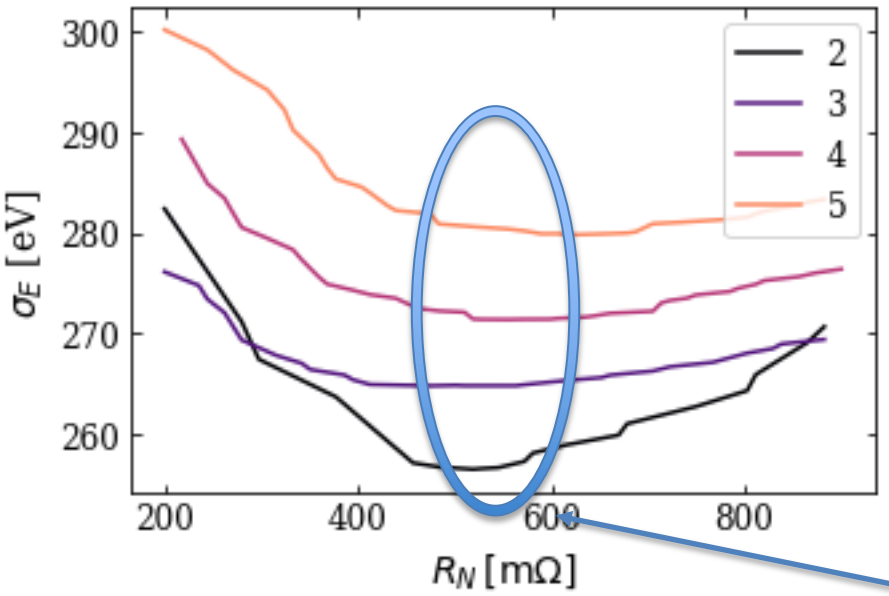
Bandwidth matched at $T_c \approx 70$ mK



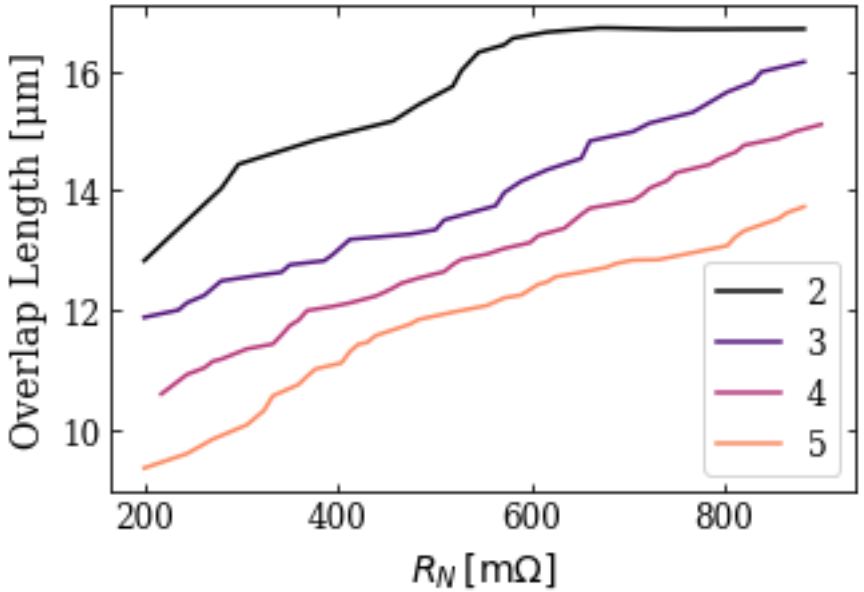
1% Coverage Device

- Optimize for normal resistance
  - Keep surface coverage fixed and optimize free QET params as a function of Rn

* W/Al effective volume factor = 0.45



Lower coverage device is forcing us to raise the normal resistance of the device



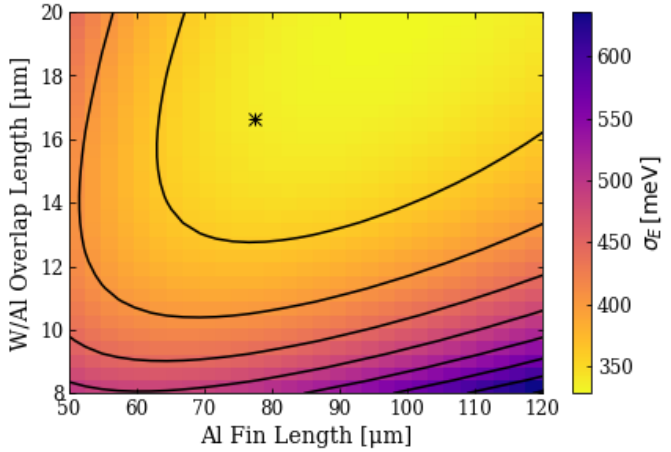
Choose Rn around 500-600, and 2 or 3 fin design

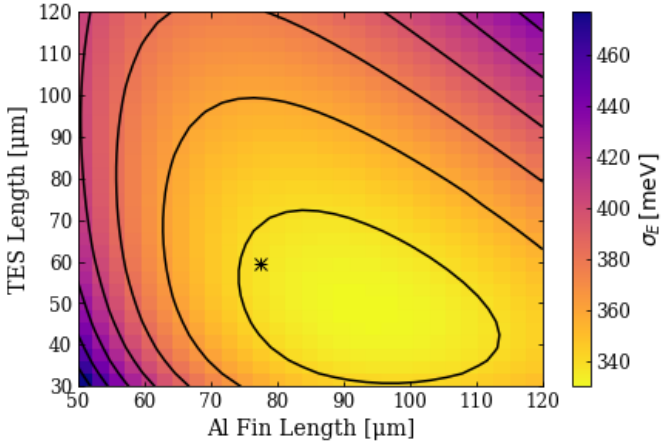
1% Coverage Device (2 Fin)

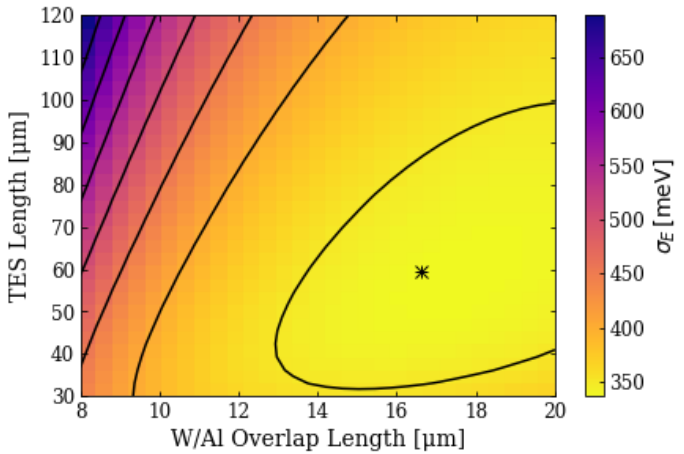
σ_E	260.3 [meV] (Tc=40mK) 337.1 [meV] (Tc=45mK)
TES Length	59.6[μm]
TES Width	2.5 [μm]
TES Thickness	40 [nm]
Al Fin Length	77.5 [μm]
Al Fin Thickness	600 [nm]
Number of Fins	2
W/Al Overlap Length	16.6 [μm]
Total Al Surface Coverage	0.949[%]
Active Al	0.700 [%]
Passive Al	0.248[%]
τ_{ETF}	53.30 [μs] (Tc=40mK) 37.47 [μs] (Tc=45mK)
τ_{ph}	102.90 [μs]
Absolute Phonon Collection Efficiency	17.74 [%]
Number of TESs	115
R_N	550 [mΩ]

Vary Parameters but fixed Number of TESs

Plots shown at bandwidth matched Tc of 45mK

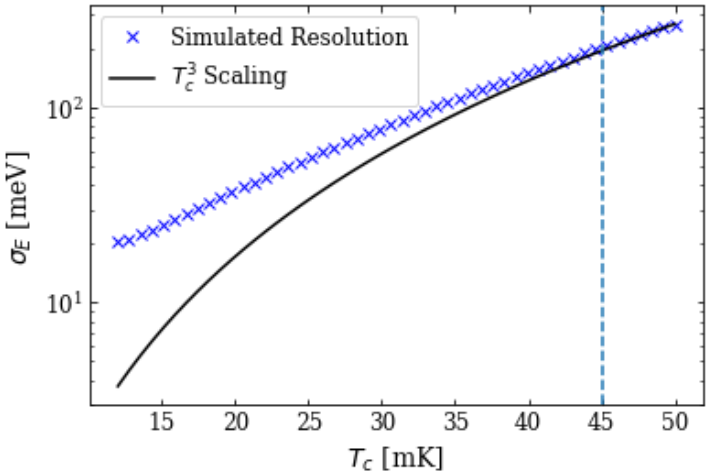






Note: plots are not always at optimum because the parameters are the average of two different Fin volume efficiencies

Bandwidth matched at $T_c \approx 45$ mK

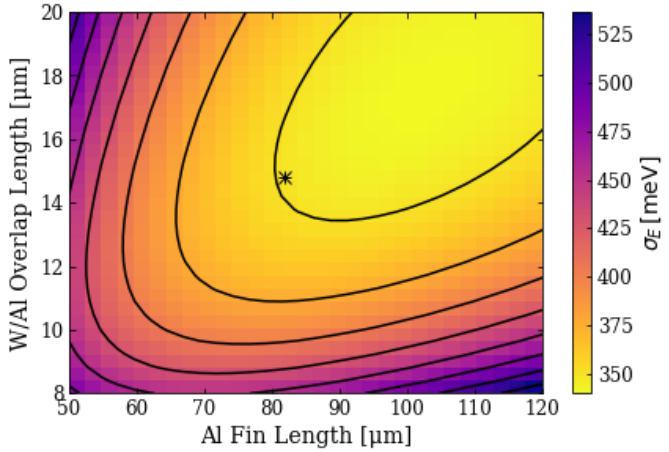


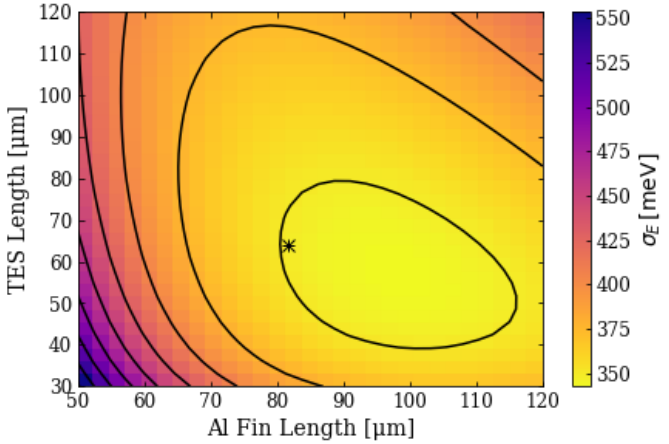
1% Coverage Device (3 Fin)

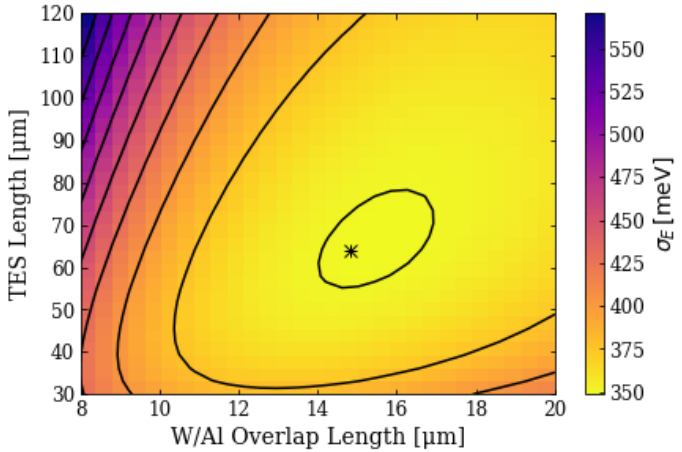
σ_E	259.5 [meV] (Tc=40mK) 348.5 [meV] (Tc=45mK)
TES Length	64.1[μm]
TES Width	2.5 [μm]
TES Thickness	40 [nm]
Al Fin Length	81.7 [μm]
Al Fin Thickness	600 [nm]
Number of Fins	3
W/Al Overlap Length	14.8 [μm]
Total Al Surface Coverage	0.999 [%]
Active Al	0.755 [%]
Passive Al	0.245 [%]
τ_{ETF}	53.30 [μs] (Tc=40mK) 37.24 [μs] (Tc=45mK)
τ_{ph}	97.68 [μs]
Absolute Phonon Collection Efficiency	18.48 [%]
Number of TESs	103
R_N	600 [mΩ]

Vary Parameters but fixed Number of TESs

Plots shown at bandwidth matched Tc of 45mK

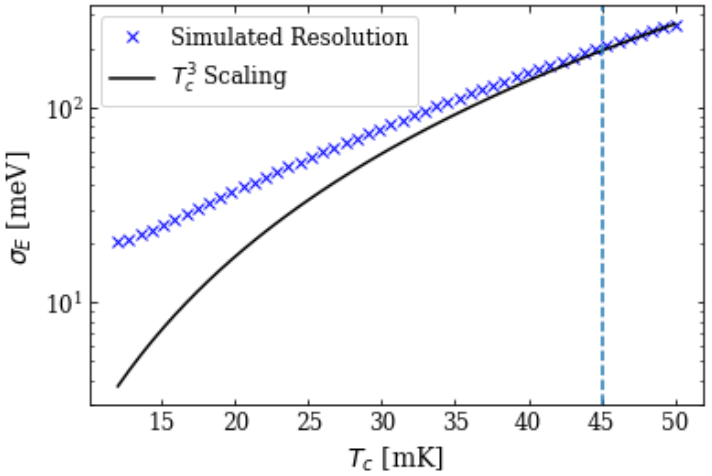






Note: plots are not always at optimum because the parameters are the average of two different Fin volume efficiencies

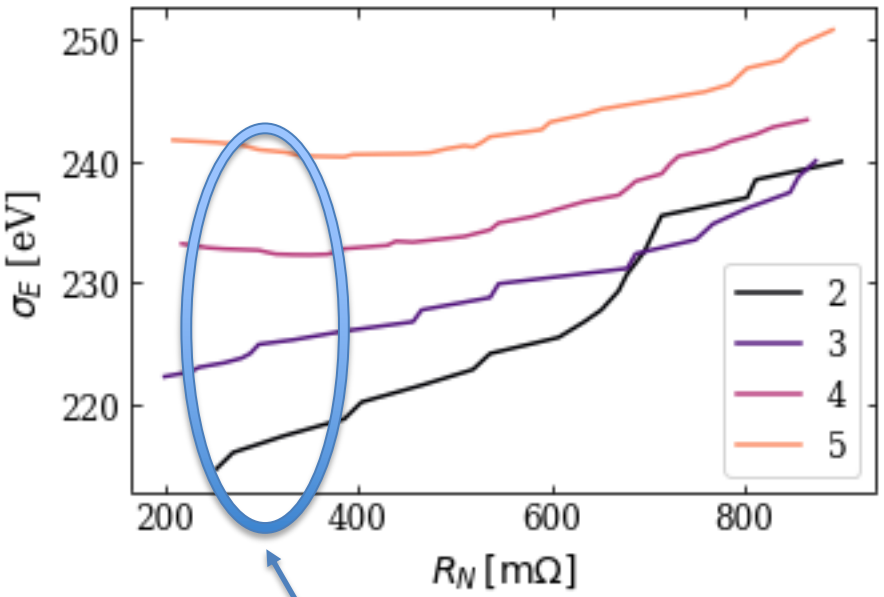
Bandwidth matched at $T_c \approx 45$ mK



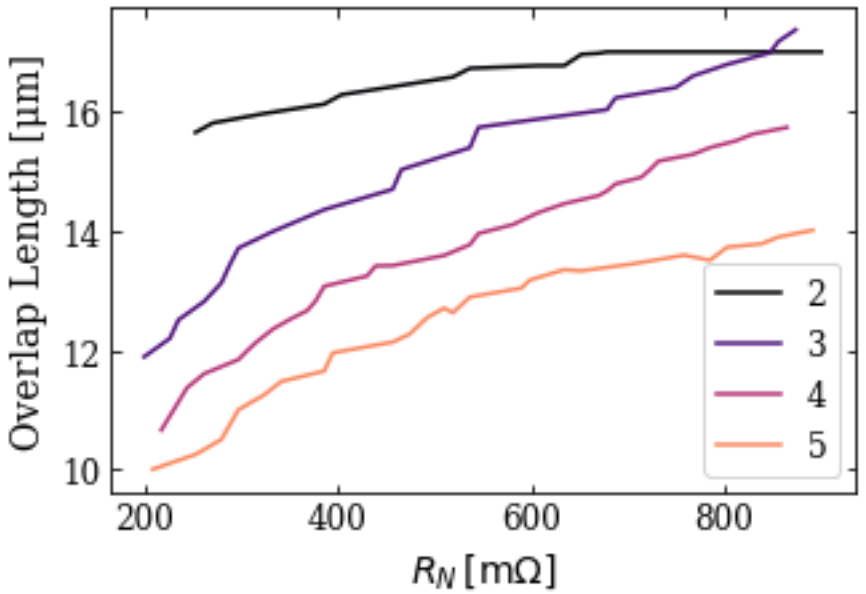
1% Coverage Device (Close Packed)

- Optimize for normal resistance
  - Keep surface coverage fixed and optimize free QET params as a function of Rn

* W/Al effective volume factor = 0.45



By not equally spacing the QETs, we no longer need to increase the Rn of the device

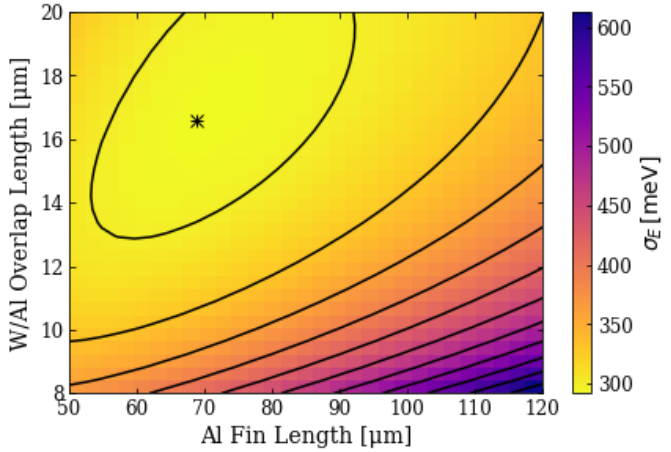


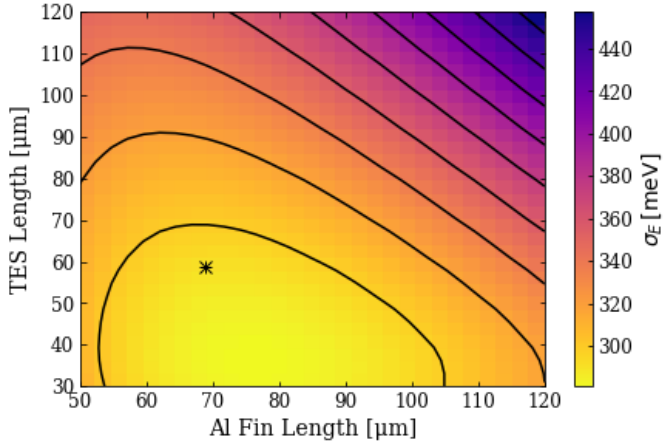
Choose Rn around 300, and 2 or 3 fin design

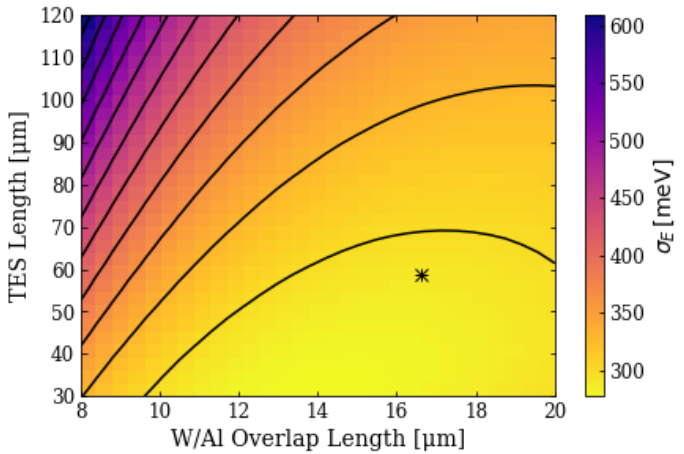
1% Coverage Device (2 Fin Close Packed)

Vary Parameters but fixed Number of TESs

σ_E	216.0 [meV] (Tc=40mK) 292.0 [meV] (Tc=45mK)
TES Length	58.9[μm]
TES Width	2.5 [μm]
TES Thickness	40 [nm]
Al Fin Length	68.9 [μm]
Al Fin Thickness	600 [nm]
Number of Fins	2
W/Al Overlap Length	16.6 [μm]
Total Al Surface Coverage	0.999[%]
Active Al	0.949 [%]
Passive Al	0.049[%]
τ_{ETF}	53.30 [μs] (Tc=40mK) 38.55 [μs] (Tc=45mK)
τ_{ph}	97.73 [μs]
Absolute Phonon Collection Efficiency	25.02 [%]
Number of TESs	177
R_N	325 [mΩ]

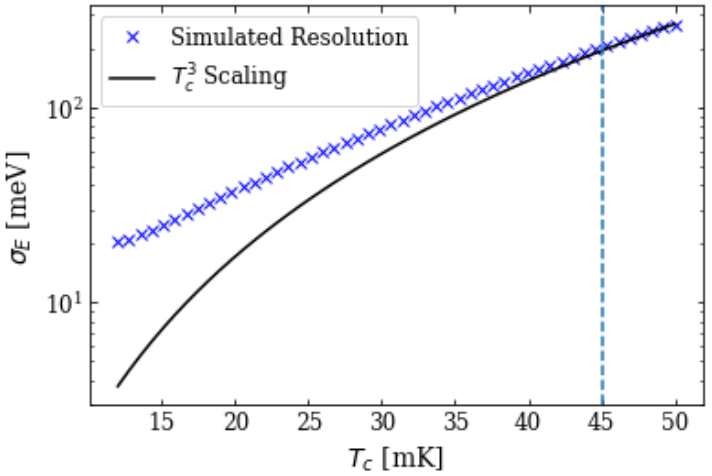






Note: plots are not always at optimum because the parameters are the average of two different Fin volume efficiencies

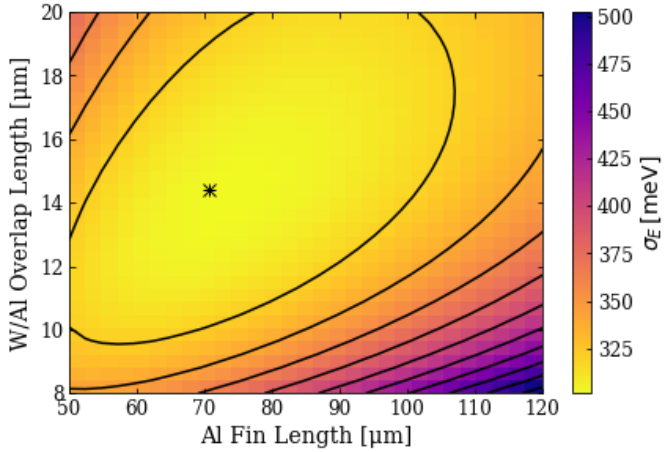
Bandwidth matched at $T_c \approx 45$ mK

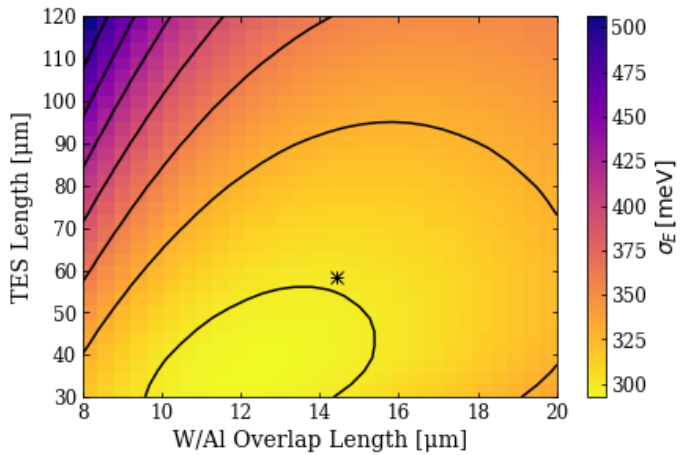


1% Coverage Device (3 Fin Close Packed)

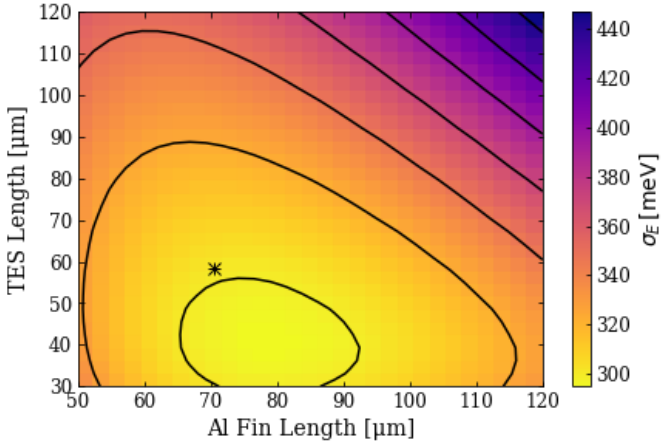
Vary Parameters but fixed Number of TESs

σ_E	223.3 [meV] (Tc=40mK) 301.9 [meV] (Tc=45mK)
TES Length	58.5[μm]
TES Width	2.5 [μm]
TES Thickness	40 [nm]
Al Fin Length	60.6 [μm]
Al Fin Thickness	600 [nm]
Number of Fins	3
W/Al Overlap Length	14.4 [μm]
Total Al Surface Coverage	1.008 [%]
Active Al	0.958 [%]
Passive Al	0.050 [%]
τ_{ETF}	53.30 [μs] (Tc=40mK) 38.55 [μs] (Tc=45mK)
τ_{ph}	96.82 [μs]
Absolute Phonon Collection Efficiency	25.52 [%]
Number of TESs	176
R_N	320 [mΩ]





Note: plots are not always at optimum because the parameters are the average of two different Fin volume efficiencies



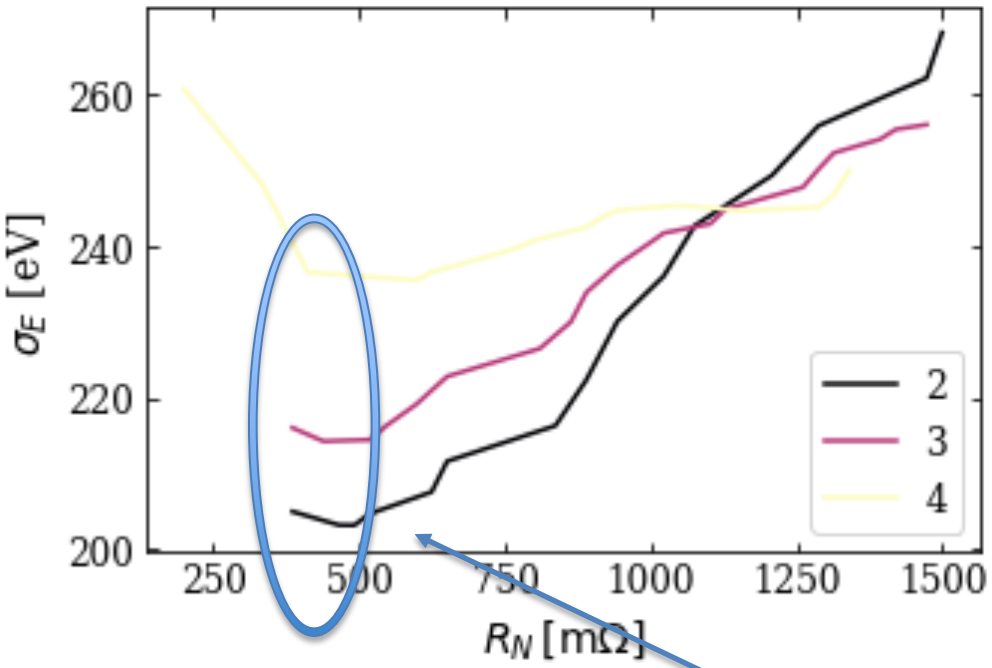
Bandwidth matched at $T_c \approx 45$ mK

The optimum is trying to push towards a shorter TES, suggesting that the 2 fin is maybe a better design

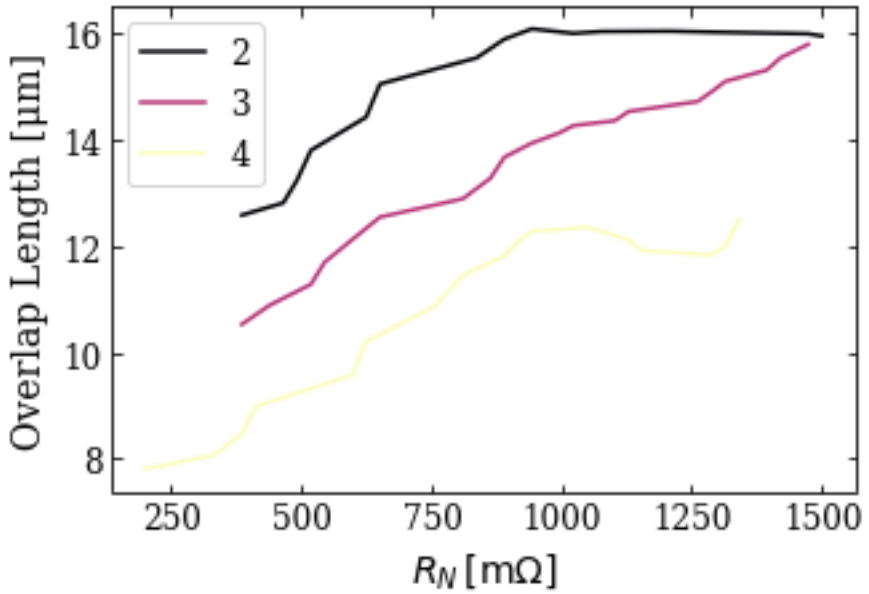
0.25% Coverage Device (Close Packed)

- Optimize for normal resistance
  - Keep surface coverage fixed and optimize free QET params as a function of Rn

* W/Al effective volume factor = 0.45



Given the results of the 1%, we only consider close packed QETs for the 0.25% device

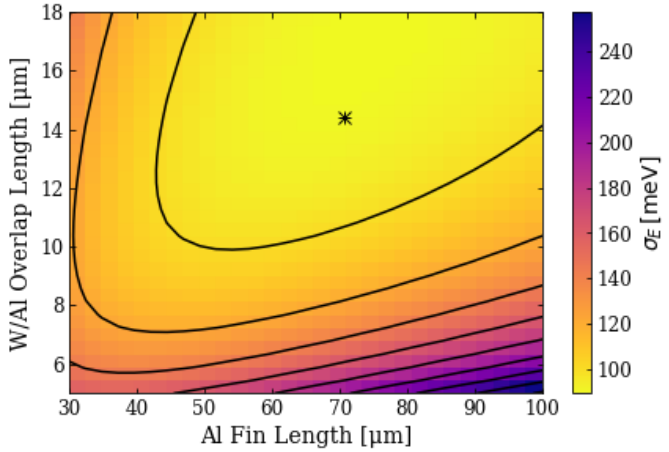


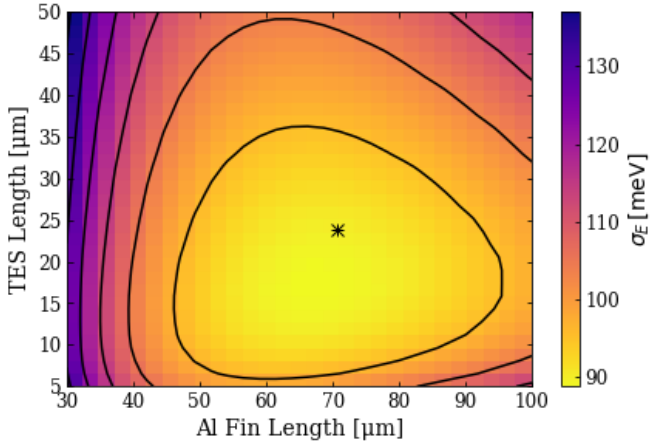
Choose Rn around 450, and 2 fin design

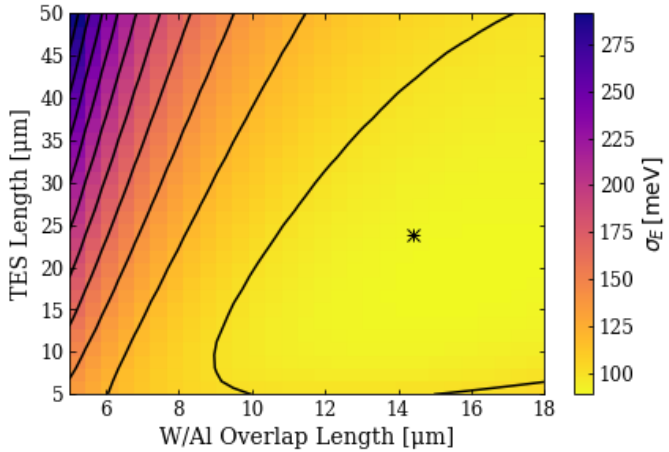
0.25% Coverage Device (Close Packed)

Vary Parameters but fixed Number of TESs

σ_E	90.3 [meV] (Tc=35mK) 130 [meV] (Tc=40mK)
TES Length	23.9[μm]
TES Width	2.5 [μm]
TES Thickness	40 [nm]
Al Fin Length	70.6 [μm]
Al Fin Thickness	600 [nm]
Number of Fins	2
W/Al Overlap Length	14.4 [μm]
Total Al Surface Coverage	0.253[%]
Active Al	0.239 [%]
Passive Al	0.015[%]
τ_{ETF}	80.74 [μs] (Tc=35mK) 53.88 [μs] (Tc=40mK)
τ_{ph}	385.60 [μs]
Absolute Phonon Collection Efficiency	21.08 [%]
Number of TESs	51
R_N	450 [mΩ]

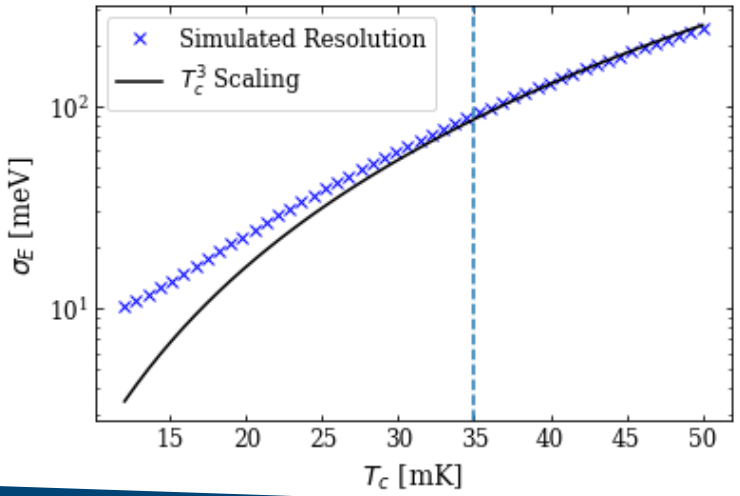






Note: plots are not always at optimum because the parameters are the average of two different Fin volume efficiencies

Bandwidth matched at $T_c \approx 35$ mK

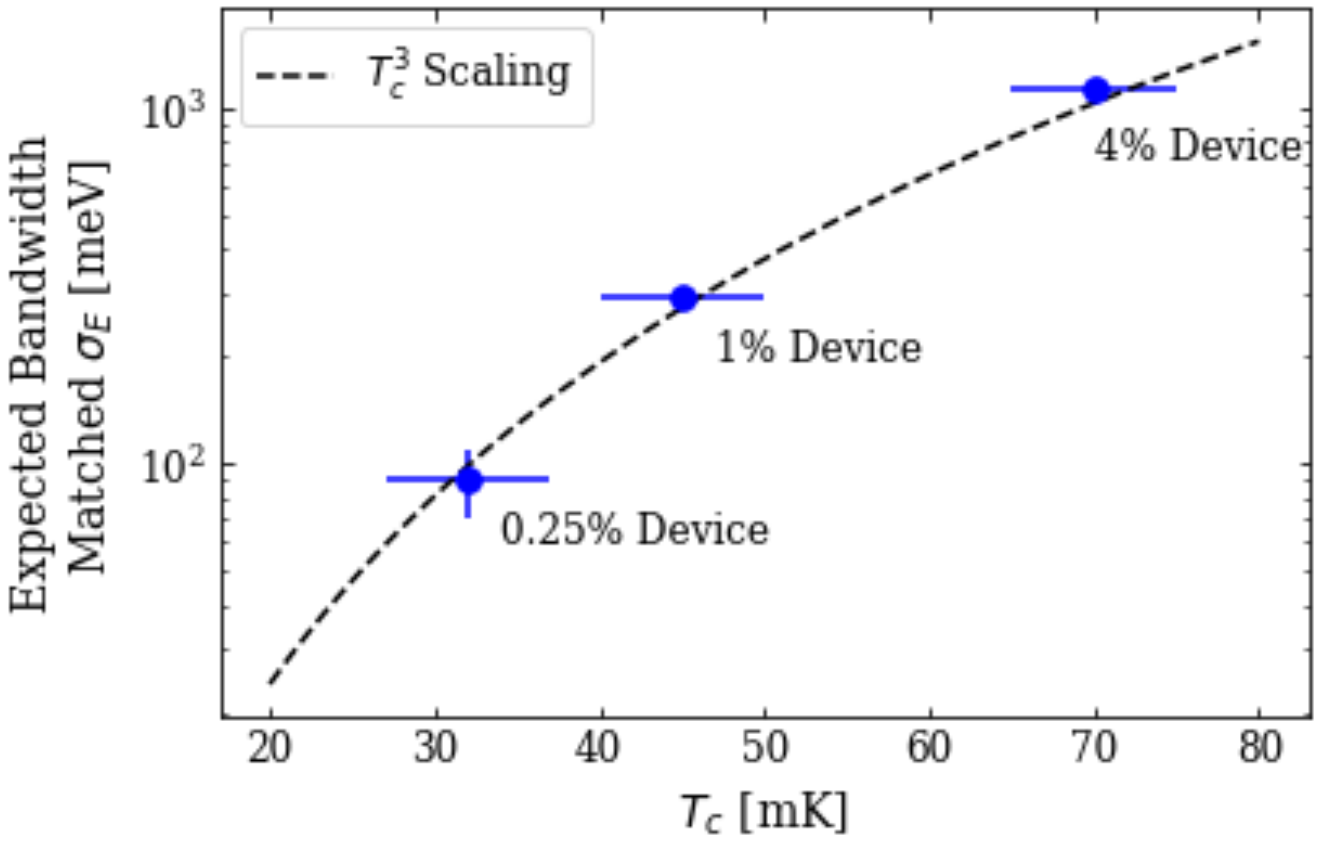


Do the Devices Scale As Expected?

- Yes!

- Considering the bandwidth matched designs, we see that the expected resolution follows:

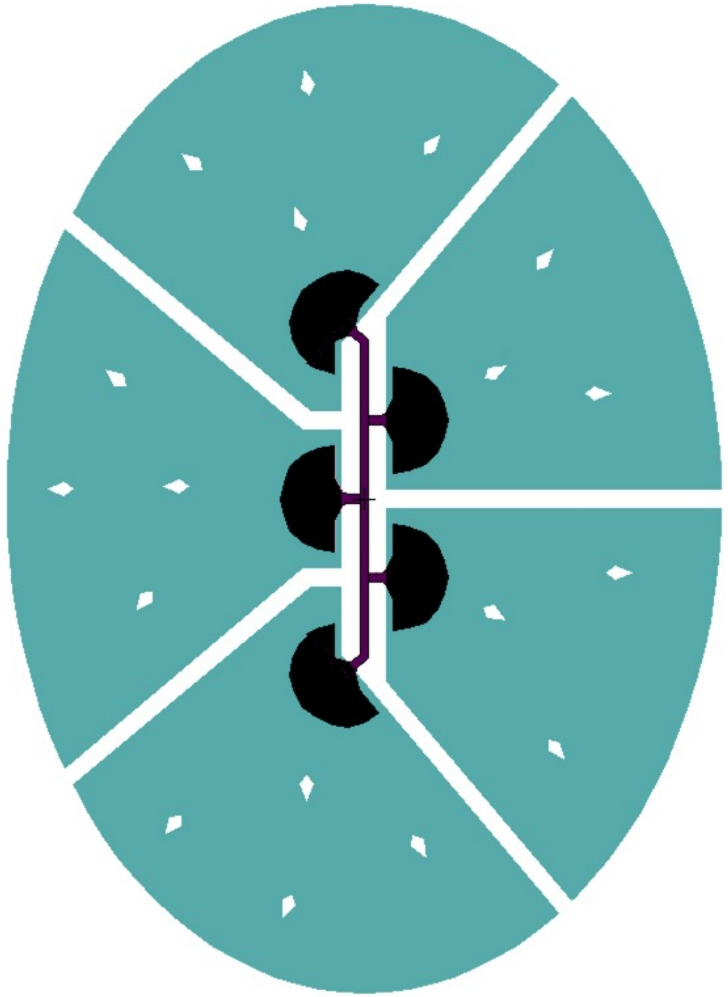
$$\sigma_E \propto T_c^3$$



Device Design Masks

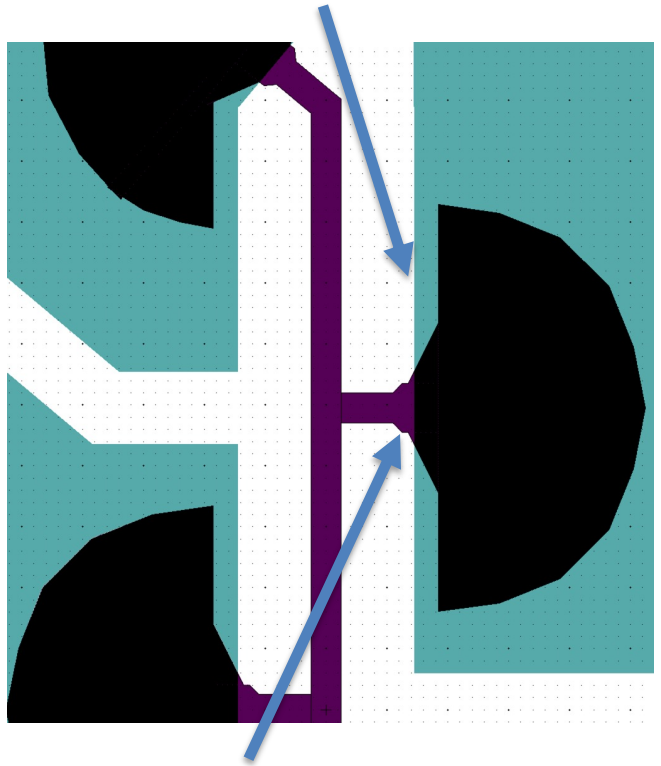
4% Device - QET

5 Equal area fins



Holes to reduce SC eddy currents

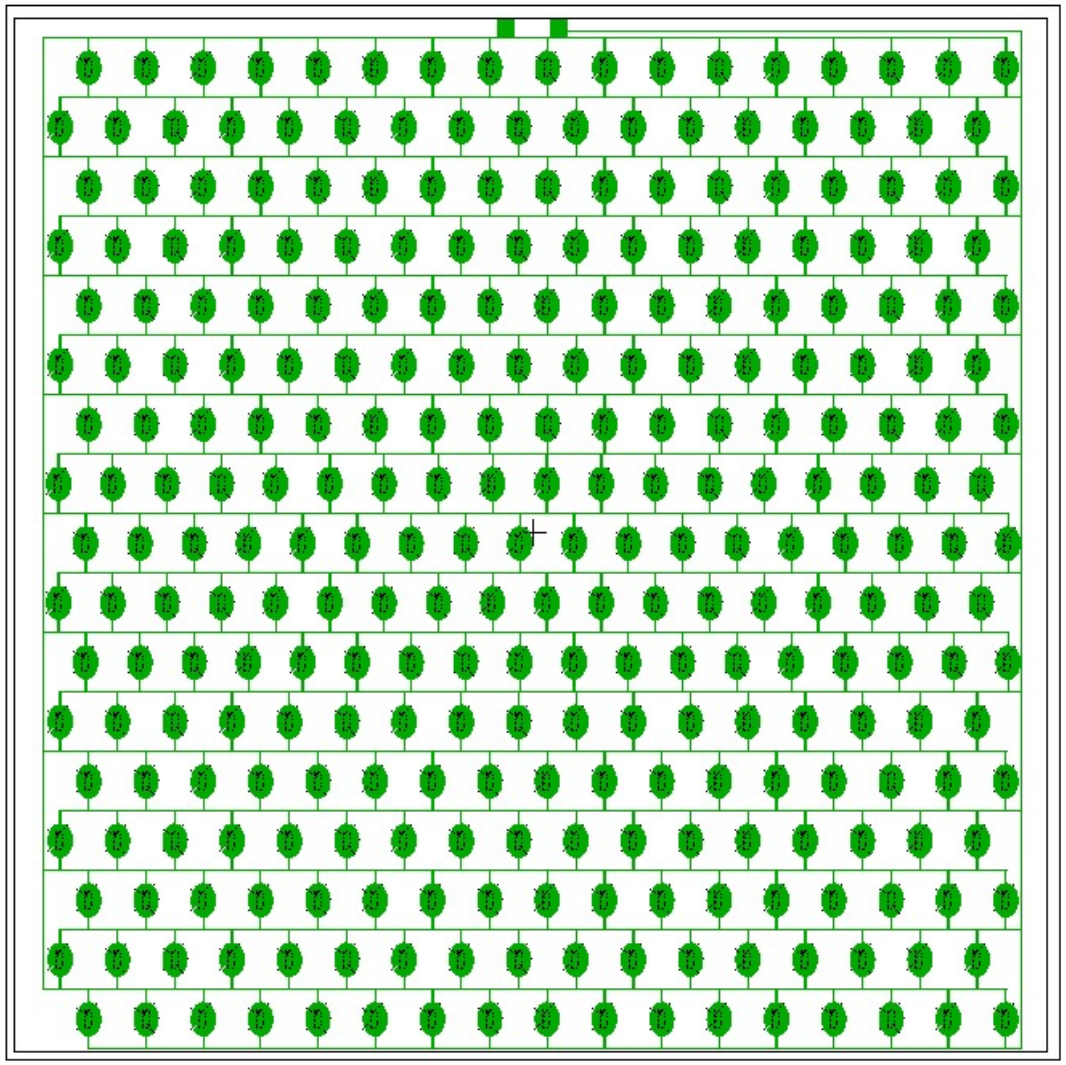
2 um ‘buffer’ of Al to allow for alignment errors



Tapered ‘neck’ from Overlap region to help reduce current QP bottle neck. Also can protect against over etching

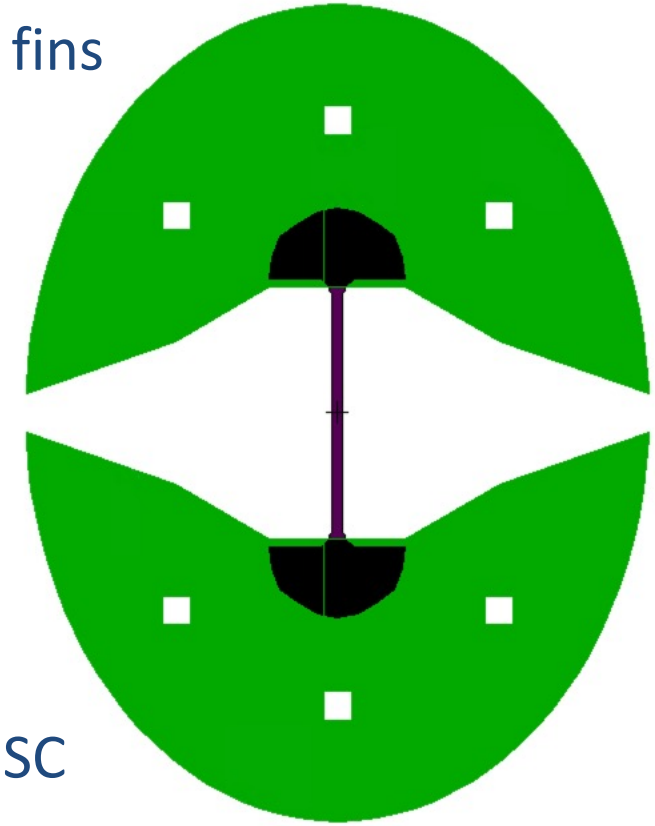
4% Device - Layout

- 293 ‘equally spaced’ QETs
- 17 rows of distance 564um
  - 13 offset rows with 17 QETs spaced x 544um
  - 4 offset rows with 18 QETs spaced x 515um

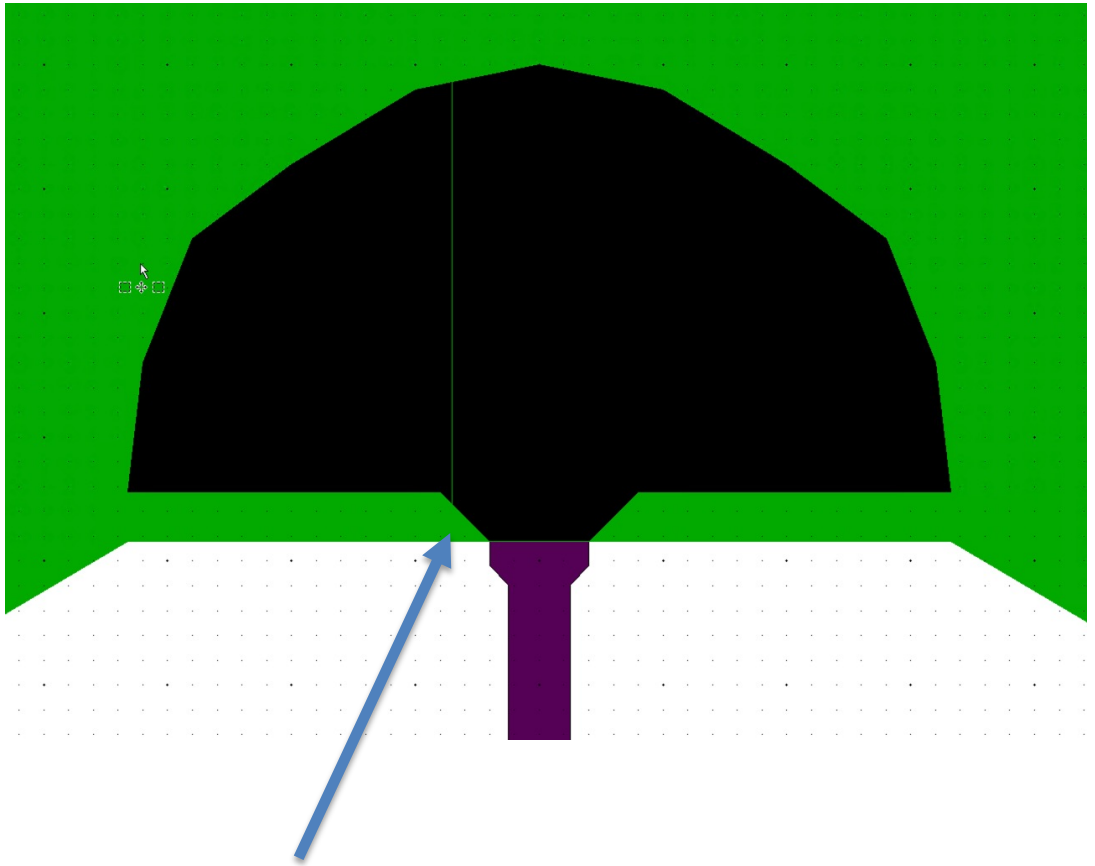


1% Device - QET

2 Equal area fins



Holes to reduce SC eddy currents



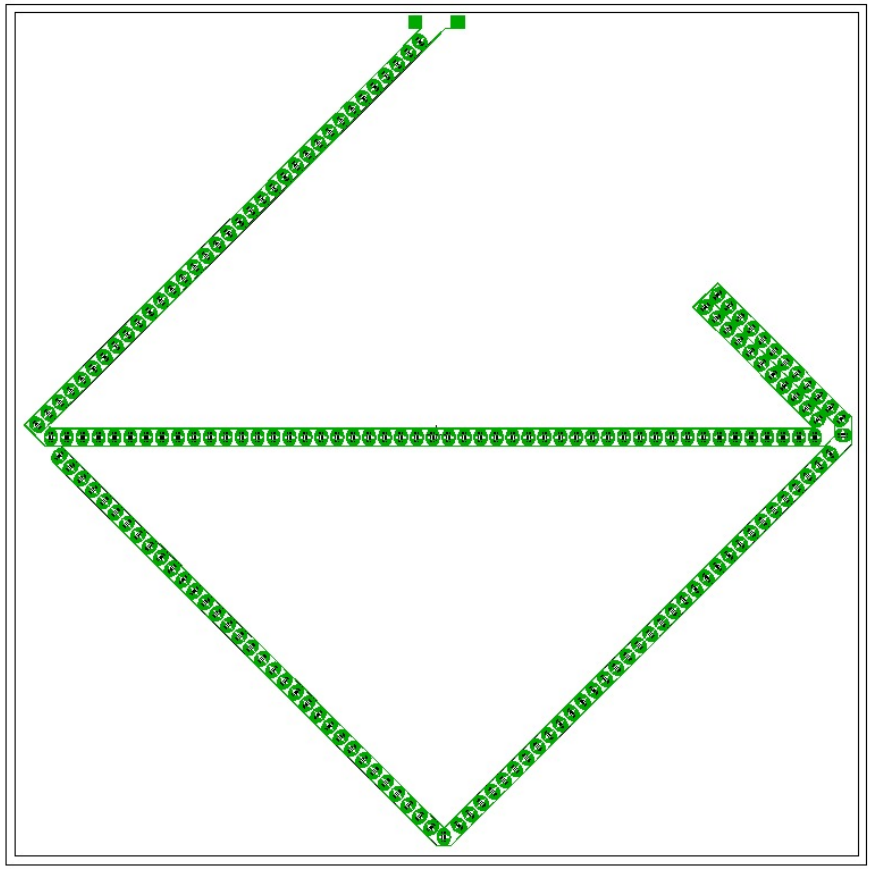
Tapered ‘neck’ from Overlap region to help reduce current QP bottle neck. Also can protect against over etching

1% Device – 3 Fin QET

- 2 fin device has lots of ‘dead space’ in the middle
- Try 3 fin design as well
- TODO

1% Device – Layout 1

- ‘Close packed’ design
- Limits positional dependence by instrumenting 4 quadrants and the center of the crystal



1% Device – Layout 2

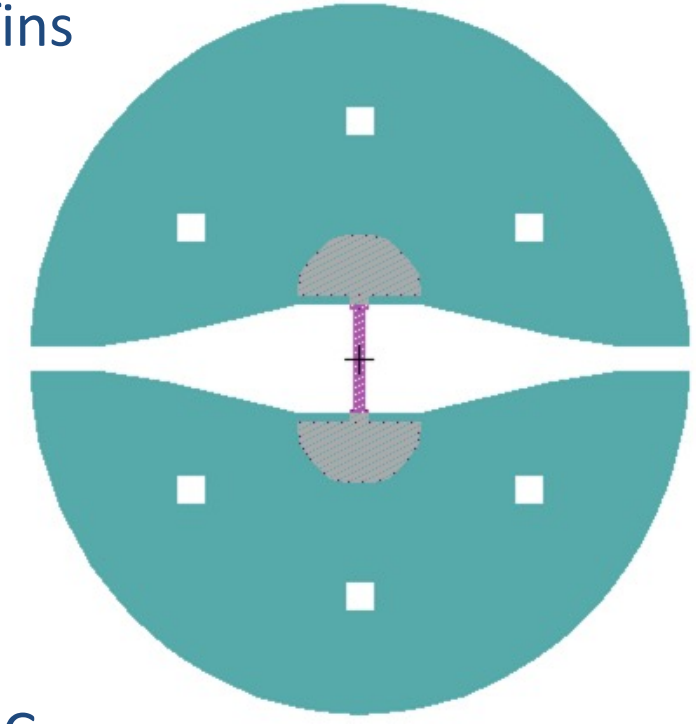
- Close packed design in center of chip

1% Device – Layout 3

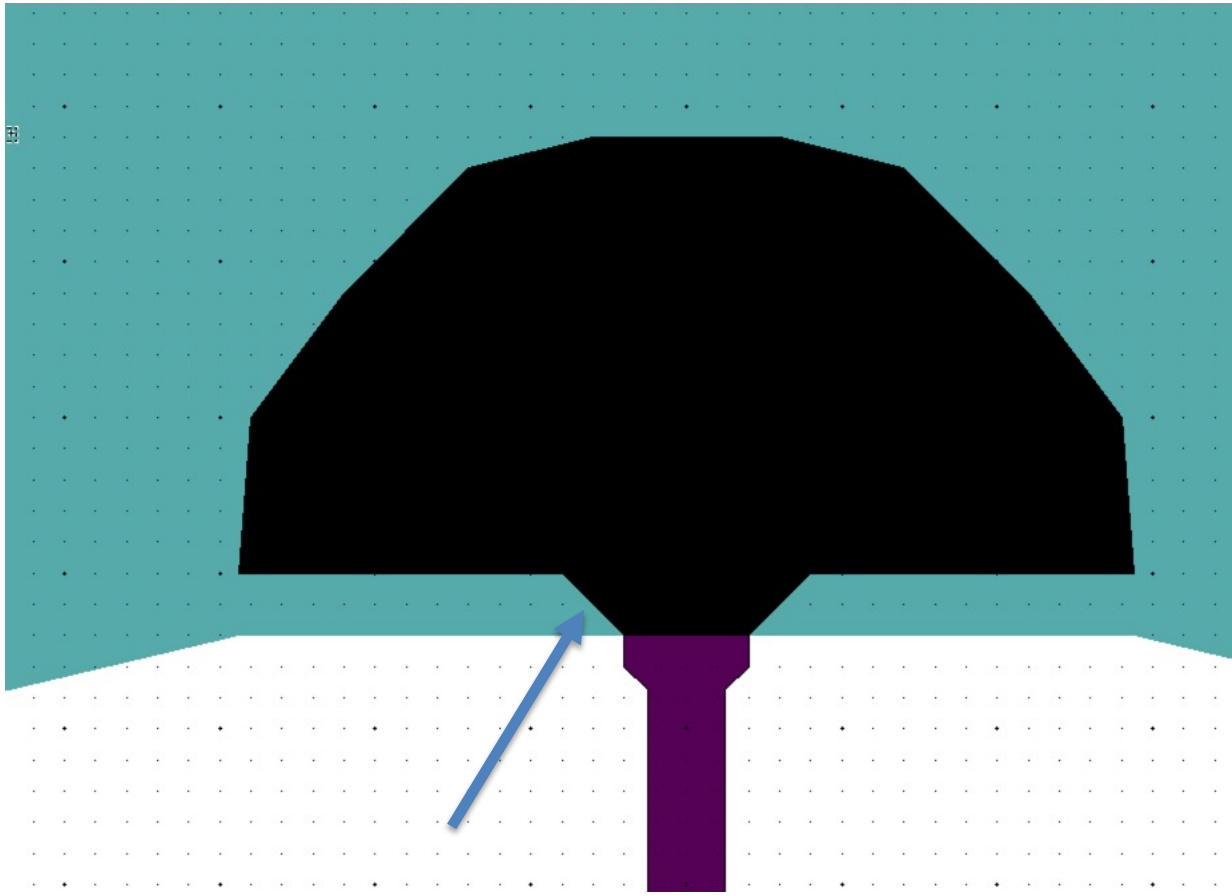
- Other layout ideas?

0.25% Device - QET

2 Equal area fins



Holes to reduce SC eddy currents

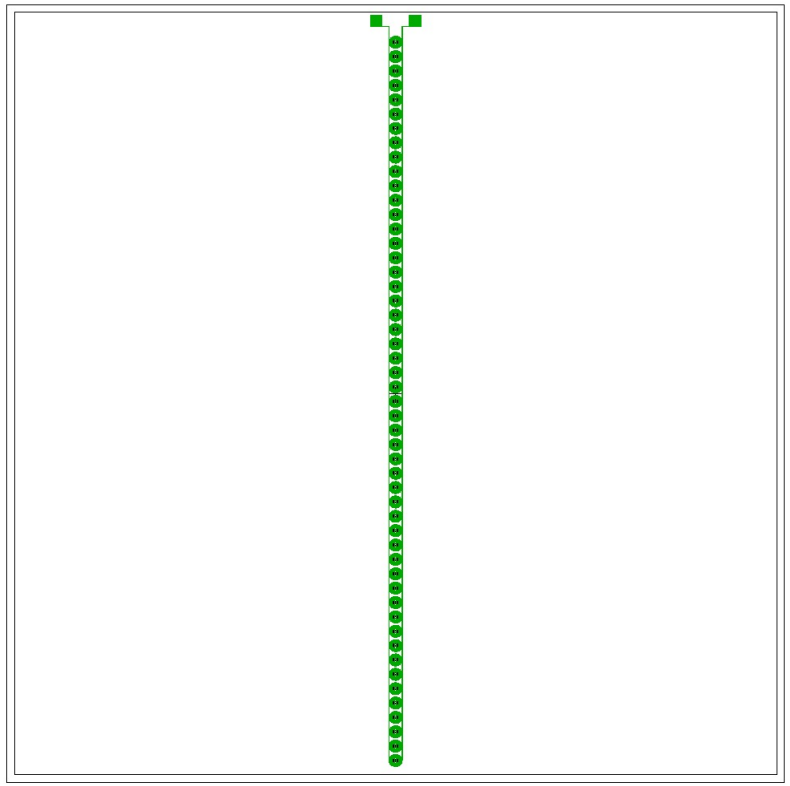


Tapered ‘neck’ from Overlap region to help reduce current QP bottle neck. Also can protect against over etching

0.25% Device - Layout

- ‘Close packed’ design

- Instruments one axis of the crystal
  - Limits positional dependance in this dimension but still will have issues with events on left of right sides



Wafer Layout

- Chips will be placed on 4’’ x 4mm (or 1mm) wafer
- 200um saw width between chips + 2mm safety around edge of wafer
  - Additionally each chips should have a 200um curb around the inside edge (outer 200um should be non-instrumented)
- ~50 chips