![Xilinx logo]

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Leveraging 7 Series FPGA Transceivers for High-Speed Serial I/O Connectivity

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To address the increasing consumer demand for bandwidth, high-bandwidth serial connectivity has become a standard design requirement in nearly every system. It has the advantage of fewer pins, simpler system clocking, lower cost and lower EMI.
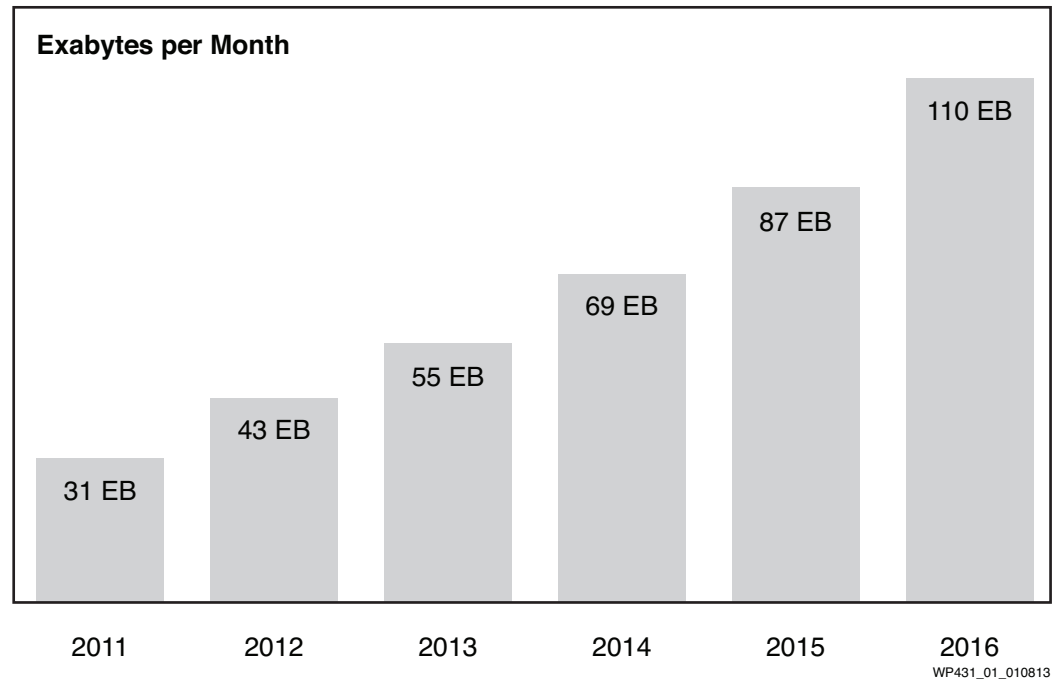
For years, FPGAs with high-speed serial I/O have been a clear choice for systems looking for bandwidth, density, performance, flexibility, and cost effectiveness. 7 series FPGAs from Xilinx, designed with the 28 nm HPL process, are equipped with a portfolio of transceivers suitable for a range of applications ranging from commercial video displays to ultra-high bandwidth wired telecommunications backplanes and optical interfaces.

This white paper gives an overview of the 7 series transceivers and elaborates on the industry-leading features that help system designers to:

- Increase system performance
- Improve system margin and robustness
- Reduce BOM cost
- Accelerate productivity

Bandwidth Growth and High-Speed Serial Interfaces

The popularity of mobile handsets and the transmission of high definition video content has led to an explosion of network traffic. The Cisco Visual Network Index (VNI) tracks and forecasts bandwidth growth. VNI projects global IP traffic to nearly quadruple from 2011 to 2016, as shown in Figure 1.

Exabytes per Month

110 EB

87 EB

69 EB

55 EB

43 EB

31 EB

2011 2012 2013 2014 2015 2016

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Figure 1: **Global IP Traffic Forecast from Cisco VNI for 2011–2016**

Electronic systems must scale with this bandwidth demand. The challenge faced by system designers is not only processing the incoming data but managing the data flow in and out of semiconductor devices. Because the number of pins on these devices does not scale proportionally with transistor count and logic capacity, each pin must allow more traffic to accommodate more total traffic. With the advantages of fewer pins, simpler system clocking, lower cost, and lower EMI, high-speed serial interfaces are ideal for managing traffic on- and off-chip.

For systems that need high bandwidth, high density, high performance, design flexibility, and low cost, FPGAs have been a clear choice for decades. Accordingly, high-speed serial interfaces are considered a must-have feature for FPGAs.

Serial Connectivity Application Classifications

In reference to connectivity, applications for serial transceivers can be categorized as the following:

- Serial backplanes
- Optical interfaces
- Host and peer communication
- Chip-to-chip communication

For target performance, such as speed, serial transceiver solutions can also be classified as:

- Low-end
- Mid-range
- High-end
- Ultra-high-end

Applications face different design challenges depending on transceiver connectivity and performance target, resulting in different criteria for transceiver selection. For example, for a low performance chip-to-chip application, the most important criteria are protocol efficiency, and easy design and integration. For a high-performance backplane system, signal integrity, system robustness, and IP support are the most critical.

7 Series Transceiver Portfolio and Architecture

7 series FPGAs are based on a scalable and optimized architecture, allowing all FPGA elements to be scaled and optimized to the target applications with IP portability from family to family. The transceiver portfolio extends this concept of scalability and portability. With line rates of 500 Mb/s to 28.05 Gb/s, the portfolio delivers a performance range that more than doubles that of any FPGA solution from previous generations.

The 7 series transceiver portfolio is described in Table 1.

Table 1: **7 Series Transceiver Portfolio**

Transceiver	Devices	Description
GTZ	Virtex-7	Ultra-high performance 28 Gb/s transceiver for 100G/400G data paths
GTH	Virtex-7	High-end transceiver with high bandwidth, low power, and best signal integrity for the toughest backplanes
GTX	Virtex-7 Kintex-7	Mid-range 10 Gb/s transceiver for PCIe®, optics, and backplanes
GTP	Artix-7	Low-end transceivers for high volume, low power, and cost-sensitive applications

7 series transceivers are based on the following architecture:

- Physical Medium Attachment Sublayer (PMA)
  - The PMA includes a serial/parallel interface (PISO, SIPO), phase-locked loop (PLL), clock data recovery (CDR), pre-emphasis, and equalization blocks.
- Physical Coding Sublayer (PCS)
  - The PCS contains logic-to-process parallel data and includes FIFO, coding/decoding, and gearbox functionality. Because the PCS blocks are running at slower rates than the PMA blocks, the challenge in transceiver design mostly lies in the PMA sub-layer.
- Package
- FPGA logic interface

Figure 2 illustrates an abstract diagram of a transceiver channel.
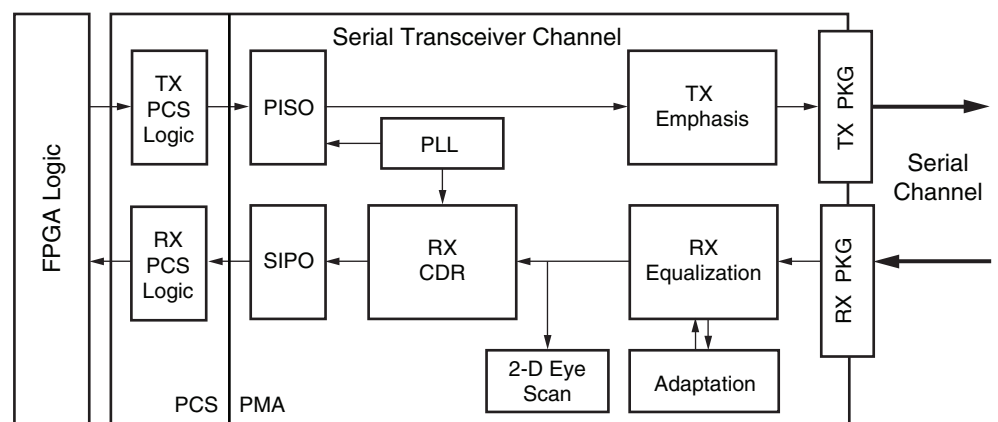
Figure 2: **7 Series Transceiver Channel Architecture**

The implementation of the blocks in each channel is different based on connectivity and performance requirements. For example, the GTZ transceiver (28 Gb/s) is designed to meet the CEI-28G-VSR (i.e., very short reach connectivity) specification. GTZ transceivers are targeted to chip-to-chip connections and connections to a CFP2 optical module. Continuous time linear equalization (CTLE) — commonly used to compensate for insertion loss — can deliver sufficient signal integrity for short-reach connections. Hence, GTZ transceivers do not need additional signal compensation technologies such as a Decision Feedback Equalizer (DFE). The GTH transceiver (13.1 Gb/s), in contrast, needs signal compensation for tough backplanes; therefore, both DFE and CTLE are required in the RX equalization block.

Key Enablers in 7 Series Transceivers

When considering a device for a serial-based design, developers have to consider a diverse set of criteria. The 7 series transceiver silicon leads the industry in line rates, aggregate bandwidth, signal integrity, and easy link tuning. Together with the intuitive design tools, broad IP support, and plentiful resources, 7 series transceivers provide the best FPGA transceiver solution available.

Line Rate, Density, and System Bandwidth

Different applications require different line rates. Table 2 shows the maximum line rate of each 7 series transceiver.

Table 2: **7 Series Transceiver Portfolio**

Transceiver	GTZ	GTH	GTX	GTP
Performance Category	Ultra-high	High-end	Mid-range	Low-end
Max Line Rate (Gb/s)	28.05	13.1	12.5	6.6

Transceiver count and transceiver mix are also important factors for meeting system bandwidth requirements. For complex communications infrastructure applications, high-end Virtex®-7 FPGAs can have a combination of GTZ and GTH transceivers, or a single type of GTH or GTX transceiver. The smaller Kintex™-7 and Artix™-7 FPGAs are equipped with GTX and GTP transceivers, respectively. Table 3 describes the maximum transceiver count for each 7 series FPGA.

Table 3: **Maximum Transceiver Count/Type in 7 Series FPGA Families**

	Virtex-7 HT	Virtex-7 XT	Virtex-7 T	Kintex-7	Artix-7
GTZ (28.05 Gb/s)	16				
GTH (13.1 Gb/s)	72	96			
GTX (12.5 Gb/s)			56	32	
GTP (6.6 Gb/s)					16

With the highest line rates and highest transceiver count, 7 series FPGAs lead the industry in total system bandwidth. Figure 3 shows the maximum bandwidth of each device. A single Virtex-7 FPGA can have an aggregate bidirectional transceiver bandwidth of over 2.7 Tb/s, while the nearest competitor stops at 1.8 Tb/s. High bandwidth is the base for building a high-performance system.

7 Series FPGA Transceiver Maximum Bandwidth

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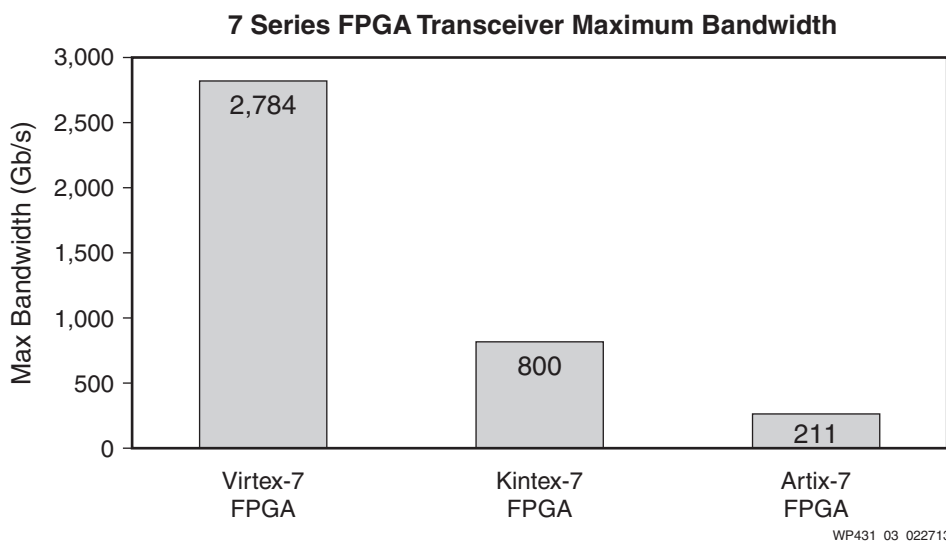
Figure 3: **Transceiver Maximum Bandwidth per Product Family**

Flexible PLL Selection and Optimal Jitter Performance

One of the most critical transceiver components is the PLL because it largely contributes to overall transceiver quality: the PLL frequency range determines transceiver line rate; the PLL jitter determines overall jitter performance and affects system margin; and the PLL power is a major contributor to total transceiver power consumption.

The type of oscillator used in the PLL is particularly important. There are two common oscillator choices in the transceiver industry: the ring oscillator and the LC tank oscillator. A ring oscillator has a wide frequency range and simple topology — thus, small area and low power consumption. However, its jitter performance is less optimal for protocols and channels at higher line rates. An LC tank oscillator has excellent jitter performance, but provides a narrower tuning range — and its topology requires more area and higher power consumption.

7 series transceivers offer both oscillator types optimized for each transceiver type, based on the target connectivity and performance. For ultra-high-end GTZ transceivers, only an LC tank oscillator with minimal clock-tree loading can guarantee the highest performance. For the low-end GTP transceiver, the performance of a ring oscillator is suitable for target applications. However, high-end GTH and mid-range GTX transceivers cover a wide variety of applications and connectivity. Some need performance, while others sacrifice performance for power and flexibility. Thus, a mix of both ring and LC tank oscillators are offered. Table 4 lists the 7 series transceivers' oscillator selections.

Table 4:   **7 Series Transceiver PLL Oscillator Selections**

Transceiver	GTZ	GTH	GTX	GTP
Ring Oscillator (Flexibility)		✓	✓	✓
LC Tank Oscillator (Performance)	✓	✓	✓	

The GTH, GTX, and GTP transceivers are implemented as Quads. Each Quad consists of four transceiver channels. Figure 4 describes the Quad architecture of GTH and GTX transceivers.

Each Quad contains one LC tank-based Quad PLL (QPLL) and four ring-based Channel PLLs (CPLL). The clock for each transmitter or receiver can be selected from either the QPLL or dedicated CPLL. The reference clock for the PLLs can come from the two dedicated reference clocks within the Quad, or from the adjacent Quads. This structure provides great flexibility and allows efficient use of all available transceiver channels, meeting various system performance requirements.
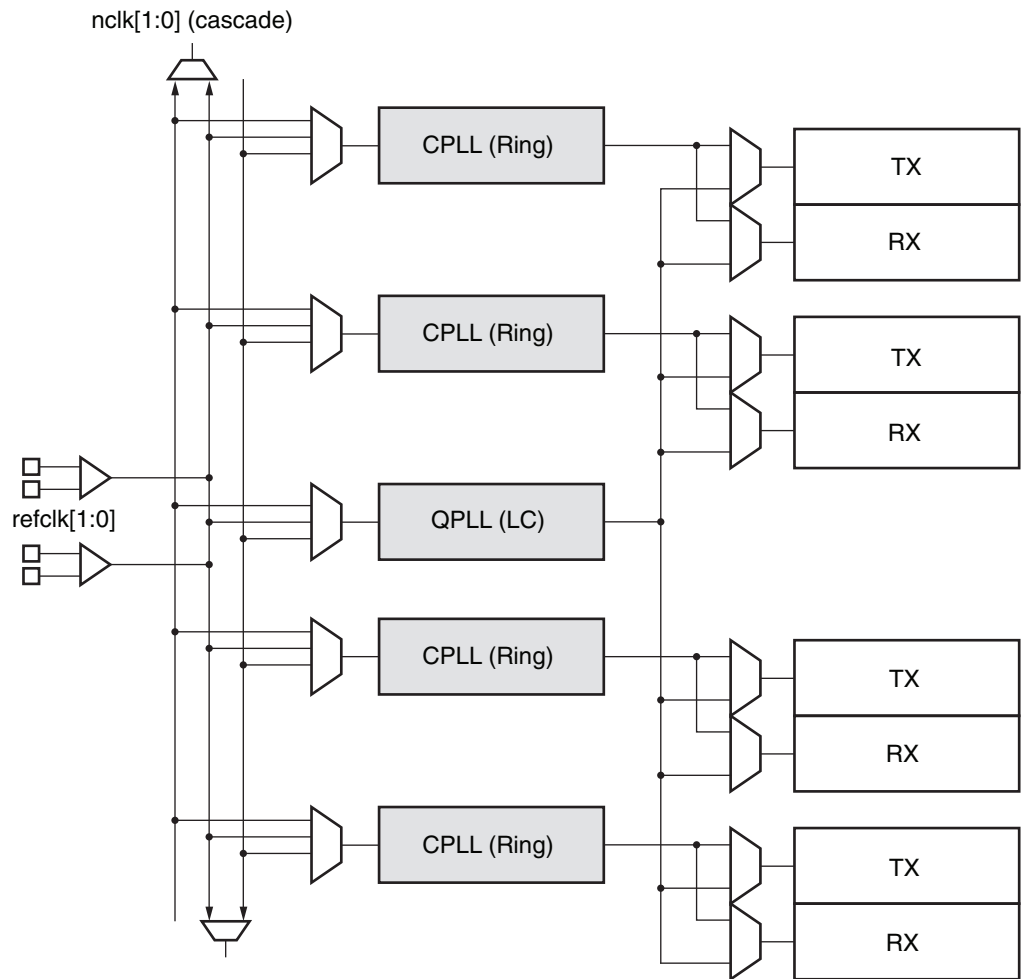
Figure 4:   **7 Series GTH and GTX Transceiver Clocking Architecture**

The Xilinx 7 series transceiver PLL design delivers industry-leading jitter performance, improving system margin and robustness. Figure 5 is a sample eye diagram of the ultra-high-end GTZ transceiver with a PRBS9 data pattern running at 28.05 Gb/s. The scope measures only 300 fs random jitter (Rj RMS) and 8.47 ps total jitter (less than 0.24 UI of the 35.6 ps eye).
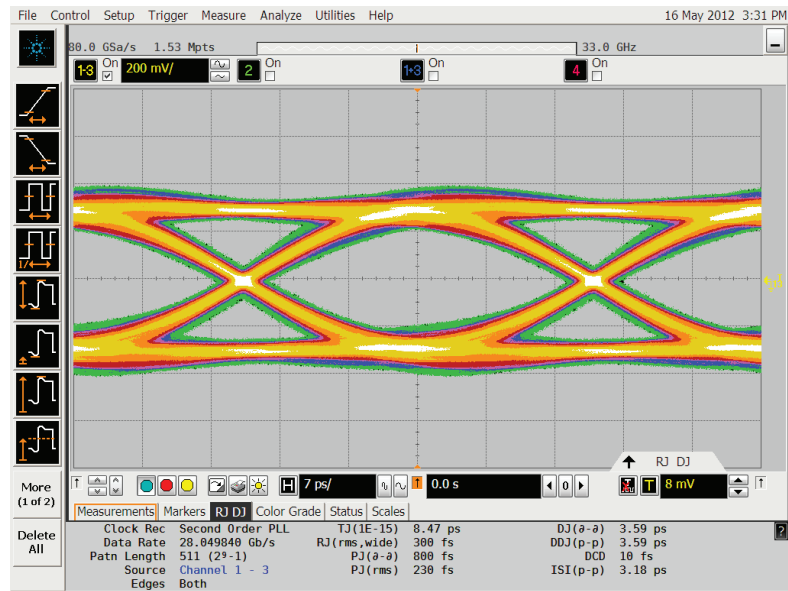

Figure 5:   **7 Series GTZ Transceiver Eye Diagram and Jitter Performance Sample**

Figure 6 is a sample eye diagram of the low-end GTP transceiver with PRBS15 data pattern at 6.6 Gb/s. The scope measures 1 ps random jitter (Rj RMS) and 19.52 ps total jitter (less than 0.13 UI of the 151 ps eye).
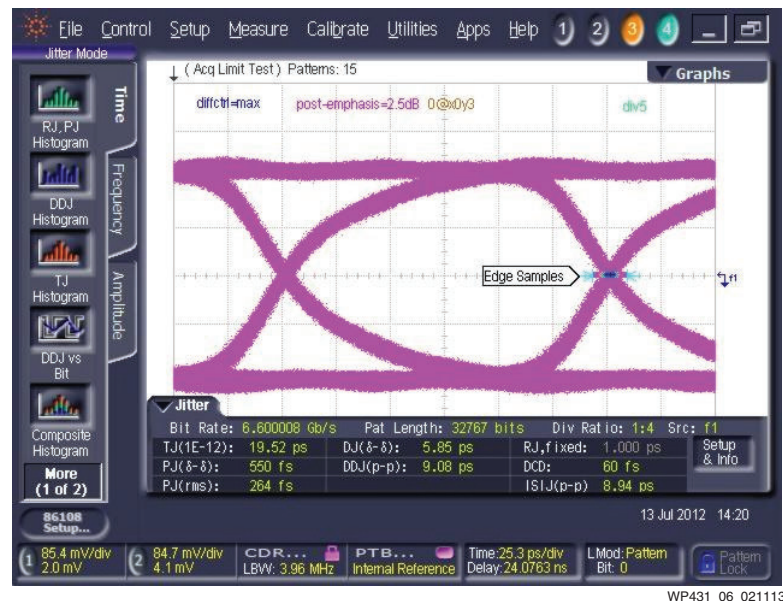
Figure 6:   **7 Series GTP Transceiver Eye Diagram and Jitter Performance Sample**

Equalization for Backplanes and Un-retired Optics

When traversing serial links with optics or backplanes, high-speed signals are degraded by impairments in the link, such as insertion loss, reflections, crosstalk, and optical dispersion. As the serial signaling rate increases, channel-driven signal degradation increases. The techniques used to compensate for this, therefore, become critical elements in the design. This compensation is usually called emphasis in the transmitter and equalization in the receiver.

The equalization features in the 7 series transceivers — in addition to the PLLs — deliver the best signal integrity in the industry. Similar to PLLs, the types of equalization features needed are based on target performance and connectivity. Combining features such as 3-tap TX emphasis, automatic gain control, auto-adaptive CTLE, and auto-adaptive DFE, 7 series transceivers deliver the most efficient, lowest bit error rate (BER) equalization solution for building a robust serial system. This optimized equalization solution improves the system margin while reducing the BOM cost by eliminating the need for re-timers.

For leading-edge backplane applications, which need extremely low bit error rates, the 7 series GTH transceiver provides the most robust 10GBase-KR solution in the FPGA industry. Unlike the marginal performance of the competition, the 7 series GTH transceiver surpasses the 10G-KR BER specification by many orders of magnitude on well-designed backplanes without exotic material.

Table 5 summarizes the equalization capabilities in each 7 series transceiver. For more details, see WP419, *Equalization for High-Speed Serial Interfaces in Xilinx 7 Series FPGA Transceivers*.

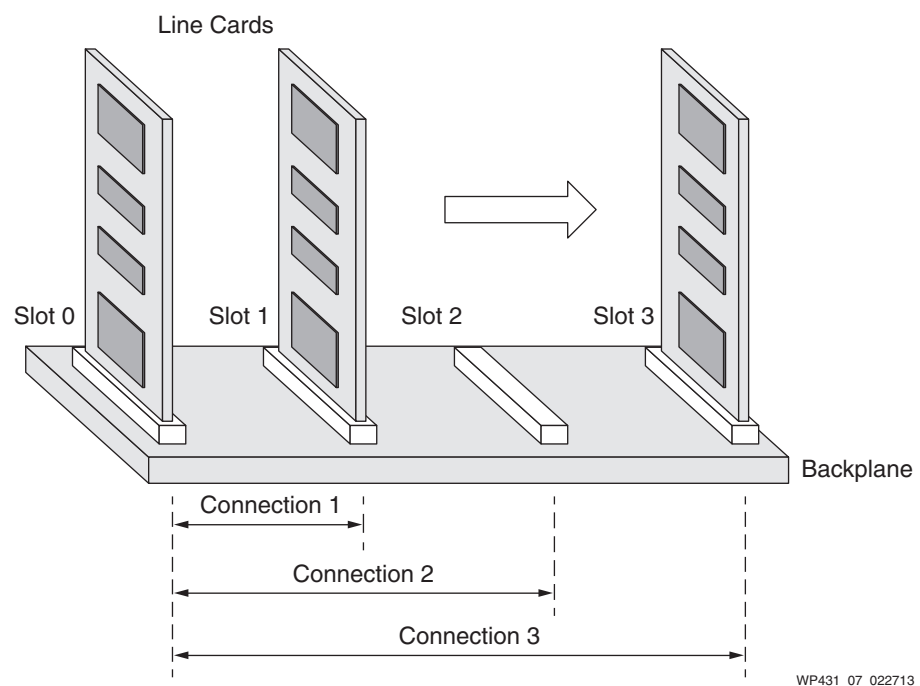*Table 5:* **7 Series Transceiver Equalization Capabilities**

Feature	GTP 6.6 Gb/s	GTX 12.5 Gb/s	GTH 13.1 Gb/s	GTZ 28.05 Gb/s
TX Emphasis	✓	✓	✓	✓
Optics	✓	✓	✓	✓
10G or less	CEI-6G	SFP+ (CPRI 9.8G, 10GE, OTU2), XFP	SFP+ (CPRI 9.8G, 10GE, OTU2), XFP	
100G		CFP (100GE, OTU4)	CFP (100GE, OTU4)	CFP2, CFP4 (100GE, OTU4)
Backplane				
Line Rate (Gb/s)	3.125	12.5	13.1	
Loss @ Nyquist (dB)	12	25+	25+	
RX CTLE	✓	✓	✓	✓
RX DFE	N	Y (5 fixed)	Y (7 fixed, 4 sliding)	N
EQ Adaptation	Y (CTLE)	Y (DFE)	Y (CTLE+DFE)	Y (CTLE)
2-D Eye Scan	✓	✓	✓	✓

Adaptive Equalization and On-Chip Eye Scan

For serial systems beyond 3 Gb/s, multiple equalization techniques are needed to compensate for signal distortion in the serial link. Each technique offers multiple settings to handle different channel conditions. The matrix of TX emphasis, RX DC gain, RX CTLE, and RX DFE settings can easily go to thousands or millions of combinations. For example, for a simple receiver with 4 DC gain settings, 16 CTLE settings, 3 tap DFE (where each tap has 4 settings), the total combination of settings is 4,096. For high-quality 10 Gb/s transceivers, such as the GTH and GTX transceivers, there are millions of settings for the receiver alone. Manually selecting the optimal setting from so many combinations is tedious and error-prone. Fortunately, to assure the highest possible performance, Xilinx FPGAs uniquely provide the best answer to this challenge: auto-adaptive receiver equalization built directly in hard logic.

All equalization techniques (gain control, CTLE, and DFE) in the receiver are available in three modes: manual, one-time calibration, and continuous adaptation. Xilinx recommends continuous adaptation. A backplane with multiple slots for line cards is an example where continuous adaptation is critical.

Figure 7 describes such a backplane. The transmitters and receivers connect to two line cards respectively. The channel condition varies when the line cards plug into different slots. Usually, different equalization settings must be applied for different slots to ensure a robust serial link. In manual mode, the system designer has to set the receiver equalization settings by hand. With one-time calibration, every time the line card plugs into a different slot, the system designer has to re-calibrate. With continuous adaptation, the same transceiver setting can build a robust serial link regardless of the slot because the adaptation adjusts the gain control, CTLE, and DFE, and thus automates what had previously been a manual task for the system designer.

Additionally, voltage and temperature changes impact transceiver performance and channel characteristics. Continuous adaptation offers protection for link margin, which manual mode and one-time calibration mode cannot provide.

Figure 7: **Multiple Line Card Slots with Backplane**

In addition to equalization, all 7 series transceivers incorporate non-destructive 2-D eye scan, which captures the post-equalization signal right before data recovery takes place at the receiver. It visualizes the effects of equalization and helps determine link margin, thereby accelerating the debug process. Figure 8 shows an example of a 2-D eye scan result for a GTH receiver. The wide-open eye proves that the link under test (13.1 Gb/s through a 16-inch Tyco backplane with more than 30 dB insertion loss) has sufficient margin.
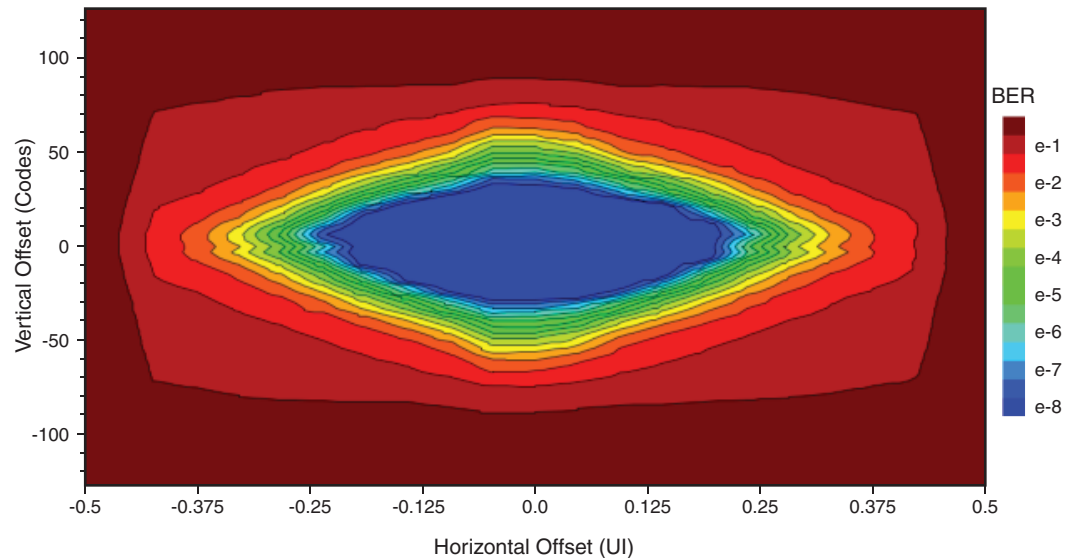
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Figure 8: **7 Series GTH Transceiver 2-D Eye Scan Sample**

The 2-D eye scan can be used in board validation as part of a system debug methodology. To learn how to implement the 2-D eye-scan for a customized design, refer to XAPP743, *Eye Scan with MicroBlaze™ Processor MCS*.

The auto-adaptive equalization and the on-chip non-destructive 2-D eye scan can dramatically reduce the workload for system bring-up, maintenance, and debug.

Design Tools and Resources

A complete transceiver solution requires more than just silicon to create a user friendly, reliable, and efficient environment. Equally important are simulation model kits, evaluation boards, design tools, and reference designs. Xilinx continues to provide such a platform for 28 nm FPGAs.

Simulation Model Kits and Evaluation Boards for Signal Integrity Analysis

Because signal integrity is critical, signal link margin analysis at an early stage of the system design phase is usually necessary before selecting a device. Xilinx provides IBIS-AMI model kits for all 7 series transceivers. The IBIS-AMI model kits provide both fast simulation speed (minutes for 1 million bits) and HSPICE-correlated accuracy. They are also fully IBIS 5.1 compatible, making them highly transportable, flexible, and usable. Figure 9 shows an example of a time domain IBIS-AMI simulation result with Agilent ADS 2012.08.
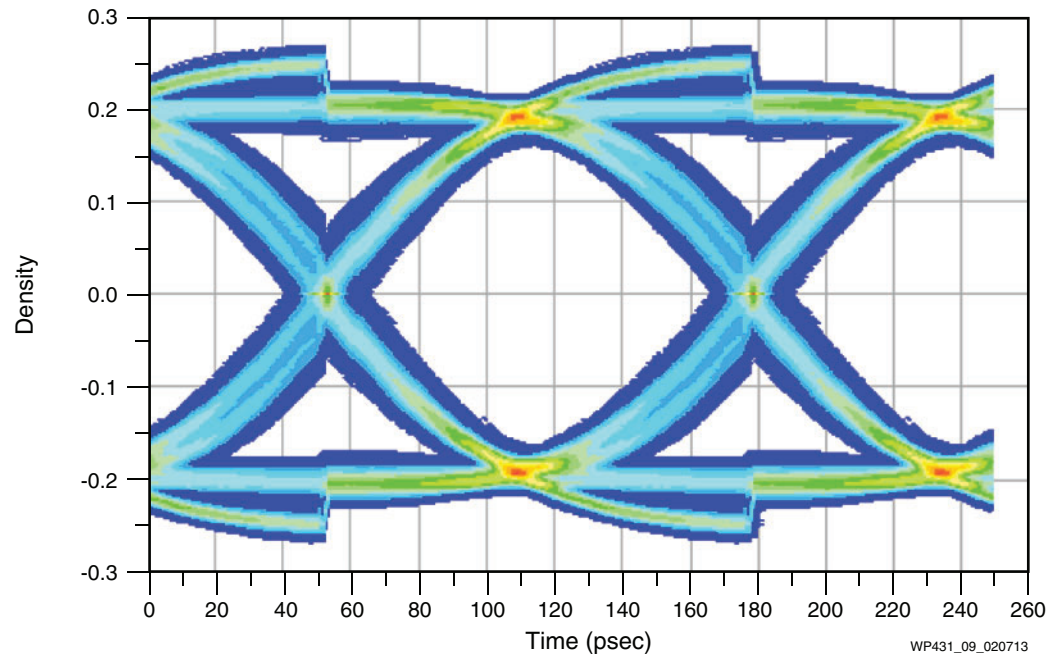
Figure 9: **7 Series GTX Transceiver IBIS-AMI Time-Domain Simulation Sample Result**

For more details on IBIS-AMI model kits and simulation capabilities, refer to WP424, *Multi-Gigabit Serial Link Simulation with Xilinx 7 Series FPGA GTX Transceiver IBIS-AMI Models*.

Designers can also validate link margin and perform analysis on real hardware with a Xilinx transceiver evaluation board, leveraging the ChipScope™ logic analyzer and IBERT GUI with on-chip 2-D eye scan. For more information on margin analysis using simulation and 2-D eye scan for board validation, refer to WP428, *Serial Link Signal Integrity Analysis with IBIS-AMI Simulation and On-Chip Eye Scan for Low-Cost, High-Volume FPGA Transceivers*.

User-Friendly Design Suite for Productivity

When signal integrity analysis shows sufficient link margin, an easy-to-use design suite with great flexibility is needed to develop a specific design. Xilinx provides configuration wizards for all 7 series transceivers to serve both the mainstream user and advanced transceiver expert. A designer can easily select protocols, line rates, and the number of channels from drop-down menus. Within a few clicks, the wizard can complete the rest of the configuration process automatically with the default implementation. Advanced users can customize the design in the configuration wizard for specific system requirements. See Figure 10.
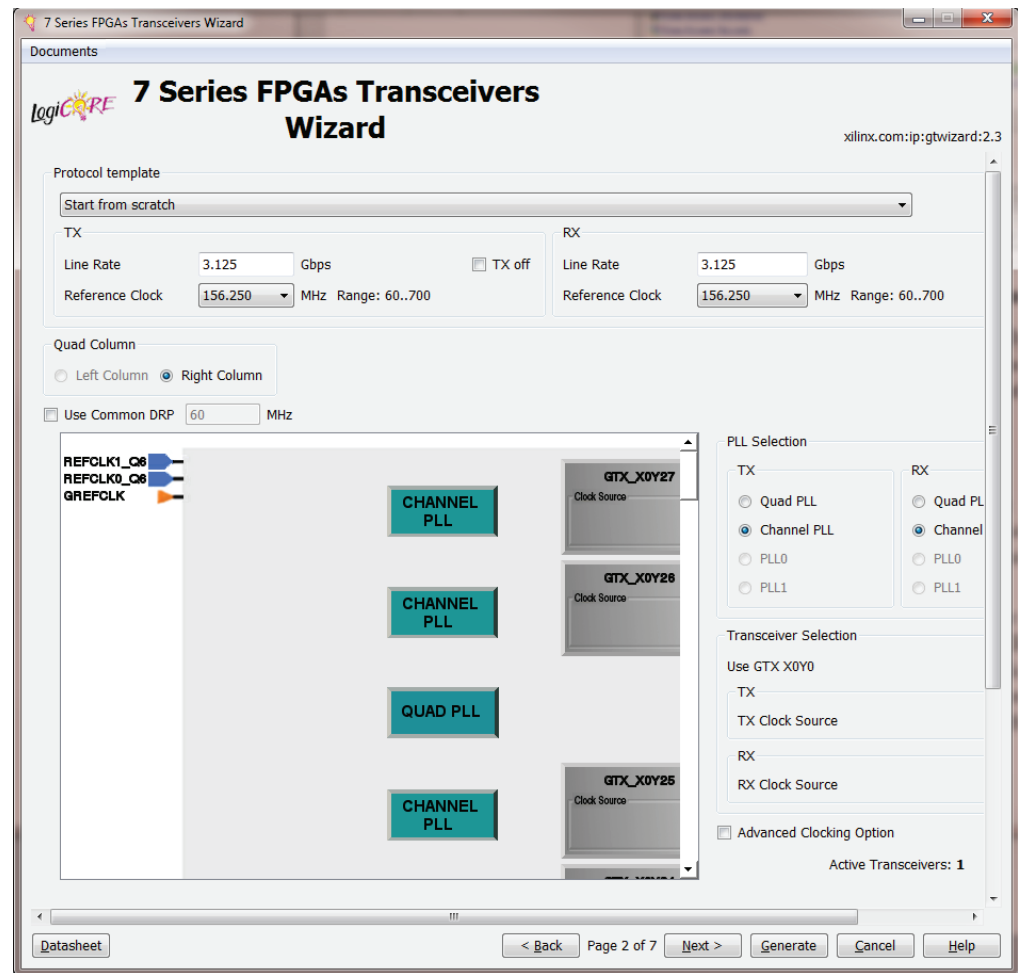
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Figure 10: **7 Series Transceiver Wizard**

Targeted Design Platforms and Targeted Reference Designs for Fast Development Time

Xilinx development kits provide out-of-the box design solutions that significantly cut development time and enhance productivity. Targeted Design Platforms (TDPs) go one step further by providing an evaluation board, Vivado™ Design Suite, IP cores, reference designs, and FPGA Mezzanine Card (FMC) support — so designers can begin application development immediately. Both development kits and TDPs are available across the product families: Virtex-7, Kintex-7, and Artix-7 FPGAs. Figure 11 illustrates the Kintex-7 FPGA connectivity kit. For more development kits, go to http://www.xilinx.com/products/boards-and-kits/index.htm.

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Figure 11: **Kintex-7 FPGA Connectivity Kit**

Broadest Range of Serial IP Protocol Support

The 7 series transceivers support a wide range of line rates (0.5G ~ 28.05 Gb/s) and numerous serial protocols associated within this range. Xilinx and its ecosystem partners, including hundreds of IP design houses, provide a comprehensive serial connectivity IP portfolio for the most popular design protocols, such as Ethernet, PCIe, Interlaken, and OTU. Table 6 shows an example of Xilinx Ethernet IP support. For a comprehensive list of protocols addressed by 7 series transceivers, visit http://www.xilinx.com/products/technology/high-speed-serial/index.htm.

Table 6: **7 Series Transceiver Ethernet IP Support**

Transceivers	100G Ethernet			40G Ethernet			10G Ethernet			
	CAUI-4 4x25G	CAUI 10x10G	10x5G PCS Lanes	XLAUI 4x10G	8x5G PCS Lanes	40G BASE-KR4	RXAUI	DXAUI	XAUI	10G BASE-R/KR
GTZ (Virtex-7 FPGAs)	✓									
GTX/GTH (Virtex-7 and Kintex-7 FPGAs)		✓	✓	✓	✓	✓	✓	✓	✓	✓
GTP (Artix-7 FPGAs)							✓		✓	

7 Series Transceiver Design Example

Figure 12 depicts an example of a 2x100GE line card with a Traffic Manager Design showing three different uses of 7 series serial transceivers.
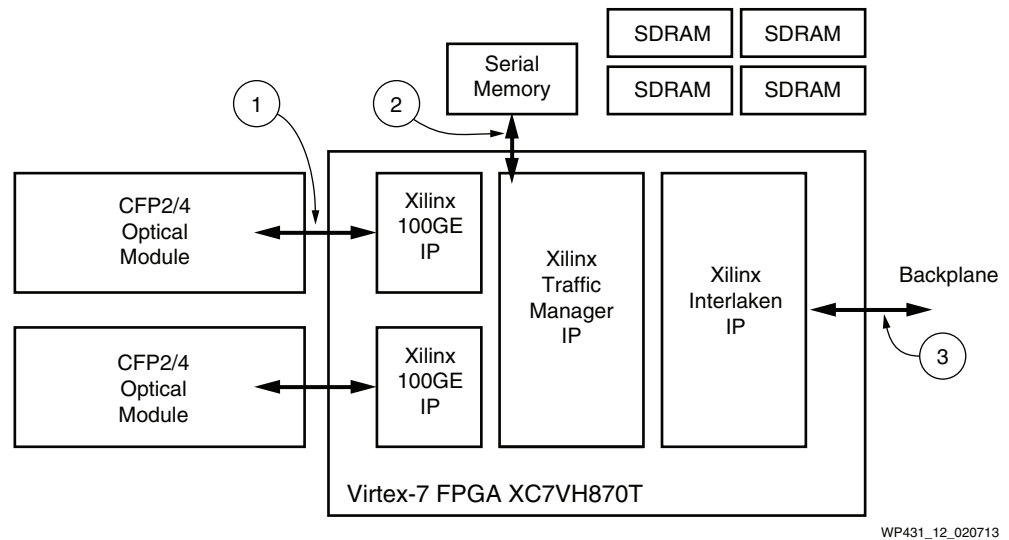
Figure 12: **2x100GE Traffic Manager - Example Transceiver Use Cases**

1. GTZ transceivers (8x25.78 Gb/s) connect directly to CFP2 optics via an OIF VSR channel (6 inch).

2. GTH transceivers (16x10.3125 Gb/s) connect to a serial memory (for storing descriptors used by the Traffic Manager IP) (6 inch).

   Note: This case uses the special "low-power mode" of the GTH transceiver to optimize power for the short channel to the serial memory using TX Emphasis and RX Linear Equalization.

3. GTH transceivers (24x12.5 Gb/s) connect over a mezzanine card connector, mid-plane, or backplane using DFE mode (40 inch).

Figure 13 illustrates a design example for wireless radio head, featuring the 6 Gb/s GTP transceiver in an Artix-7 FPGA. The XC7A200T device has two connections running 6.144 Gb/s Common Public Radio Interface (CPRI) through SFP optical modules. It also talks to Analog Digital Converters (ADC) and Digital Analog Converters (DAC) through JESD204b at 6.25 Gb/s.
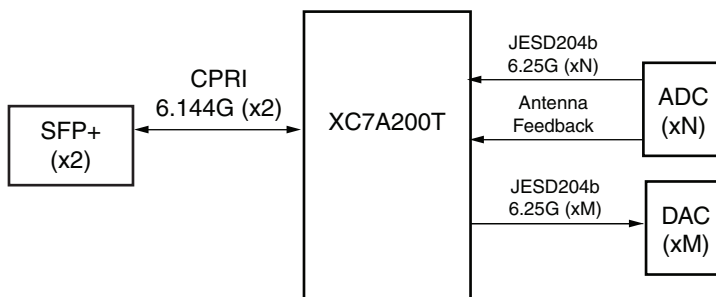
Figure 13: **Artix-7 FPGA Wireless Radio Example**

Summary

7 series FPGAs offer a portfolio of transceivers to scale and optimize from low-end consumer devices to ultra-high-end applications. Each transceiver runs at different target line rates with appropriate signal integrity features.

The Xilinx 28 nm transceiver portfolio delivers value to customers in the following ways:

- High line rate, density, and unmatched system bandwidth
- Flexible clocking architecture and superior jitter performance
- Auto-adaptive receiver equalization for robust backplanes and un-retimed optics
- Hardware eye scan and debug features for easy link tuning
- Tools and resources for transceiver design and implementation

In addition to the silicon, Xilinx continues to provide a series of design resources and an efficient environment for customers using 7 series transceivers.

For more information on 7 series transceivers, such as user guide, white papers, development kits, etc., go to:
http://www.xilinx.com/products/technology/high-speed-serial/.

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
03/18/13	1.0	Initial Xilinx release.

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