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Getting Started with Artix-7 FPGAs

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The scalable, optimized architecture of the Xilinx® 7 series FPGAs provides for easy design migration between members of its families. This permits the designer to use an available 7 series device from one family as a hardware emulation platform for a device in another family—in advance of the target device's availability. Some key similarities between the Artix™-7 and Kintex™-7 FPGA families are described, and an example illustrates how the available Kintex-7 XC7K325T FPGA can be used as a hardware emulation platform for designs that will ultimately target Artix-7 FPGAs.

Introduction

The Xilinx 7 series families, Artix-7, Kintex-7, and Virtex®-7 FPGAs, employ a scalable, optimized architecture, providing unparalleled portability, scalability, and productivity. Devices in these three families are designed with the same architectural building blocks using the fourth-generation ASMBL™ architecture, including the same logic fabric (CLB and routing), block RAM, DSP slices, and clocking technology. In the past, Xilinx products were designed uniquely for each silicon family, requiring device-specific handling and processes throughout development. Beginning with the 7 series FPGAs, Xilinx has adopted a reuse approach that leverages design blocks across the entire family. This approach has not only reduced complexity in terms of layout, simulation, characterization, test development, and reliability, but also streamlines activities that contribute to a more repeatable and reliable technology delivery process.These design, manufacturing, and test advantages benefit the user by providing faster device availability and the ability to migrate designs between the different 7 series families with ease.

Design tools supporting the Artix-7, Kintex-7, and Virtex-7 FPGAs are available today, enabling the user to design towards the device of their choice. Artix-7 FPGA designs can be created and simulated to verify fit and timing in advance of having silicon. For example, a design can be started in an Artix-7 device and then be retargeted to a Kintex-7 device for hardware emulation to ensure that the design will fit in the final Artix-7 device. This document helps the user to target a design to a Kintex-7 FPGA with the goal of performing hardware emulation and evaluation of the Artix-7 FPGA to be used in the end application.

Artix-7 vs. Kintex-7 FPGA Families

Conceived and designed for high-volume markets, Artix-7 FPGAs deliver the lowest power consumption and lowest cost in the 7 series. The family shares the same building blocks as the Kintex-7 and Virtex-7 FPGA architecture on the same 28 nm High Performance, Low Power (HPL) process, but transistor-level design choices enable the Artix-7 family to offer much lower power consumption while still meeting the performance needs of the target applications. The Artix-7 family establishes a new standard for best cost for higher-speed interfaces, including memories and transceivers. By leveraging wire-bond, chip-scale BGA technology, Artix-7 FPGAs further reduce system cost through their fabrication in some of the smallest footprint packages available.

While most architectural components are identical between Artix-7 and Kintex-7/Virtex-7 devices, optimizing some components for data rates required by the target applications enables additional power reductions relative to Kintex-7/Virtex-7 devices. For example, the GTP transceiver in Artix-7 FPGAs is similar to the GTX and GTH transceivers provided in the other 7 series families, but the Artix-7 family is not designed to reach the same very high data rates. Therefore, design modifications can be made to the Artix-7 device to provide a greater power reduction than running a higher performance transceiver at a lower data rate.

Table 1 compares the Artix-7 architecture to the Kintex-7 architecture.

Table 1: **Comparing Architectural Resources in Artix-7 and Kintex-7 FPGAs**

Architectural Resource	Artix-7	Kintex-7	Notes
CLB	Same	Same	Same features so designs can port easily between families. The Artix-7 FPGA has reduced maximum frequency due to reduced power architecture.
DSP	Same	Same	
Block RAM	Same	Same	
Clocking Architecture	Same	Same	
I/O	High Range (HR) only	HR and High Performance (HP)	Artix-7 FPGA has lower maximum frequency of operation than families offering HP I/O banks.
Memory Interface	Same components	Same components	Same architectural components and I/O standards for supporting DDR3, DDR3L, DDR2, QDRII+, and RLDRAM II. The Artix-7 FPGA maximum interface rate is limited by I/O performance.
Transceiver	GTP	GTX	The Artix-7 FPGA is optimized for lower power and lower maximum data rate.
PCI Express	X4 Gen2	X8 Gen2	Fewer lanes are possible in Artix-7 devices.
XADC	Same	Same	Same Agile Mixed Signal capability in all 7 series FPGAs.

The performance differences due to the various transistor-level design choices are shown in Table 2.

Note: Always refer to the most current device data sheets on www.xilinx.com for the latest performance characteristics.

Table 2: **Artix-7 and Kintex-7 Data Sheet Parameters**

	Artix-7 Family			Kintex-7 Family		
Speed Grade:	**-1**	**-2**	**-3**	**-1**	**-2**	**-3**
General FPGA Block Performance						
Fabric Performance (relative to Artix-7 FPGA -1 speed grade)	1	1.15	1.3	1.67	1.9	2.15
I/O Performance						
HR LVDS (Mb/s)	950	1,250	1,250	950	1,250	1,250
HP LVDS (Mb/s)	–	–	–	1,250	1,400	1,600
PCIe Maximum Lane Width Supported						
PCIe Gen2	–	x4	x4	x4	x8	x8
Transceiver Performance						
GTP (Gb/s)	3.75	6.6	6.6	–	–	–
GTX (Gb/s)	–	–	–	6.6	10.5	12.5
Memory Interface Performance						
DDR3 (Mb/s) HR I/O	800	800	1,066	800	1,066	1,066
DDR3 (Mb/s) HP I/O	–	–	–	1,600		1,866

Logic, Interconnect, DSP, Clocking, and Block RAM

The configurable logic block (CLB), interconnect, DSP slice, clock management tiles (CMTs), and block RAM in the Artix-7 architecture are identical to the blocks in Kintex-7 FPGAs. Both families use the fourth-generation ASMBL architecture, which allows columns of identical resources to be combined, providing the optimum mix to achieve target system performance, cost, and device size.

Figure 1 and Figure 2 show a graphical representation of the relative number of DSP slices and block RAM blocks per logic density of the Artix-7 family and the Kintex-7 XC7K325T FPGA.

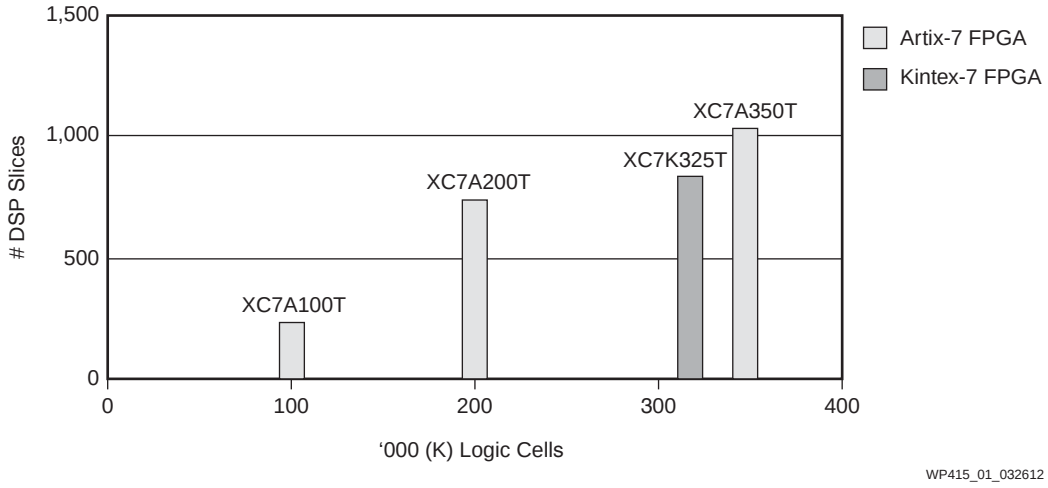

Figure 1: **Artix-7 and Kintex-7 FPGA DSP Resources**

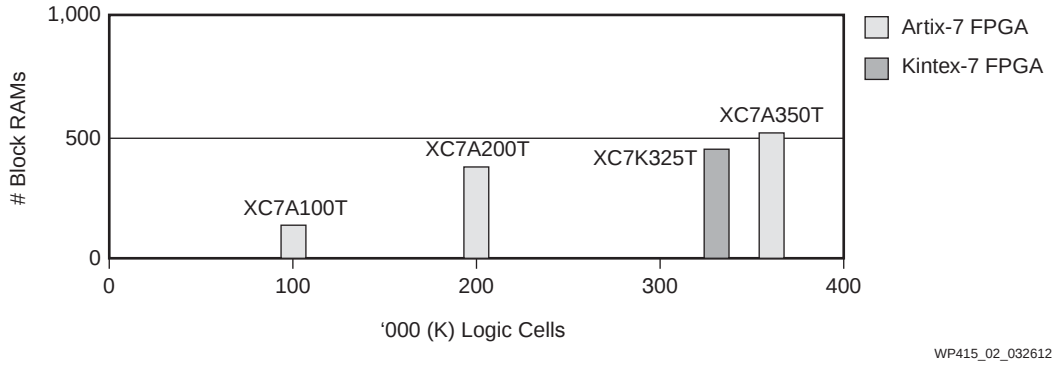

Figure 2: **Artix-7 and Kintex-7 FPGA Block RAM Resources**

Table 3 provides the exact number of DSP and block RAM resources in the Artix-7 FPGAs and the XC7K325T. The XC7K325T provides more block RAM and DSP capability than the XC7A100T and XC7A200T devices. The block RAM and DSP resources in the XC7A350T exceed those of the XC7K325T, so the design must not exceed the maximum resources in the target Artix-7 FPGA.

Table 3: **Resources in Artix-7 FPGAs vs. the Kintex-7 XC7K325T FPGA**

Resources	Artix-7			Kintex-7
	XC7A100T	XC7A200T	XC7A350T	XC7K325T
Logic Cells	101,440	215,360	360,000	326,080
DSP Slices	240	740	1,040	840
Block RAM	135	365	515	445

I/O Blocks

There are two styles of I/O in 7 series FPGAs: High Range (HR) I/O, supporting interface voltages up to 3.3V, and High Performance (HP) I/O, supporting interface voltages up to 1.8V—but at a higher level of maximum performance. All 7 series FPGA I/O is arranged in banks of 50; the total number of bonded I/Os varies, depending on the device size and package. Artix-7 FPGAs use only HR I/O blocks, whereas most Kintex-7 device/package offerings combine HR *and* HP I/O blocks. The Performance Characteristics section of each device data sheet provides the maximum interface voltages and speeds for the I/O types available in that device.

Table 4 contains a full list of the differences between the HR and HP I/O banks, shown grouped under Artix-7 and Kintex-7 devices.

Table 4: **Comparison of HR and HP I/O Bank Capabilities**

Features	Artix-7 Devices: HR I/O Only		Kintex-7 Devices: HR and HP I/O(1)	
	HR	HP	HR	HP(1)
1.2V to 1.8V I/O standards	✓	N/A	✓	✓
2.5V to 3.3V I/O standards	✓	N/A	✓	*no*
SSTL12, DIFF_SSTL12, HSTL_I_12, LVDS (1.8V), LVCMOS (2mA) I/O standards	*no*	N/A	*no*	✓
24 mA drive option for LVCMOS18 outputs	✓	N/A	✓	*no*
V_{CCAUX_IO} supply rail	*Note 2*	N/A	*Note 2*	✓
Digitally-controlled impedance (DCI) and DCI cascading	*no*	N/A	*no*	✓
IN_TERM	✓	N/A	✓	*no*
Internal V_{REF}	✓	N/A	✓	✓
Internal differential termination (DIFF_TERM)	✓	N/A	✓	✓
IDELAY	✓	N/A	✓	✓
ODELAY	*no*	N/A	*no*	✓
IDELAYCTRL	✓	N/A	✓	✓
ISERDES	✓	N/A	✓	✓
OSERDES	✓	N/A	✓	✓
ZHOLD_DELAY	✓	N/A	✓	*no*

Notes:

1. A small number of Kintex-7 device/package combinations do not provide any HP I/O banks. See DS180, *7 Series FPGAs Overview* for details.
2. V_{CCAUX_IO} supply rail not required for HR I/O.

One of the major differences between HR I/O and HP I/O banks is the termination. The HP I/O banks feature digitally controlled impedance (DCI), which controls the output impedance of the driver or adds parallel termination at the driver and/or receiver to match the characteristic impedance of the transmission line. The HR I/O banks have a simpler method for terminating the I/O: uncalibrated input termination, known as IN_TERM. It is available on all SSTL and HSTL I/O standards. *The behavior of these two termination methods is different*, and this must be taken into account when migrating between HP and HR I/O banks. For more information, see UG471, *7 Series FPGAs SelectIO Resources User Guide*.

Memory Interface

Memory interfaces in all 7 series FPGAs use the dedicated memory interface logic located in the clock management tile (CMT) column and the I/O column. This logic is the same in Artix-7 and Kintex-7 FPGAs, resulting in minimal effort to transport a memory interface design from a Kintex-7 to an Artix-7 device. The maximum physical interface rate for memory interfaces is dictated by the maximum performance of the I/O banks. The HR I/O banks available in the Artix-7 architecture are capable of interfacing to DDR3 at up to 1,066 Mb/s. This I/O implementation provides a very high interface performance that is more than adequate for most applications; the HP I/O available in most Kintex-7 FPGAs, however, is even faster, capable of interface rates as high as 1,866 Mb/s. The Performance Characteristics sections of the device data sheets provide the maximum physical interface rates for memory interfaces.

Memory interfaces implemented in an HP I/O bank typically take advantage of the DCI termination, whereas memory interfaces implemented in an HR I/O bank normally use IN_TERM termination. In addition, Kintex-7 devices in the FFG package have the ability to separate out the V_{CCAUX_IO} pre-driver power supply and elevate it to 2.0V for higher performance memory interfacing. All Artix-7 devices, as well as Kintex-7 devices in FBG packages, simply use the common 1.8V V_{CCAUX} supply to bias the I/O pre-drivers. When emulating an Artix-7 design in a Kintex-7 FPGA, V_{CCAUX_IO} can be connected to the same supply as V_{CCAUX}.

GTX and GTP Transceivers

Transceivers in 7 series FPGAs are arranged in Quads. A Quad is a cluster or set of four transceiver channels that share certain resources.The location of the Quads varies depending on the device targeted. The GTP transceivers in the Artix-7 XC7A100T device occupy a portion of the I/O and CMT column on the right side of the device, similar to the location of the GTX transceivers in Kintex-7 FPGAs. The GTP transceivers in the Artix-7 XC7A200T and XC7A350T, however, are located nearer the center of the device, adjacent to the global clocking column, allowing multiple transceivers and a high I/O count in the same package. Figure 3 shows the different device layouts.

> ***Note:*** This figure is a symbolic representation intended to illustrate transceiver location on the die. It does not depict all the device's resources and is not drawn to scale.

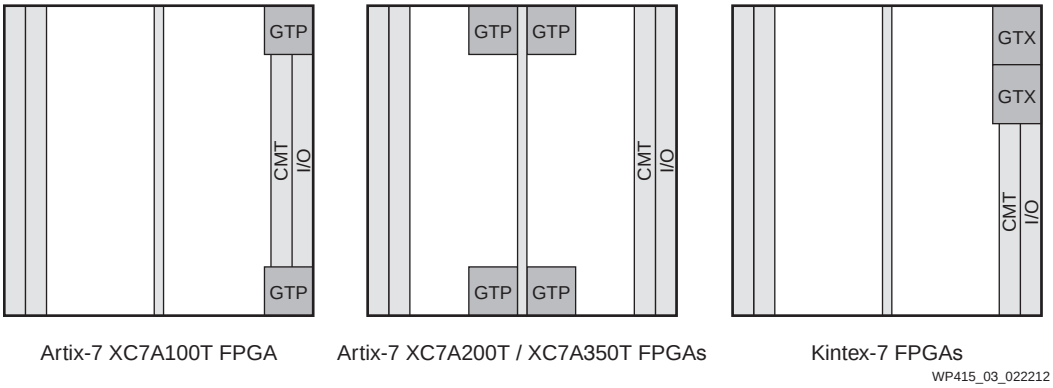

Figure 3: **Location of Transceivers in Artix-7 and Kintex-7 Architectures**

Moving between the Kintex-7 FPGA GTX and the Artix-7 FPGA GTP Transceivers

The transceivers in the Kintex-7 and Artix-7 FPGAs are very closely related, simplifying the migration process from a GTX transceiver design in a Kintex-7 device to a GTP transceiver design in an Artix-7 device. Taking advantage of those similarities requires some planning at the outset of the design to ensure that the features being used are coherent between the two families. The following sections are intended to help guide designers through the necessary choices to make the transition as simple as possible.

Using the 7 Series Transceiver Wizard

The 7 series Transceiver Wizard, found in the CORE Generator™ tool, is the recommended interface for generating transceiver instantiations in Xilinx FPGAs. The GUI provided gives designers all of the options available for the 7 series transceivers and generates HDL code that implements the transceivers and the necessary surrounding logic for resets and clocking. By using the wizard for both Kintex-7 and Artix-7 FPGA designs, the ports presented to the user HDL are kept largely the same, limiting the changes needed to be implemented in the design.

Implementation Decisions

Even when using the wizard, certain considerations need to be reviewed to ensure easy portability between Kintex-7 and Artix-7 FPGA designs. This is due to select architectural differences between the GTX and GTP transceivers.

PLL Selection

The GTP transceiver can support two native line rates within a Quad. While each transceiver in a Quad has its own dividers on the PLL clock, enabling /2, /4, or /8 versions of that native rate, there are two PLLs from which to derive this clock. The Kintex-7 FPGA GTX transceiver can support up to five line rates within a Quad (between TX and RX) so only two native rates can be implemented via the 7 Series Transceiver Wizard to ensure portability of the design.

There are differences in the clocking structures and the rates they support between the Kintex-7 FPGA GTX and Artix-7 FPGA GTP transceivers. The Artix-7 FPGA GTP transceiver uses two highly flexible ring oscillators for performance up to 6.6 Gb/s, both located within a primitive referred to as the GTPE2_COMMON, that can each drive the RX or TX datapaths of any transceiver in the Quad. The Kintex-7 FPGA GTX

transceiver has the same ring oscillators, but they are located in individual GTX transceiver instances and cannot be shared by transceivers in a Quad. The GTXE2_COMMON block in the Kintex-7 device houses a single LC tank oscillator that can be shared by each transceiver in the Quad.

These comparisons and differences are shown in the schematic diagram in Figure 4.

Implementing more than a single protocol within a GTP transceiver Quad requires sharing the GTPE2_COMMON outputs between wizard instances. This resembles sharing the GTXE2_COMMON outputs among multiple protocols and wizard instances, but it can support two native line rates because it contains both ring oscillators.

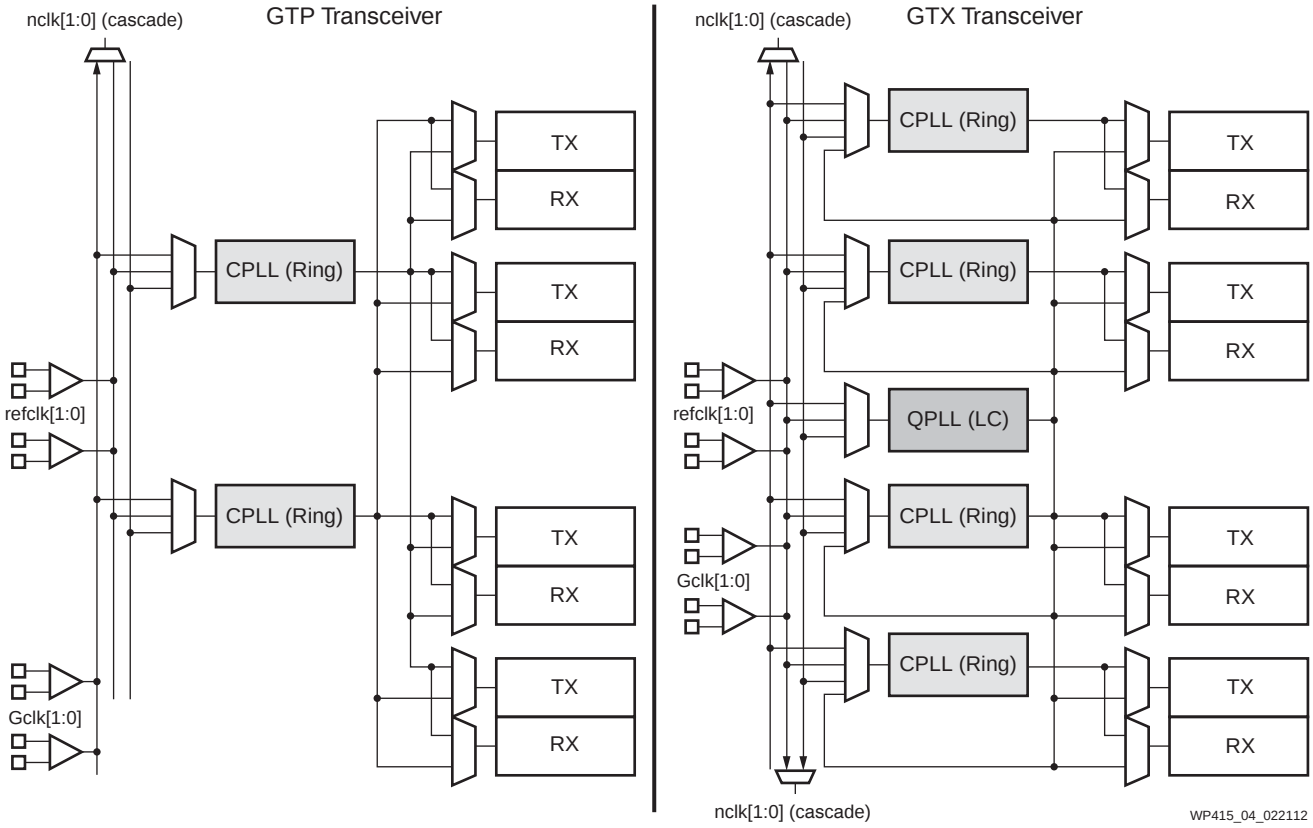

Figure 4: **Comparison of GTP and GTX Transceiver Layouts**

Reference Clock Routing

Reference clock forwarding is performed slightly differently in the GTP and GTX transceivers, as illustrated in Figure 5. To share a reference clock across multiple Quads, those Quads must be immediately adjacent to each other. In the Kintex-7 device, the GTX transceivers are vertically adjacent to one another on the right-hand side of all devices, enabling one GTX transceiver above or below to share the reference clock at rates below 6.6 Gb/s. The Artix-7 architecture has two possible layouts, both of which put one set of transceivers at the top of the device and another set at the bottom of the device. Only in the larger Artix-7 devices, the XC7A200T and XC7A350T, are there two Quads at the top and bottom of the device, and in those situations the reference clock can be shared only between those Quads.

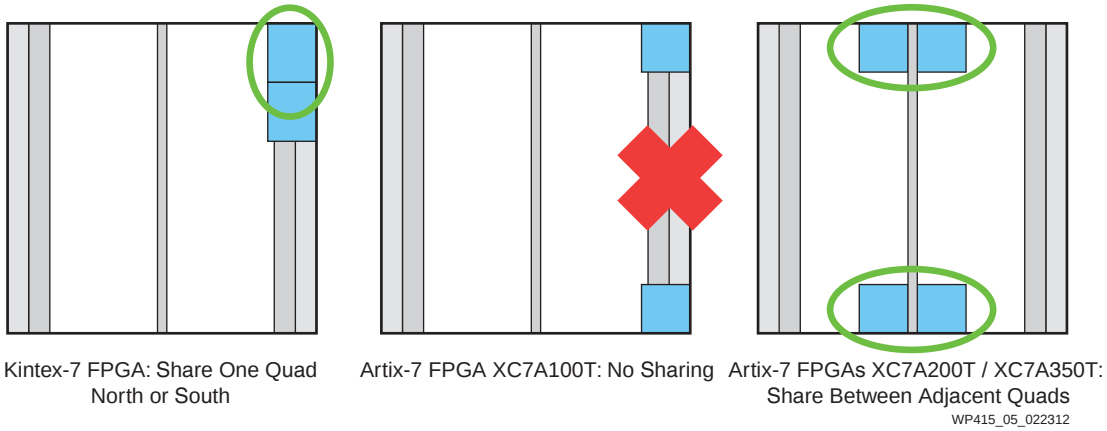

Figure 5: **Transceiver Quads That Can Share Reference Clocks**

Designing a board that can be easily ported to an Artix-7 device requires considering the equalization capabilities of the GTX and GTP transceivers and the power supplies that they require.

Fabric Clocking

The Kintex-7 FPGA GTX transceiver can optionally use an internal 4-byte datapath width (required only for the highest data rates) that does not exist in Artix-7 devices. The major impact of this difference is the requirement for different frequency USRCLK signals. The transceiver wizard generates the necessary clock topologies required for each family of devices. However, if a designer is leveraging the GTX/GTP transceiver clocking in the rest of the design, choosing the 2-byte internal datapath in the Kintex-7 device allows the design to port more readily to an Artix-7 device.

Board-Level Considerations

Channel Design

The GTX transceiver has a decision feedback equalizer (DFE) in conjunction with a continuous time linear equalizer (CTLE) that allows it to compensate for very difficult channels. Since even the most difficult 6.6 Gb/s channels do not require the advanced equalization provided by a DFE circuit, the Artix-7 FPGA GTP transceiver implements only a CTLE circuit. While this is sufficient for the vast majority of designs, it is important to consider this in the board design.

Power Supply

Because the Artix-7 FPGA GTP transceivers do not possess the LC tank oscillator, the MGTVCCAUX supply does not exist. To simplify the Kintex-7 FPGA board design, the ring oscillators in the channel PLLs can be utilized, and MGTVCCAUX can be connected to V_{CCAUX} without filtering. Additionally, the termination resistor calibration circuit is implemented inside the device itself; it does not need to be implemented by the board designer.

PCIe Integrated Block

All 7 series FPGAs include at least one integrated block for PCI Express®. Kintex-7 FPGAs support PCIe up to x8 Gen2, whereas Artix-7 FPGAs support fewer channels, up to x4 Gen2. For easiest transition to Artix-7 FPGAs, the user should not implement a PCIe interface wider than x4 Gen2.

Device Layout

To make identification of I/O banks and Quads easier, the banks and Quads are numbered based on their location. All I/O banks on the left side of the device start with a '1,' e.g., '12.' All I/O banks on the right side start with a '3,' e.g., '32.' Similarly, all Quads on the right side of the device start with a '1,' e.g., '112,' and all transceivers on the left center of the device (XC7A200T and XC7A350T) start with a '2,' e.g., '212.' See Figure 6.

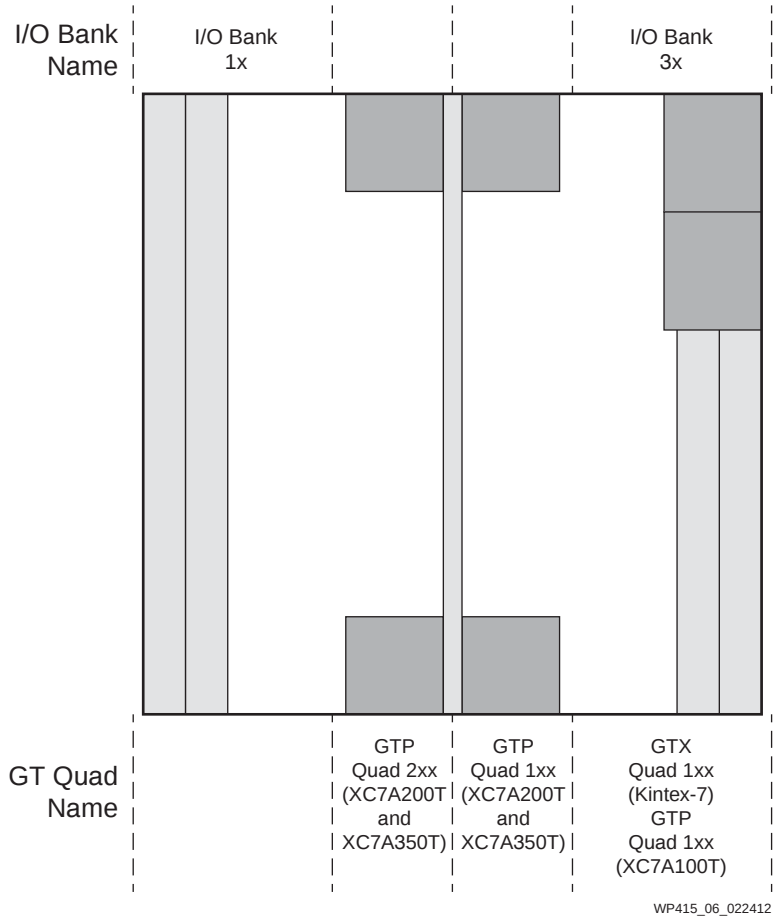

Figure 6: **I/O Banks and Quad Numbering**

Packaging

The packages used by Artix-7 FPGAs are focused on delivering the best cost point possible for the performance required. To accomplish the lowest possible costs and deliver the desired Artix-7 FPGA value, exact pin migration between Artix-7 and Kintex-7 FPGAs was not implemented. For design migration, 7 series FPGAs feature a

scalable, optimized architecture, which eases the transition from one family to another.

While there are different quantities of resources in the different devices and families, all 7 series FPGAs have clock regions 50 CLB rows tall associated with I/O banks of 50 I/Os. When the Kintex-7 XC7K325T-FFG900 device is used on the KC705 board as a hardware emulation platform for an Artix-7 FPGA, the user must consider which I/O banks and transceivers are available in the destination device/package. Table 5 describes the available I/O banks and transceivers in the different device/package combinations, showing which I/O banks and transceivers are fully bonded, partially bonded, unbonded, or not present in the different device/package combinations.

Table 5: **Decoder Ring of Available and Bonded I/O Banks and Transceivers**

Left Side		XC7A100T				XC7A200T				XC7A350T			XC7K 325T	Right Side	
I/O Bank	GT Quad	FTG 256	CSG 324	FGG 484	FGG 676	SBG 484	FBG 484	FBG 676	FFG 1156	FBG 484	FBG 676	FFG 1156	FFG 900	I/O Bank	GT Quad
		X	X	X	X	X	X	X	X			HR	X	37	
		X	X	X	X				HR			HR	X	36	
		HR	HR	HR	HR	HR	HR	HR	HR	HR	HR	HR	X	35	
		HR	HR	HR	HR	HR	HR	HR	HR	HR	HR	HR	HP	34	
		X	X	X	X			HR	HR		HR	HR	HP	33	
		X	X	X	X				HR			HR	HP	32	
18		X	X	X	X	X	X	X	X	X	X	X	HR		
17		X	X	X	X	X	X	X	X			HR	HR		
16			HR	HR	HR	HR	HR	HR	HR	HR	HR	HR	HR		
15		HR	HR	HR	HR	HR	HR	HR	HR	HR	HR	HR	HR		
14		HR	HR	HR	HR	HR	HR	HR	HR	HR	HR	HR	HR		
13				HR	HR	HR	HR	HR	HR	HR	HR	HR	HR		
12		X	X	X	X			HR	HR		HR	HR	HR		
	217	X	X	X	X	X	X	X	X	GTP	GTP	GTP	X		
	216	X	X	X	X	GTP	GTP	GTP	GTP	X	X	X	X		
	212	X	X	X	X			GTP	GTP		GTP	GTP	X		
		X	X	X	X	X	X	X	X	X	X	X	GTX		118
		X	X	X	X	X	X	X	X			GTP	GTX		117
				GTP	GTP				GTP	X	X	X	GTX		116
		X	X	X	X	X	X	X	X	X	X	X	GTX		115
					GTP	X	X	X	X	X	X	X	X		113
		X	X	X	X				GTP			GTP	X		112

Fully bonded
Partially bonded
Unbonded

X	Not present in this device
HR	High Range I/O banks
HP	High Performance I/O banks
GTP	GTP transceivers
GTX	GTX transceivers

KC705 Connections

For the Kintex-7 XC7K325T FPGA KC705 board to be a useful hardware emulation platform for Artix-7 FPGAs, it is necessary to know which components are connected to which I/O banks and transceivers of the Kintex-7 FPGA. Figure 7 provides an illustration of the main functions performed by the I/O banks and transceivers on the KC705 board. For a full list of KC705 pinouts and UCF, refer to UG810, *KC705 Evaluation Board for the Kintex-7 FPGA User Guide*.

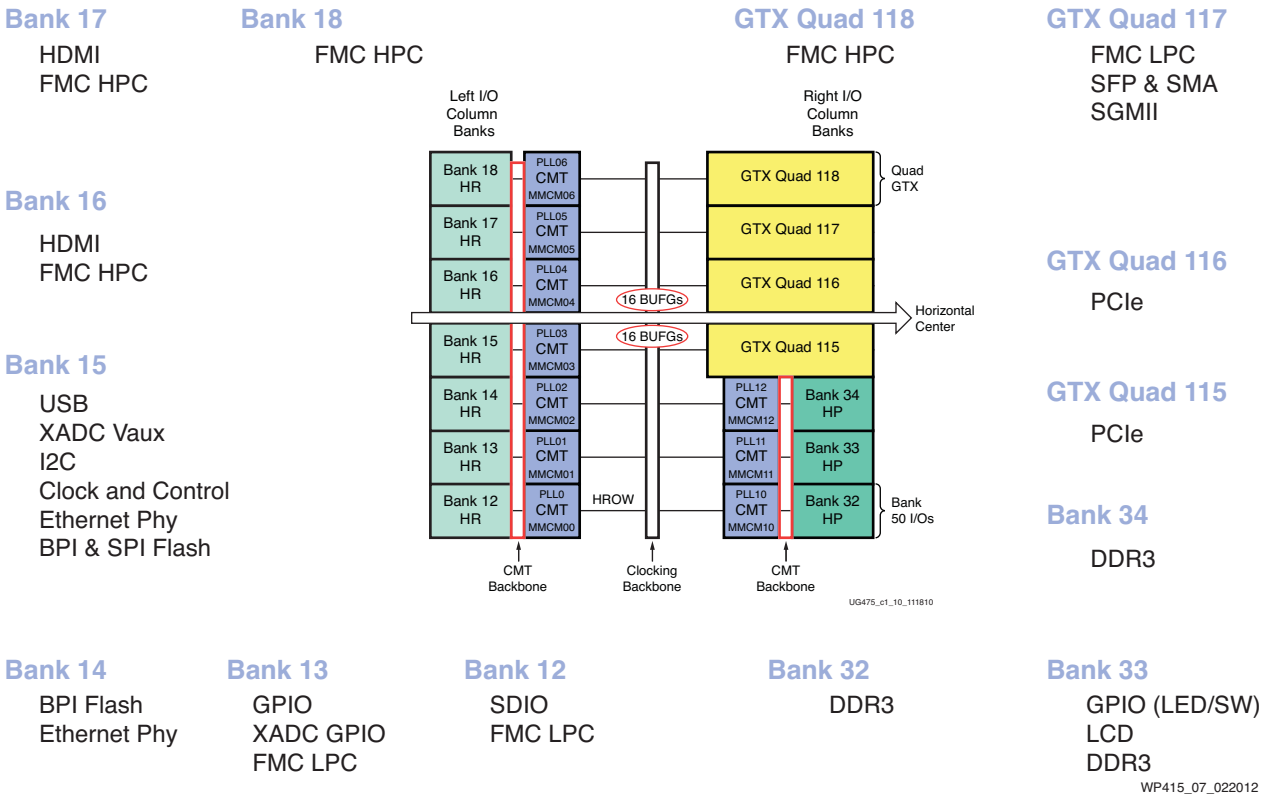

Figure 7: **Main Functions of I/O Banks and Transceivers on KC705 Board**

Design Guidelines

The simplest route to using a KC705 board as a hardware emulation platform for an Artix-7 FPGA is to use only those features that are present in both devices. Some specific areas on which to focus attention are listed here:

- There are 32 global clock buffers in every 7 series FPGA; 16 are driven from resources *above* the horizontal center of the device, and 16 are driven from resources *below* the horizontal center.
- While there are four transceiver Quads in the XC7A200T, XC7A350T, and XC7K325T devices, the location of the Quads relative to the horizontal center of the device varies due to the different device layouts illustrated in Figure 3.
- While the transceiver Quads in the XC7A200T and XC7A350T are located toward the center of the device, the connectivity is largely the same as the transceivers on the right edge of the device, as seen in the Kintex-7 family.

    - Clock signals generated by the transceivers can drive both the BUFH and BUFG buffers located in the vertical clocking column in the vertical center of the device.
    - Clock signals generated by the transceivers cannot drive the BUFMR multi-region clock buffer in either Artix-7 or Kintex-7 FPGAs.
    - Only adjacent GTP transceiver Quads (in the XC7A200T and XC7A350T devices) can share reference clocks between GTP transceivers in different Quads.
- The GT Wizard tool is the recommended flow for generating transceiver instantiations. There are several features supported in the GTX transceivers that are either not present or not required by the GTP transceivers.
    - GTP transceivers support two line rates per Quad, as opposed to the five line rates supported by the GTX transceivers.
    - The GTP transceiver maximum line rate is 6.6 Gb/s, which the GTX transceiver can support identically using ring oscillators/PLLs or by using the LC tank oscillators and the TX- and RX-specific output dividers.
    - The power supplies are the same for the GTP and GTX transceivers, except that the GTP transceiver does not use the MGTVCCAUX supply.
- There are fewer DSP and block RAM resources in some Artix-7 devices than in comparable Kintex-7 devices. Kintex-7 FPGA resources must be tracked carefully to avoid using more than are available in the target Artix-7 device.
    - If use of the XC7A350T device is intended, note that this device has more block RAM and more DSP slices than the XC7K325T, so the user can use all the block RAM and DSP slices in the XC7K325T.
    - If use of the XC7A200T or XC7A100T device is intended, note that these devices have less block RAM and less DSP slices than the XC7K325T, so the user must limit resource usage to the quantity available in the destination device. See Table 5.
- Avoid using the I/O features that are unique to the HP I/O (DCI and ODELAY).
    - The HR I/O in Artix-7 devices does not have DCI or ODELAY, so for the easiest transition to the Artix-7 family, the user should avoid using these features.
- The maximum performance of the HR banks in Artix-7 devices is lower than the maximum performance of the HP I/O banks on which the memory interface is implemented on the KC705 board.
- The DDR3 memory on the KC705 board is connected to the HP I/O banks (32, 33, 34), which are HR I/O banks in the Artix-7 family.
    - Banks 32, 33, and 34 are not available in all Artix-7 device/package combinations.

Summary

The scalable, optimized architecture upon which the Xilinx 7 series FPGAs are built enables users to use the Kintex-7 XC7K325T on the KC705 evaluation board as an early hardware emulation platform for their Artix-7 designs. There are many similarities between Artix-7 and Kintex-7 FPGAs, but there are also some differences, due to the optimizations designed in to the Artix-7 family. The result is a family of FPGAs featuring both lowest cost and lowest power consumption. With the guidelines provided, the user can focus on the critical differences between the families to ensure an easy transition from a Kintex-7 FPGA design to an Artix-7 FPGA design.

For more information about the features and resources of the Artix-7 family, go to the Artix-7 FPGA family web page at:
http://www.xilinx.com/products/silicon-devices/fpga/artix-7/index.htm

Also refer to:

DS181, Artix-7 FPGAs Data Sheet: DC and Switching Characteristics

DS182, Kintex-7 FPGAs Data Sheet: DC and Switching Characteristics

UG471, 7 Series FPGAs SelectIO Resources

UG472, 7 Series FPGAs Clocking Resources

UG483, 7 Series FPGAs PCB Design and Pin Planning Guide

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
03/02/12	1.0	Initial Xilinx release.
03/27/12	1.0.1	Corrected graph color per legends in Figure 1 and Figure 2.

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