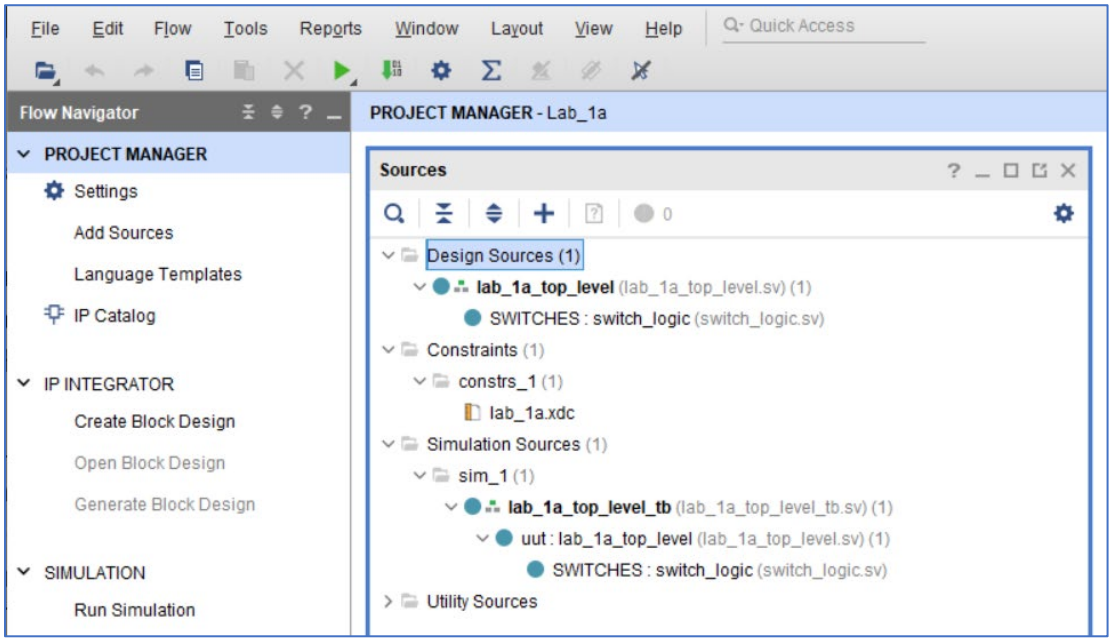
Lab 1a – Introduction to Vivado and Basys3

Introduction

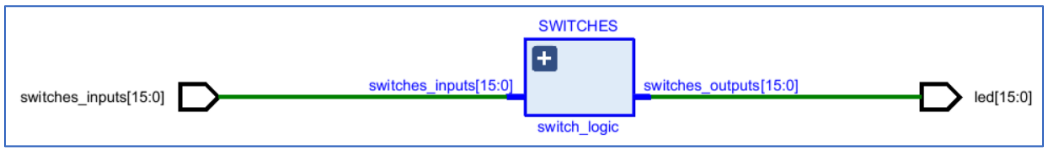
Lab 1a and 1b will help you become familiar with Xilinx Vivado and the Digilent Basys3 FPGA board. You will learn how to synthesize a design, simulate it, and download it to the board for testing.

Procedure

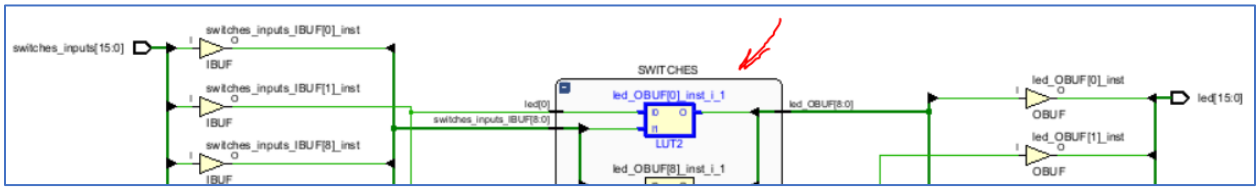
1. Prior to the lab*, watch the all the lecture videos for this week and the previous week. Also watch the tutorial video for this lab, where you will learn how to use Xilinx Vivado and the Basys3 board. This video shows the main steps in this lab activity. Also read this lab document in full and be prepared to start the lab immediately. **the term "Lab" is used in this document for convenience and it translates to "Active Learning Mini-Project," in terms of the Course Outline.*
2. Create a new project in Vivado and be sure to pick the correct FPGA part (xc7a35tcpg236-1).
3. Add the **Design Sources**: *lab_1a_top_level.sv* and *switch_logic.sv*.
4. Add the testbench in **Simulation Sources**: *lab_1a_top_level_tb.sv*.
5. Create a copy of the *Basys_3_Master.xdc* file and rename it *lab_1a.xdc*. Add the constraints file to **Constraints**. Edit the constraints file to match the top level signals in *lab_1a_top_level.sv*. You should just need to change "*sw*" to "*switches_inputs*" in the *##Switches* section (starting around line 13).
6. Double-check that your Sources look similar to the picture below. If not, go back and correct your project.

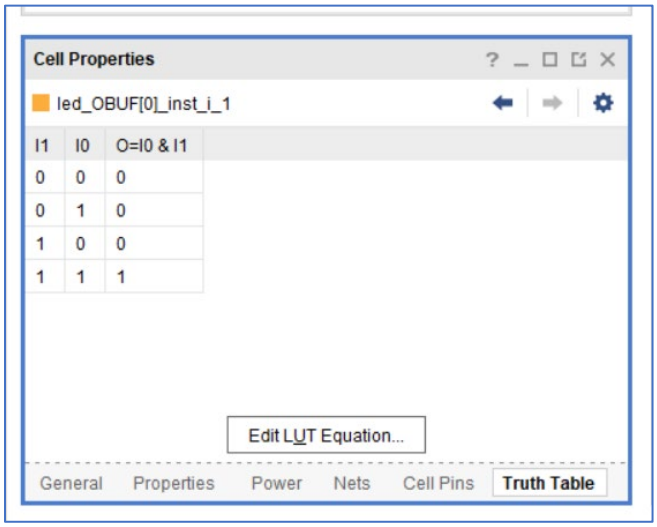


7. Under RTL ANALYSIS, click Run Linter, then Schematic. You should see a schematic like the picture below. Click on the "+" sign inside the SWITCHES block and the internal circuit should be exposed (with the AND and INVERTER). This schematic is the more "human readable" schematic, that is comprised of generic digital logic components, irrespective of the actual FPGA circuits that implement the logic. We will call this the "RTL Schematic." **DO: Take a snip of the entire RTL Schematic, like the picture below, but with the internal circuit also shown, and paste it into your Design Record document.**



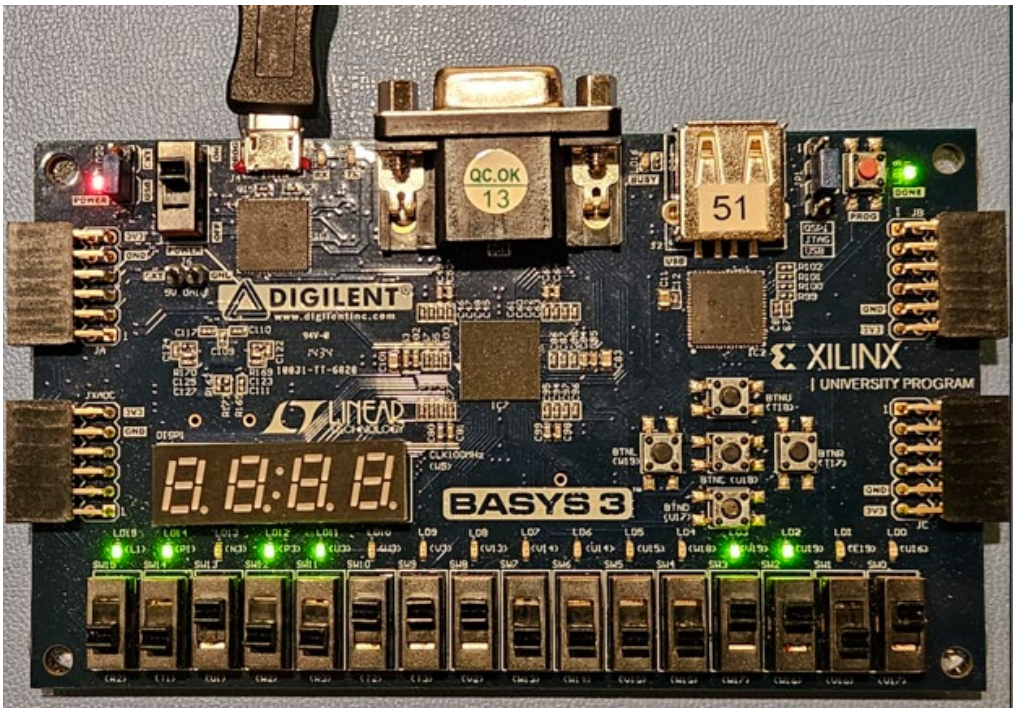
8. Under SYNTHESIS, click Run Synthesis, then Schematic. Again, click the "+" sign inside the SWITCHES block, to expose the internal circuit. You should see components such as IBUF, LUT, and OBUF. This schematic is the how the logic is implemented with the available FPGA resources. We will call this the "Technology View." **DO: Take a snip of the entire Technology View Schematic with the internal circuit also shown, and paste it into your Design Record document.**
9. Double-click on the LUT2, inside SWITCHES (see picture below). Then the Cell Properties window should pop up (see picture below). Click on the Truth Table and try to understand what LUT2 represents in your design, with regard to the RTL Schematic. **DO: Take a snip of your Cell Properties window and paste it into your Design Record document. Write an explanation of what LUT2 represents in the design.**





10. Under PROGRAM AND DEBUG, click Generate Bitstream. This will also run the Implementation step. Follow the steps as show in the video to connect the Basys3 to the computer and to download the bitstream to the Basys3. That is, Open Hardware Manager > Open Target > Program Device. These steps will vary, depending on your Vivado session and whether you have already connected to the Basys3.

11. Your Basys3 should look something like the picture below. Move the slide switches and verify that the LEDs light up as expected for all the slide switches and their positions, based on the SystemVerilog code. Press down on the push buttons and see what happens. **DO: record your observations for the slide switches and pushbuttons, in the Design Record.**



12. Under SIMULATION, click on Run Simulation. Change the Radix of the signals to Binary. Click the Zoom Fit button so that you can see all the waveforms. Examine the waveforms to confirm the functionality on the SystemVerilog code. **DO: take a snip of your simulation waveforms and paste it in the Design Record.** NOTE: you normally do this in the reverse order, i.e. simulate first, then verify on the Basys3.
13. Modify the SystemVerilog code so that all the LEDs are OFF when the slide switches are in the up position (i.e. pointed towards the center of the Basys3), and ON when they are in the down position. Be sure to write explanatory comments. Resynthesize and download the new design to the Basys3 and verify that your changes worked. **DO: copy and paste your edited SystemVerilog module, in the Design Record.**
14. Under SIMULATION, click on Run Simulation. Change the Radix of the signals to Binary. Click the Zoom Fit button so that you can see all the waveforms. Examine the waveforms to confirm the functionality on the SystemVerilog code. **DO: take a snip of your simulation waveforms and paste it in the Design Record.** NOTE: you normally do this in the reverse order, i.e. simulate first, then verify on the Basys3.
15. Now do the opposite. Modify the SystemVerilog code so that all the LEDs are ON when the slide switches are in the up position (i.e. pointed towards the center of the Basys3), and OFF when they are in the down position. Be sure to write explanatory comments. Resynthesize and download the new design to the Basys3 and verify that your changes worked. **DO: copy and paste your edited SystemVerilog module, in the Design Record.**
16. Under SIMULATION, click on Run Simulation. Change the Radix of the signals to Binary. Click the Zoom Fit button so that you can see all the waveforms. Examine the waveforms to confirm the functionality on the SystemVerilog code. **DO: take a snip of your simulation waveforms and paste it in the Design Record.** NOTE: you normally do this in the reverse order, i.e. simulate first, then verify on the Basys3.
17. For extra practice, write a testbench for the switch_logic module, and test it with the first version of the design (the one with the AND and INVERTER gates). You can adapt the lab_1a_top_level_tb module, to create the switch_logic_tb. Be sure to set the “top level” files correctly within the Vivado simulator!!

Deliverables

By the end of the lab period **or** the beginning of the next lab period, demonstrate to the TA:

1. Your Basys3 board running with the latest iteration of the lab 1 project, be prepared to explain the design and any part of the Vivado design and programming flow.
2. Your latest simulation and be prepared to explain the signals and their meaning.
3. Your Design Record document.

Your TA may ask any team members at random to answer any questions. Work together to ensure that all team members fully understand the lab project and its deliverables. You may also be asked to demonstrate your ability to proceed through the entire design flow, including:

1. Create and start a new project.
2. Synthesize and download your design to the Basys3.
3. Simulate your design and setup the waveforms.

Rubric

As the term progresses, the expectations will increase as your skills develop. All team members are required to participate in the entire lab period and to present their project to the TA. Missing team members will not receive a mark for the project. The three strikes policy outlined in the Course Outline, will be in effect for all labs.

Points	Criteria
4	Fully complete and high quality, questions answered well.
3	Fully complete and high quality, some questions not answered well or had to have other team members answer.
2	Mostly complete or answers are weakly answered by team members
0	Below acceptable for credit.

There is no 1 point given. Fractional points, e.g. 2.5, are not given.