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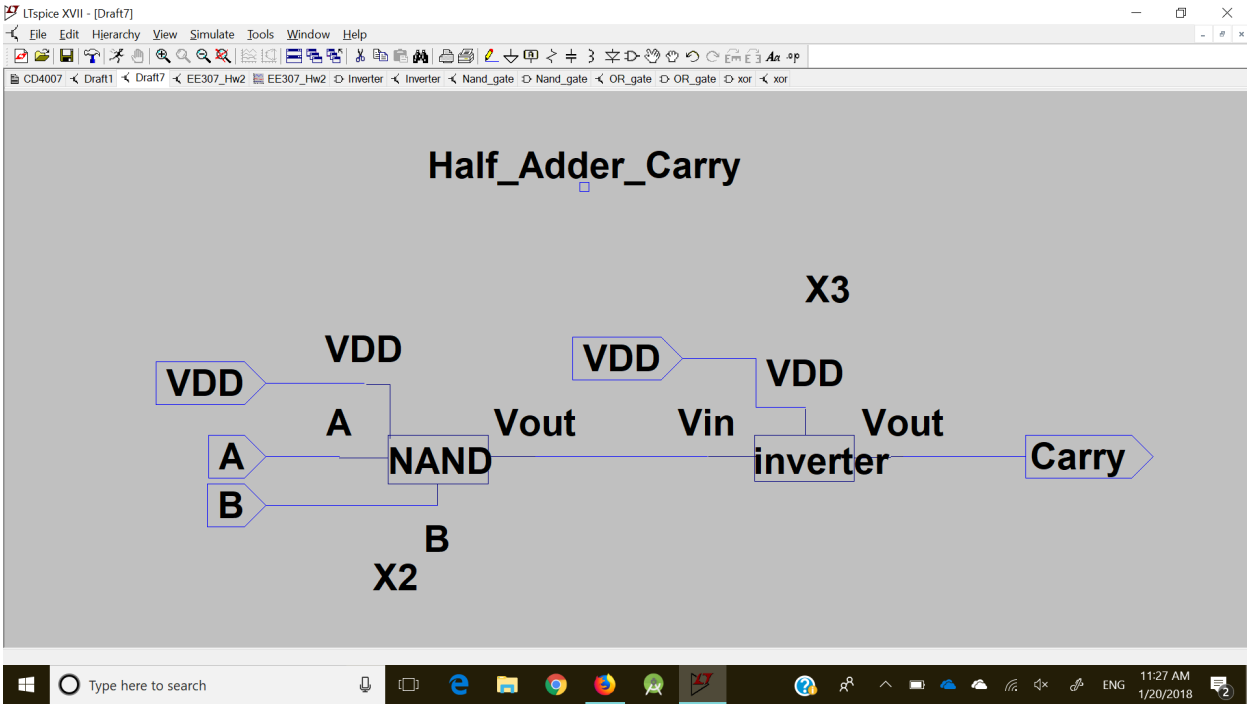
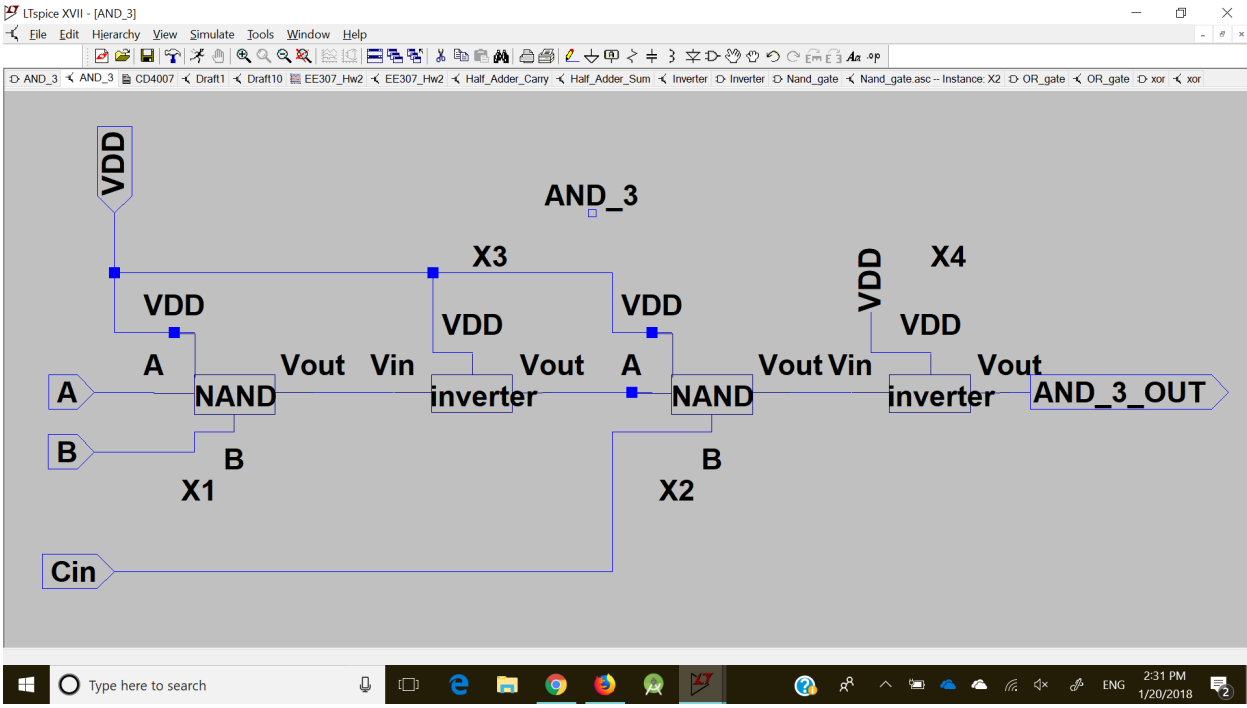
c.



d.



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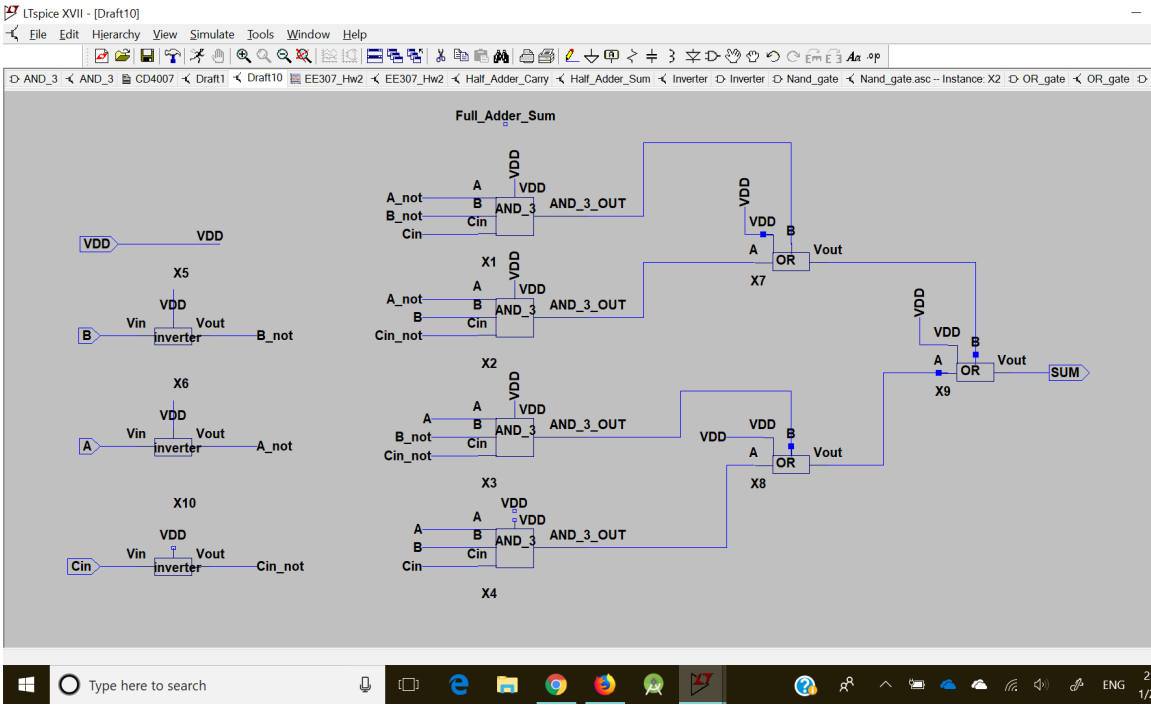
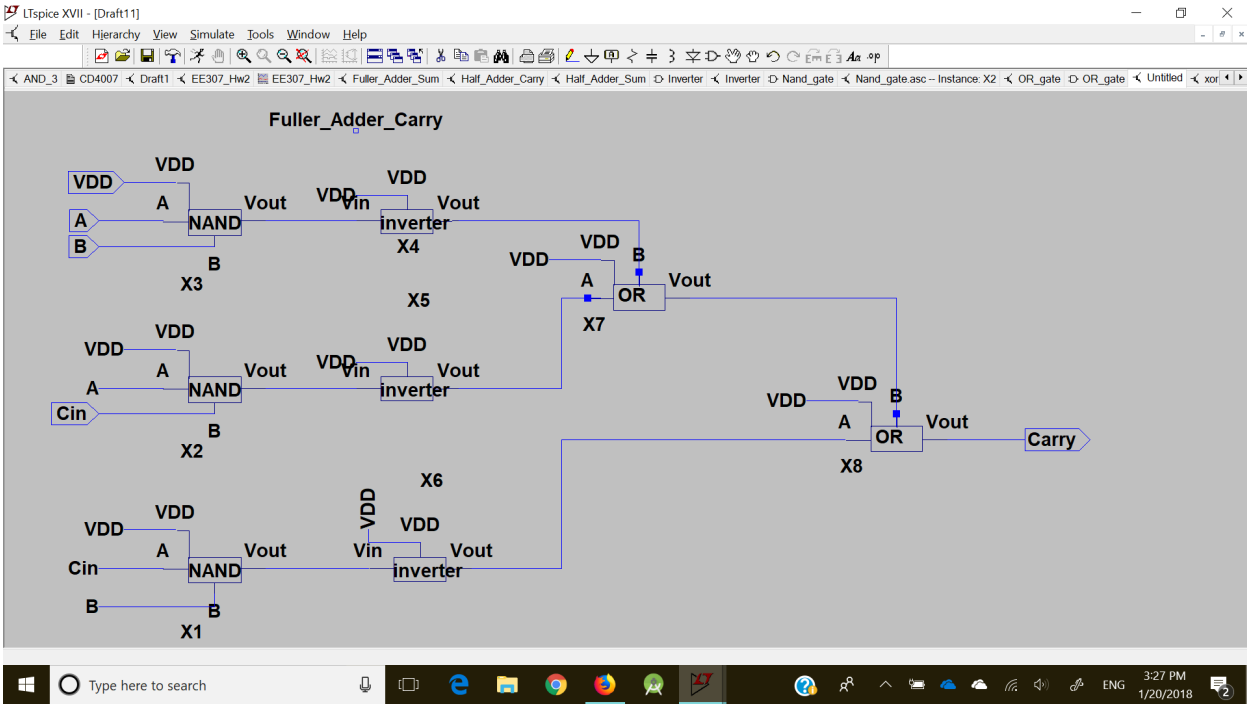
i.



e.



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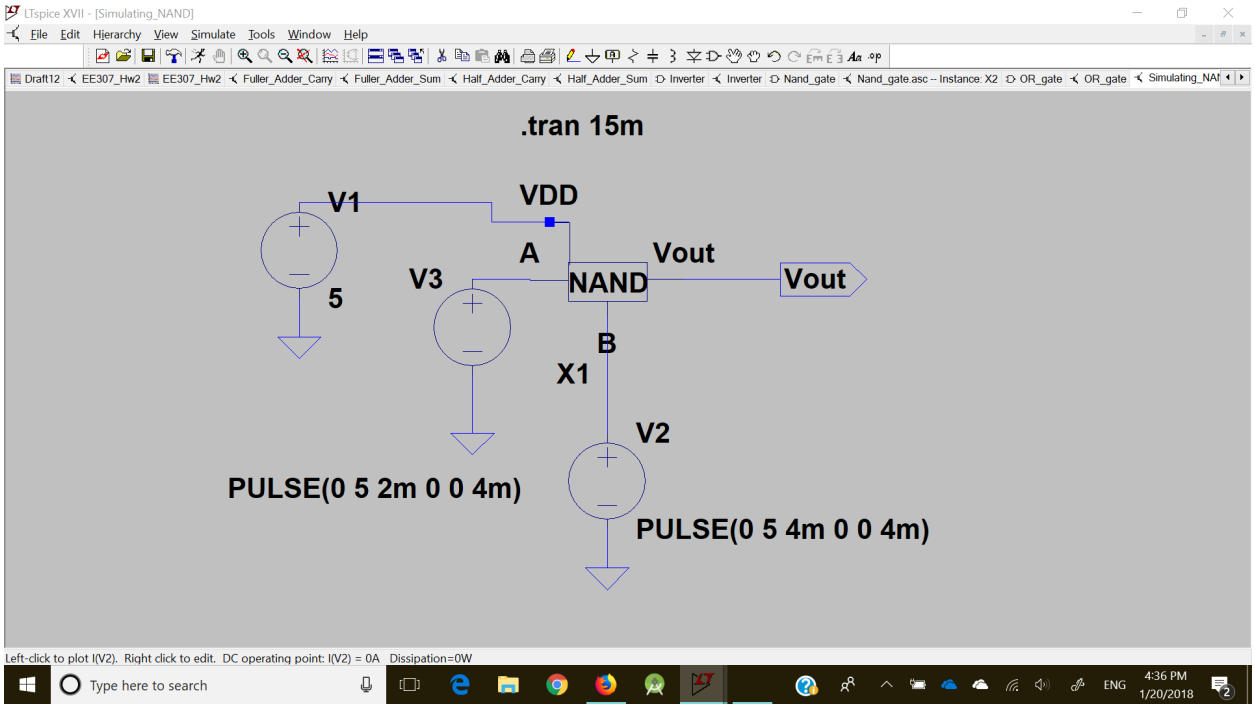
Problem 6

6.



a.

The voltage pulses were chosen based off of:

A											
B											
AB	00	00	10	10	11	11	01	01	00	00	00

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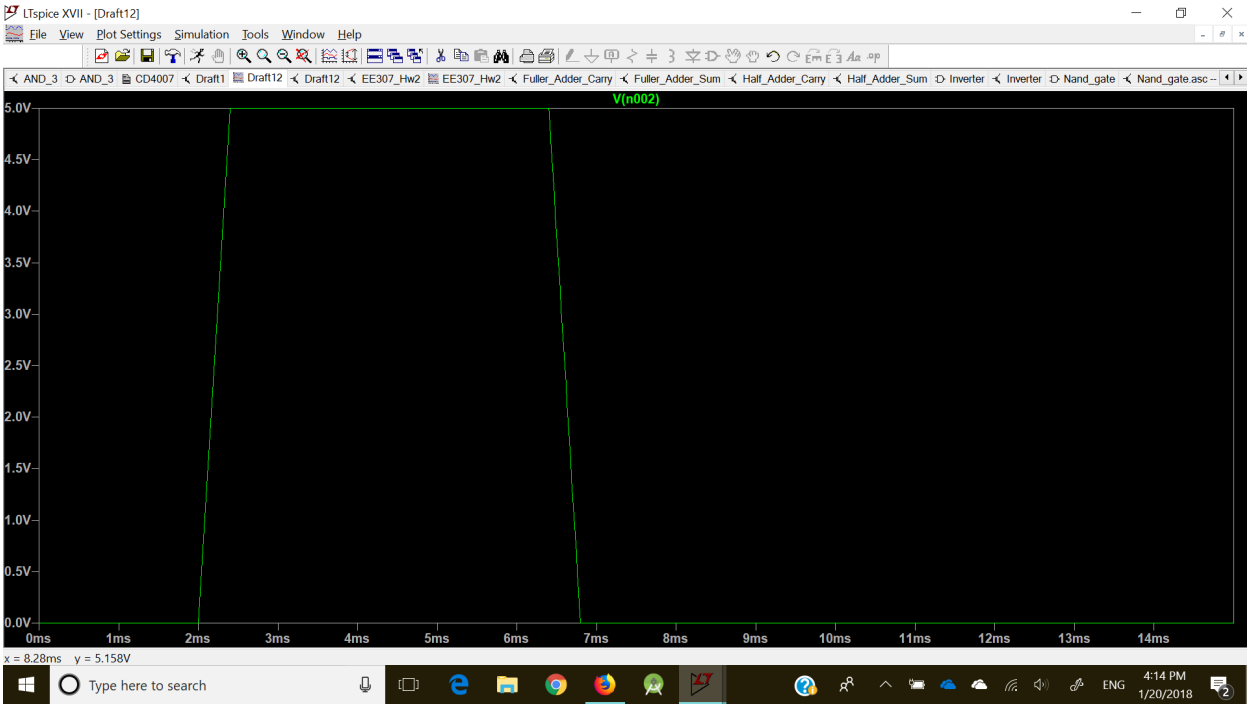
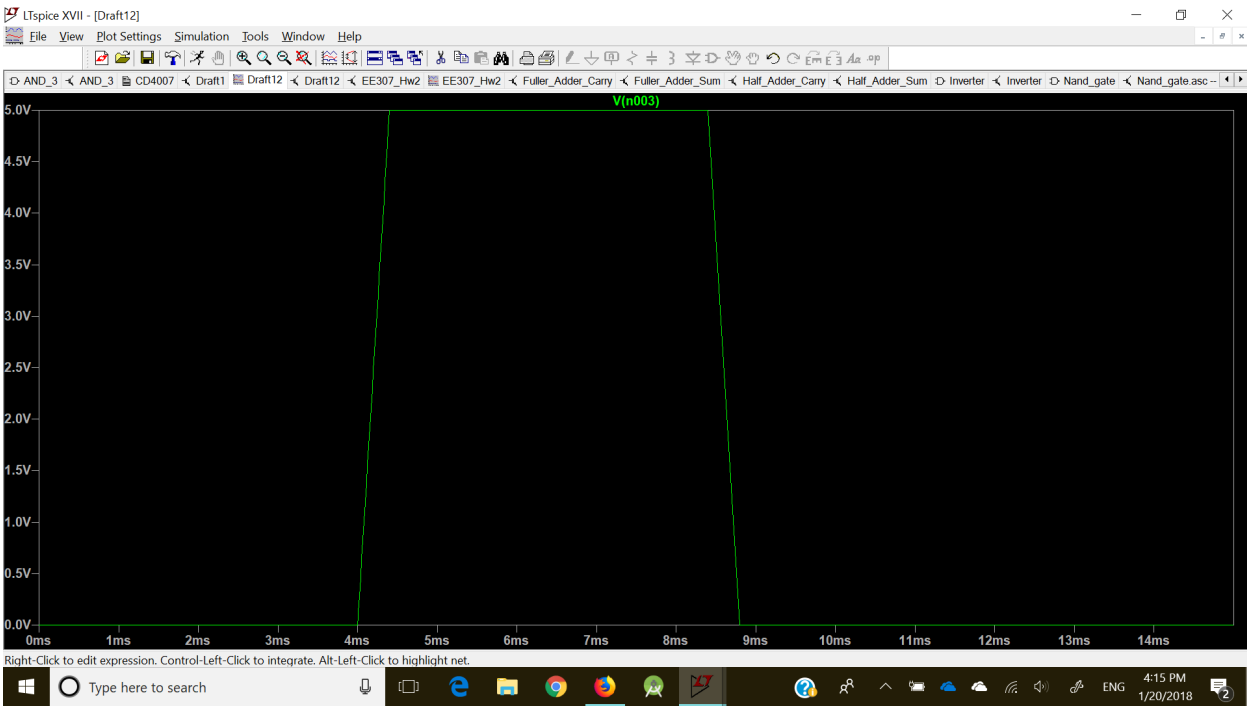
b. Below is the simulation graph for my NAND gate, the Green is input A starting at 2ms and ending at 7ms.



c. Below is the simulation graph for my NAND gate; the Green is input B starting at 4ms and ending at 9ms.



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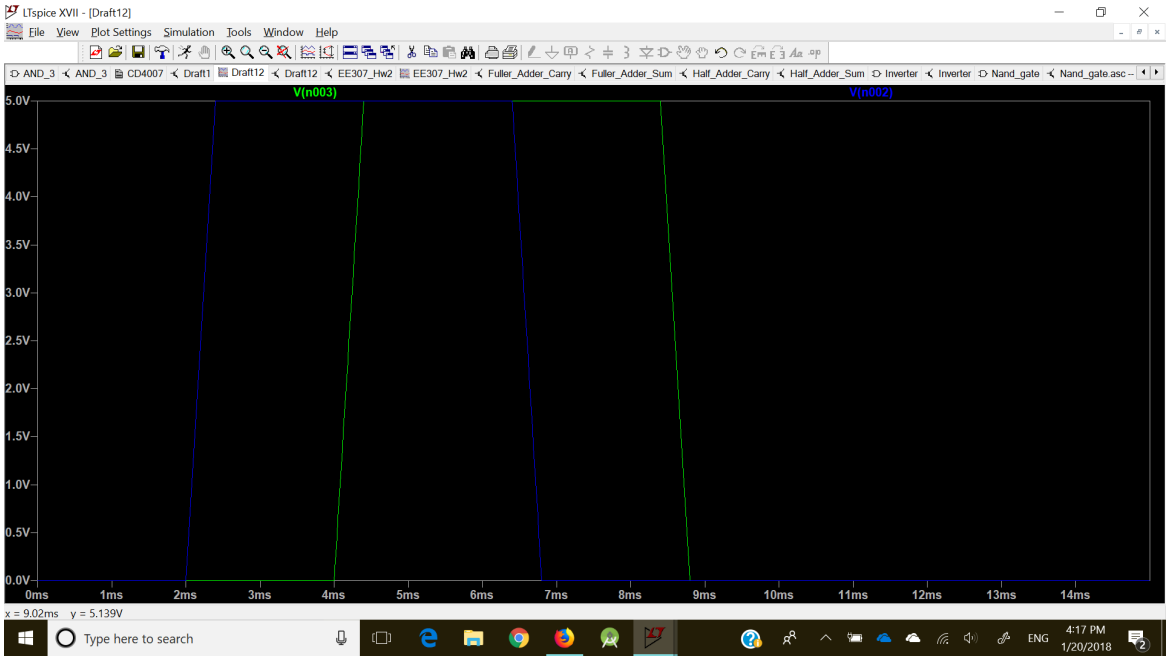
Below is the simulation graph for my NAND gate; the Blue is input A and the Green is input B.



A											
B											
AB	00	00	10	10	11	11	01	01	00	00	00

In the simulation graph for my NAND gate, the outupt Vout is 5V from 0ms to approx. 4.5ms, 5V from approx. 6.5ms to 15ms and 0V from approx. 4.5ms to 6.5ms.
This is the expected output of a NAND gate because 4ms and 6ms correspond to when AB = 11.