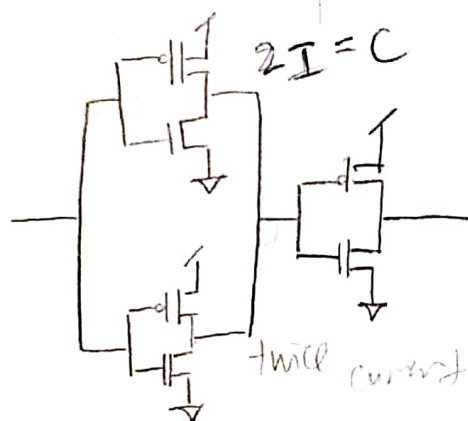


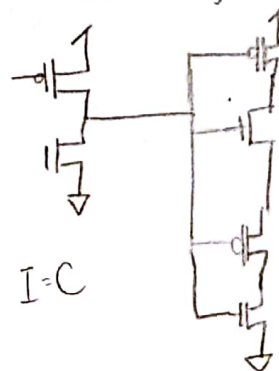
1. a) Circuit 1



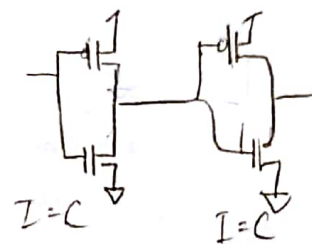
$$\tau = 2 \times N \times t_p$$

less cap is faster

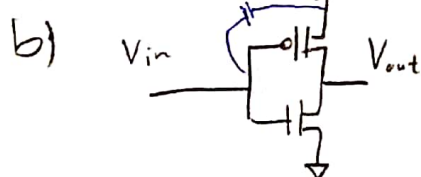
Circuit 2 $2I=C$



Circuit 3



1. a) Circuit 1 fastest
Circuit 2 middle speed
Circuit 3 slowest



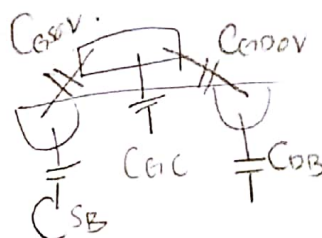
Circuit 4

c) capacitance on NMOS gate

$$C_{ox} = \epsilon_0 \cdot \frac{\epsilon_r}{t_{ox}}$$

$$= (8.854 \times 10^{-12} \text{ F/m}) \left(\frac{3.9}{8 \times 10^{-9}} \right)$$

$$C_{ox} = 0.00432$$



$$C = 2C_{GSov} + C_{GC} + 2C_{GDov} \text{ gate} + C_{GSovN} + C_{GCN} + 2C_{GDovN}$$

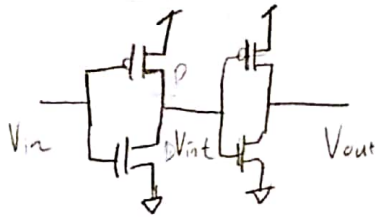
$$\text{Cap on NMOS gate} = 1.298 \times 10^{-13} \text{ F}$$

$$\begin{aligned} \text{PMOS gate } C_{GC} + C_{GSov} + C_{GDov} &= C_{ox} W_p L_p + C_{GSov} \cdot W + C_{GDov} \cdot W \\ &= (0.00432)(2 \times 10^{-6} \text{ m})(100 \times 10^{-6} \text{ m}) \\ &\quad + (5.3752 \times 10^{-11})(2 \times 10^{-6}) \\ &\quad + (5.3752 \times 10^{-11})(2 \times 10^{-6}) \end{aligned}$$

$$\text{Cap on PMOS gate} = 8.6421 \times 10^{-13} \text{ F}$$

$$V_{in} \text{ cap} = C_p + C_n = 9.939 \times 10^{-13} \text{ F}$$

1. d)



$$C = \left[C_{GSOVP} + C_{GCP} + 2C_{GDOVP} + C_{GSOVN} + C_{GCN} + 2C_{GDOVN} \right] = C_{partC}$$

$$+ C_{GDOVP} + C_{DBP}$$

$$+ C_{GDOVN} + C_{DBN}$$

$$e) C = C_{partC} + (C_{ox} W_P L_P + C_{DBP} \cdot W_P) + (C_{ox} W_N L_N + C_{DBN} \cdot W_N)$$

$$= C_{partC} + (0.00432)(2 \times 10^{-6} \text{m})(100 \times 10^{-6} \text{m}) + (3.365 \times 10^{-10}) \times (2 \times 10^{-6})$$

$$+ (0.00432)(0.3 \times 10^{-6} \text{m})(100 \times 10^{-6} \text{m}) + (5.75 \times 10^{-10})(0.3 \times 10^{-6})$$

$$= 1.988 \times 10^{-12} \text{F}$$

f) Area (M2) 116 aF/ μm^2

20 μm = L
2 μm = W

$$C = \text{Area} \times C_{\text{per unit area}}$$

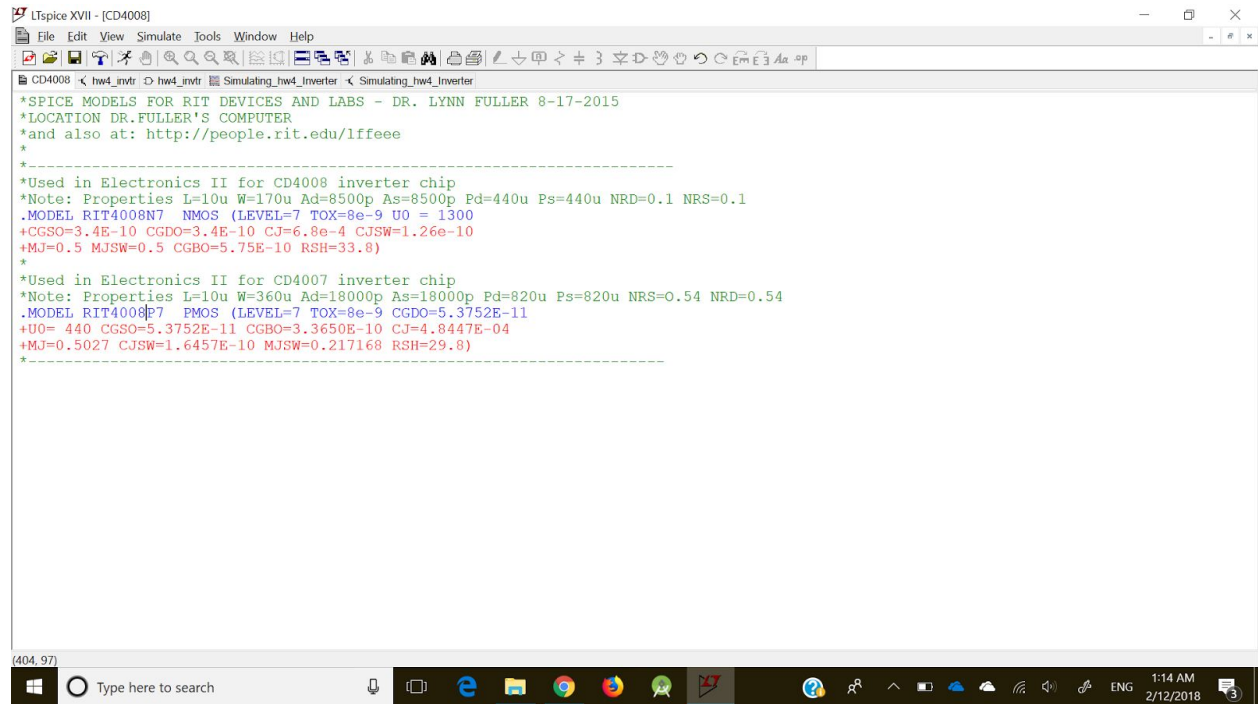
$$= (20 \mu\text{m})(2 \mu\text{m})(116 \text{ aF}/\mu\text{m}^2)$$

$$C = 4640 \text{ aF}$$

2h) $T = 2 \times N \times t_P$; $t_P = \frac{t_r + t_f}{2}$

$$= 2 \times 17 \times \left(\frac{(0.05 + 0.12) \times 10^{-9}}{2} \right)$$

$$= 2.89 \times 10^{-9} \text{sec}$$



```
CD4008 < hwr4_invtr > hwr4_invtr Simulating_hwr4_inverter < Simulating_hwr4_inverter
*SPICE MODELS FOR RIT DEVICES AND LABS - DR. LYNN FULLER 8-17-2015
*LOCATION DR.FULLER'S COMPUTER
*and also at: http://people.rit.edu/lffeee
*
*-----
*Used in Electronics II for CD4008 inverter chip
*Note: Properties L=10u W=170u Ad=8500p As=8500p Pd=440u Ps=440u NRD=0.1 NRS=0.1
.MODEL RIT4008N7 NMOS (LEVEL=7 TOX=8e-9 UO = 1300
+CGSO=3.4E-10 CGDO=3.4E-10 CJ=6.8e-4 CJSW=1.26e-10
+MJ=0.5 MJSW=0.5 CGBO=5.75E-10 RSH=33.8)
*
*Used in Electronics II for CD4007 inverter chip
*Note: Properties L=10u W=360u Ad=18000p As=18000p Pd=820u Ps=820u NRS=0.54 NRD=0.54
.MODEL RIT4008P7 PMOS (LEVEL=7 TOX=8e-9 CGDO=5.3752E-11
+UO= 440 CGSO=5.3752E-11 CGBO=3.3650E-10 CJ=4.8447E-04
+MJ=0.5027 CJSW=1.6457E-10 MJSW=0.217168 RSH=29.8)
*-----
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