Circuit 1 T = 2 x Nxtp Circuit 4 C) capacitance on NMOS gate CGC + CGSov + CGDov = Cox W, LN + Case · WN + Caso · W Cox = EO . Ex = $(8.854 \times 10^{-12} \text{ F/m}) \left(\frac{3.7}{8 \times 10^{-9}}\right)$ Cux = 0.00432) PMOS gate CCC + CGSov + CGDov = Cox Wp Lp + CGSo·W + CGDov·W

tox = 8×10-9
=(0.00427.117×10-6...) + (5.3752×10")(2×10-6) + (5.3752×10-")(2×10-6) Cap on PMOSgale = 8.6421 × 10-13 F

Vn cap = Cp + CN = 9.939 × 10-13 =

e)
$$C = C_{part} c + (C_{ox} W_{p} L_{p_{3}} + C_{p_{3}} v_{p}) + (C_{ox} W_{n} L_{n} + C_{p_{3}} v_{p}) + (C_{ox} W_{$$

2G)
$$T = 2 \times N \times t_{P}$$
; $t_{P} = \frac{t_{P} + t_{P}}{2}$
= $2 \times 17 \times \left(\frac{(0.05 + 0.12) \times 10^{-9}}{2}\right)$
= $2.89 \times 10^{-9} \text{sec}$