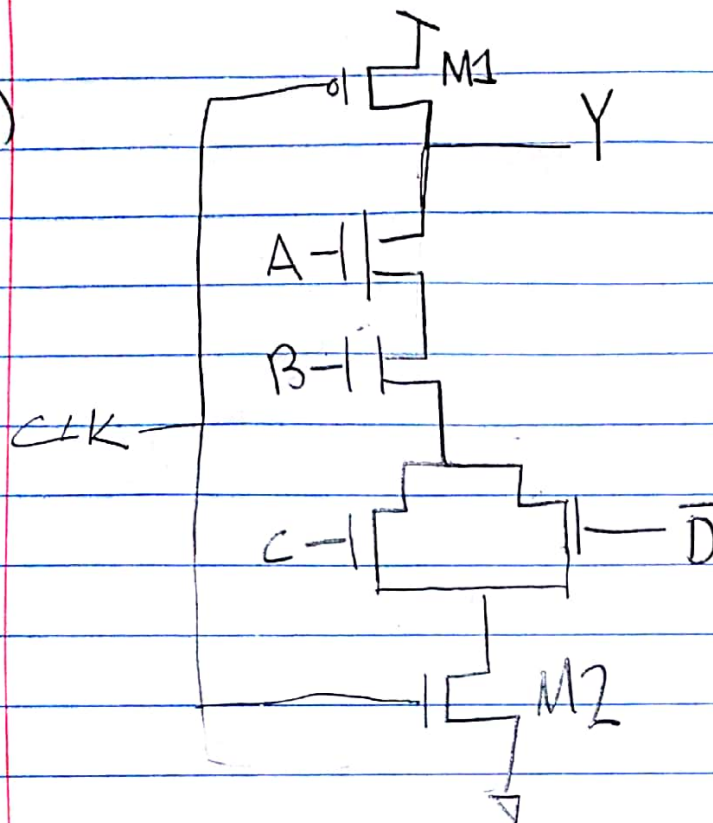


2a)



$$b) \tau_{H \rightarrow L} = (4 + 3 + 2 + 1) RC = 10 RC = 10 \times 145 \Omega \times 15 \text{ fF} = 21.750 \text{ ps}$$

$$\tau_{p, H \rightarrow L} = 0.69 \cdot \tau_{H \rightarrow L} = 15.008 \text{ ps}$$

$$\tau_{L \rightarrow H} = 8.7 \text{ ns}$$

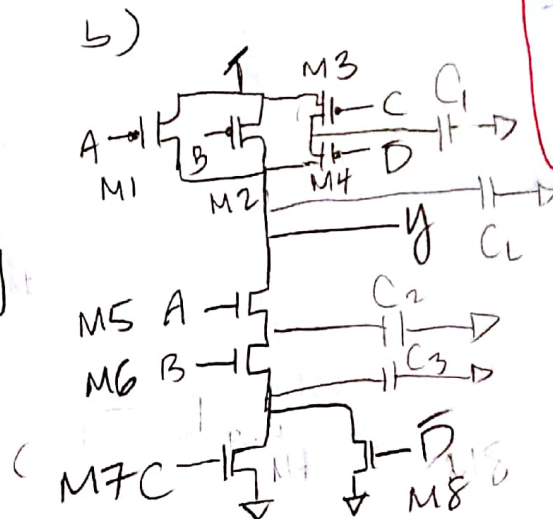
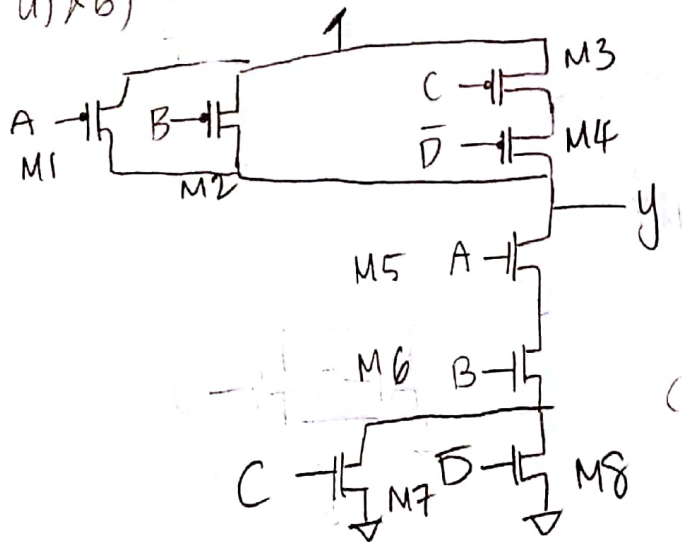
Colleen Lau  
EE 307 HW 7  
Mar 2, 2018

Collaborated  
w/  
TJ

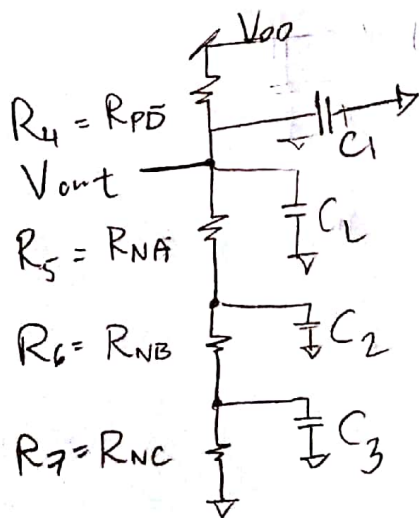
Jessie Folan

$$\begin{aligned} 1. \quad Y &= \overline{A \cdot B + (C + \bar{D})} \\ &= \overline{\overline{A \cdot B + (C + \bar{D})}} \\ &= (A \cdot B) \cdot (C + \bar{D}) \end{aligned}$$

a) & b)



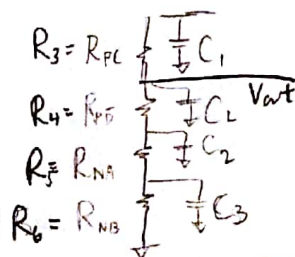
c)  $A = B = D = 1$  &  $C = 0$   
to  $A = B = D = C = 1$



$$\begin{aligned} d) \quad T &= (R_{M7} \cdot C_3) + (R_{M6} + R_{M7}) \cdot C_2 \\ &\quad + (R_{M7} + R_{M6} + R_{M5}) \cdot C_L \\ &\quad + (R_{M7} + R_{M6} + R_{M5} + \dots) \cdot C_1 \end{aligned}$$

Assume

e) when  $A = B = C = D = 1 \Rightarrow A = B = D = 1$  &  $C = 0$   
 $\Rightarrow R_{PC} \cdot C_1$  turns on

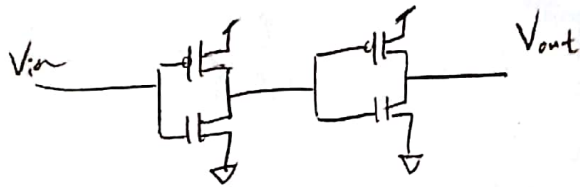


$$\begin{aligned} T &= (R_3 \cdot C_1) + (R_3 + R_4) C_L \\ &\quad + (R_3 + R_4 + R_5) C_2 + \\ &\quad (R_3 + R_4 + R_5 + R_6) C_3 \end{aligned}$$

Assuming all transistors have same  $R_{on}$

$$T = R_{on} (C_1 + 2C_L + 3C_2 + 4C_3)$$

3.  $R_{onN} = 145 \Omega$   $R_{onP} = 325 \Omega$  &  $C_{out} = 20.2 fF$   
 $C$  on the input  $26.82 fF$ , wire is in  $N^+$   
 wire  $2 \mu m$  long &  $0.05 \mu m$  wide



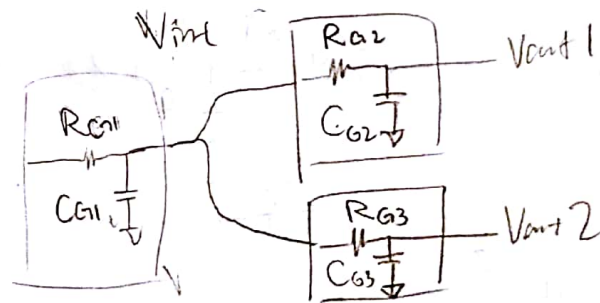
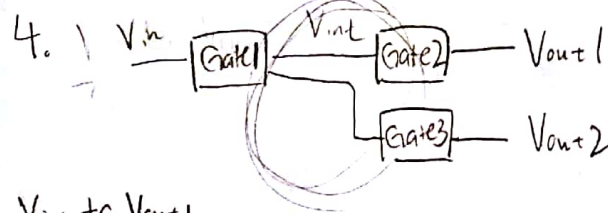
$$R_{wire} = \frac{L}{W} \frac{\Omega}{sq}$$

$$= (6.2 \frac{\Omega}{sq}) (\frac{2 \mu m}{0.05 \mu m}) = 248 \Omega$$

$$\tau = (145 \Omega \times 20.2 fF) + (145 + 248 \Omega) \times 26.82 fF = 13.47 ps$$

$$t_p = (0.69)(13.47 ps)$$

$$t_{p0toVDD} = 9.2943 ps$$



$V_{in}$  to  $V_{out1}$

$$\tau_{int} = R_{a1} C_{a1} + (R_{a1} + R_{a2}) C_{a2} + (R_{a1} + R_{a3}) C_{a3}$$

$$\tau_1 = R_{a1} C_{a1} + R_{a1} C_{a3} + (R_{a1} + R_{wire}) C_{a2}$$

$$t_{p1} = t_{pa1} + 0.69(\tau_1)$$

$$\tau_2 = R_{a2} C_{a2}$$

$$t_{p2} = t_{pa2} + 0.69(R_{a2} C_{a2})$$

$$t_{p total} = t_{p1} + t_2$$

$$= t_{pa1} + 0.69(R_{a1} C_{a1} + R_{a1} C_{a3} + (R_{a1} + R_{wire}) C_{a2} + t_{pa2} + 0.69 R_{a2} C_{a2})$$

$V_{in}$  to  $V_{out2}$

$$\tau_3 = R_{a1} C_{a1} + R_{a1} C_{a2} + (R_{a1} + R_{wire}) C_{a3}$$

$$t_{p3} = t_{pa1} + 0.69(R_{a1} C_{a1} + R_{a1} C_{a2} + (R_{a1} + R_{wire}) C_{a3})$$

$$\tau_4 = R_{a3} C_{a3}$$

$$t_{p4} = t_{pa3} + 0.69 R_{a3} C_{a3}$$

$$t_{p total} = t_{pa1} + 0.69(R_{a1} C_{a1} + R_{a1} C_{a2} + (R_{a1} + R_{wire}) C_{a3} + t_{pa2} + 0.69 R_{a2} C_{a2} + t_{pa3} + 0.69 R_{a3} C_{a3})$$



5.

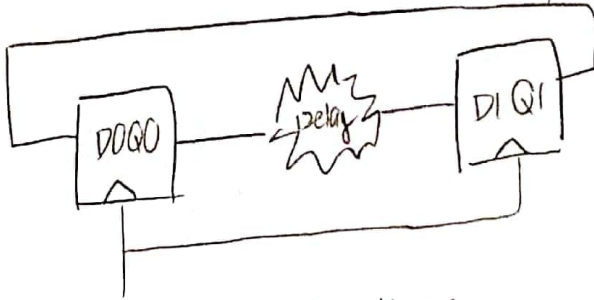
$$a) t_{PINV_b} = t_{PNANDC} + t_{PNANDE} + t_{PNANDF}$$

$$b) t_{Phold} = t_{PINVB}$$

$$c) t_{CLK \rightarrow a} = t_{INVB} + t_{PNANDd} + t_{PNANDC} + t_{PNANDE} + t_{PNANDF}$$

$$d) t_{setup} = t_{INVA}$$

\*e)



i) There is a violation for these  
Hold time violation

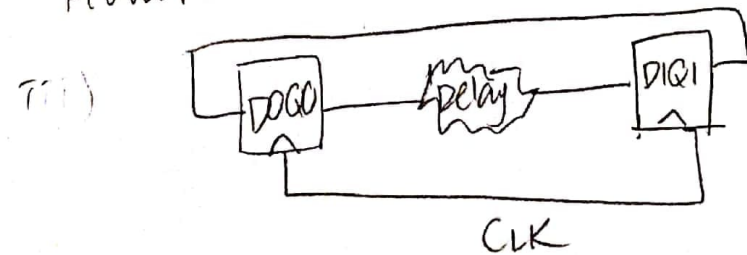
$$t_{axao} + t_{delay} = 2ns + 3ns = 5ns < t_{hold1} = 8ns$$

Setup-time violation

$$t_{axao} + t_{delay} = 8ns + 6ns = 14ns < t_{setup1} = 20ns$$

ii) The setup violation  
can be fixed w/  
adjusted clock speed.  
The hold violation  
cannot.

iii) The setup violation and hold time violation can be solved by  
adding inverters to increase the transition time.  
However this will increase the power consumption.



$$iv) f = \frac{1}{T} = \frac{1}{20ns + 14ns} = 29MHz$$

The hold time shouldn't be affected by the clock speed.

v) The setup violation can be fixed by slowing the clock