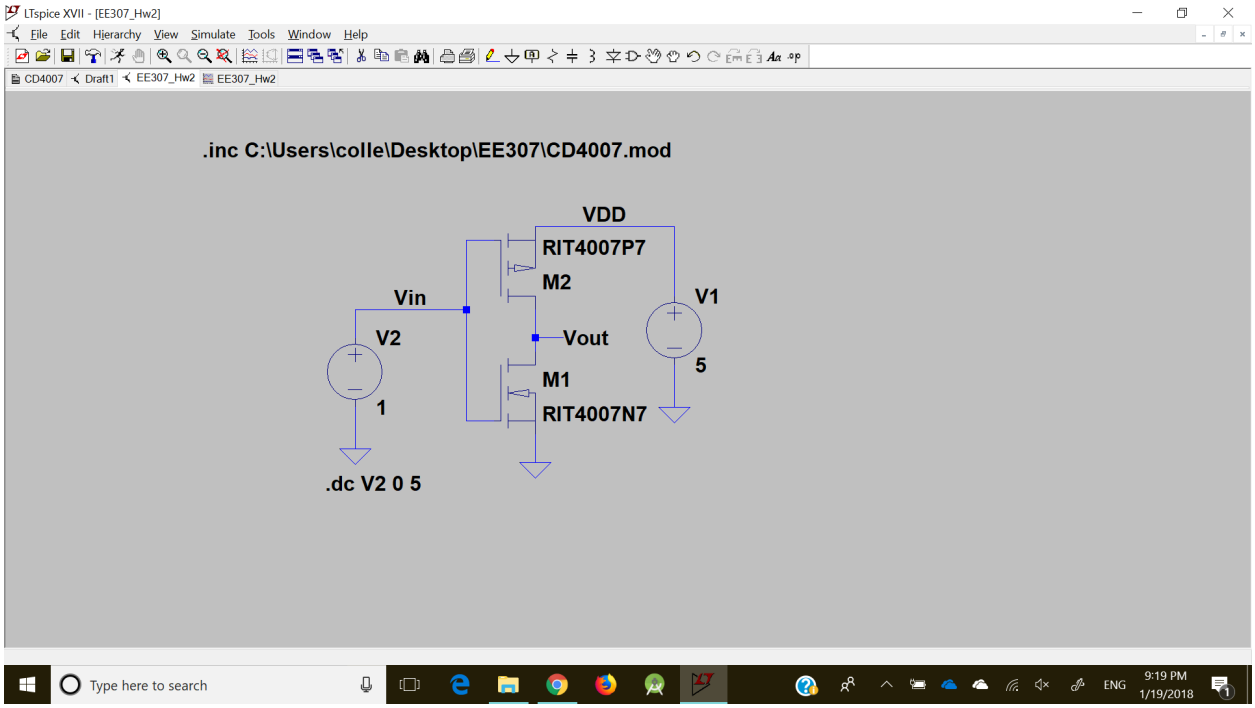
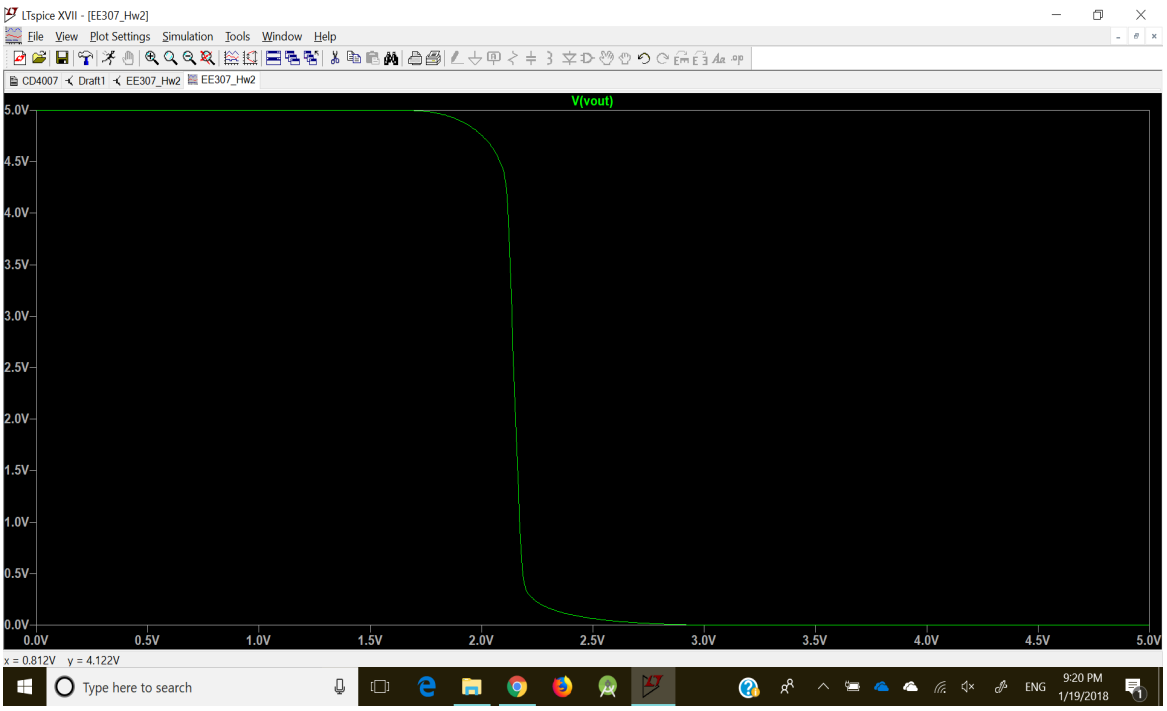
Colleen Lau
Jan 19, 2018

1. HW2
    a. I did it
    b. Digikey sells 7,072,345 parts
    c. 6999 FET arrays
    d. I read it and understand
2. 

    a. 

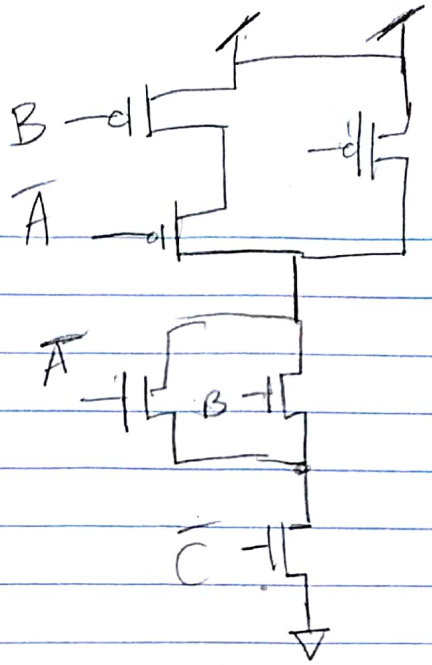
3. See paper

Colleen Law
EE 307-06
HW2

3. a) $Out = A \cdot \overline{B} + C$

$= \overline{\overline{(A \cdot \overline{B}) + C}}$

$Out = \overline{(\overline{A} + B) \cdot \overline{C}}$



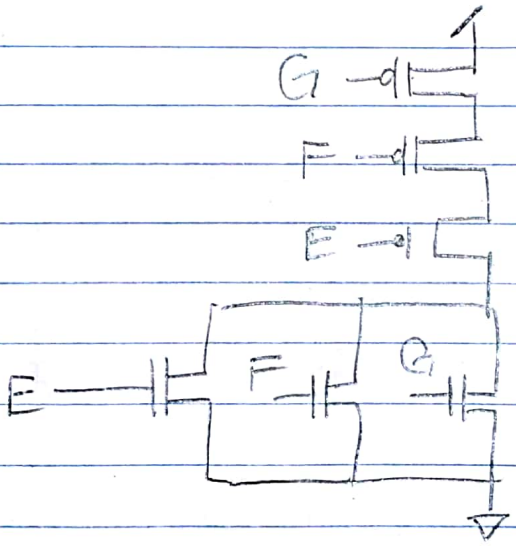
b) $D_X = \overline{\overline{(E + \overline{F}) \cdot G}}$

$= \overline{(E + \overline{F}) + \overline{G}}$

$= \overline{\overline{(A + B) \cdot C}}$

$\overline{\overline{(A+B)} + C}$ → demorgan

$\overline{(\overline{A} \cdot \overline{B}) + C}$

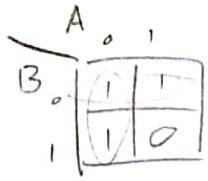


Colleen Lau EE 307-06 HW2

4. a)

NAND

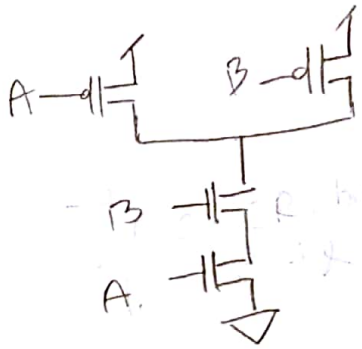
A	B	Vout
0	0	1
0	1	1
1	0	1
1	1	0



$\overline{A}+\overline{B}$

$\overline{\overline{A}+\overline{B}}$

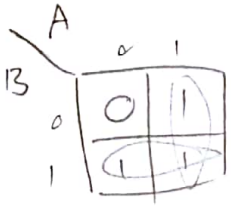
$A \cdot B$



b)

OR

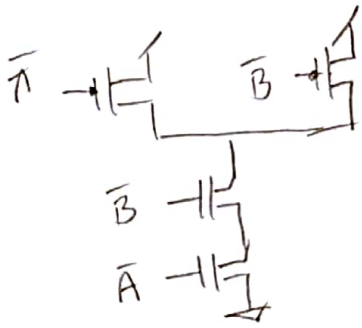
A	B	Vout
0	0	0
0	1	1
1	0	1
1	1	1



$A + B$

$\overline{A+B}$

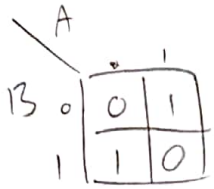
$\overline{\overline{A} \cdot \overline{B}}$



d)

XOR

A	B	Vout
0	0	0
0	1	1
1	0	1
1	1	0

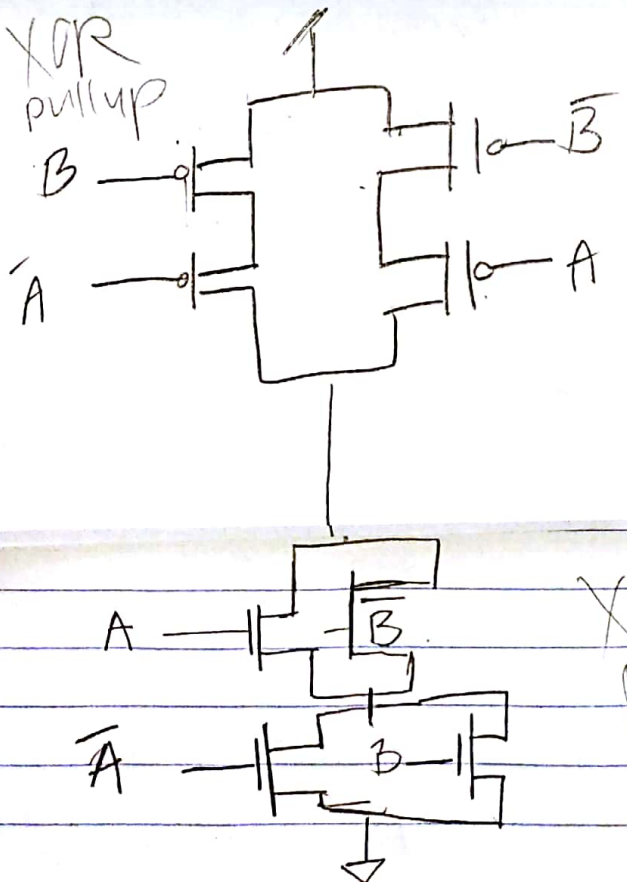


$(A \cdot \overline{B}) + (\overline{A} \cdot B)$

$\overline{(A \cdot \overline{B}) + (\overline{A} \cdot B)}$

$\overline{(A \cdot \overline{B})} \cdot \overline{(\overline{A} \cdot B)}$

$(\overline{A}+B) \cdot (A+\overline{B})$



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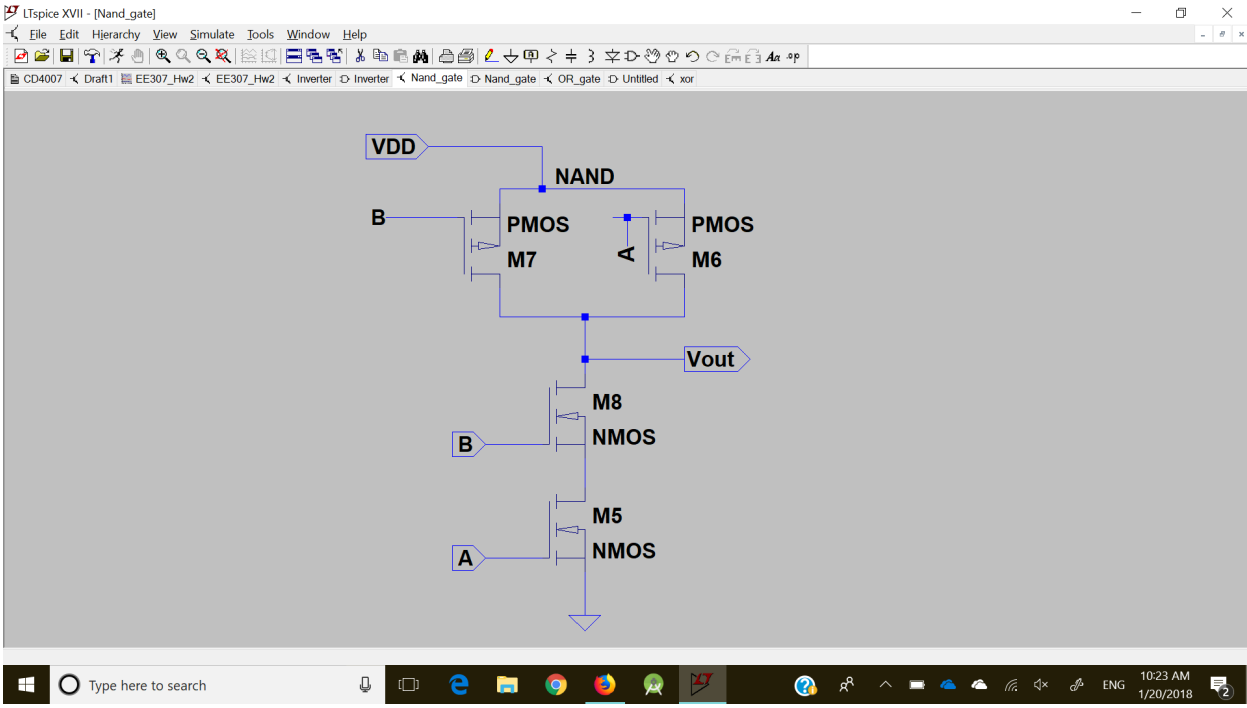
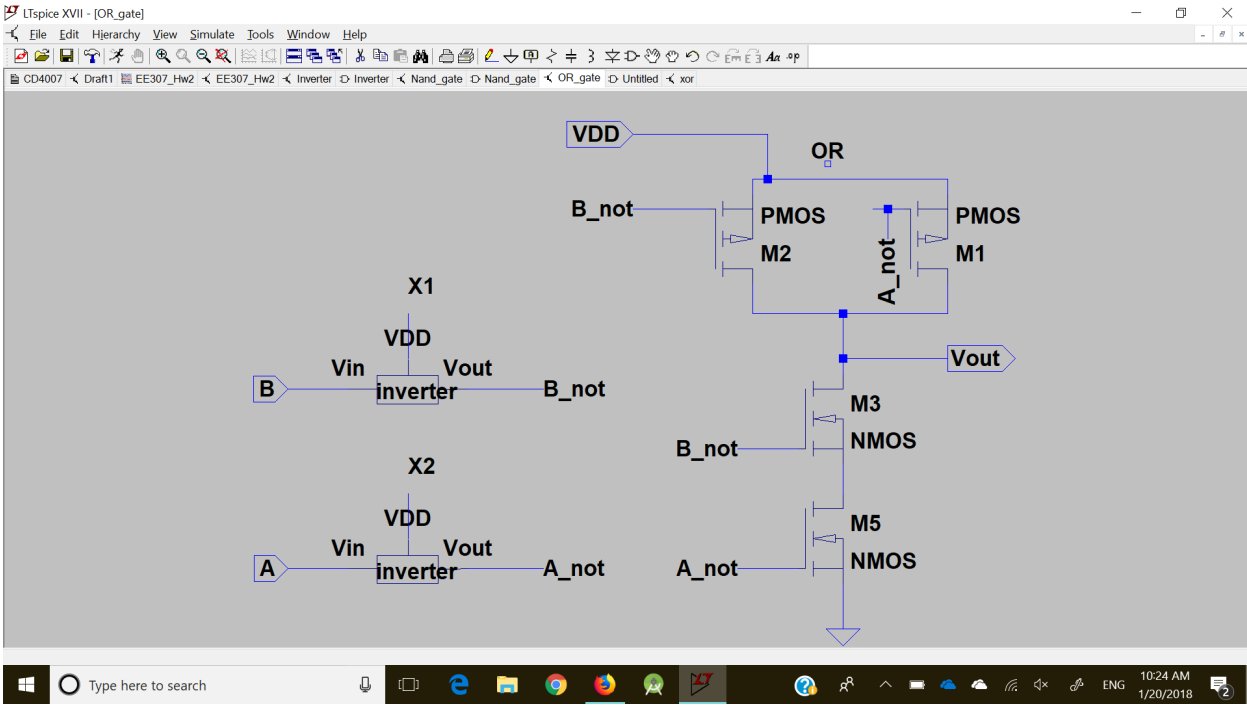
4. See page 3

a.



b.



c.

Inputs			Output Pull up network	Pull down network
A	B	Output		
0	0	0	OFF	ON
0	1	1	ON	OFF
1	0	1	ON	OFF
1	1	1	ON	OFF

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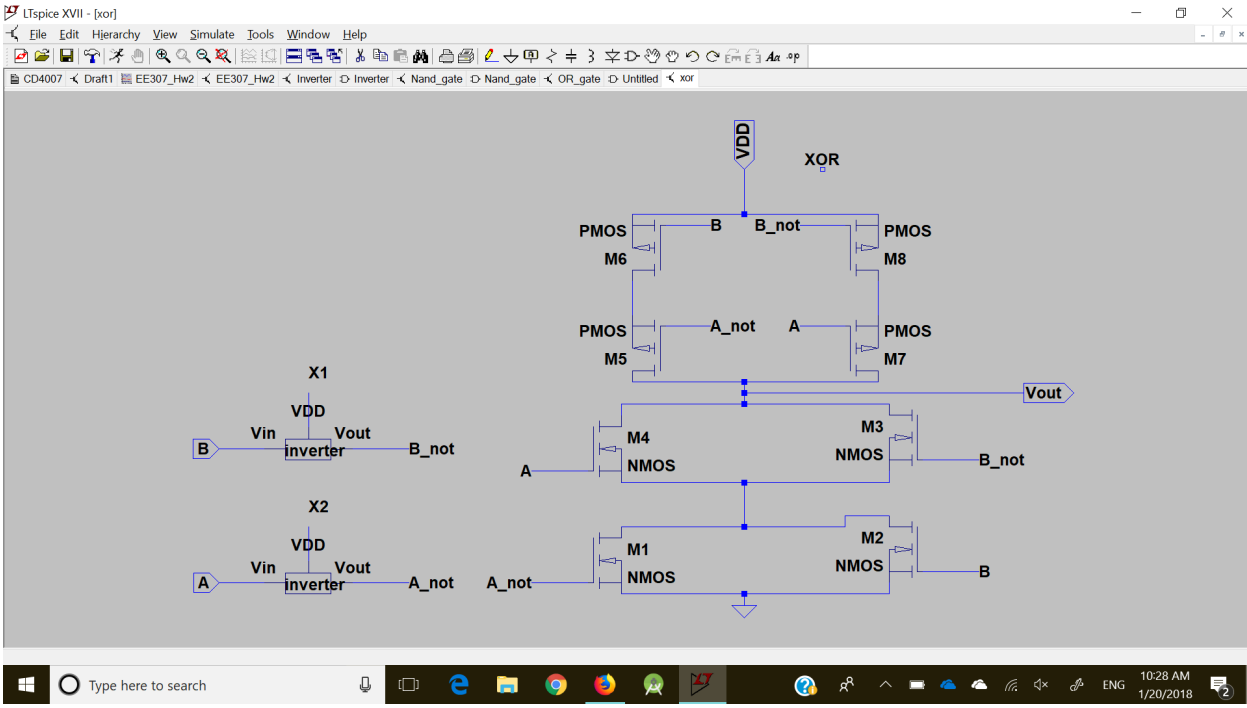
d.



5b. Half adder summing circuit

b) i) Truth Table

Input		Output	
A	B	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

i)

A	B	sum
0	0	0
0	1	1
1	0	1
1	1	0

ii)

A \ B	0	1
0	0	1
1	1	0

Like XOR

c) Half adder carry circuit

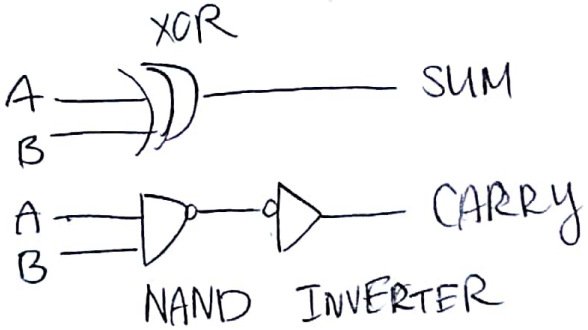
i)

A	B	Carry
0	0	0
0	1	0
1	0	0
1	1	1

ii)

A \ B	0	1
0	0	0
1	0	1

Like AND



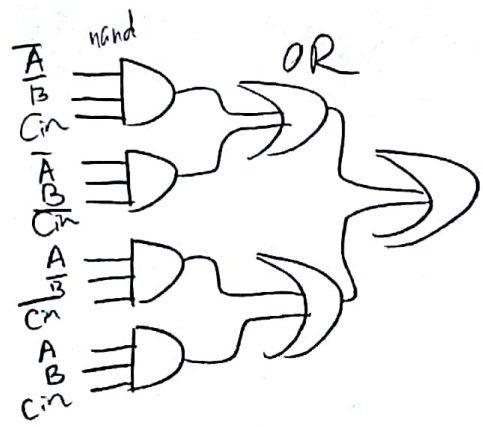
Full adder sum

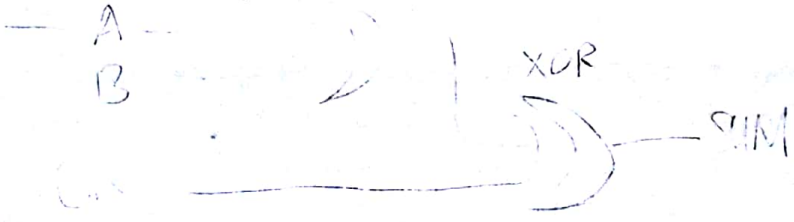
d)

Input			Output
A	B	Cin	Sum
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

A \ BCin	00	01	11	10
0	0	1	0	1
1	1	0	1	0

$S = \bar{A}\bar{B}Cin + \bar{A}B\bar{C}in + ABCin + A\bar{B}\bar{C}in$





Colleen Lau EE 307
hw 2
#5

5.e) Fuller adder carry circuit

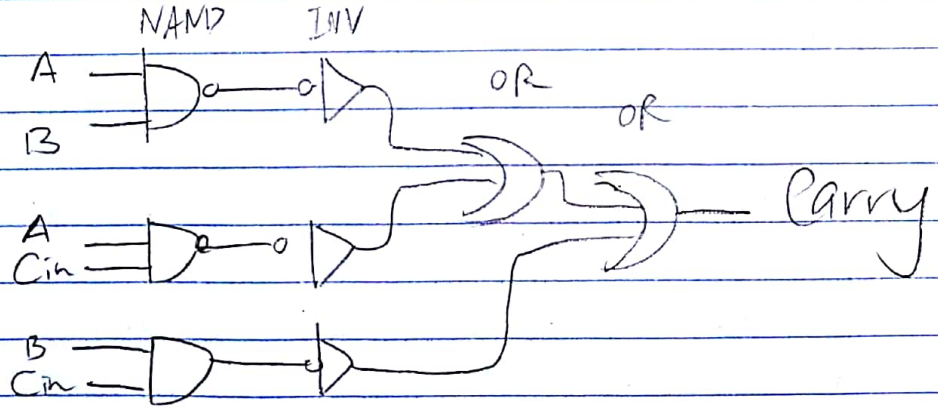
I

Input			Output	
A	B	Cin	sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

II Carry kmap

A \ BCin	00	01	11	10
0	0	0	1	0
1	0	1	1	1

Carry = AB + ACin + BCin



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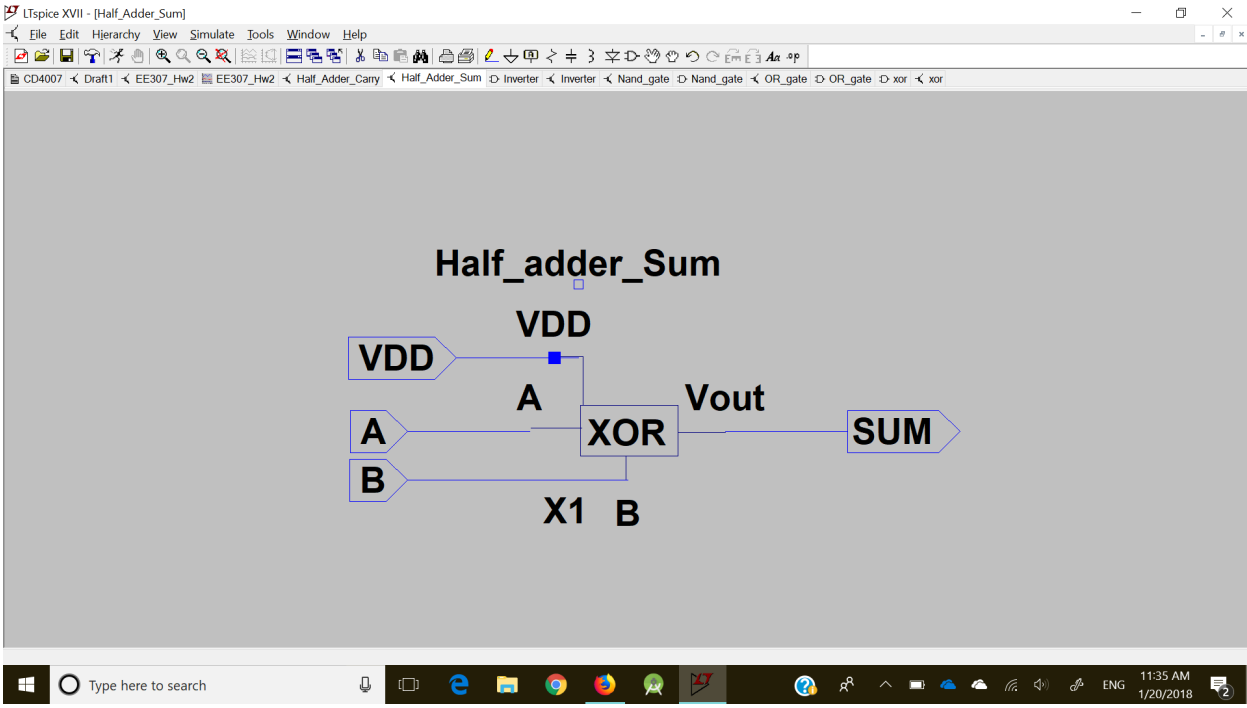
Problem 5

5. I want to eat a cookie...
    a. I did it.
    b.



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5b. Half adder summing circuit

b) i) Truth Table

Input A	Input B	Output S	Output C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

i)

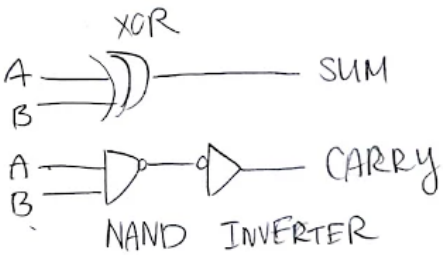
A	B	sum
0	0	0
0	1	1
1	0	1
1	1	0

ii)

A \ B	0	1
0	0	1
1	1	0

Like XOR

c) Half adder carry circuit



i)

A	B	Carry
0	0	0
0	1	0
1	0	0
1	1	1

ii)

A \ B	0	1
0	0	0
1	0	1

Like AND

Full adder sum

d)

Input A	Input B	Input Cin	Output Sum
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

A \ BCin	00	01	11	10
0	0	1	0	1
1	1	0	1	0

$S = \bar{A}\bar{B}Cin + \bar{A}B\bar{C}in + AB\bar{C}in$

i.

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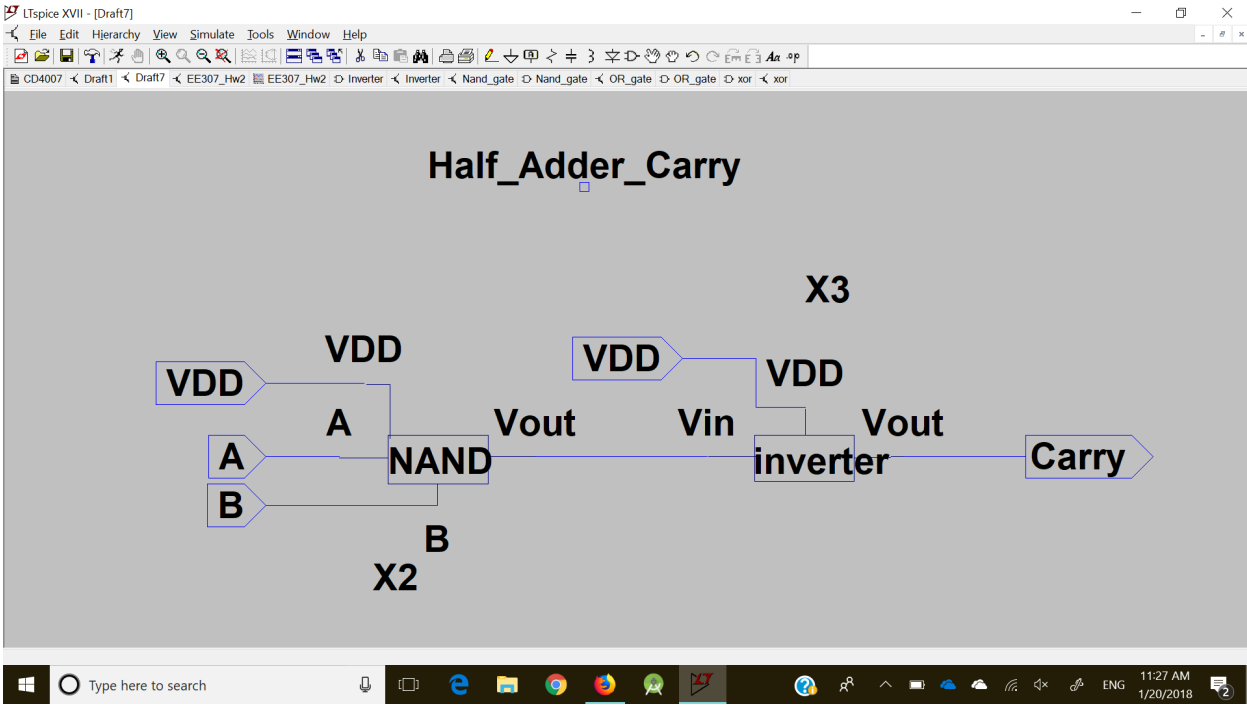
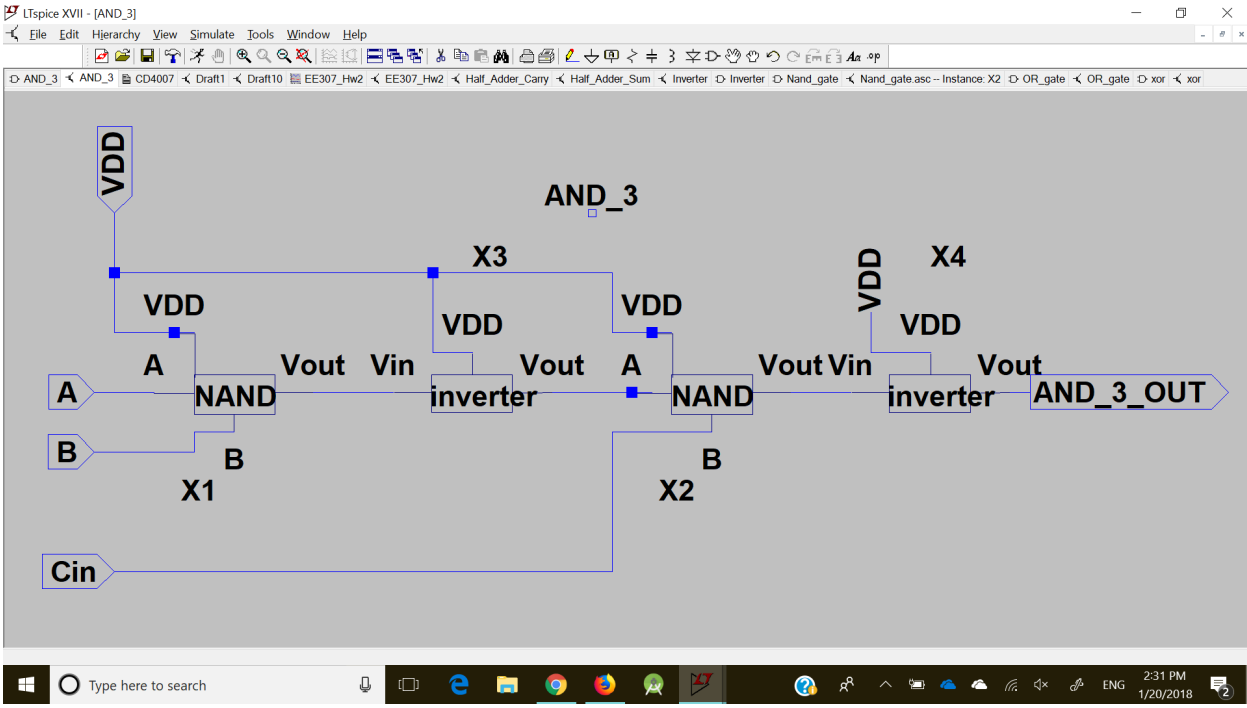
c.



d.



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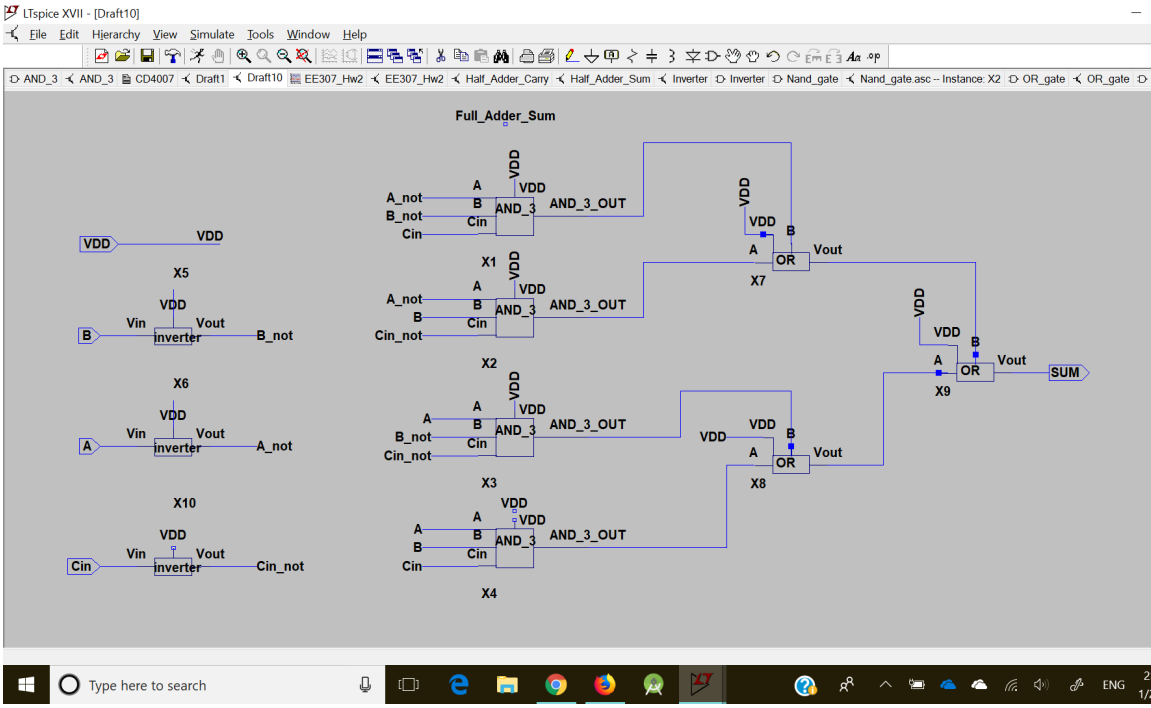
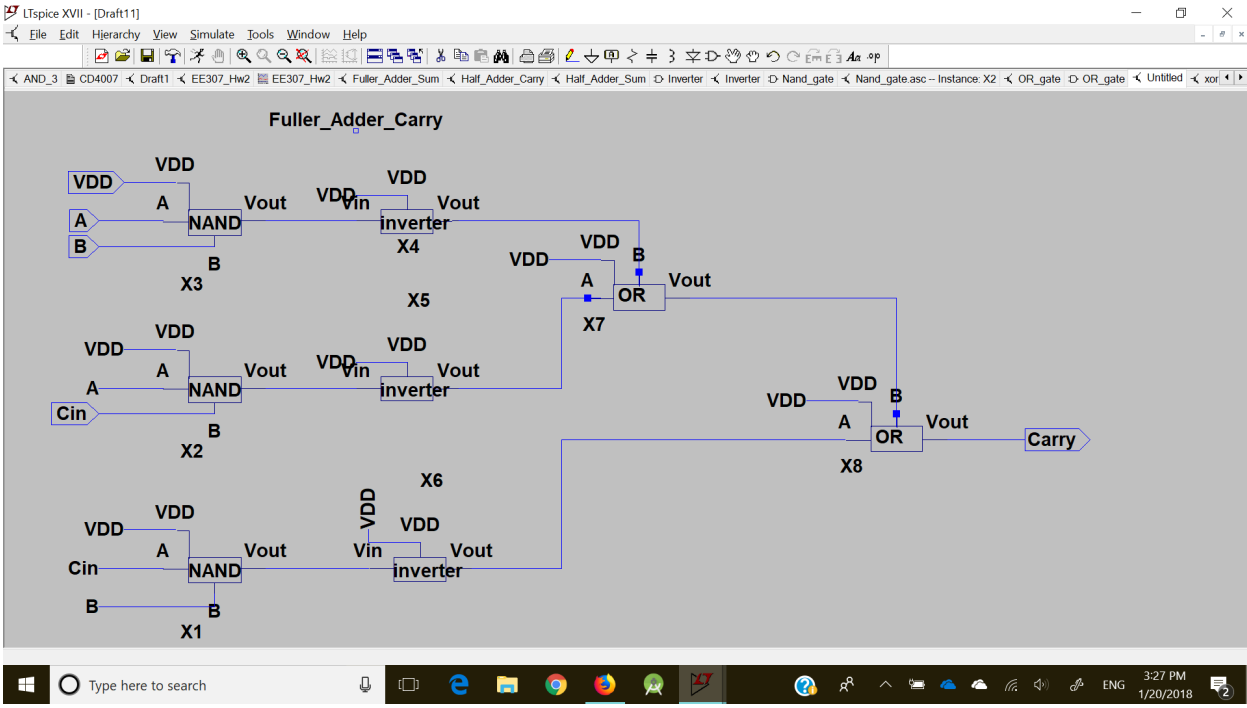
i.



e.



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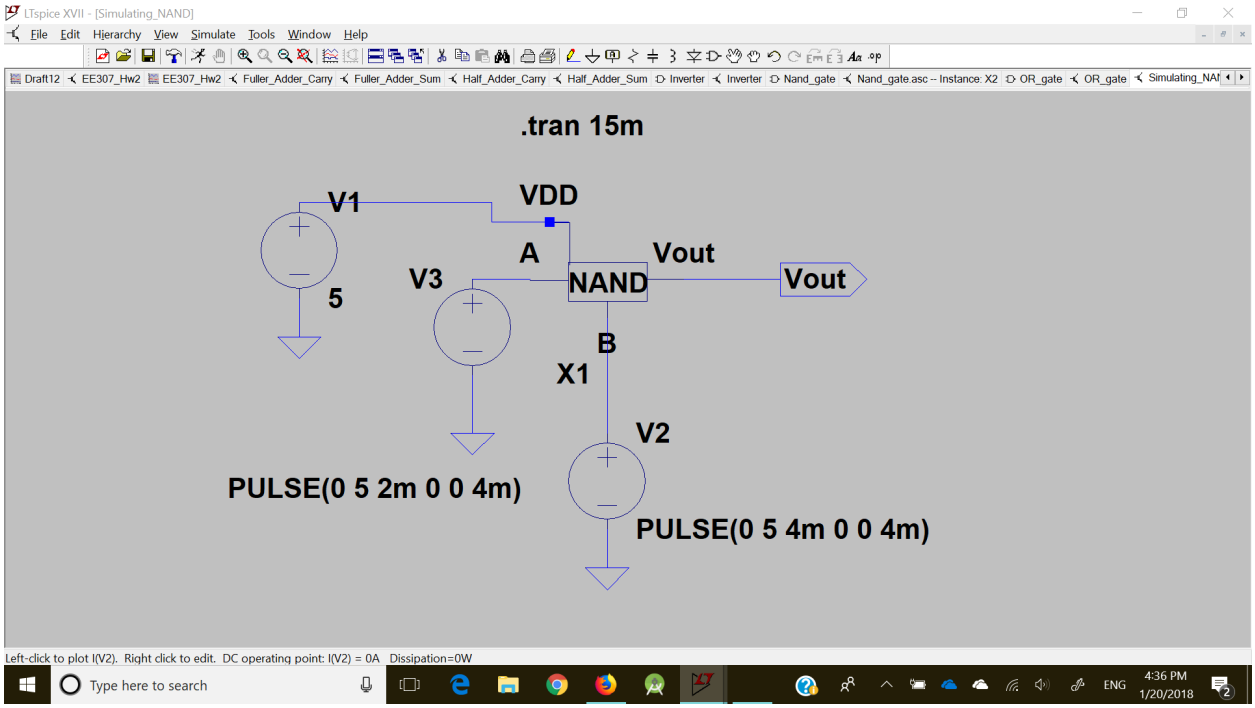
Problem 6

6.



a.

The voltage pulses were chosen based off of:

A											
B											
AB	00	00	10	10	11	11	01	01	00	00	00

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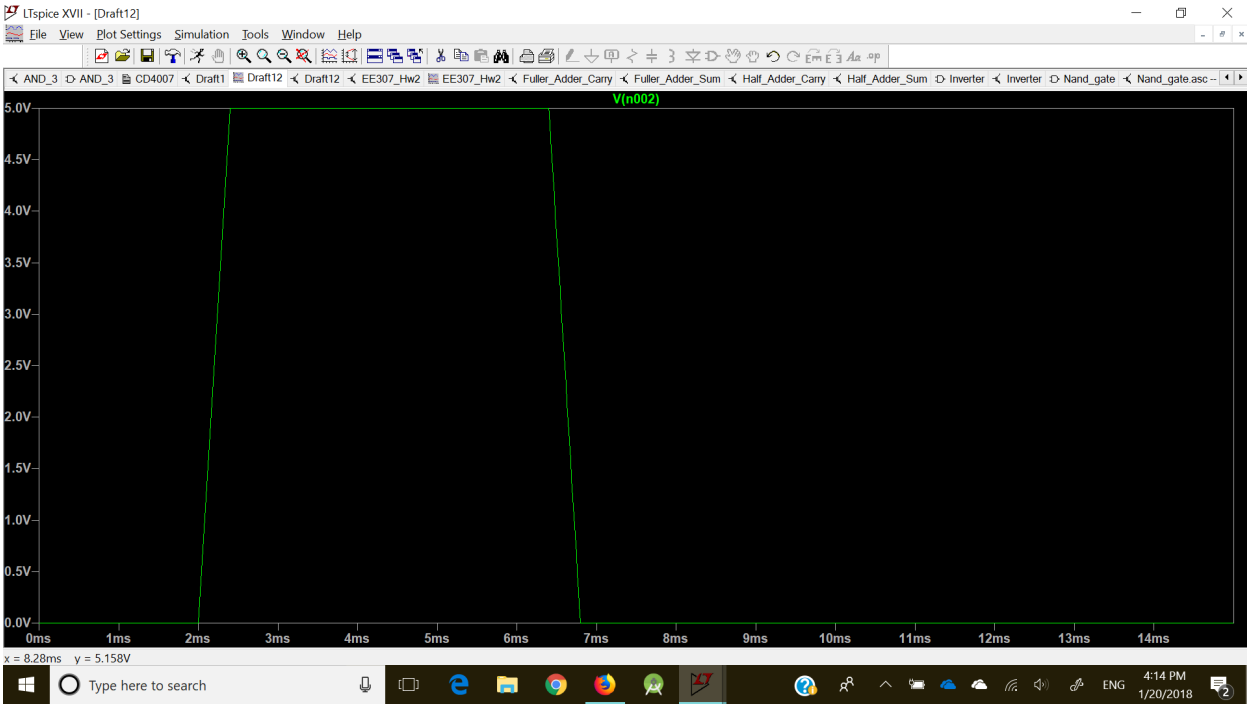
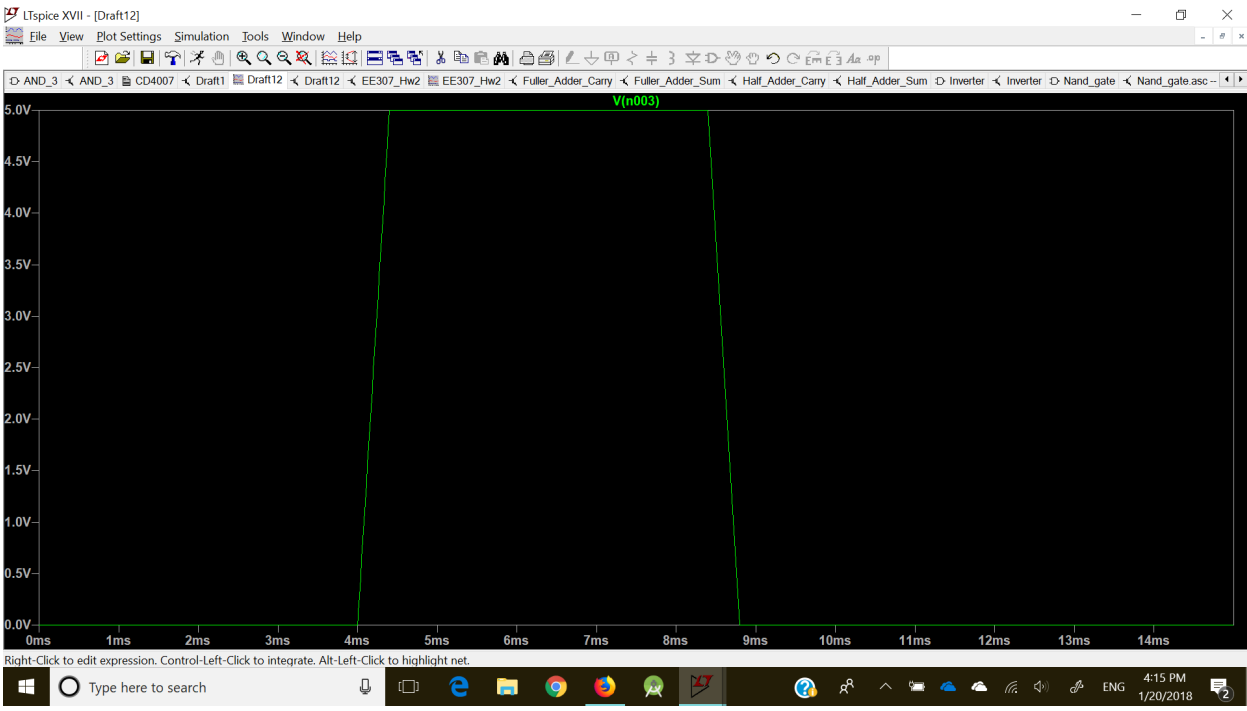
b. Below is the simulation graph for my NAND gate, the Green is input A starting at 2ms and ending at 7ms.



c. Below is the simulation graph for my NAND gate; the Green is input B starting at 4ms and ending at 9ms.



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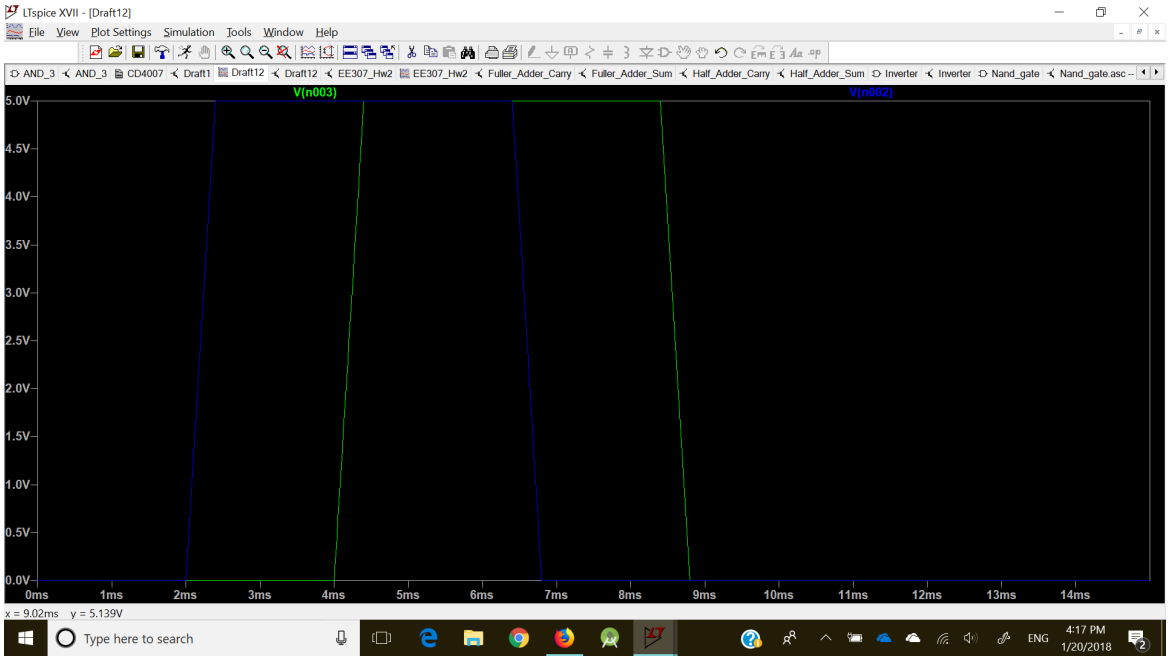
Below is the simulation graph for my NAND gate; the Blue is input A and the Green is input B.



A											
B											
AB	00	00	10	10	11	11	01	01	00	00	00

In the simulation graph for my NAND gate, the outupt Vout is 5V from 0ms to approx. 4.5ms, 5V from approx. 6.5ms to 15ms and 0V from approx. 4.5ms to 6.5ms.
This is the expected output of a NAND gate because 4ms and 6ms correspond to when AB = 11.