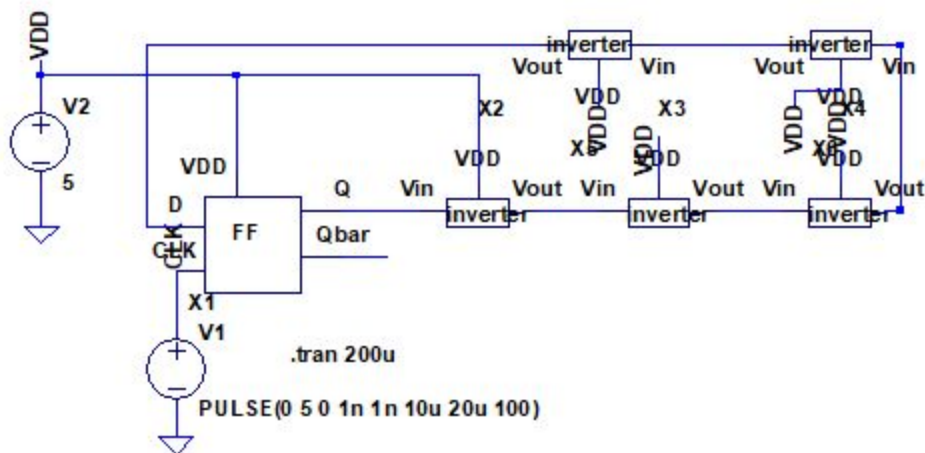
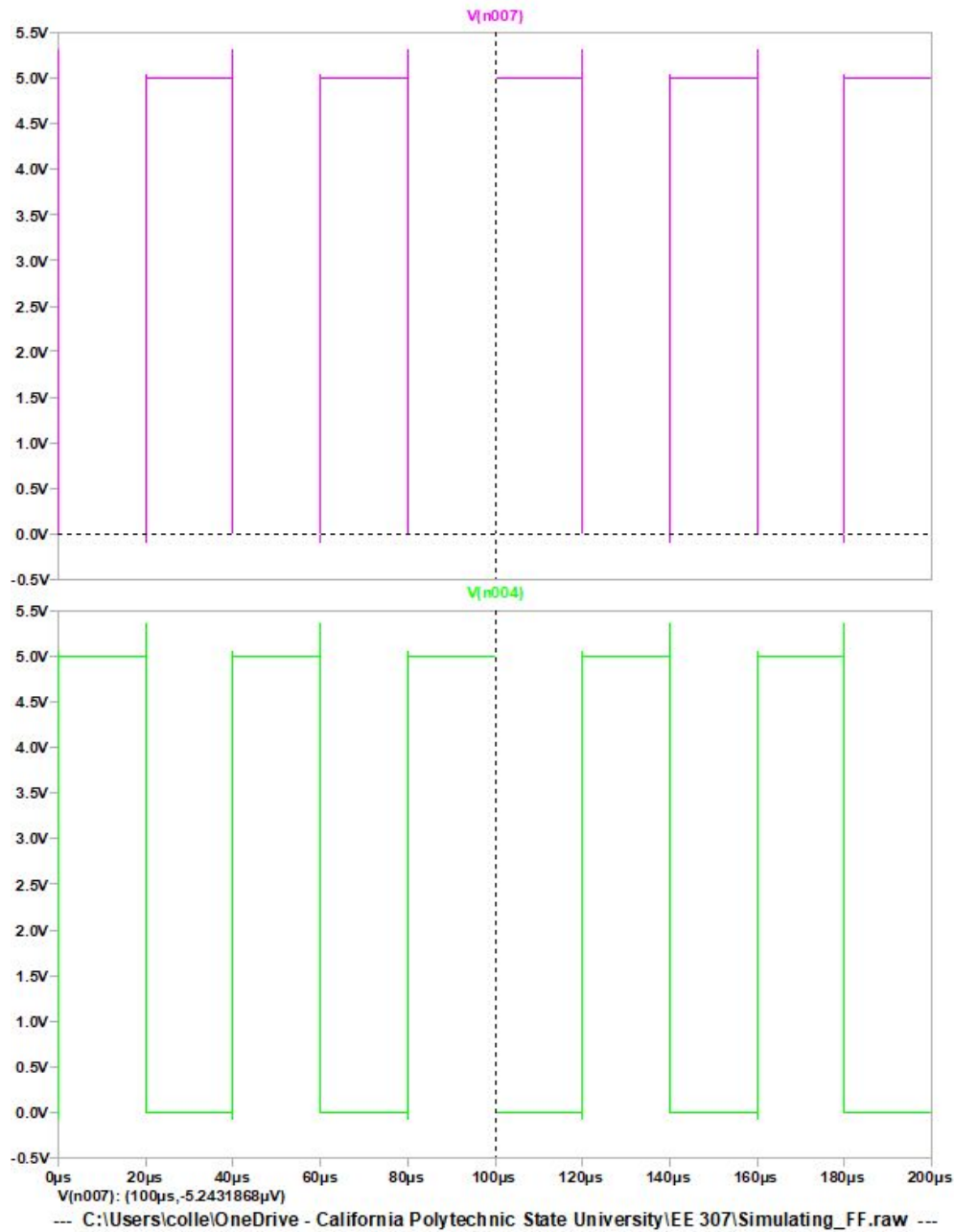


On behalf of our group, we would like to apologize for the timeliness of our homework 6 submission. We appreciate any feedback and commentary for this assignment. We only wish to demonstrate to you that we understand the application of inverters and NAND gates to create a D-flip flop and hope to receive any credit if possible.

.inc "C:\Users\colle\OneDrive - California Polytechnic State University\EE 307\FinalFiles\CD4009.mod"





Pink = \overline{Q}

Green = Q

We have a successful simulation of the flip-flop with Q going from 0 to VDD and VDD to 0 on a clock edge.