**EE307 Digital Electronics and Integrated Circuits**

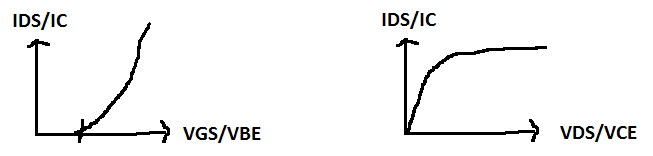
**Class Midterm 1**, **February 7, 2014**

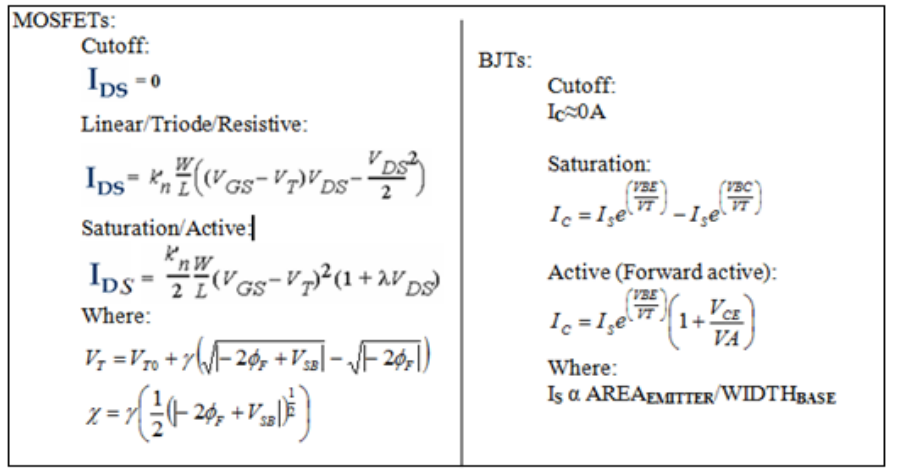
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| --- | --- |
| Powers of Euler’s #, e | |
| Power | Value |
| 1 | 2.718282 |
| 2 | 7.389056 |
| 3 | 20.08554 |
| 4 | 54.59815 |
| 5 | 148.4132 |
| 6 | 403.4288 |
| 7 | 1096.633 |

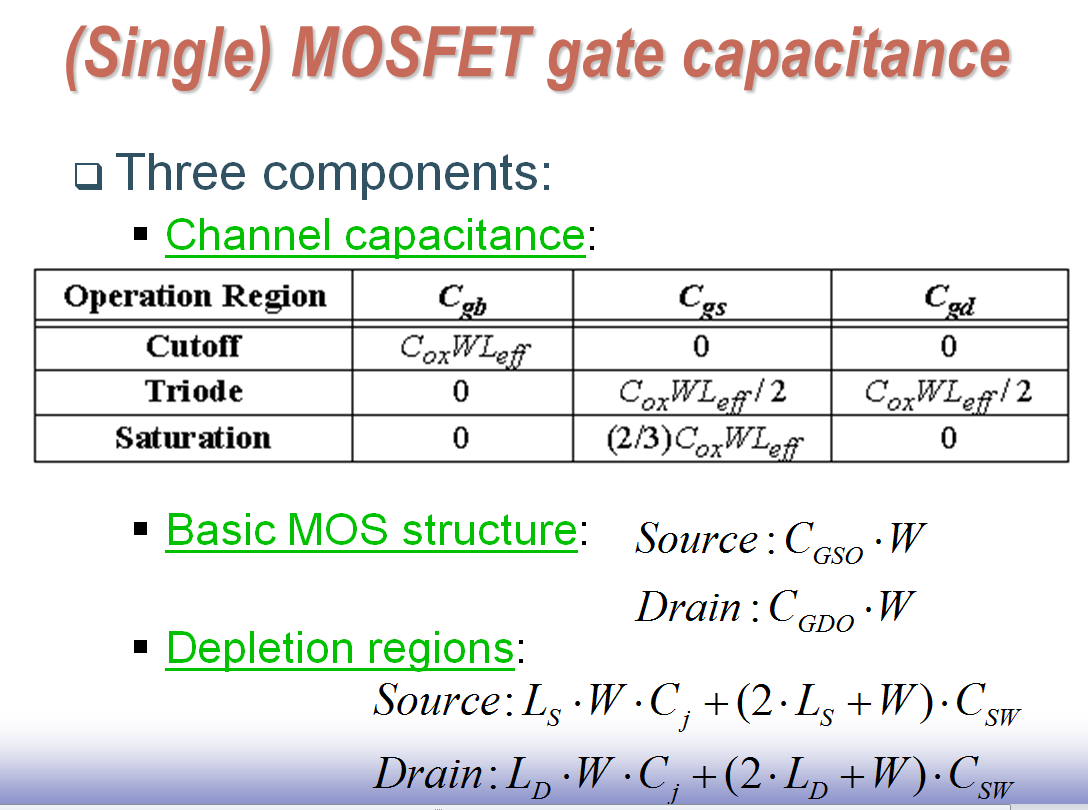
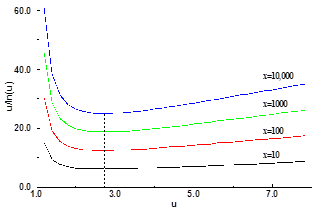
Inverter sizing: 

Delay: 

Power: 







‘***f***’ values and delay. Minimum at ‘e’.

Definition: VTC or transfer characteristics: Vout on Y-axis, Vin on X-axis. More generally: Input on X-axis, output on Y-axis.

Rules:

No calculators.

Only the attached cheat sheet allowed.

No cheating.

Show work where asked (or no credit!).

|  |  |  |
| --- | --- | --- |
| Question | Pts | Score |
| 1a-d | 20 |  |
| 2 | 5 |  |
| 3 | 8 |  |
| 4 | 8 |  |
| 5 | 5 |  |
| Total | 46 |  |



**NAME:** \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

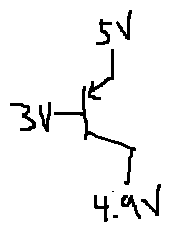
I promise not to discuss this exam with those that have not taken it yet.

Signature:\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

**EXAM:**

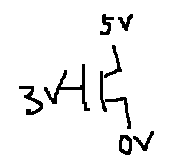
1. Regions of operation. Questions 1a through question 1c assume: VT=0.65V, VBE**ON**=0.3V, VBC**ON**=0.45V, and VCESAT=0.2V.
   1. Draw a pnp. Draw in voltages at the terminals that would put the pnp in the linear region.

**ANSWER:**

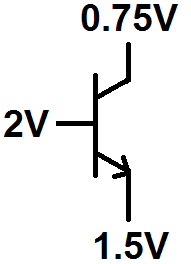


* 1. Draw a NMOS. Draw in voltages at the terminals that would put the NMOS in the active region.

**ANSWER:**

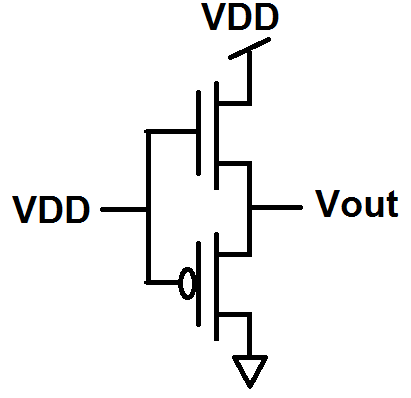


* 1. What region of operation is the following transistor in?



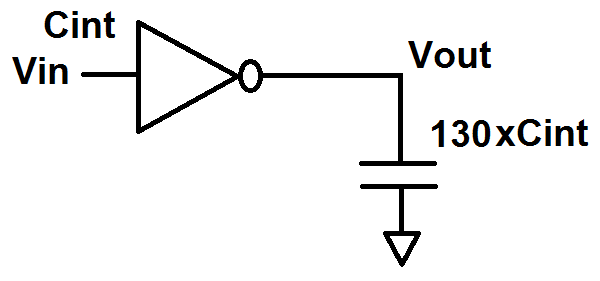
**ANSWER:** Cutoff

1. Short questions
   1. What is Vout for the following circuit? Note that both devices are NMOS.



**ANSWER:** VDD-VT. NMOS turn themselves off at VDD-VT. VG=Vin and VS =Vout so VGS=Vin-Vout

* 1. How many inverters would you cascade to drive the load, CL, efficiently?



**ANSWER:** If each subsequent inverter was ‘e’ times bigger, then picking 5 inverters would be best. 5 inverters would be able to drive 148xCint.

* 1. Is your answer to question 2b ideal? Why? (Short answers are GOOD!)

**ANSWER:** No. If you use all ‘e’ times bigger inverters then the last inverter is more powerful than what you need. If you find ‘f’ by using the f=F**(1/N)** you can find a more appropriate ‘f’ or you could just downsize the last inverter.

* 1. If you could pick one value to reduce by 5%, which value would it be if you were trying to lower power usage? Why?

**ANSWER:** VDD. It shows up as a squared value in the power equation so you get more kick for a change.

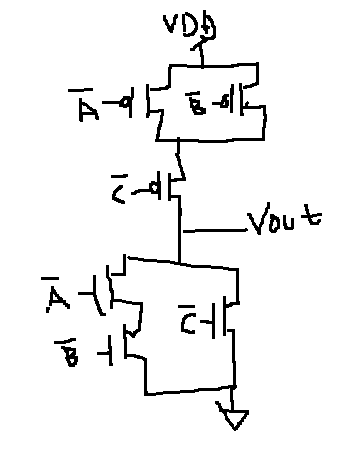
* 1. Why is frequency in the power equation? (Short answers are GOOD!)

**ANSWER:** C x V**2** is the energy for a single transition. Power is energy per second so you need to multiply the energy per conversion by how many times it transitions in a second. The probability term is in there because there isn’t a low to high transition on every clock tick. The probability term says how many of the clock ticks (of all the clock ticks) are low to high transitions.

1. Draw the complex COMPLEMENTARY circuit in MOSFET transistors that implements the logic equation: 

**ANSWER:**





1. Circuit characteristics. The last three pages of the exam have the graphs to use to answer questions 4a through 4h. Answer questions 4a through 4h using these graphs. You may tear off those pages if it’s more convenient. No math is needed 🡪 JUST SET UP EQUATIONS! No need to solve for final values but use numbers from graphs in equations. If you need capacitance for an answer, find it in terms of CGD, CDB etc. from the circuit diagram. \*\*\*\*Say which graph(s) you used in finding each answer when a graph is used\*\*\*\*
   1. What is the circuit’s logic equation?

**ANSWER:** 

* 1. How much noise can Vin have and still have the output solid as a HIGH? Assume Vin is 0V when there is no noise. \*\*\*\*

**ANSWER:** Graph 1: If Vout is HIGH, that means Vin is LOW. Vin can go up to the VIL point≈A little under 1V without messing up a HIGH Vout.

* 1. Is that different than NML?

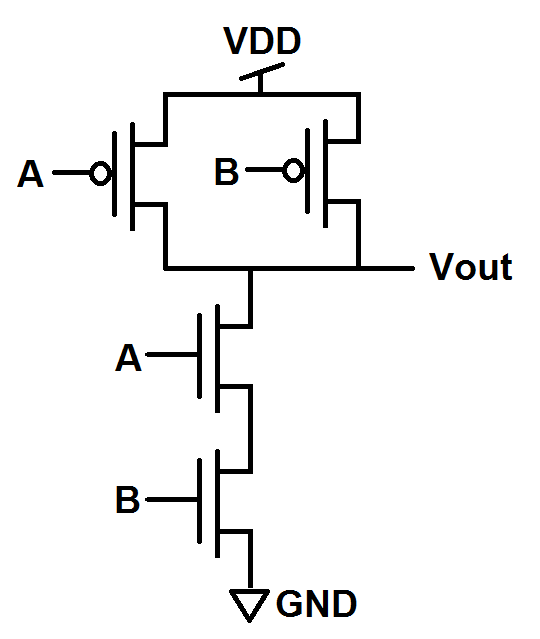
**ANSWER:** This tells you how much noise you can have on the low output value if you are chaining a number of these inverters together. So, yes, this is NML.

* 1. What is tpHL? \*\*\*\*
  2. What is tr? \*\*\*\*
  3. Where is this circuit’s regenerative region? Use voltages in your answer. \*\*\*\*
  4. How much energy is used for the tpHL transition? \*\*\*\*

**ANSWER:** None. You only dissipate power on a low to high transition.

* 1. How much energy is used for the tpLH transition? \*\*\*\*

Circuit and graphs for question 4. Assume B=1 and only A is changing so circuit can be analyzed as an inverter. VDD=2.5V.



**Graph 1:**

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| **VOUT** | | |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
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| **0** |  |  |  | **0.5** | |  |  | **1** | |  |  | **1.5** | |  |  | **2** | |  |  | **2.5** | | **VIN** | | |  |

**Graph 2:**

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| **I for PUN (Pull up network) - mA** | | | | | | | | | | | | | | | | | | | | | |  |  |  |  |
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| **0** |  |  |  | **0.5** | |  |  | **1** | |  |  | **1.5** | |  |  | **2** | |  |  | **2.5** | | **VDS** | | | |
| **Graph 3:** | | | | | | | | | | | | | | | | | | |  |  |  |  |  |  |  |
| **I for PDN (Pull down network) - mA** | | | | | | | | | | | | | | | | | | | | | | | |  |  |
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**Graph 4:**

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| **VOUT** | | |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| **2.5** |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
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| **1.5** |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
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