EGR 234 – Digital Logic Design Lab 8: Modular Approach for a Double-Digit BCD Adder

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Exercise 1

VHDL Code for Single Bit Comparator Module

```
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-- single bit comparator module
______
library ieee;
use ieee.std_logic_1164.all;
entity bit comp is
 port (Gin, Ein, Lin, x, y: in std logic;
  Gout, Eout, Lout : out std logic);
end bit comp;
architecture bit comp arch of bit comp is
begin
 process(Gin, Ein, Lin, x, y)
 begin
   if (Gin = '1' \text{ and } Ein = '0' \text{ and } Lin = '0') then
                    Gout <= '1';
                    Eout <= '0';
                    Lout <= '0';
   elsif (Gin = '0' and Ein = '0' and Lin = '1') then
                    Gout <= '0';
                    Eout <= '0';
                    Lout <= '1';
   elsif (Gin = '0' and Ein = '1' and Lin = '0') then
                    if (x > y) then
                           Gout <= '1';
                           Eout <= '0';
                           Lout <= '0';
                    elsif (x = y) then
                           Gout <= '0':
                           Eout <= '1';
                           Lout <= '0';
                    else
                           Gout <= '0';
                           Eout <= '0';
                           Lout <= '1';
                    end if;
    else
                    Gout <= '0';
                    Eout <= '0';
```

Functional Simulation Waveform

	Master	Time Bar:		0 ps	111	Pointer:	5.9 ns	Interva	l:	5.9 ns	Start:			End:		
A ⊛ ⊕		Name	Value at 0 ps	0 ps 0 ps	10.0 ns	20.0 ns	30.0 ns	40.0 ns	50.0 ns	60.0 ns	70.0 ns	80.0 ns	90.0 ns	100 _i 0 ns	110 _, 0 ns	120.0 ns
⊕(□ 0	Gin	U ps B 1	1 2 2 3									1			
_	<u>→</u> 1	Ein	B 0													
44	1 ≥ 2	Lin	B 0													
	1 3 1 4 1 1 1 1 1 1 1 1 1 1	x v	B 0 B 0			_	_					_				
	⊚ 5	Gout	B 1													
煕	⊕ 6	Eout	B 0	-												
≜ ↓	⊚ 7	Lout	B 0	1												

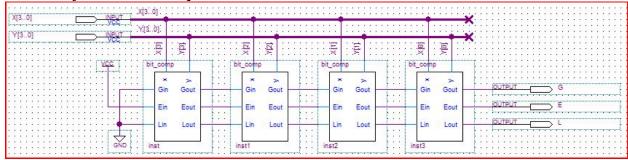
Truth Table for Single Bit Comparator Module

Truin Tuble for Single Bu Compartior Module								
Gin	Ein	Lin	X	Y		Gout	Eout	Lout
1	0	0	0	0		1	0	0
1	0	0	0	1		1	0	0
1	0	0	1	0		1	0	0
1	0	0	1	1		1	0	0
0	0	1	0	0		0	0	1
0	0	1	0	1		0	0	1
0	0	1	1	0		0	0	1
0	0	1	1	1		0	0	1
0	1	0	0	0		0	1	0
0	1	0	0	1		0	0	1
0	1	0	1	0		1	0	0
0	1	0	1	1		0	1	0

This table accurately interprets the functional simulation and proves the VHDL code works.

Exercise 2

Schematic for the 4-bit Comparator Module

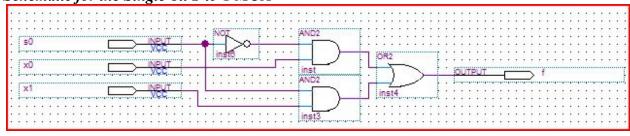


Function Simulation Waveform for 4-bit Comparator Module

		Value	0 ps	10.0 ns	20.0 ns	30.0 ns		40.0 ns	50.0 ns 60	0.0 ns
	Name	0 p	0 ps							
₽ 0	ΞX	н	5	X	В	6 X	E	<u>X</u> 1	χ c	
<u></u> 1 1	—X[3]	Н								_
<u></u> 2	—X[2]	Н								_
<u>→</u> 3	—X[1]	Н								
<u>□▶</u> 4	_×[0]	Н								
₽ 5	ΞY	H:	2	X	7 X	6	E	χ 8	X F	
→ 5 → 6	—Y[3]	Н								
<u>m</u> >7	—Y[2]	Н								
® 8	-Y[1]	Н								
■ 9	──Y[0]	H								$\overline{}$
⊚ 10	G	В			2					
	E	В						¬		
⊕ 12	L	В								\neg

Exercise 3

Schematic for the Single-bit 2-to-1 MUX



Function Simulation Waveform for Single-bit 2-to-1 MUX

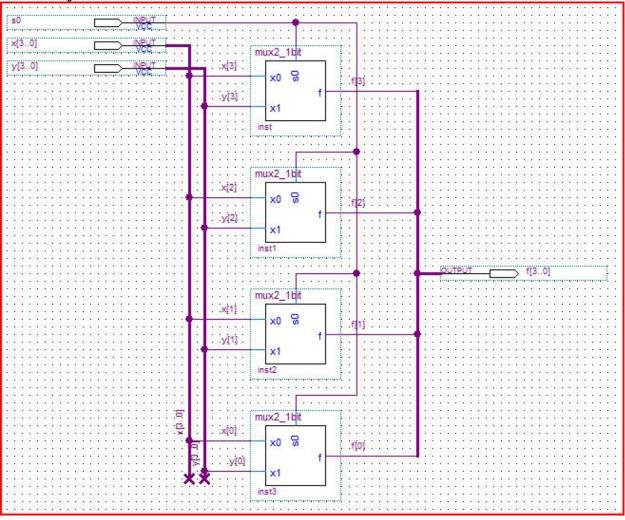
	120	Value at	0 ps	10.0 ns	20.0 ns	30.0 ns	40.0 ns	50.0 ns	60.0 ns	70.0 ns	80.0 ns
	Name	0 ps	0 ps								
i 0 €	s0	B 0									- 5
<u>→</u> 1	x0	B 0									7
<u></u> 2	x1	B 0							-		
- 3	f	B 0									100

Truth Table for Single-bit 2-to-1 MUX

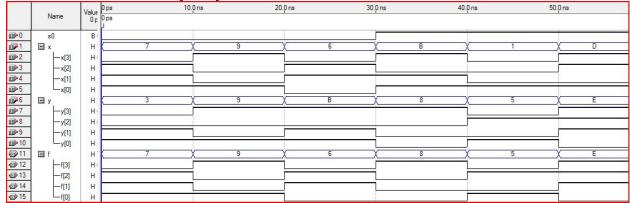
	<u>, </u>		
s0	x0	x 1	f
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

The Truth Table matches up with the functional waveform and shows the 2-to-1 MUX is functioning correctly.

Schematic for the 4-bit 2-to-1 MUX



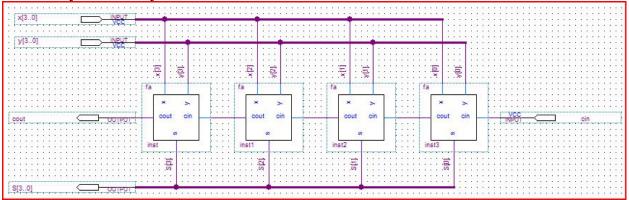
Function Simulation Waveform for 4-bit 2-to-1 MUX



The outputs for the 2-to-1 MUX are correct which shows the MUX is working properly.

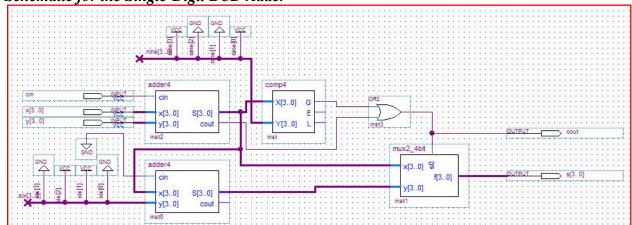
Exercise 4

Schematic for the modified 4-bit Adder

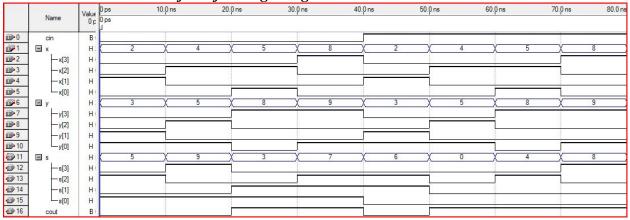


Exercise 5

Schematic for the Single-Digit BCD Adder



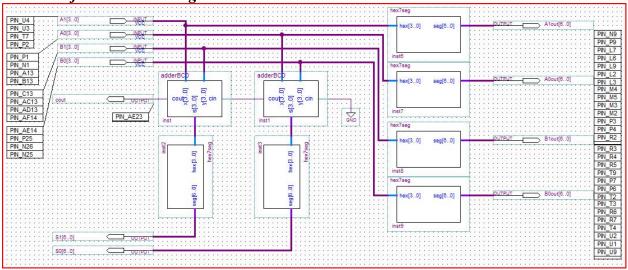
Function Simulation Waveform for Single-Digit BCD Adder



The waveform shows the correct output for the various cases. This shows the single-digit BCD adder is functional.

Exercise 6

Schematic for the Double-Digit BCD Adder



The BCD adder was tested on the DE2 board and functioned as it should have. This shows each module is functional and the overall Double Digit BCD Adder is also correct.