RT_Main.vi
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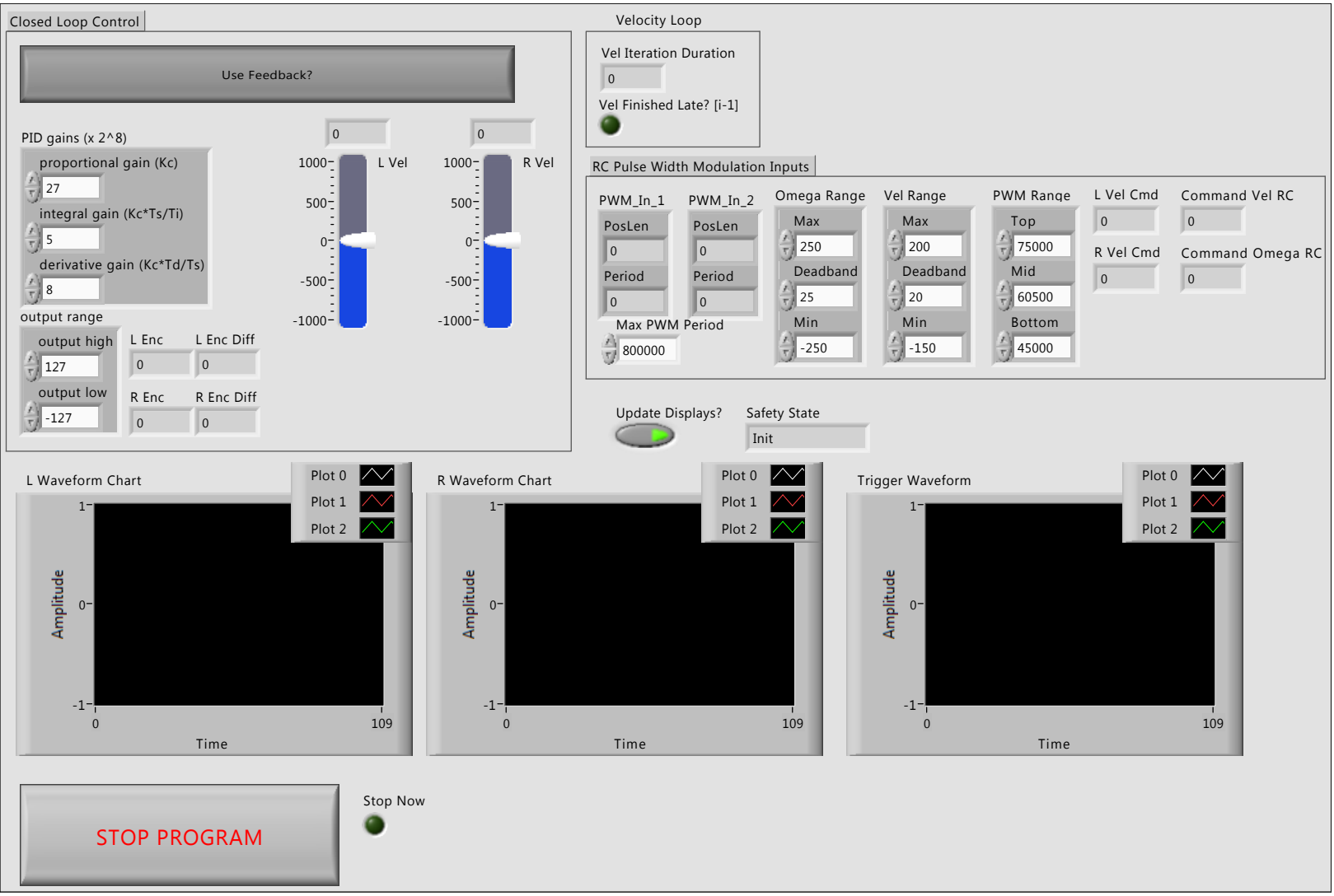
Connector Pane

RT_Main.vi

Main Real-Time Loop for the CWRU Cutter Hex Compact RIO. Executes the FPGA bitfile. Set to run on Startup.

Responsibilities:
Start the FPGA
Supply velocity values to the FPGA from various sources
Run the safety state machine. Control inputs/outputs (relays, beeper, etc)
Communicate with the ITX computer (not implemented yet)

Front Panel



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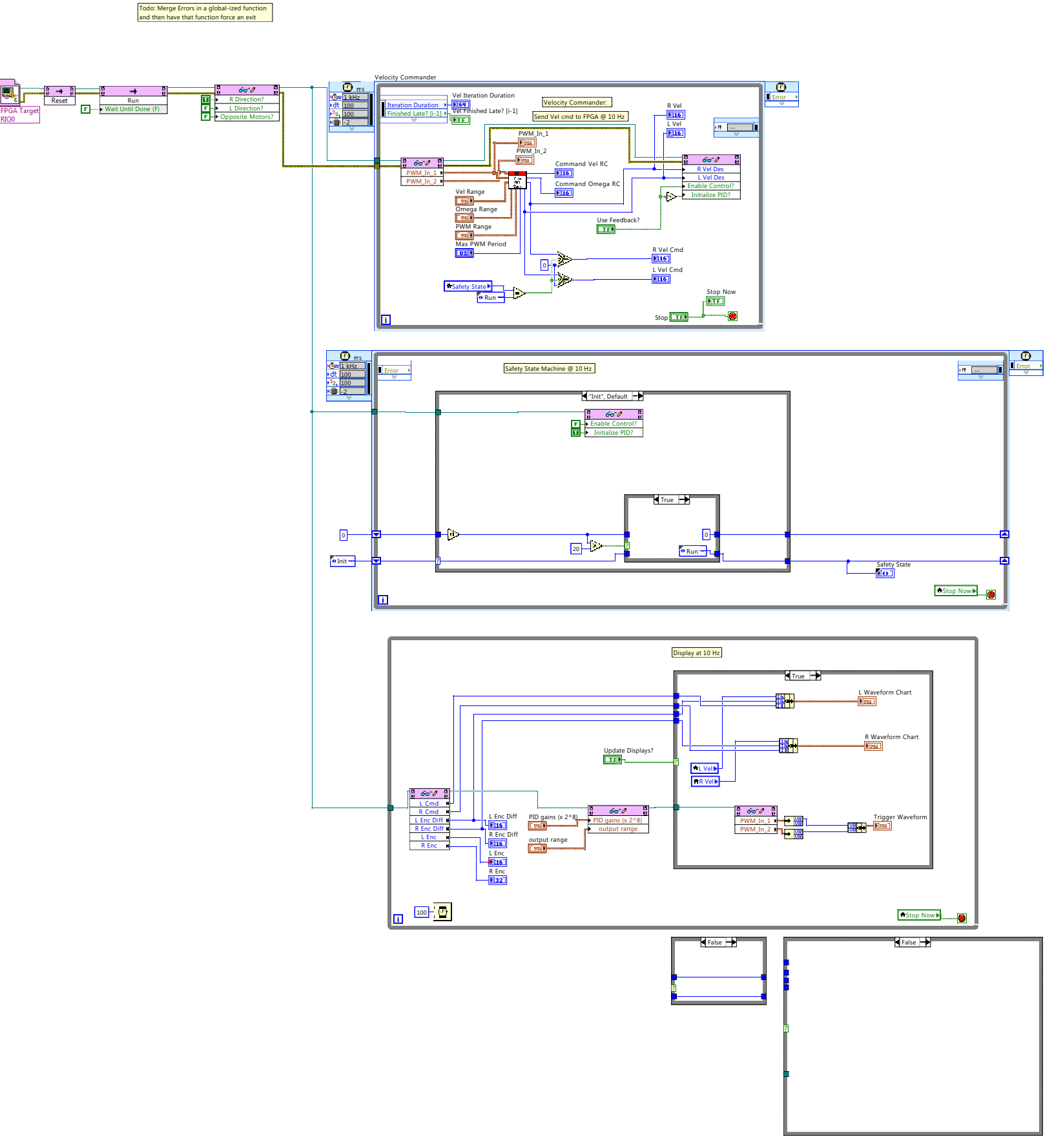
Block Diagram



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