

RT\_Main.vi  
M:\CWRUCutterHex\LabVIEW\src\RT\_Main.vi  
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## Connector Pane

### RT\_Main.vi



Main Real-Time Loop for the CWRU Cutter Hex Compact RIO. Executes the FPGA bitfile. Set to run on Startup.

### Responsibilities:

Start the FPGA

Supply velocity values to the FPGA from various sources

Run the safety state machine. Control inputs/outputs (relays, beeper, etc)

Communicate with the ITX computer (not implemented yet)

## Front Panel

Use Feedback?

PID gains (x 2^8)

proportional gain (Kc)

27

integral gain (Kc\*Ts/Ti)

5

derivative gain (Kc\*Td/Ts)

8

output range

output high

127

output low

-127

L Enc

0

L Enc Diff

0

R Enc

0

R Enc Diff

0

0

L Vel

0

R Vel

0

Velocity Loop

Vel Iteration Duration

0

Vel Finished Late? [i-1]

RC Pulse Width Modulation Inputs

PWM\_In\_1

PosLen

0

Period

0

Max PWM Period

800000

PWM\_In\_2

PosLen

0

Period

0

Omega Range

Max

250

Deadband

25

Min

-250

Vel Range

Max

200

Deadband

20

Min

-150

PWM Range

Top

75000

Mid

60500

Bottom

45000

L Vel Cmd

0

R Vel Cmd

0

Command Vel RC

0

Command Omega RC

0

Update Displays?

Safety State

Init

L Waveform Chart

Plot 0

Plot 1

Plot 2

R Waveform Chart

Plot 0

Plot 1

Plot 2

Trigger Waveform

Plot 0

Plot 1

Plot 2

STOP PROGRAM

Stop Now



RT\_Main.vi

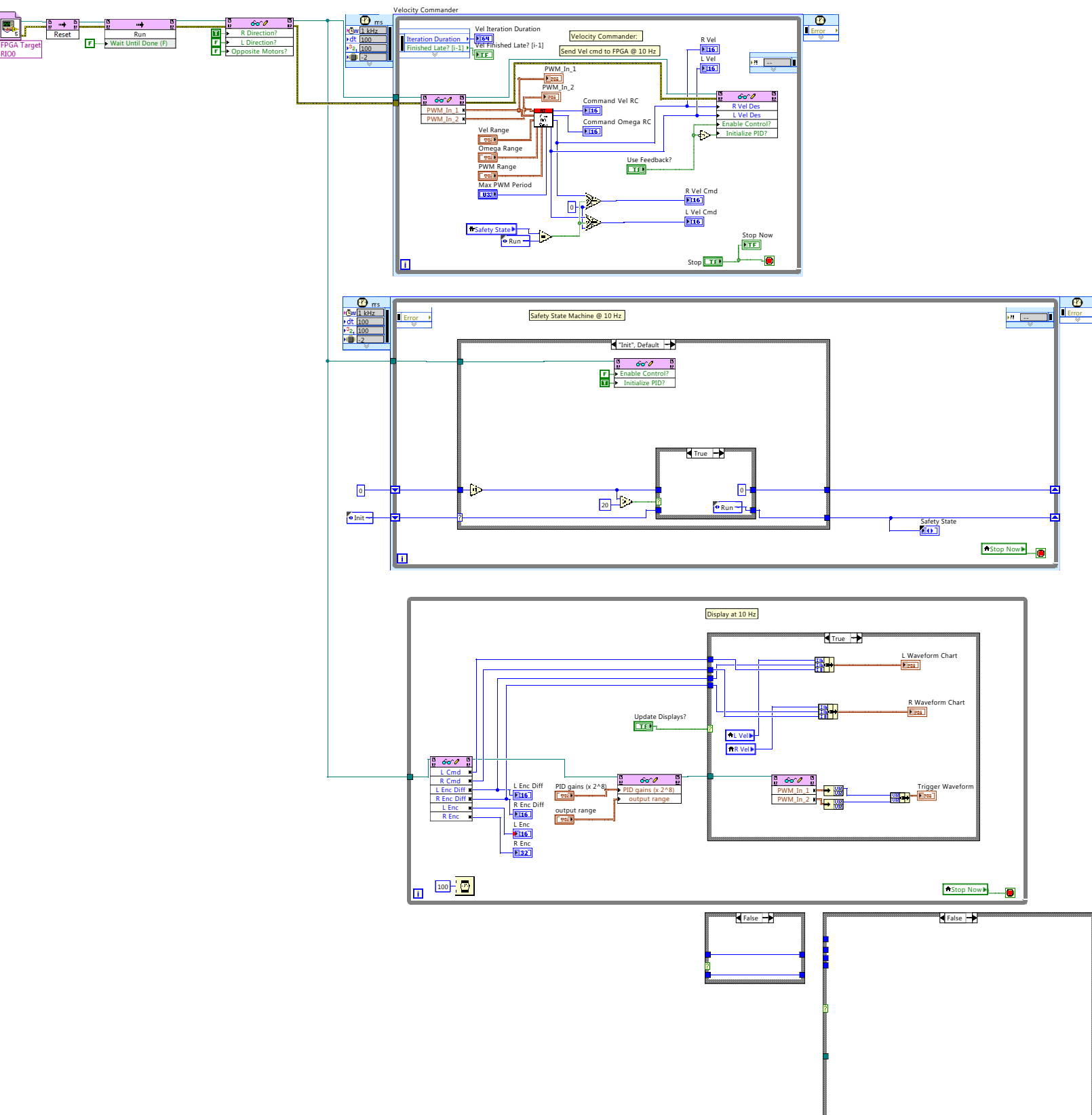
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## Block Diagram

Todo: Merge Errors in a global-ized function and then have that function force an exit





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