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Part1

见图 1.

图 1: Part1

Part2

见图 2.

```
cwy@ubuntu:~/gem5$ build/ARM/gem5.opt configs/proj1/simple.py
gem5 Simulator System. https://www.gem5.org
gem5 is copyrighted software; use the --copyright option for details.
gem5 version 22.0.0.2
gem5 compiled Sep 20 2022 12:08:12
gem5 started Sep 20 2022 19:32:40
gem5 executing on ubuntu, pid 11976
command line: build/ARM/gem5.opt configs/proj1/simple.py
Global frequency set at 1000000000000 ticks per second
warn: No dot file generated. Please install pydot to generate the dot file and p
build/ARM/mem/dram_interface.cc:692: warn: DRAM device capacity (32768 Mbytes) d
oes not match the address range assigned (2048 Mbytes)
0: system.remote gdb: listening for remote gdb on port 7000
build/ARM/sim/simulate.cc:194: info: Entering event queue @ 0. Starting simulat
ion...
Hello world!
Exiting @ tick 289397500 because exiting with last active thread context
cwy@ubuntu:~/gem5$
```

图 2: Part2

Part3

见图 3.

```
cwy@ubuntu: ~/gem5
rne Edit View Search Terminal Help
system.cpu.mmu.stage2_itb.flushTlbAsid 0
system.cpu.mmu.stage2_itb.flushTlbAsid 0
system.cpu.mmu.stage2_itb.instAccesses 0
system.cpu.mmu.stage2_itb.hits 0
system.cpu.mmu.stage2_itb.hits 0
system.cpu.mmu.stage2_itb.misses 0
system.cpu.mmu.stage2_itb.misses 0
system.cpu.mmu.stage2_itb_walker.walks 0
system.cpu.mmu.stage2_itb_walker.requestOrigin_Requested::Data
(Count)
                                                                                                                                                                                                                                                                                                                            # Number of times TLB was flushed by ASID (Count)
# Number of entries that have been flushed from TLB (Count)
# Inst accesses (Count)
# Total TLB (inst and data) hits (Count)
# Total TLB (inst and data) misses (Count)
# Total TLB (inst and data) accesses (Count)
# Table walker walks requested (Count)
# Table walker requests started/comple
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         requests started/completed, data/inst
  .
Count)
system.cpu.mmu.stage2_itb_walker.requestOrigin_Requested::Inst
                                                                                                                                                                                                                                                                                                                                                                                                                        # Table walker requests started/completed, data/inst
       stem.cpu.mmu.stage2_itb_walker.requestOrigin_Requested::total
                                                                                                                                                                                                                                                                                                                                                                                                                            # Table walker requests started/completed, data/inst
    ystem.cpu.mmu.stage2_itb_walker.requestOrigin_Completed::Data
                                                                                                                                                                                                                                                                                                                                                                                                                        # Table walker requests started/completed, data/inst
       stem.cpu.mmu.stage2_itb_walker.request0rigin_Completed::Inst
                                                                                                                                                                                                                                                                                                                                                                                                                         # Table walker requests started/completed, data/inst
                           .
cpu.mmu.stage2_itb_walker.request0rigin_Completed::total
                                                                                                                                                                                                                                                                                                                                                                                                                            # Table walker requests started/completed, data/inst
  o (count)
cystem.cpu.mmu.stage2_itb_walker.requestOrigin_Completed::total
o (count)
cystem.cpu.mmu.stage2_itb_walker.power_state.pwrStateResidencyTicks::UNDEFINED
system.cpu.mmu.stage2_itb_walker.power_state.pwrStateResidencyTicks::UNDEFINED
spower_states (Tick)
system.cpu.power_state.pwrStateResidencyTicks::ON
289397500
system.cpu.thread_0.numInsts
0 #Ni
system.cpu.thread_0.numOps
0 #Ni
system.cpu.thread_0.numMops
13 #Ni
system.cpu.thread_0.numMyscalls
system.mem_ctrl.avgPriority_cpu.inst::samples
so30.00
system.mem_ctrl.avgPriority_cpu.data::samples
so30.00
system.mem_ctrl.priorityMinlatency
system.mem_ctrl.priorityMinlatency
system.mem_ctrl.priorityMinlatency
system.mem_ctrl.priorityMinlatency
system.mem_ctrl.numReadWriteTurnArounds
0 #Ni
system.mem_ctrl.numReadWriteTurnArounds
0 #Ni
system.mem_ctrl.numStayReadState
12966
#Ni
system.mem_ctrl.numStayReadState
0 #Ni
system.mem_ctrl.numStayReadState
0 #Ni
system.mem_ctrl.readReqs
6091
#Ni
system.mem_ctrl.readBursts
6091
#Ni
system.mem_ctrl.writeReqs
936
#Ni
system.mem_ctrl.writeRequestr
                                                                                                                                                                                                                                                                                                                                                    # Table walker requests started/completed, data/inst (Count)
289397500  # Cumulative time (in ticks) in vari
                                                                                                                                                                                                                                                                                                                          # Cumulative time (in ticks) in various power states (Tick)

# Number of Instructions committed (Count)

# Number of Ops committed (Count)

# Number of Memory References (Count)

# Number of system calls (Count)

# Average QoS priority value for accepted requests (Count)

# Average QoS priority value for accepted requests (Count)

# per QoS priority minimum request to response latency (Second)

# per QoS priority maximum request to response latency (Second)

# Number of turnarounds from READ to WRITE (Count)

# Number of times bus staying in READ state (Count)

# Number of times bus staying in WRITE state (Count)

# Number of read requests accepted (Count)

# Number of write requests accepted (Count)

# Number of write requests accepted (Count)

# Number of controller read busses, including those serviced by the write q
   ystem.nem_ctrl.readBursts
eue (Count)
ystem.nem_ctrl.writeBursts
ue (Count)
ystem.mem_ctrl.servicedByWrQ
ystem.nem_ctrl.mergedWrBursts
ystem.nem_ctrl.avgRdQLen
ystem.nem_ctrl.avgRdQLen
                                                                                                                                                                                                                936
                                                                                                                                                                                                                                                                                                                             # Number of controller write bursts, including those merged in the write qu
                                                                                                                                                                                                                                                                                                                             # Number of controller read bursts serviced by the write queue (Count)
# Number of controller write bursts merged with an existing one (Count)
# Number of requests that are neither read nor write (Count)
# Average read queue length when enqueuing ((Count/Tick))
```

图 3: Part3

Part4

1和2

见图 4-2, DDR3-2133-8x8 对 4 个 test bench 都是最优的.

	Α	В	В С		Е	F	G	Н	
1	IPC	ddr3_1600_8x8	ddr3_2133_8x8	ddr4_2400_16x4	ddr4_2400_8x8	lpddr2_s4_1066_1x32	wideio_200_1x128	lpddr3_1600_1x32	
2	2mm	0.360110349	0.362531674	0.362086769	0.362061551	0.351232583	0.345761534	0.354820663	
3	bfs	0.354015748	0.354118715	0.35399409	0.35399409	0.353681581	0.353192462	0.353816916	
1	bzip2	0.215339269	0.216952216	0.215875045	0.215881085	0.19971445	0.198100758	0.208397094	
5	mcf	0.176221438	0.178670182	0.17790945	0.177876007	0.162198158	0.149833988	0.164771174	
3									
7									
}	bandwidth	ddr3_1600_8x8	ddr3_2133_8x8	ddr4_2400_16x4	ddr4_2400_8x8	lpddr2_s4_1066_1x32	wideio_200_1x128	lpddr3_1600_1x32	
)	2mm	106444101	107159814	107028306	107020852	103819945	102202771	104880536	
0	bfs	10052051	10054974	10051436	10051436	10042562	10028674	10046405	
1	bzip2	365731446	368470870	366641406	366651664	339194309	336453620	353940881	
2	mcf	419570354	425400634	423589385	423509760	386181949	356743766	392308112	
3									
4									

图 4: 4-2

3

见图 4-3.

对于 2mm, o3 1.8GHZ 在两个指标上总体较好. 对于 bfs, o3 3.6GHZ 在两个指标上总体较好. 对于

/	А	В	С	D	Е	F	G	Н	1	J	К	L
1	IPC	2mm	bfs	bzip2	mcf			sim seconds	2mm	bfs	bzip2	mcf
2	o3 0.3GHZ	2.1884982	2.2387285	1.5572603	1.2214921			o3 0.3GHZ	1.522962	1.488791	2.140297	2.72863
3	o3 0.6GHZ	2.0045784	2.2266416	1.4021432	0.9414125			o3 0.6GHZ	0.831596	0.748661	1.188894	1.770743
4	o3 0.9GHZ	1.83101	2.2153374	1.2684961	0.7651734			o3 0.9GHZ	0.606769	0.501504	0.87584	1.451958
5	o3 1.8GHZ	1.4289197	2.1803474	0.9670497	0.4857382			o3 1.8GHZ	0.389105	0.255005	0.574945	1.144649
6	o3 2.7GHZ	1.162486	2.1428539	0.7784939	0.3542958			o3 2.7GHZ	0.318283	0.172667	0.475277	1.044325
7	o3 3.6GHZ	0.9789714	2.0895617	0.6491703	0.279431			o3 3.6GHZ	0.283972	0.133042	0.428239	0.994879
8	o3 5GHZ	0.7865969	2.0704371	0.5144498	0.2107843			o3 5GHZ	0.25426	0.096598	0.388765	0.948837
9	o3 8GHZ	0.5523084	1.9789789	0.3594151	0.137465			o3 8GHZ	0.226323	0.063164	0.347787	0.909323
10	inorder 0.3GHZ	0.8736385	0.8792597	0.6965177	0.6183073			inorder 0.3GHZ	3.815079	3.790689	4.785233	5.390523
11	inorder 0.6GHZ	0.8368605	0.8761815	0.6329134	0.4958912			inorder 0.6GHZ	1.991969	1.902574	2.633852	3.361624
12	inorder 0.9GHZ	0.8000167	0.8730132	0.5798084	0.414508			inorder 0.9GHZ	1.388721	1.272604	1.91615	2.680286
13	inorder 1.8GHZ	0.7101239	0.8640435	0.4559188	0.2764957			inorder 1.8GHZ	0.782962	0.643486	1.219515	2.010881
14	inorder 2.7GHZ	0.6390454	0.8552249	0.3728923	0.2068693			inorder 2.7GHZ	0.578989	0.432635	0.992244	1.788569
15	inorder 3.6GHZ	0.5815876	0.8462894	0.3205835	0.1651292			inorder 3.6GHZ	0.478002	0.328493	0.867169	1.68353
16	inorder 5GHZ	0.5108434	0.8344598	0.2605685	0.126244			inorder 5GHZ	0.391509	0.239676	0.767552	1.584233
17	inorder 8GHZ	0.3985478	0.8100018	0.1858863	0.0835935			inorder 8GHZ	0.313639	0.154321	0.672454	1.495331

图 5: 4-3

bzip2, o3 0.9GHZ 在两个指标上总体较好. 对于 mcf, o3 2.7GHZ 在两个指标上总体较好.