

Lab #3

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Part1

1

把 L2Cache 和 L3Cache 连起来、L3Cache 和 membus 连起来就行. 结果如图 1.

```
1 [root]
2 type=Root
3 children=system
4 eventq_index=0
5 full_system=false
6 sim_quantum=0
7 time_sync_enable=false
8 time_sync_period=100000000000
9 time_sync_spin_threshold=100000000
10
11 [system]
12 type=System
13 children=clk_domain cpu dvfs_handler l2bus l2cache l3cache mem_ctrl membus workload
14 auto_unlink_shared_backstore=false
15 cache_line_size=64
16 eventq_index=0
17 exit_on_work_items=false
18 init_param=0
19 m5ops_base=0
20 mem_mode=timing
21 mem_ranges=0:2147483648
22 memories=system.mem_ctrl.dram
23 mmap_using_noreserve=false
24 multi_thread=false
25 num_work_ids=16
26 readfile=
27 redirect_paths=
28 shadow_rom_ranges=
29 shared_backstore=|
30 symbolfile=
31 thermal_components=
32 thermal_model=None
33 work_begin_ckpt_count=0
34 work_begin_cpu_id_exit=-1
35 work_begin_exit_count=0
36 work_cpus_ckpt_count=0
37 work_end_ckpt_count=0
38 work_end_exit_count=0
39 work_item_id=-1
40 workload=system.workload
41 system_port=system.membus.cpu_side_ports[1]
```

图 1: 1_1

2

需要一个 l1bus 用来连 cpu 的 icache_port 和 dcache_port, 并将其与 l1Cache 相连. 结果如图 2.

```

1 [root]
2 type=Root
3 children=system
4 eventq_index=0
5 full_system=false
6 sim_quantum=0
7 time_sync_enable=false
8 time_sync_period=10000000000
9 time_sync_spin_threshold=100000000
10
11 [system]
12 type=System
13 children=clk_domain cpu dvfs_handler l1bus l1cache l2cache mem_ctrl membus workload
14 auto_unlink_shared_backstore=false
15 cache_line_size=64
16 eventq_index=0
17 exit_on_work_items=false
18 init_param=0
19 m5ops_base=0
20 mem_mode=timing
21 mem_ranges=0:2147483648
22 memories=system.mem_ctrl.dram
23 mmap_using_noreserve=false
24 multi_thread=false
25 num_work_ids=16
26 readfile=
27 redirect_paths=
28 shadow_rom_ranges=
29 shared_backstore=
30 symbolfile=
31 thermal_components=
32 thermal_model=None
33 work_begin_ckpt_count=0
34 work_begin_cpu_id_exit=-1
35 work_begin_exit_count=0
36 work_cpus_ckpt_count=0
37 work_end_ckpt_count=0
38 work_end_exit_count=0
39 work_item_id=-1
40 workload=system.workload
41 system_port=system.membus.cpu_side_ports[1]

```

图 2: 1_2

3

不需要 l1bus 或 l2bus 了. 将 L2D Cache 和 L2I Cache 到连到 membus 就行. 结果如图 3.

Part2

对于 2mm 这个 workload, IPC 见图 4.

对于 2mm 这个 workload, L1 Cache miss rate 见图 5.

```

1 [root]
2 type=Root
3 children=system
4 eventq_index=0
5 full_system=false
6 sim_quantum=0
7 time_sync_enable=false
8 time_sync_period=10000000000
9 time_sync_spin_threshold=10000000
10
11 [system]
12 type=System
13 children=clk_domain cpu dvfs_handler l2dcache l2icache mem_ctrl membus workload
14 auto_unlink_shared_backstore=false
15 cache_line_size=64
16 eventq_index=0
17 exit_on_work_items=false
18 init_param=0
19 m5ops_base=0
20 mem_mode=timing
21 mem_ranges=0:2147483648
22 memories=system.mem_ctrl.dram
23 mmap_using_noreserve=false
24 multi_thread=false
25 num_work_ids=16
26 readfile=
27 redirect_paths=
28 shadow_rom_ranges=
29 shared_backstore=
30 symbolfile=
31 thermal_components=
32 thermal_model=NULL
33 work_begin_ckpt_count=0
34 work_begin_cpu_id_exit=-1
35 work_begin_exit_count=0
36 work_cpus_ckpt_count=0
37 work_end_ckpt_count=0
38 work_end_exit_count=0
39 work_item_id=-1
40 workload=system.workload
41 system_port=system.membus.cpu_side_ports[2]

```

图 3: 1_3

对于 2mm 这个 workload, L2 Cache miss rate 见图 6.

对于 bfs 这个 workload, IPC 见图 7.

对于 bfs 这个 workload, L1 Cache miss rate 见图 8.

对于 bfs 这个 workload, L2 Cache miss rate 见图 9.

对于 bzip2 这个 workload, IPC 见图 10.

对于 bzip2 这个 workload, L1 Cache miss rate 见图 11.

对于 bzip2 这个 workload, L2 Cache miss rate 见图 12.

对于 mcf 这个 workload, IPC 见图 13.

对于 mcf 这个 workload, L1 Cache miss rate 见图 14.

对于 mcf 这个 workload, L2 Cache miss rate 见图 15.



图 4: 2mm_IPC

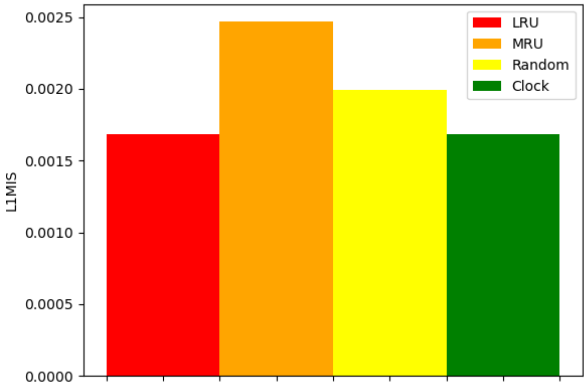


图 5: 2mm_L1MIS



图 6: 2mm_L2MIS



图 7: bfs_IPC

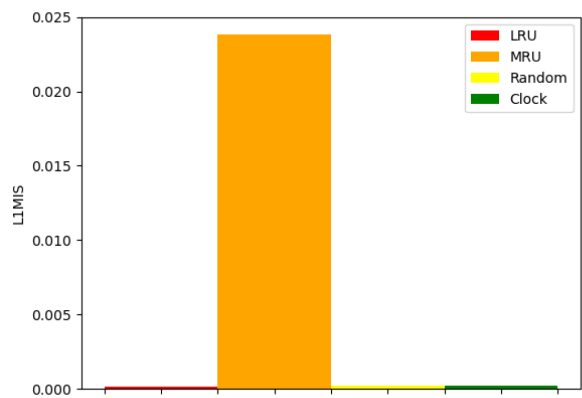


图 8: bfs_L1MIS

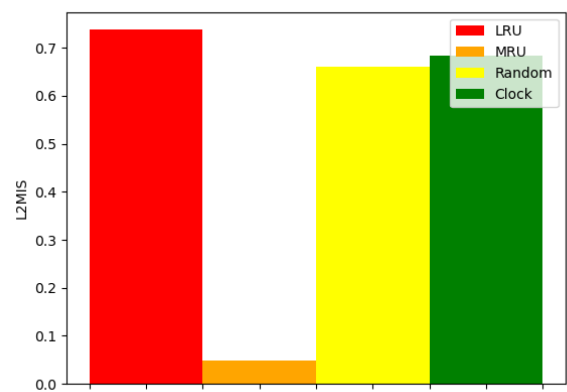


图 9: bfs_L2MIS

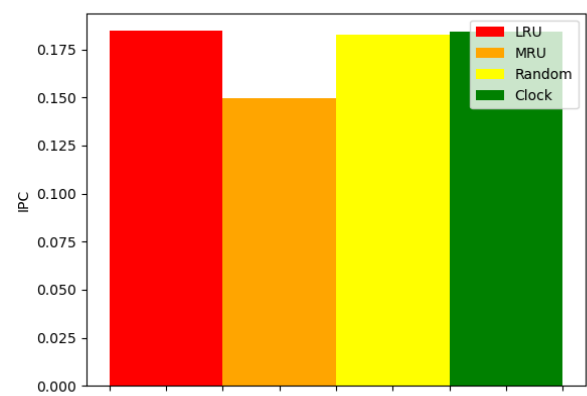


图 10: bzip2_IPC

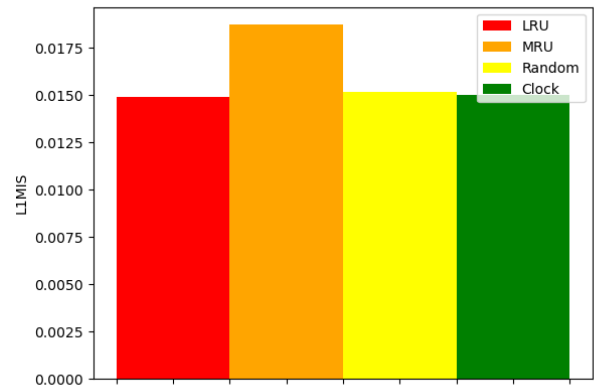


图 11: bzip2_L1MIS

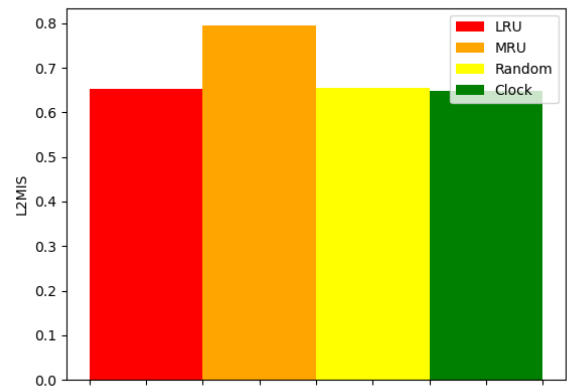


图 12: bzip2_L2MIS

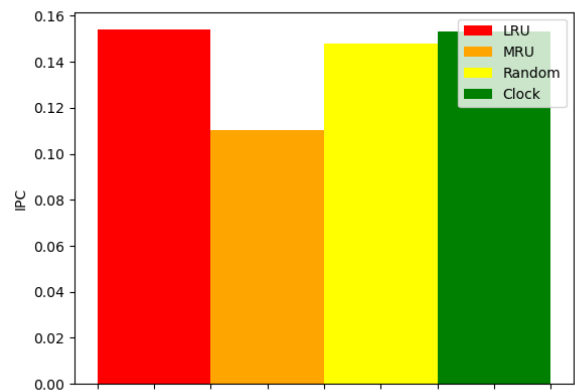


图 13: mcf_IPC

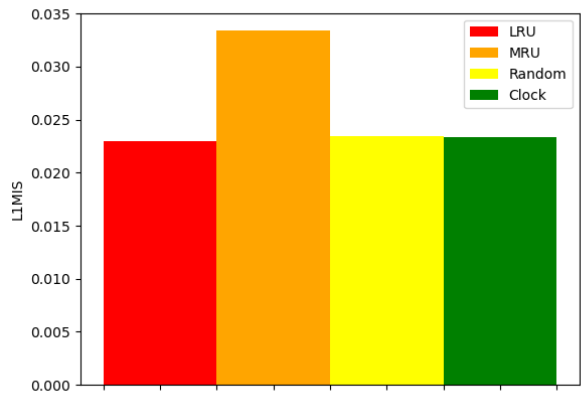


图 14: mcf_L1MIS

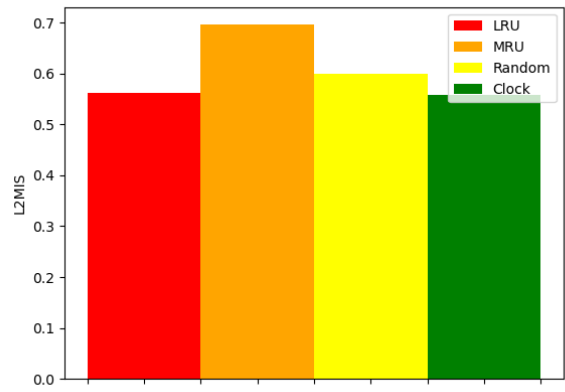


图 15: mcf_L2MIS