Chris Abajian

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OBJECTIVE

To build upon and utilize knowledge of RTL design, synthesis, and verification principles and gain valuable experience through co-op employment. Available Spring through Summer 2021.

EDUCATION

Rochester Institute of Technology, Rochester, NY
Bachelor of Science, Major in Computer Engineering, Minor in Mathematics. Expected May 2022.
GPA: 3.78/4.00
Awards: Dean's List Fall 2017 - present.
Courses:

Digital System Design I, II	Intro to Embedded Systems	Reconfigurable Computing
Interface & Digital Electronics	Digital Signal Processing	Circuits I, II

SKILLS

Languages:

- Most experience with: Verilog, VHDL, C, ARM Assembly, Java, HTML
- Some experience with: C++, JavaScript, Tcl, Bash, Python

Software: Linux (Ubuntu, CentOS), Git, RCS, ModelSim/Riviera, Vivado Design Suite, Altera Quartus, Keil uVision
Development: Familiar with Agile and Scrum development processes.

PROJECTS/LABS

- Developed an intelligent autonomous race car using the FRDM K64F microcontroller, a steering servo, two DC motors and a line scan camera. The car was developed using C and won first place in the class competition.
- Created a median filter on a Nexys4 DDR FPGA that utilizes AXI Stream to receive an image via UART, filter said image to remove salt and pepper artifacts, and return the filtered image over UART.
- Designed and developed a Morse Code decoder on an Artix-7 Basys 3 FPGA in Verilog.
- Created a portable, solar-powered Bluetooth weather station using Arduino and developed an Android application for the User Interface (www.instructables.com/id/BLEWeather-a-Portable-Bluetooth-Weather-Station/).
- Developed a color matching game for the Freedom KL46Z board which incorporated a serial I/O driver, a timer driver, and general-purpose I/O pins for LED indicators. Written in both ARM Assembly and C.

EXPERIENCE

Teaching Assistant, RIT *August 2020 – December 2020*

- Responsibilities include providing in-lab assistance and grading Applied for C laboratory assignments.

Design Engineer Co-op, Xelic, Inc. *January 2020 – August 2020*

- Converted a pre-existing OTN Ethernet core designed for an ASIC to a design suitable for the Stratix V FPGA family.
- Optimized LUT utilization wherever possible to minimize overall design size. Resolved timing errors by pipelining certain modules and keeping logic levels around 5 for any given path.
- Independently wrote Verilog RTL and verified newly created modules using System Verilog.
- Used Xilinx Vivado for synthesis and Riviera for large-scale simulation using a pre-existing verification environment.
- Learned and adhered to IEEE 802.3 Ethernet Specifications.

Web Developer, Schill Insurance Group, LLC. *May 2018 – September 2018*

- Designed and built the company website from the ground-up using Grav CMS for dynamic client creation and page edits. Implemented PGP encryption for enrollment forms that contain sensitive information.

ACTIVITIES/INTERESTS

Consumer PC hardware; Paddle boarding; Weightlifting; Soccer; Guitar; STEM Academy 2013-2017.