Anatomy of Ethernet Physical Layer Transceivers

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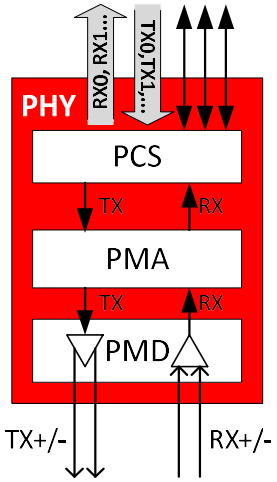
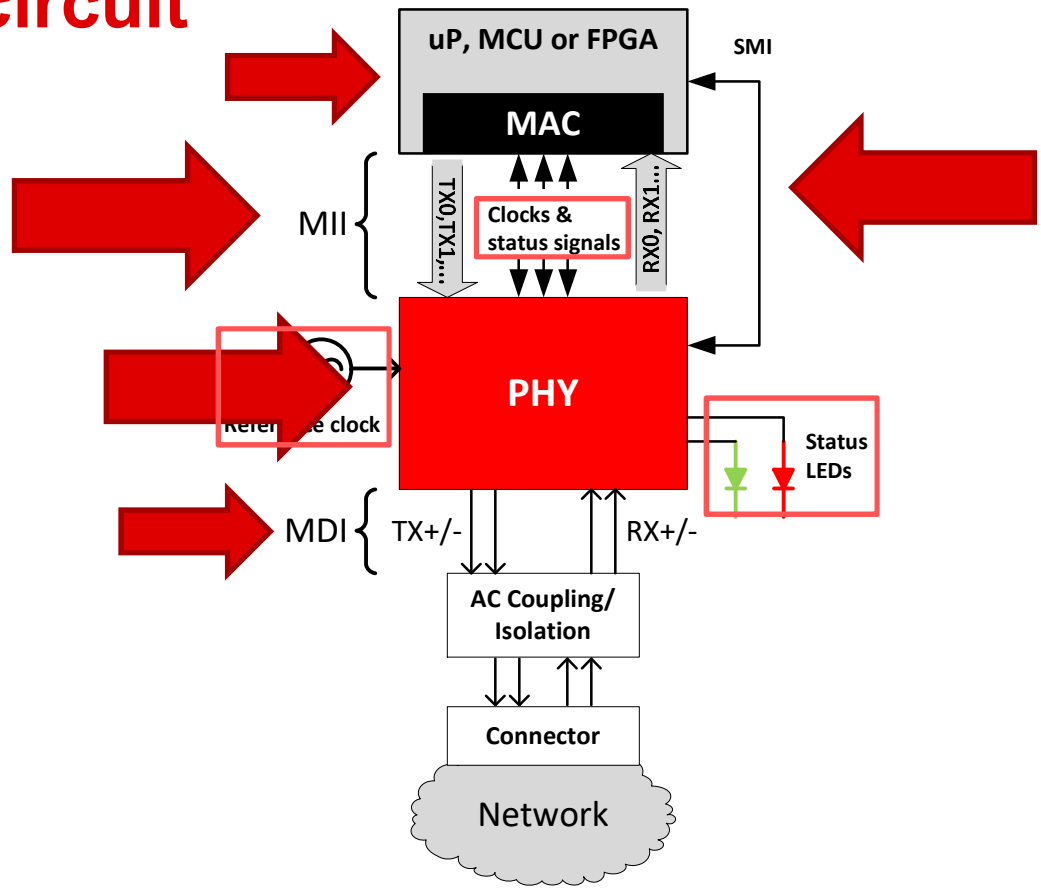
Anatomy of Ethernet PHY

- Typical application circuit
- Ethernet PHY block diagram
- PHY functions

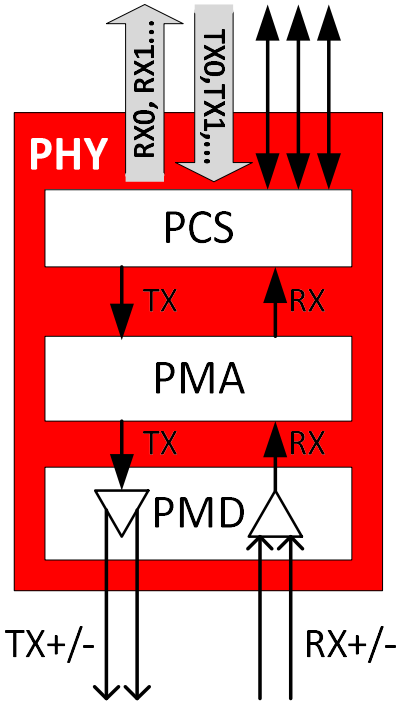


Typical application circuit



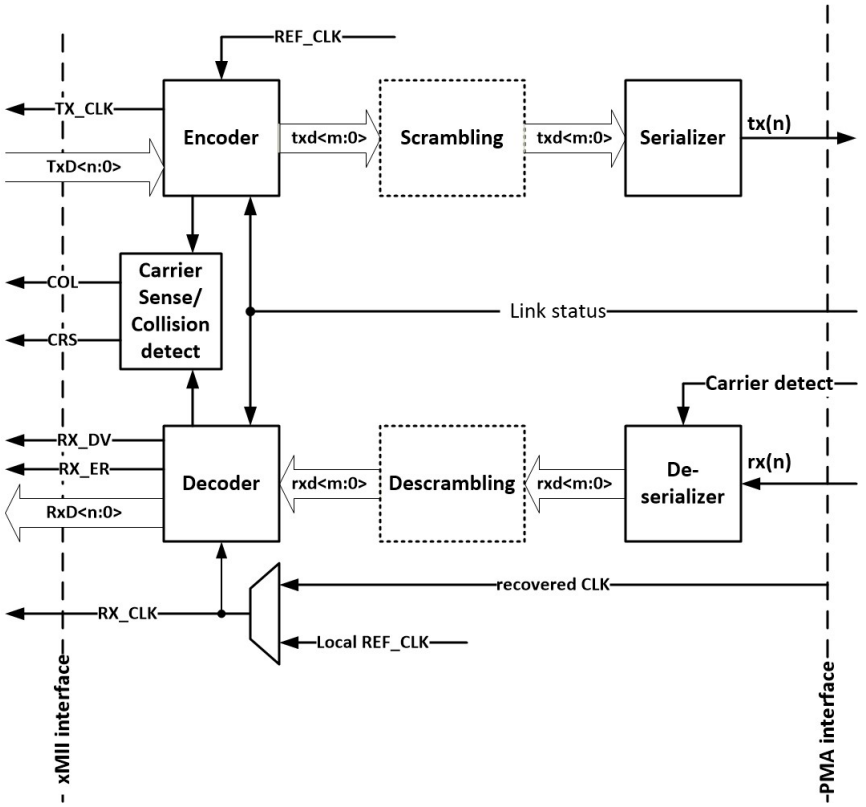
Internal PHY functional blocks

- The PHY consists of three sublayers:
  - **PCS -** Physical Coding Sublayer
  - **PMA -** Physical Medium Attachment layer
  - **PMD -** Physical Medium Dependent layer



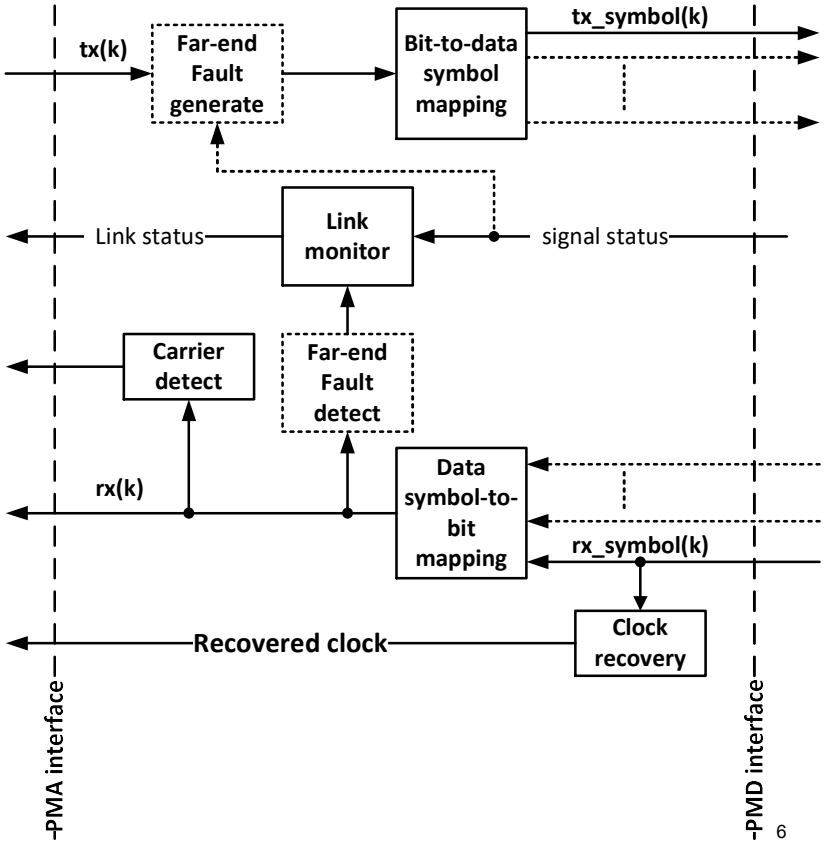
Physical Coding Sublayer (PCS)

- Responsible for encoding/decoding data
- Input to Carrier Sense and Collision Detect block, if used by the protocol
- Serializing/deserializing code groups at PMA interface
- Important for loopback testing



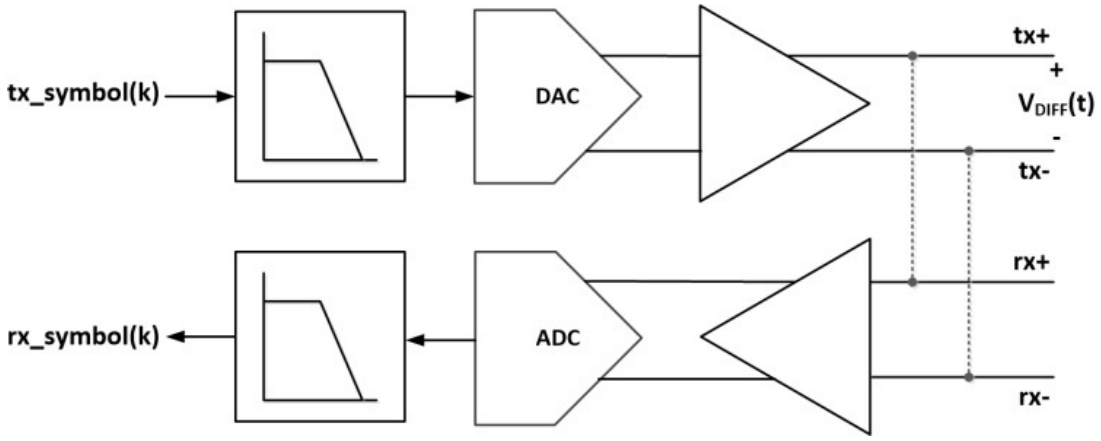
Physical Medium Attachment (PMA) sublayer

- Maps transmit and receive code-bits between the PCS and PMD, if present
  - Otherwise, directly maps code-bits to signal values used for the particular network implementation
- Recovers clock from received signal
- Generates indications and carrier errors from the PMD (if present) and sensing receive channel failures (Used for debugging)

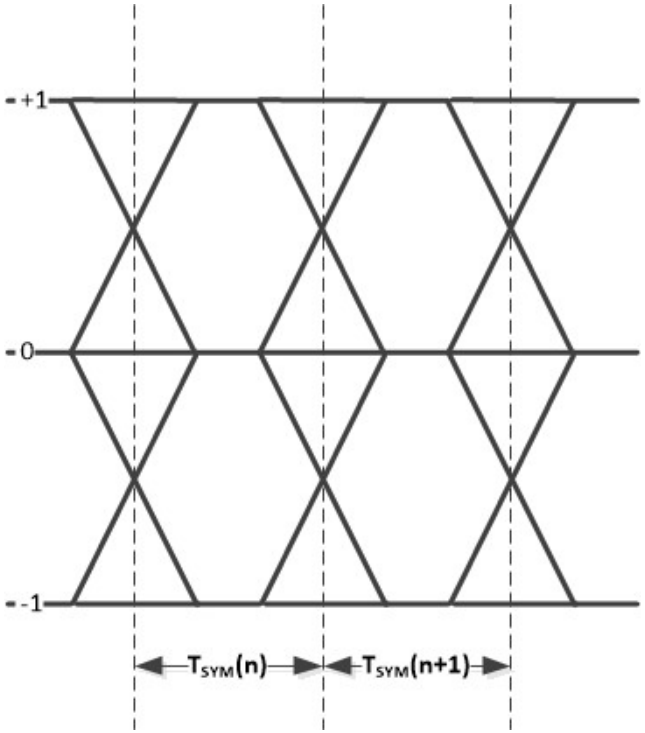


Physical Medium Dependent (PMD) sublayer

- Maps TX and RX symbol streams to signal values appropriate to medium used
- The PMD may not always be part of the PHY
  - Use of the PMD is defined by the specific version of the standard implemented by the PHY
- Provides inputs to line drivers, and accepts input from line receivers



Physical Medium Dependent (PMD) sublayer



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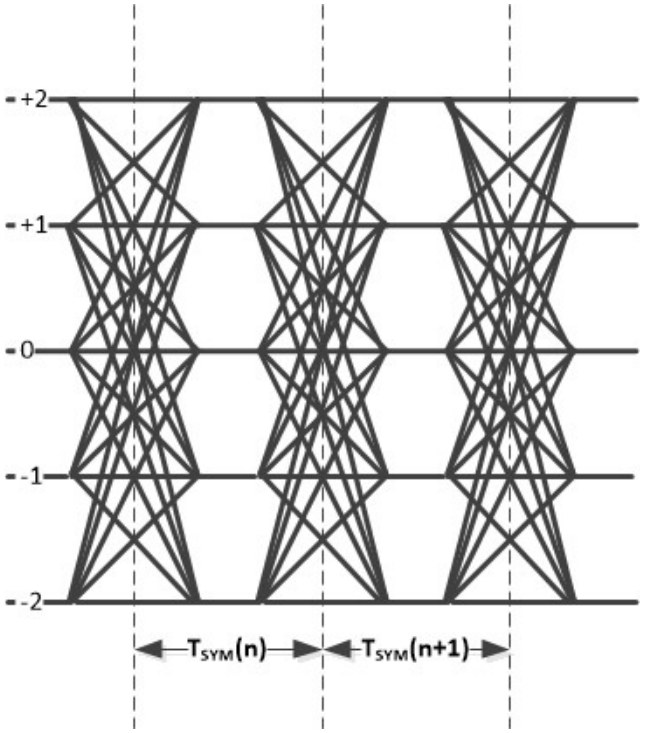

PAM5

For more information

- 100BASE-X PCS, PMA and PMD specifications can be found in Section 2 of the IEEE802.3 Standard: Clauses 24, 25 and 26.
- Section 3 of the IEEE802.3 Standard describes various versions of 1 Gbps Ethernet versions. Clause 40 describes 1000BASE-T.
  - Clauses 36 through 39 describe long and short wave fiber, as well as short haul copper.

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