AMD
XILINX

UltraScale Architecture Libraries Guide (UG974)

Primitive Groups

Primitive Groups

The following Primitive Groups correlate to the PRIMITIVE_GROUP cell property in the Vivado software. Similarly, the listed Primitive Subgroup correlates to the PRIMITIVE_SUBGROUP property on the cells in the software. These can be used in filters to specify a class of cells for constraint processing and other tasks within Vivado.

ADVANCED

Design Element	Description	Primitive Sub
CMAC	Primitive: 100G MAC Block	MAC
CMACE4	Primitive: 100G MAC Block	MAC
GTHE3_CHANNEL	Primitive: Gigabit Transceiver for UltraScale devices	GT
GTHE3_COMMON	Primitive: Gigabit Transceiver for UltraScale devices	GT
GTHE4_CHANNEL	Primitive: Gigabit Transceiver for UltraScale+ devices	GT
GTHE4_COMMON	Primitive: Gigabit Transceiver for UltraScale+ devices	GT
GTYE3_CHANNEL	Primitive: Gigabit Transceiver for UltraScale devices	GT
GTYE3_COMMON	Primitive: Gigabit Transceiver for UltraScale devices	GT

Design Element	Description	Primitive Sub
GTYE4_CHANNEL	Primitive: Gigabit Transceiver for UltraScale+ devices.	GT
GTYE4_COMMON	Primitive: Gigabit Transceiver for UltraScale+ devices	GT
IBUFDS_GTE3	Primitive: Gigabit Transceiver Buffer	GT
IBUFDS_GTE4	Primitive: Gigabit Transceiver Buffer	GT
ILKN	Primitive: Interlaken MAC	INTERLAKEN
ILKNE4	Primitive: Interlaken MAC	INTERLAKEN
OBUFDS_GTE3	Primitive: Gigabit Transceiver Buffer	GT
OBUFDS_GTE3_ADV	Primitive: Gigabit Transceiver Buffer	GT
OBUFDS_GTE4	Primitive: Gigabit Transceiver Buffer	GT
OBUFDS_GTE4_ADV	Primitive: Gigabit Transceiver Buffer	GT
PCIE40E4	Primitive: Integrated Block for PCI Express	PCIE
PCIE_3_1	Primitive: Integrated Block for PCI Express	PCIE
SYSMONE1	Primitive: Xilinx Analog-to-Digital Converter and System Monitor	SYSMON
SYSMONE4	Primitive: Xilinx Analog-to-Digital Converter and System Monitor	SYSMON

ARITHMETIC

Design Element	Description	Primitive Sub
DSP48E2	Primitive: 48-bit Multi-Functional Arithmetic Block	DSP

BLOCKRAM

Design Element	Description	Primitive Sub
FIFO18E2	Primitive: 18Kb FIFO (First-In-First-Out) Block RAM Memory	FIFO
FIFO36E2	Primitive: 36Kb FIFO (First-In-First-Out) Block RAM Memory	FIFO
RAMB18E2	Primitive: 18K-bit Configurable Synchronous Block RAM	BRAM
RAMB36E2	Primitive: 36K-bit Configurable Synchronous Block RAM	BRAM
URAM288	Primitive: 288K-bit High-Density Memory Building Block	URAM
URAM288_BASE	Primitive: 288K-bit High-Density Base Memory Building Block	URAM

CLB

Design Element	Description	Primitive Sub
LUT6_2	Primitive: Six-input, 2-output, Look-Up Table	LUT
RAM128X1D	Primitive: 128-Deep by 1-Wide Dual Port Random Access Memory (Select RAM)	LUTRAM
RAM128X1S	Primitive: 128-Deep by 1-Wide Random Access Memory (Select RAM)	LUTRAM
RAM256X1D	Primitive: 256-Deep by 1-Wide Dual Port Random Access Memory (Select RAM)	LUTRAM

Design Element	Description	Primitive Sub
RAM256X1S	Primitive: 256-Deep by 1-Wide Random Access Memory (Select RAM)	LUTRAM
RAM32M	Primitive: 32-Deep by 8-bit Wide Multi Port Random Access Memory (Select RAM)	LUTRAM
RAM32M16	Primitive: 32-Deep by 16-bit Wide Multi Port Random Access Memory (Select RAM)	LUTRAM
RAM32X1D	Primitive: 32-Deep by 1-Wide Static Dual Port Synchronous RAM	LUTRAM
RAM32X1S	Primitive: 32-Deep by 1-Wide Static Synchronous RAM	LUTRAM
RAM512X1S	Primitive: 512-Deep by 1-Wide Random Access Memory (Select RAM)	LUTRAM
RAM64M	Primitive: 64-Deep by 4-bit Wide Multi Port Random Access Memory (Select RAM)	LUTRAM
RAM64M8	Primitive: 64-Deep by 8-bit Wide Multi Port Random Access Memory (Select RAM)	LUTRAM
RAM64X1D	Primitive: 64-Deep by 1-Wide Dual Port Static Synchronous RAM	LUTRAM
RAM64X1S	Primitive: 64-Deep by 1-Wide Static Synchronous RAM	LUTRAM
AND2B1L	Primitive: Two input AND gate implemented in place of a CLB Latch	LATCH

Design Element	Description	Primitive Sub
CARRY8	Primitive: Fast Carry Logic with Look Ahead	CARRY
CFGLUT5	Primitive: 5-input Dynamically Reconfigurable Look-Up Table (LUT)	LUT
LUT1	Primitive: 1-Bit Look-Up Table	LUT
LUT2	Primitive: 2-Bit Look-Up Table	LUT
LUT3	Primitive: 3-Bit Look-Up Table	LUT
LUT4	Primitive: 4-Bit Look-Up Table	LUT
LUT5	Primitive: 5-Bit Look-Up Table	LUT
LUT6	Primitive: 6-Bit Look-Up Table	LUT
MUXF7	Primitive: CLB MUX to connect two LUT6's Together	MUXF
MUXF8	Primitive: CLB MUX to connect two MUXF7's Together	MUXF
MUXF9	Primitive: CLB MUX to connect two MUXF8s Together	MUXF
OR2L	Primitive: Two input OR gate implemented in place of a CLB Latch	LATCH
RAM32X16DR8	Primitive: Asymmetric LUTRAM	LUTRAM
RAM64X8SW	Primitive: 64-Deep by 8-bit Wide Random Access Memory with Single-Bit Write (Select RAM)	LUTRAM
SRL16E	Primitive: 16-Bit Shift Register Look-Up Table (LUT)	SRL
SRLC32E	Primitive: 32-Bit Shift Register Look-Up Table (LUT)	SRL

CLOCK

Design Element	Description	Primitive Sub
BUFG	Primitive: General Clock Buffer	BUFFER
BUFG_GT	Primitive: Clock Buffer Driven by Gigabit Transceiver	BUFFER
BUFG_GT_SYNC	Primitive: Synchronizer for BUFG_GT Control Signals	CLOCK_SYNC
BUFG_PS	Primitive: A high-fanout buffer for low-skew distribution of the PS Clock signals	BUFFER
BUFGCE	Primitive: General Clock Buffer with Clock Enable	BUFFER
BUFGCE_1	Primitive: General Clock Buffer with Clock Enable and Output State 1	BUFFER
BUFGCE_DIV	Primitive: General Clock Buffer with Divide Function	BUFFER
BUFGCTRL	Primitive: General Clock Control Buffer	MUX
BUFGMUX	Primitive: General Clock Mux Buffer	MUX
BUFGMUX_1	Primitive: General Clock Mux Buffer with Output State 1	MUX
BUFGMUX_CTRL	Primitive: 2-to-1 General Clock MUX Buffer	MUX
MMCME3_ADV	Primitive: Advanced Mixed Mode Clock Manager (MMCM)	PLL
MMCME3_BASE	Primitive: Base Mixed Mode Clock Manager (MMCM)	PLL

Design Element	Description	Primitive Sub
MMCME4_ADV	Primitive: Advanced Mixed Mode Clock Manager (MMCM)	PLL
MMCME4_BASE	Primitive: Base Mixed Mode Clock Manager (MMCM)	PLL
PLLE3_ADV	Primitive: Advanced Phase-Locked Loop (PLL)	PLL
PLLE3_BASE	Primitive: Base Phase-Locked Loop (PLL)	PLL
PLLE4_ADV	Primitive: Advanced Phase-Locked Loop (PLL)	PLL
PLLE4_BASE	Primitive: Base Phase-Locked Loop (PLL)	PLL

CONFIGURATION

Design Element	Description	Primitive Sub
BSCANE2	Primitive: Boundary-Scan User Instruction	BSCAN
DNA_PORTE2	Primitive: Device DNA Access Port	DNA
EFUSE_USR	Primitive: 32-bit non-volatile design ID	EFUSE
FRAME_ECCE3	Primitive: Configuration Frame Error Correction	ECC
FRAME_ECCE4	Primitive: Configuration Frame Error Correction	ECC
ICAPE3	Primitive: Internal Configuration Access Port	ICAP
MASTER_JTAG	Primitive: JTAG Port Access	MASTER_JTAG

Design Element	Description	Primitive Sub
STARTUPE3	Primitive: STARTUP Block	STARTUP
USR_ACCESSE2	Primitive: Configuration Data Access	USR_ACCESS

I/O

Design Element	Description	Primitive Sub
BITSLICE_CONTROL	Primitive: BITSLICE_CONTROL for control using Native Mode	BITSLICE
DCIRESET	Primitive: Digitally Controlled Impedance Reset Component	DCI_RESET
HPIO_VREF	Primitive: VREF Scan	INPUT_BUFFER
IBUF	Primitive: Input Buffer	INPUT_BUFFER
IBUF_ANALOG	Primitive: Analog Auxiliary SYSMON Input Buffer	INPUT_BUFFER
IBUF_IBUFDISABLE	Primitive: Input Buffer With Input Buffer Disable	INPUT_BUFFER
IBUF_INTERMDISABLE	Primitive: Input Buffer With Input Buffer Disable and On-die Input Termination Disable	INPUT_BUFFER
IBUFDS	Primitive: Differential Input Buffer	INPUT_BUFFER
IBUFDS_DIFF_OUT	Primitive: Differential Input Buffer With Complementary Outputs	INPUT_BUFFER
IBUFDS_DIFF_OUT_IBUFDISABLE	Primitive: Differential Input Buffer With Complementary Outputs and Input Buffer Disable	INPUT_BUFFER
IBUFDS_DIFF_OUT_INTERMDISABLE	Primitive: Differential Input Buffer with Complementary Outputs, Input	INPUT_BUFFER

Design Element	Description	Primitive Sub
	Path Disable and On-die Input Termination Disable	
IBUFDS_DPHY	Primitive: Differential Input Buffer with MIPI support	INPUT_BUFFER
IBUFDS_IBUFDISABLE	Primitive: Differential Input Buffer With Input Buffer Disable	INPUT_BUFFER
IBUFDS_INTERMDISABLE	Primitive: Differential Input Buffer With Input Buffer Disable and On-die Input Termination Disable	INPUT_BUFFER
IBUFDSE3	Primitive: Differential Input Buffer with Offset Calibration	INPUT_BUFFER
IBUFE3	Primitive: Input Buffer with Offset Calibration and VREF Tuning	INPUT_BUFFER
IDELAYCTRL	Primitive: IDELAYE3/ODELAYE3 Tap Delay Value Control	DELAY
IDELAYE3	Primitive: Input Fixed or Variable Delay Element	DELAY
IOBUF	Primitive: Input/Output Buffer	BIDIR_BUFFER
IOBUF_DCIEN	Primitive: Input/Output Buffer DCI Enable	BIDIR_BUFFER
IOBUF_INTERMDISABLE	Primitive: Bidirectional Buffer with Input Path Disable and On-die Input Termination Disable	BIDIR_BUFFER
IOBUFDS	Primitive: Differential Input/Output Buffer	BIDIR_BUFFER
IOBUFDS_DCIEN	Primitive: Differential Bidirectional Buffer With Input Buffer Disable and On-die Input Termination Disable	BIDIR_BUFFER

Design Element	Description	Primitive Sub
IOBUFDS_DIFF_OUT	Primitive: Differential Input/Output Buffer Primitive With Complementary Outputs for the Input Buffer	BIDIR_BUFFER
IOBUFDS_DIFF_OUT_DCIEN	Primitive: Differential Bidirectional Buffer with Complementary Outputs, Input Path Disable, and On-die Input Termination Disable	BIDIR_BUFFER
IOBUFDS_DIFF_OUT_INTERMDISABLE	Primitive: Differential Bidirectional Buffer with Complementary Outputs, Input Buffer Disable and On-die Input Termination Disable	BIDIR_BUFFER
IOBUFDS_INTERMDISABLE	Primitive: Differential Bidirectional Buffer With Input Buffer Disable and On-die Input	BIDIR_BUFFER
IOBUFDSE3	Primitive: Differential Bidirectional I/O Buffer with Offset Calibration	BIDIR_BUFFER
IOBUFE3	Primitive: Bidirectional I/O Buffer with Offset Calibration and VREF Tuning	BIDIR_BUFFER
ISERDESE3	Primitive: Input SERial/DESerializer	SERDES
KEEPER	Primitive: I/O Weak Keeper	WEAK_DRIVER
OBUF	Primitive: Output Buffer	OUTPUT_BUFFER
OBUFDS	Primitive: Differential Output Buffer	OUTPUT_BUFFER
OBUFDS_DPHY	Primitive: Differential Output Buffer with MIPI support	OUTPUT_BUFFER
OBUFT	Primitive: 3-State Output Buffer	OUTPUT_BUFFER
OBUFTDS	Primitive: Differential 3-state Output Buffer	OUTPUT_BUFFER

Design Element	Description	Primitive Sub
ODELAYE3	Primitive: Output Fixed or Variable Delay Element	DELAY
OSERDESE3	Primitive: Output SERial/DESerializer	SERDES
PULLDOWN	Primitive: I/O Pulldown	WEAK_DRIVER
PULLUP	Primitive: I/O Pullup	WEAK_DRIVER
RIU_OR	Primitive: Register Interface Unit Selection Block	BITSLICE
RX_BITSLICE	Primitive: RX_BITSLICE for input using Native Mode	BITSLICE
RXTX_BITSLICE	Primitive: RXTX_BITSLICE for bidirectional I/O using Native Mode	BITSLICE
TX_BITSLICE	Primitive: TX_BITSLICE for output using Native Mode	BITSLICE
TX_BITSLICE_TRI	Primitive: TX_BITSLICE_TRI for tristate using Native Mode	BITSLICE

REGISTER

Design Element	Description	Primitive Sub
FDCE	Primitive: D Flip-Flop with Clock Enable and Asynchronous Clear	SDR
FDPE	Primitive: D Flip-Flop with Clock Enable and Asynchronous Preset	SDR
FDRE	Primitive: D Flip-Flop with Clock Enable and Synchronous Reset	SDR
FDSE	Primitive: D Flip-Flop with Clock Enable and Synchronous Set	SDR

Design Element	Description	Primitive Sub
HARD_SYNC	Primitive: Metastability Hardened Registers	METASTABILITY
IDDRE1	Primitive: Dedicated Double Data Rate (DDR) Input Register	DDR
LDCE	Primitive: Transparent Latch with Clock Enable and Asynchronous Clear	LATCH
LDPE	Primitive: Transparent Latch with Clock Enable and Asynchronous Preset	LATCH
ODDRE1	Primitive: Dedicated Double Data Rate (DDR) Output Register	DDR