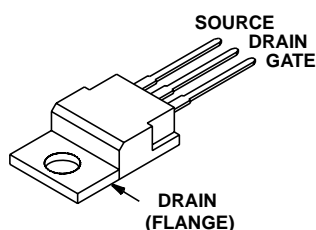


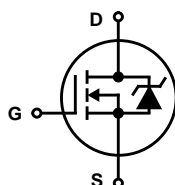
# 33A, 100V, 0.040 Ohm, N-Channel Power MOSFET

## Packaging

JEDEC TO-220AB



## Symbol



## Features

- Ultra Low On-Resistance
  - $r_{DS(ON)} = 0.040\Omega$ ,  $V_{GS} = 10V$
- Simulation Models
  - Temperature Compensated PSPICE<sup>TM</sup> and SABER<sup>®</sup> Electrical Models
  - Spice and SABER<sup>®</sup> Thermal Impedance Models
  - [www.intersil.com](http://www.intersil.com)
- Peak Current vs Pulse Width Curve
- UIS Rating Curve

## Ordering Information

PART NUMBER	PACKAGE	BRAND
IRF540N	TO-220AB	IRF540N

## Absolute Maximum Ratings $T_C = 25^\circ C$ , Unless Otherwise Specified

	IRF540N	UNITS
Drain to Source Voltage (Note 1) . . . . .	100	V
Drain to Gate Voltage ( $R_{GS} = 20k\Omega$ ) (Note 1) . . . . .	100	V
Gate to Source Voltage . . . . .	$\pm 20$	V
Drain Current		
Continuous ( $T_C = 25^\circ C$ , $V_{GS} = 10V$ ) (Figure 2) . . . . .	33	A
Continuous ( $T_C = 100^\circ C$ , $V_{GS} = 10V$ ) (Figure 2) . . . . .	23	A
Pulsed Drain Current . . . . .	Figure 4	
Pulsed Avalanche Rating . . . . .	Figures 6, 14, 15	
Power Dissipation . . . . .	120	W
Derate Above $25^\circ C$ . . . . .	0.80	W/ $^\circ C$
Operating and Storage Temperature . . . . .	-55 to 175	$^\circ C$
Maximum Temperature for Soldering		
Leads at 0.063in (1.6mm) from Case for 10s. . . . .	300	$^\circ C$
Package Body for 10s, See Techbrief TB334. . . . .	260	$^\circ C$

### NOTES:

1.  $T_J = 25^\circ C$  to  $150^\circ C$ .

**CAUTION:** Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

## IRF540N

### Electrical Specifications $T_C = 25^\circ\text{C}$ , Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS	
OFF STATE SPECIFICATIONS							
Drain to Source Breakdown Voltage	BV <sub>DSS</sub>	I <sub>D</sub> = 250μA, V <sub>GS</sub> = 0V (Figure 11)	100	-	-	V	
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 95V, V <sub>GS</sub> = 0V	-	-	1	μA	
		V <sub>DS</sub> = 90V, V <sub>GS</sub> = 0V, T <sub>C</sub> = 150°C	-	-	250	μA	
Gate to Source Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> = ±20V	-	-	±100	nA	
ON STATE SPECIFICATIONS							
Gate to Source Threshold Voltage	V <sub>GS(TH)</sub>	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = 250μA (Figure 10)	2	-	4	V	
Drain to Source On Resistance	r <sub>DS(ON)</sub>	I <sub>D</sub> = 33A, V <sub>GS</sub> = 10V (Figure 9)	-	0.033	0.040	Ω	
THERMAL SPECIFICATIONS							
Thermal Resistance Junction to Case	R <sub>θJC</sub>	TO-220	-	-	1.25	°C/W	
Thermal Resistance Junction to Ambient	R <sub>θJA</sub>		-	-	62	°C/W	
SWITCHING SPECIFICATIONS (V <sub>GS</sub> = 10V)							
Turn-On Time	t <sub>ON</sub>	V <sub>DD</sub> = 50V, I <sub>D</sub> = 33A V <sub>GS</sub> = 10V, R <sub>GS</sub> = 9.1Ω (Figures 18, 19)	-	-	100	ns	
Turn-On Delay Time	t <sub>d(ON)</sub>		-	9.5	-	ns	
Rise Time	t <sub>r</sub>		-	57	-	ns	
Turn-Off Delay Time	t <sub>d(OFF)</sub>		-	40	-	ns	
Fall Time	t <sub>f</sub>		-	55	-	ns	
Turn-Off Time	t <sub>OFF</sub>		-	-	145	ns	
GATE CHARGE SPECIFICATIONS							
Total Gate Charge	Q <sub>g(TOT)</sub>	V <sub>GS</sub> = 0V to 20V	V <sub>DD</sub> = 50V, I <sub>D</sub> = 33A, I <sub>g(REF)</sub> = 1.0mA (Figures 13, 16, 17)	-	66	79	nC
Gate Charge at 10V	Q <sub>g(10)</sub>	V <sub>GS</sub> = 0V to 10V		-	35	42	nC
Threshold Gate Charge	Q <sub>g(TH)</sub>	V <sub>GS</sub> = 0V to 2V		-	2.4	2.9	nC
Gate to Source Gate Charge	Q <sub>gs</sub>			-	5.4	-	nC
Gate to Drain "Miller" Charge	Q <sub>gd</sub>			-	13	-	nC
CAPACITANCE SPECIFICATIONS							
Input Capacitance	C <sub>ISS</sub>	V <sub>DS</sub> = 25V, V <sub>GS</sub> = 0V, f = 1MHz (Figure 12)	-	1220	-	pF	
Output Capacitance	C <sub>OSS</sub>		-	295	-	pF	
Reverse Transfer Capacitance	C <sub>RSS</sub>		-	100	-	pF	

### Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage	$V_{SD}$	$I_{SD} = 33\text{A}$	-	-	1.25	V
		$I_{SD} = 17\text{A}$	-	-	1.00	V
Reverse Recovery Time	$t_{rr}$	$I_{SD} = 33\text{A}$ , $dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	-	112	ns
Reverse Recovered Charge	$Q_{RR}$	$I_{SD} = 33\text{A}$ , $dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	-	400	nC

## Typical Performance Curves

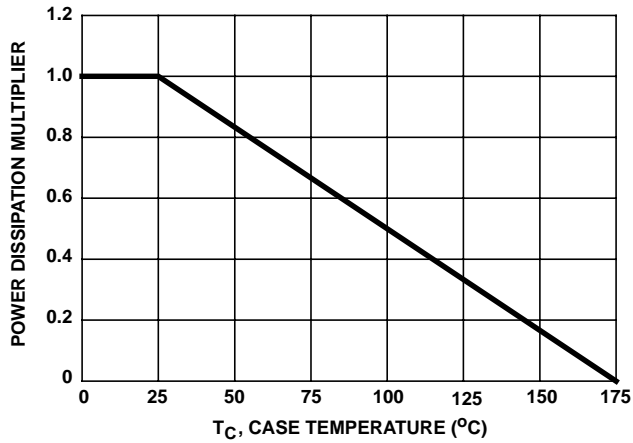


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

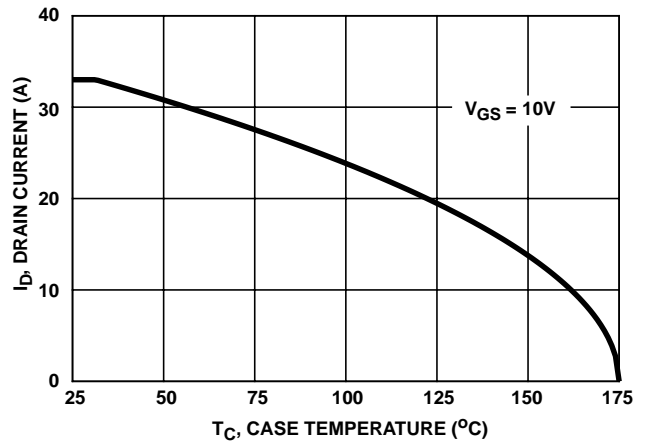


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

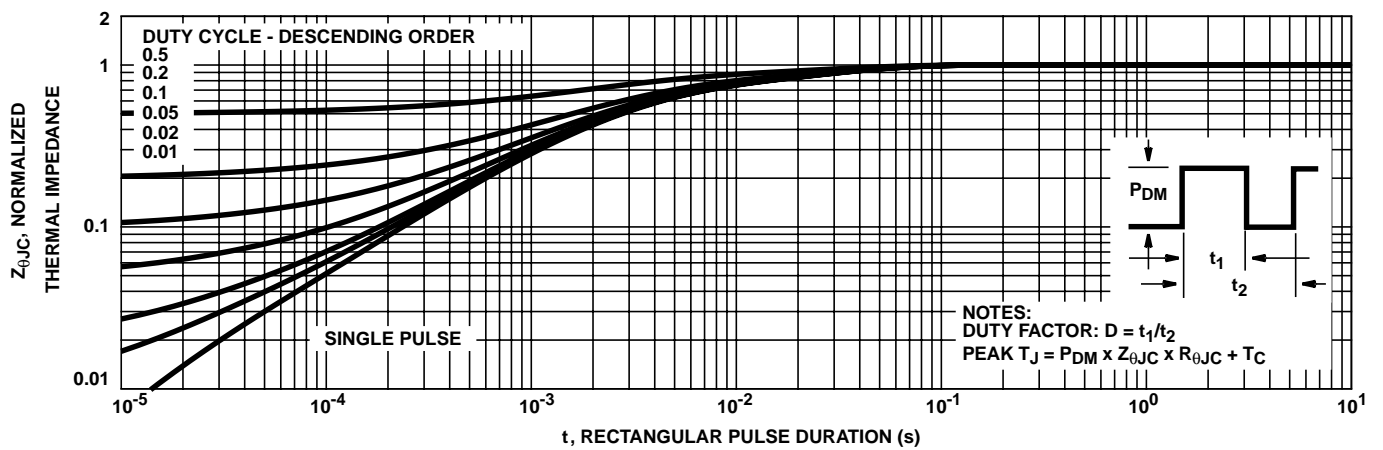


FIGURE 3. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

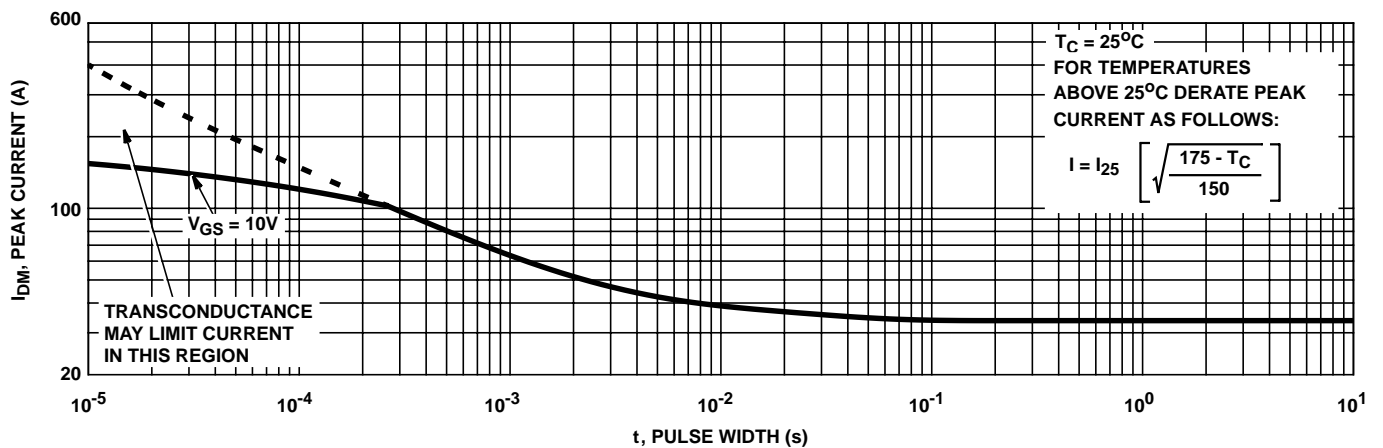


FIGURE 4. PEAK CURRENT CAPABILITY

# Typical Performance Curves (Continued)

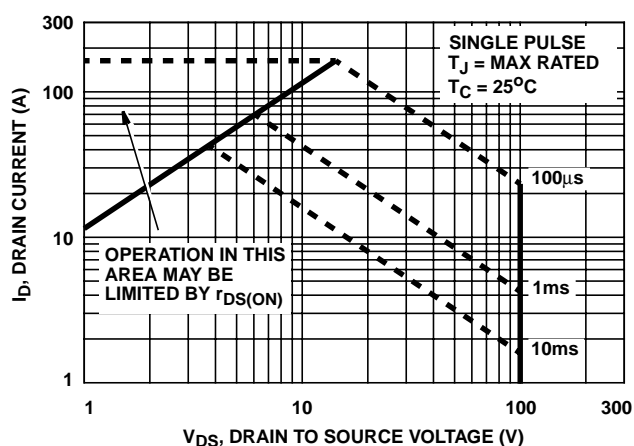
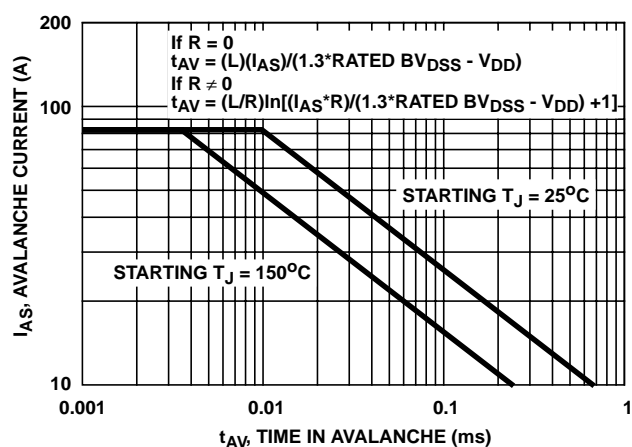


FIGURE 5. FORWARD BIAS SAFE OPERATING AREA



NOTE: Refer to Intersil Application Notes AN9321 and AN9322.

FIGURE 6. UNCLAMPED INDUCTIVE SWITCHING CAPABILITY

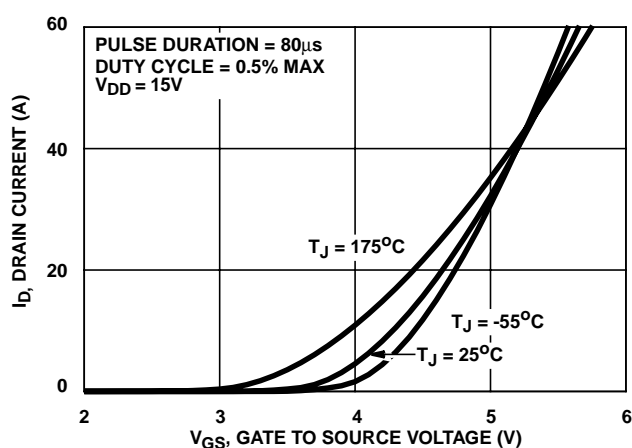


FIGURE 7. TRANSFER CHARACTERISTICS

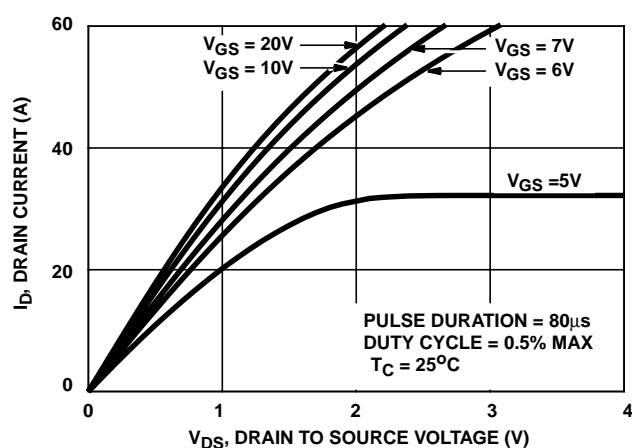


FIGURE 8. SATURATION CHARACTERISTICS

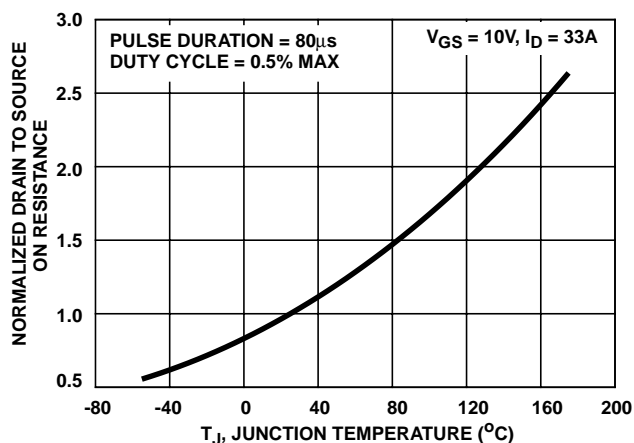


FIGURE 9. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

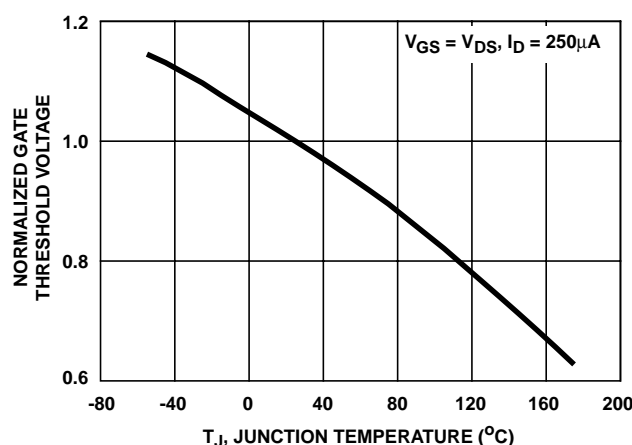


FIGURE 10. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

Typical Performance Curves (Continued)

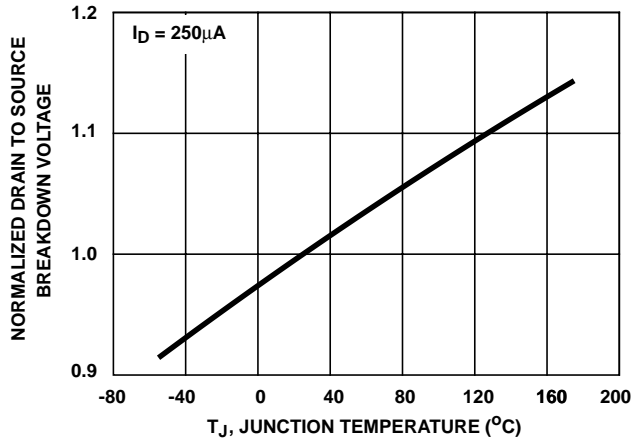


FIGURE 11. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

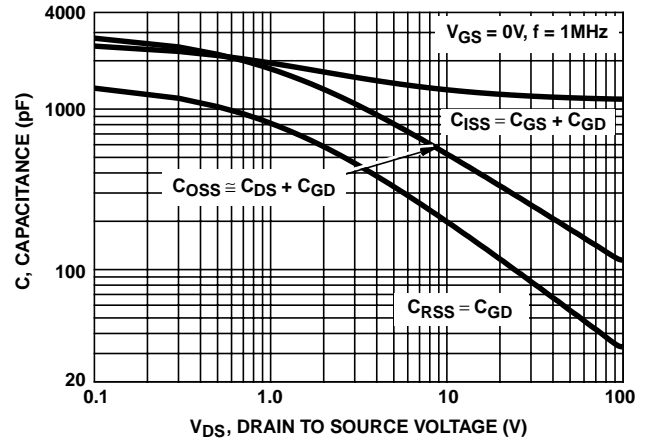
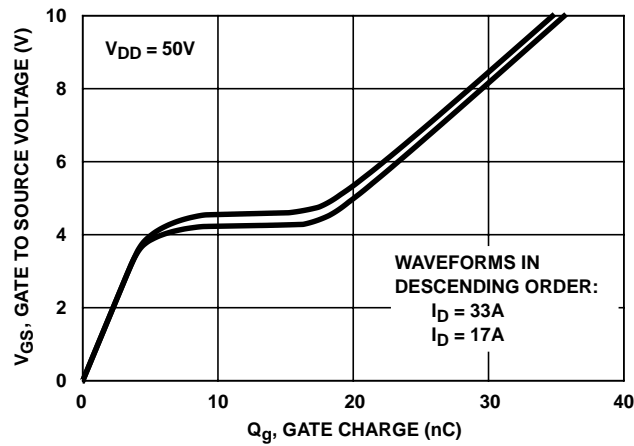


FIGURE 12. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE



NOTE: Refer to Intersil Application Notes AN7254 and AN7260.

FIGURE 13. GATE CHARGE WAVEFORMS FOR CONSTANT GATE CURRENT

## Test Circuits and Waveforms

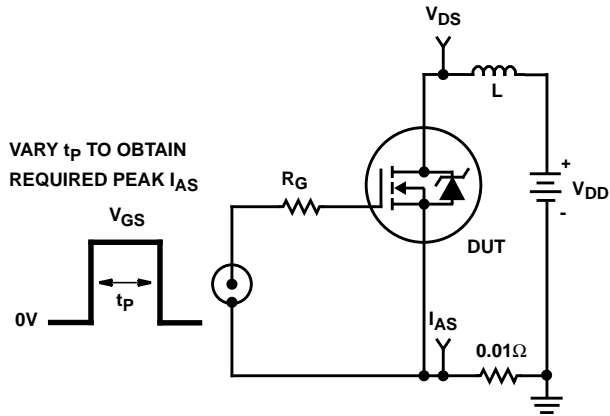


FIGURE 14. UNCLAMPED ENERGY TEST CIRCUIT

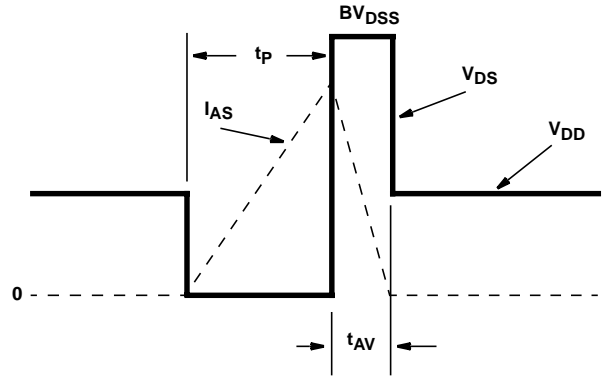


FIGURE 15. UNCLAMPED ENERGY WAVEFORMS

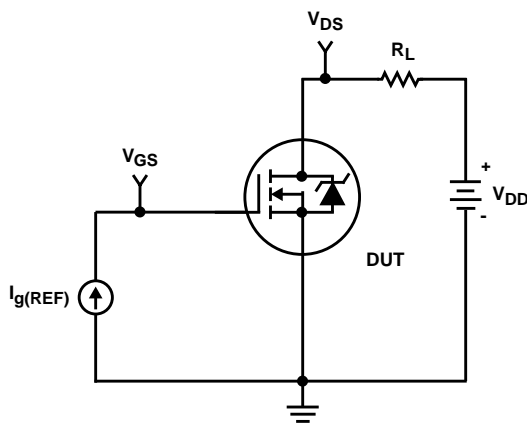


FIGURE 16. GATE CHARGE TEST CIRCUIT

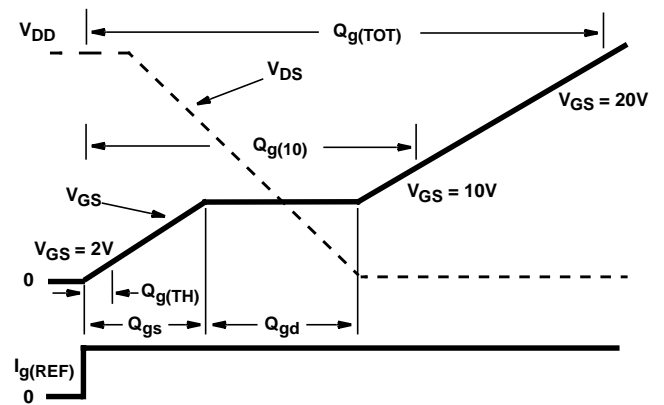


FIGURE 17. GATE CHARGE WAVEFORMS

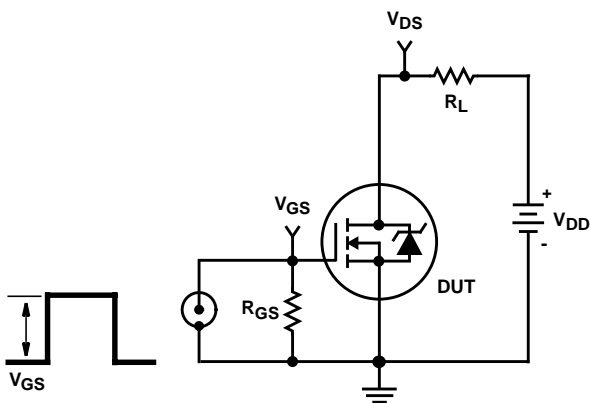


FIGURE 18. SWITCHING TIME TEST CIRCUIT

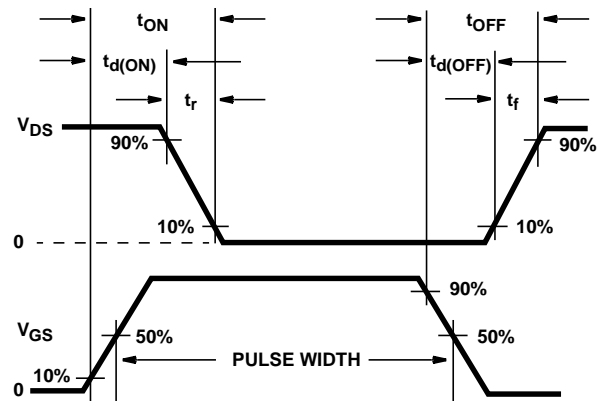


FIGURE 19. SWITCHING TIME WAVEFORM

## IRF540N

### PSPICE Electrical Model

.SUBCKT IRF540N 2 1 3 ; rev 19 July 1999

CA 12 8 1.95e-9  
CB 15 14 1.90e-9  
CIN 6 8 1.12e-9

DBODY 7 5 DBODYMOD  
DBREAK 5 11 DBREAKMOD  
DPLCAP 10 5 DPLCAPMOD

EBREAK 11 7 17 18 112.8  
EDS 14 8 5 8 1  
EGS 13 8 6 8 1  
ESG 6 10 6 8 1  
EVTHRES 6 21 19 8 1  
EVTEMP 20 6 18 22 1

IT 8 17 1

LDRAIN 2 5 1.0e-9  
LGATE 1 9 6.19e-9  
LSOURCE 3 7 2.18e-9

MMED 16 6 8 8 MMEDMOD  
MSTRO 16 6 8 8 MSTROMOD  
MWEAK 16 21 8 8 MWEAKMOD

RBREAK 17 18 RBREAKMOD 1  
RDRAIN 50 16 RDRAINMOD 2.00e-2  
RGATE 9 20 1.77  
RLDRAIN 2 5 10  
RLGATE 1 9 26  
RLSOURCE 3 7 11  
RSLC1 5 51 RSLCMOD 1e-6  
RSLC2 5 50 1e3  
RSOURCE 8 7 RSOURCEMOD 6.5e-3  
RVTHRES 22 8 RVTHRESMOD 1  
RVTEMP 18 19 RVTEMPMOD 1

S1A 6 12 13 8 S1AMOD  
S1B 13 12 13 8 S1BMOD  
S2A 6 15 14 13 S2AMOD  
S2B 13 15 14 13 S2BMOD

VBAT 22 19 DC 1

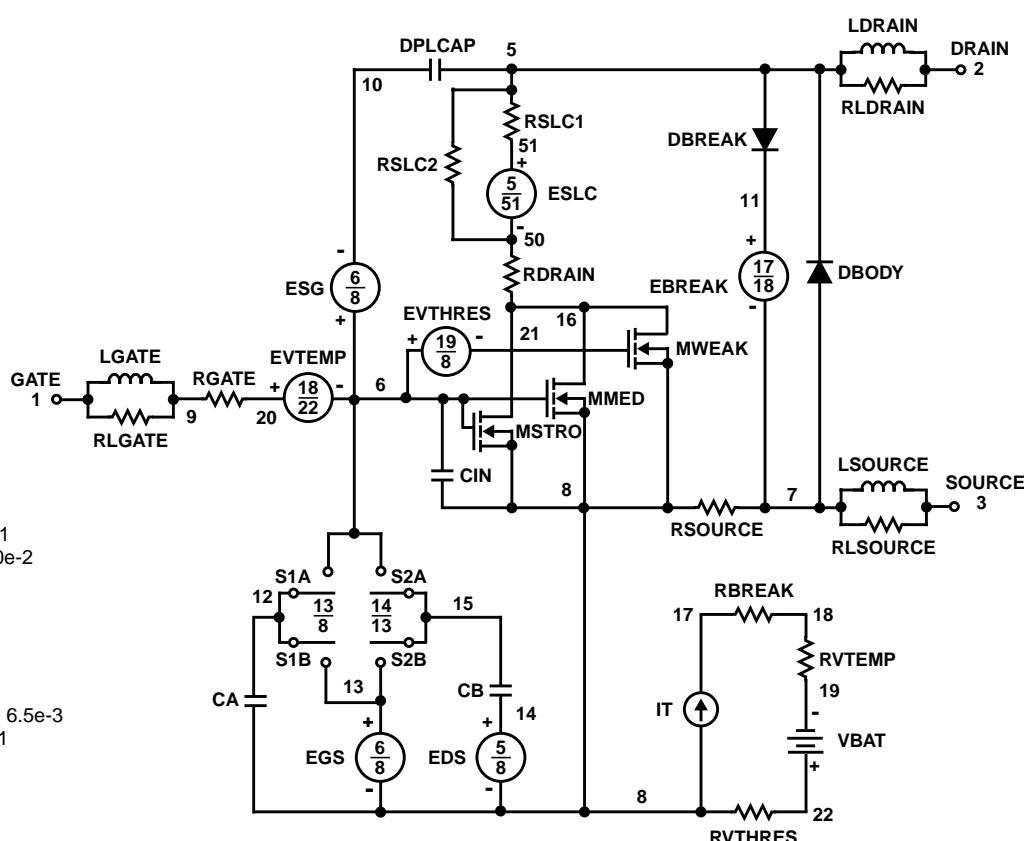
ESLC 51 50 VALUE={{(V(5,51)/ABS(V(5,51)))\*(PWR(V(5,51)/(1e-6\*71),3.5))}}

.MODEL DBODYMOD D (IS = 1.20e-12 RS = 4.2e-3 XTI = 5 TRS1 = 1.3e-3 TRS2 = 8.0e-6 CJO = 1.50e-9 TT = 7.47e-8 M = 0.63)  
.MODEL DBREAKMOD D (RS = 4.2e-1 TRS1 = 8e-4 TRS2 = 3e-6)  
.MODEL DPLCAPMOD D (CJO = 1.45e-9 IS = 1e-30 M = 0.82)  
.MODEL MMEDMOD NMOS (VTO = 3.11 KP = 5 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u RG = 1.77)  
.MODEL MSTROMOD NMOS (VTO = 3.57 KP = 33.5 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u)  
.MODEL MWEAKMOD NMOS (VTO = 2.68 KP = 0.09 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u RG = 17.7 )  
.MODEL RBREAKMOD RES (TC1 = 1.05e-3 TC2 = -5e-7)  
.MODEL RDRAINMOD RES (TC1 = 9.40e-3 TC2 = 2.93e-5)  
.MODEL RSLCMOD RES (TC1 = 3.5e-3 TC2 = 2.0e-6)  
.MODEL RSOURCEMOD RES (TC1 = 1e-3 TC2 = 1e-6)  
.MODEL RVTHRESMOD RES (TC1 = -1.8e-3 TC2 = -8.6e-6)  
.MODEL RVTEMPMOD RES (TC1 = -3.0e-3 TC2 = 1.5e-7)

.MODEL S1AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -6.2 VOFF = -3.1)  
.MODEL S1BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -3.1 VOFF = -6.2)  
.MODEL S2AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -1.0 VOFF = 0.5)  
.MODEL S2BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = 0.5 VOFF = -1.0)

.ENDS

NOTE: For further discussion of the PSPICE model, consult **A New PSPICE Sub-Circuit for the Power MOSFET Featuring Global Temperature Options**; IEEE Power Electronics Specialist Conference Records, 1991, written by William J. Hepp and C. Frank Wheatley.



# SABER Electrical Model

REV 19 July 1999

template IRF540N n2,n1,n3

electrical n2,n1,n3

```
{
var i iscl
d..model dbodymod = (is = 1.20e-12, cjo = 1.50e-9, tt = 7.47e-8, xti = 5, m = 0.63)
d..model dbreakmod = ()
d..model dplcapmod = (cjo = 1.45e-9, is = 1e-30, m = 0.82)
m..model mmedmod = (type=_n, vto = 3.11, kp = 5, is = 1e-30, tox = 1)
m..model mstrongmod = (type=_n, vto = 3.57, kp = 33.5, is = 1e-30, tox = 1)
m..model mweakmod = (type=_n, vto = 2.68, kp = 0.09, is = 1e-30, tox = 1)
sw_vcsp..model s1amod = (ron = 1e-5, roff = 0.1, von = -6.2, voff = -3.1)
sw_vcsp..model s1bmod = (ron = 1e-5, roff = 0.1, von = -3.1, voff = -6.2)
sw_vcsp..model s2amod = (ron = 1e-5, roff = 0.1, von = -1.0, voff = 0.5)
sw_vcsp..model s2bmod = (ron = 1e-5, roff = 0.1, von = 0.5, voff = -1.0)
```

```
c.ca n12 n8 = 1.95e-9
c.cb n15 n14 = 1.90e-9
c.cin n6 n8 = 1.12e-9
```

```
d.dbody n7 n71 = model=dbodymod
d.dbreak n72 n11 = model=dbreakmod
d.dplcap n10 n5 = model=dplcapmod
```

```
i.it n8 n17 = 1
```

```
l.l drain n2 n5 = 1e-9
l.l gate n1 n9 = 6.19e-9
l.l source n3 n7 = 2.18e-9
```

```
m.mmed n16 n6 n8 n8 = model=mmedmod, l=1u, w=1u
m.mstrong n16 n6 n8 n8 = model=msstrongmod, l=1u, w=1u
m.mweak n16 n21 n8 n8 = model=mweakmod, l=1u, w=1u
```

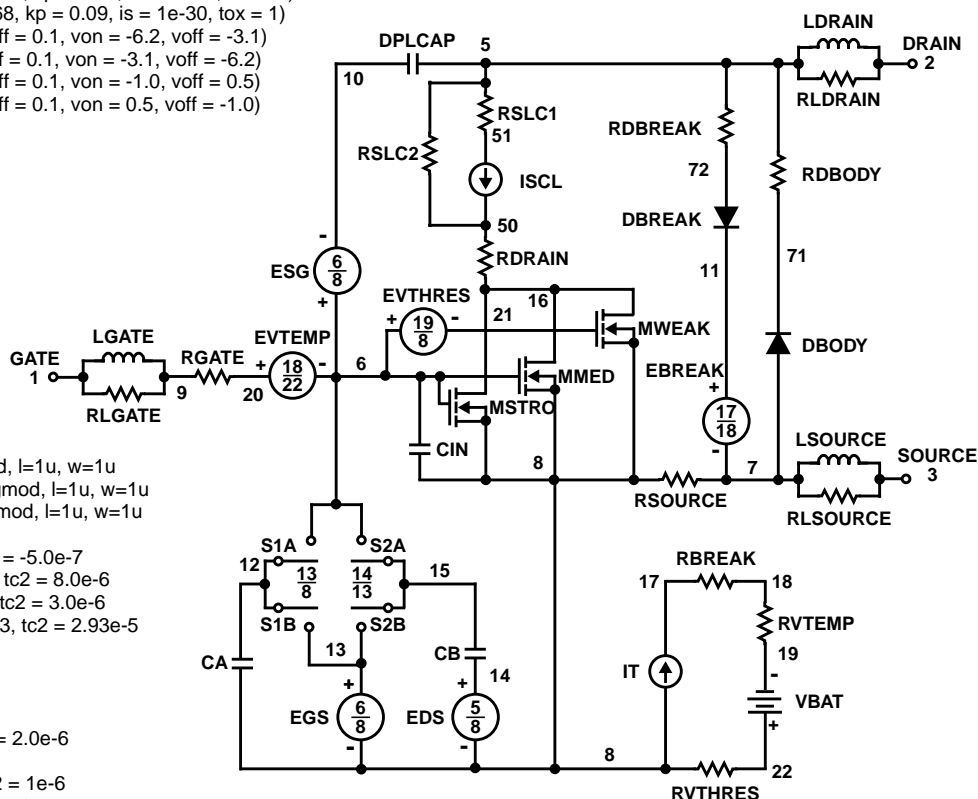
```
res.rbreak n17 n18 = 1, tc1 = 1.05e-3, tc2 = -5.0e-7
res.rbody n71 n5 = 4.2e-3, tc1 = 1.30e-3, tc2 = 8.0e-6
res.rdrain n72 n5 = 4.2e-1, tc1 = 8.0e-4, tc2 = 3.0e-6
res.rgate n9 n20 = 1.77
res.rldrain n2 n5 = 10
res.rlgate n1 n9 = 26
res.rls source n3 n7 = 11
res.rslc1 n5 n51 = 1e-6, tc1 = 3.5e-3, tc2 = 2.0e-6
res.rslc2 n5 n50 = 1e3
res.rsource n8 n7 = 6.5e-3, tc1 = 1e-3, tc2 = 1e-6
res.rvtemp n18 n19 = 1, tc1 = -3.0e-3, tc2 = 1.5e-7
res.rvthres n22 n8 = 1, tc1 = -1.8e-3, tc2 = -8.6e-6
```

```
spe.ebreak n11 n7 n17 n18 = 112.8
spe.eds n14 n8 n5 n8 = 1
spe.egs n13 n8 n6 n8 = 1
spe.esg n6 n10 n6 n8 = 1
spe.evtemp n20 n6 n18 n22 = 1
spe.evthres n6 n21 n19 n8 = 1
```

```
sw_vcsp.s1a n6 n12 n13 n8 = model=s1amod
sw_vcsp.s1b n13 n12 n13 n8 = model=s1bmod
sw_vcsp.s2a n6 n15 n14 n13 = model=s2amod
sw_vcsp.s2b n13 n15 n14 n13 = model=s2bmod
```

```
v.vbat n22 n19 = dc=1
```

```
equations {
i (n51->n50) +=iscl
iscl: v(n51,n50) = ((v(n5,n51)/(1e-9+abs(v(n5,n51))))*((abs(v(n5,n51))*1e6/71))** 3.5))
}
}
```





## SPICE Thermal Model

REV 26 July 1999

IRF540NT

CTHERM1 th 6 2.60e-3  
 CHERM2 6 5 8.85e-3  
 CHERM3 5 4 7.60e-3  
 CHERM4 4 3 7.65e-3  
 CHERM5 3 2 1.22e-2  
 CHERM6 2 tl 8.70e-2

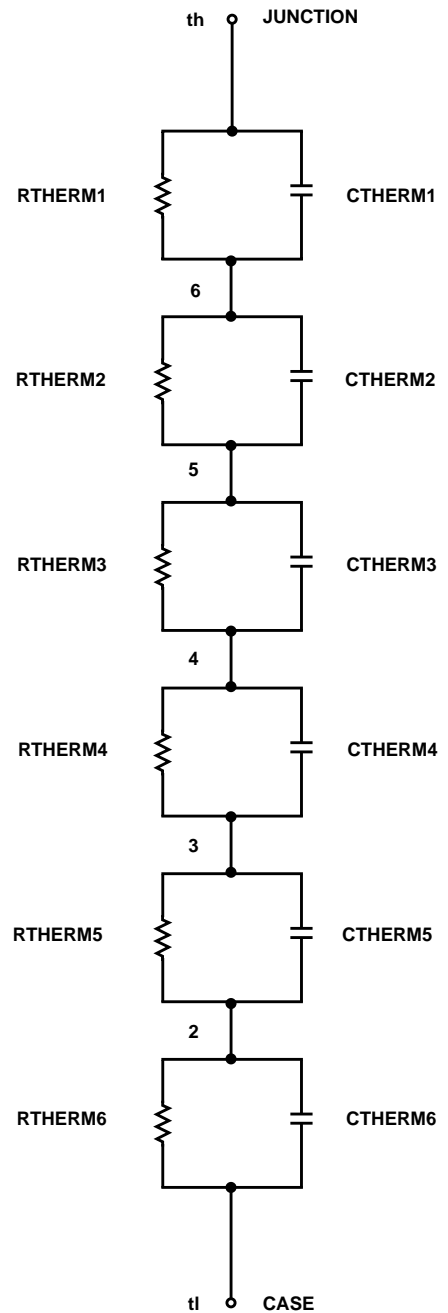
RHERM1 th 6 9.00e-3  
 RHERM2 6 5 1.80e-2  
 RHERM3 5 4 9.15e-2  
 RHERM4 4 3 2.43e-1  
 RHERM5 3 2 3.10e-1  
 RHERM6 2 tl 3.21e-1

## SABER Thermal Model

SABER thermal model IRF540NT

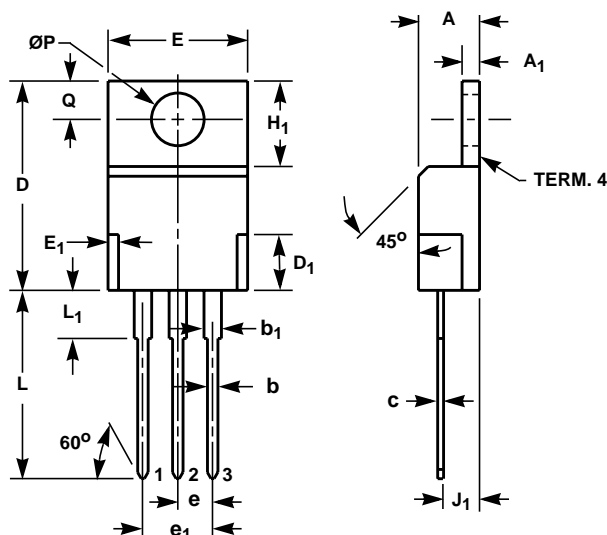
```
template thermal_model th tl
thermal_c th, tl
{
    ctherm.ctherm1 th 6 = 2.60e-3
    ctherm.ctherm2 6 5 = 8.85e-3
    ctherm.ctherm3 5 4 = 7.60e-3
    ctherm.ctherm4 4 3 = 7.65e-3
    ctherm.ctherm5 3 2 = 1.22e-2
    ctherm.ctherm6 2 tl = 8.70e-2

    rtherm.rtherm1 th 6 = 9.00e-3
    rtherm.rtherm2 6 5 = 1.80e-2
    rtherm.rtherm3 5 4 = 9.15e-2
    rtherm.rtherm4 4 3 = 2.43e-1
    rtherm.rtherm5 3 2 = 3.10e-1
    rtherm.rtherm6 2 tl = 3.21e-1
}
```



# TO-220AB

## 3 LEAD JEDEC TO-220AB PLASTIC PACKAGE



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.170	0.180	4.32	4.57	-
A <sub>1</sub>	0.048	0.052	1.22	1.32	-
b	0.030	0.034	0.77	0.86	3, 4
b <sub>1</sub>	0.045	0.055	1.15	1.39	2, 3
c	0.014	0.019	0.36	0.48	2, 3, 4
D	0.590	0.610	14.99	15.49	-
D <sub>1</sub>	-	0.160	-	4.06	-
E	0.395	0.410	10.04	10.41	-
E <sub>1</sub>	-	0.030	-	0.76	-
e	0.100 TYP		2.54 TYP		5
e <sub>1</sub>	0.200 BSC		5.08 BSC		5
H <sub>1</sub>	0.235	0.255	5.97	6.47	-
J <sub>1</sub>	0.100	0.110	2.54	2.79	6
L	0.530	0.550	13.47	13.97	-
L <sub>1</sub>	0.130	0.150	3.31	3.81	2
ØP	0.149	0.153	3.79	3.88	-
Q	0.102	0.112	2.60	2.84	-

### NOTES:

1. These dimensions are within allowable dimensions of Rev. J of JEDEC TO-220AB outline dated 3-24-87.
2. Lead dimension and finish uncontrolled in L<sub>1</sub>.
3. Lead dimension (without solder).
4. Add typically 0.002 inches (0.05mm) for solder coating.
5. Position of lead to be measured 0.250 inches (6.35mm) from bottom of dimension D.
6. Position of lead to be measured 0.100 inches (2.54mm) from bottom of dimension D.
7. Controlling dimension: Inch.
8. Revision 2 dated 7-97.

All Intersil semiconductor products are manufactured, assembled and tested under **ISO9000** quality systems certification.

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