7.7 D flip-flops and registers

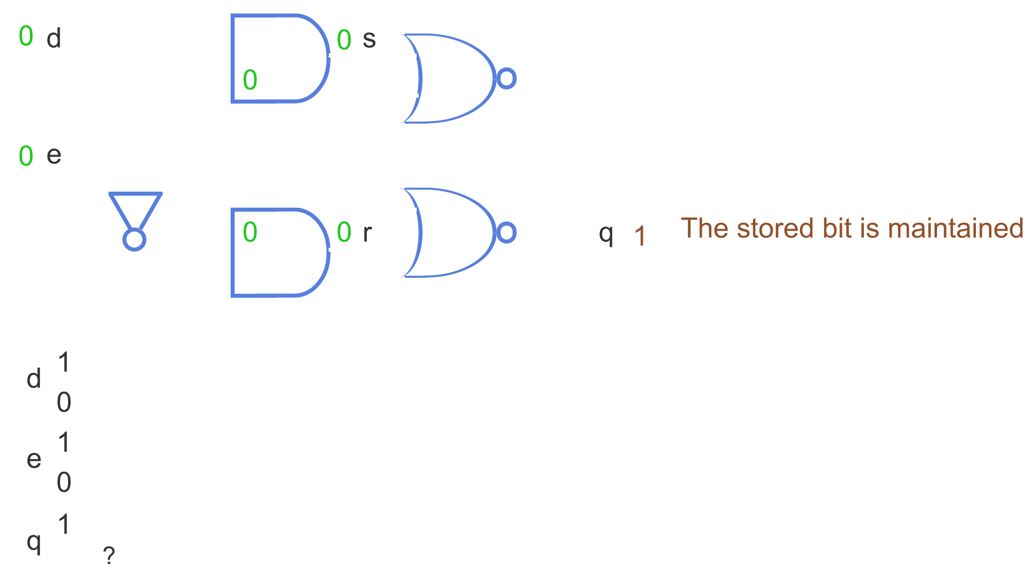
D latch

A ***D latch*** stores one bit, with an input d having the bit to be stored, an input e that when 1 enables storing the bit, and with t appearing on output q. D and d are short for "data", and e for "enable".

An SR latch has an oscillation problem if both inputs were 1's then both change back to 0's. A D latch can be implemented SR latch with s = d and r = d'. Because sr = 11 is impossible, the SR latch oscillation problem is avoided. When e = 1, the AN to s, and d' to r. So d = 1 sets the SR latch, and d = 0 resets. When e = 0, the AND gates pass 0's to s and r, so the SR latch n stored bit.

PARTICIPATION ACTIVITY 7.7.1: D latch.

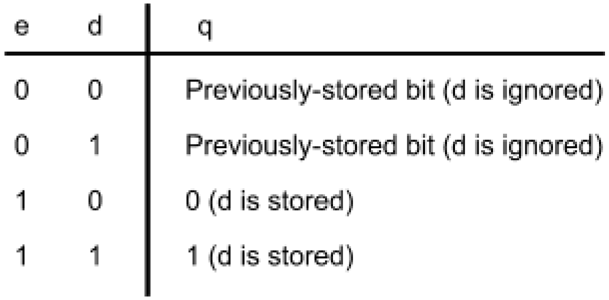
Start □ 2x speed



The stored bit is maintained

0

Figure 7.7.1: D latch behavior.



e	d	q
0	0	Previously-stored bit (d is ignored)
0	1	Previously-stored bit (d is ignored)
1	0	0 (d is stored)
1	1	1 (d is stored)

PARTICIPATION ACTIVITY 7.7.2: D latch.

Indicate q's present value for the given input sequence. "d: 0..1" means d was 0 and is presently 1.

1) d: 0
e: 1

○ 1

○ 0

2) d: 0..0
e: 1..0

○ 1

○ 0

3) d: 0..0..1
e: 1..0..0

○ 1

○ 0

4) d: 0..0..1..1
e: 1..0..0..1

○ 1

○ 0

5) d: 0..0..1..1..0
e: 1..0..0..1..0

○ 1

○ 0

Clock

For reasons that will be clear in later sections relating to synchronizing bit storage in a circuit, most digital circuits use a reg
signal, called a ***clock*** signal, to control when to store bits. Ex: A clock signal may oscillate at a frequency of 1 GHz (1 billion
second). Rather than bits being stored while an enable signal is high, bits are stored only at the instant a clock signal chang
known as a ***rising edge***.

PARTICIPATION ACTIVITY 7.7.3: Clocking synchronizes components.

Start □ 2x speed

0 0 1 1

PARTICIPATION ACTIVITY 7.7.4: Clocks.

Consider the example above.

1) A change of the clock signal from 0 to 1 is called a rising _____ .

○ edge

○ cliff

2) The three boxes represent three stored bits. On each rising clock edge, those bits move one place to the _____ .

○ left

○ right

3) On each rising clock edge, the bits move _____ .

○ one at a time

○ simultaneously

D flip-flop

A ***latch*** stores a new bit while an enable input is 1. A latch is said to be ***level sensitive***, storing when the enable's "level" is hi ***flip-flop*** stores a new bit only at the instant of an enable signal's rising edge. A flip-flop is said to be ***edge-triggered***.

PARTICIPATION ACTIVITY 7.7.5: D flip-flop.

Given a single D flip-flop with data input d, clock input clk, and output q.

1) d is 0, clk is 0, q is 0.
d changes to 1. Moments later, what is q?

○ 1

○ 0

2) d is 0, clk is 0, q is 0.
clk changes to 1. Moments later, what is q?

○ 1

○ 0

3) d is 0, clk is 0, q is 0.
d changes to 1, then clk changes to 1.
Moments later, what is q?

○ 1

○ 0

4) d is 1, clk is 0, q is 1.
d changes to 0. Moments later, what is q?

○ 1

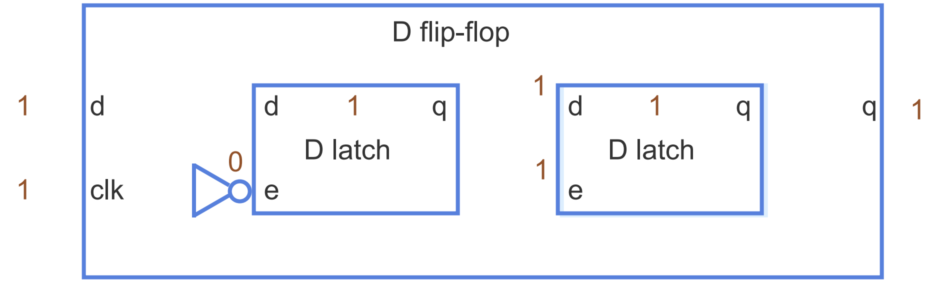
○ 0

A D flip-flop can be implemented by cascading two D latches, with the first latch's enable inverted. A flip-flop implemented b
with the first latch's enable inverted, has a ***master-servant*** arrangement. (Actually, master-slave is the common term, which

avoids for obvious reasons). The first latch is the master, the second the servant. Other implementations exist.

PARTICIPATION ACTIVITY 7.7.6: D flip-flop: Master-servant implementation.

Start □ 2x speed



PARTICIPATION ACTIVITY 7.7.7: D flip-flop implemented as master-servant.

Given a single D flip-flop implemented with a master-servant arrangement.

1) d is 0, clk is 0, q is 1.
What is in the first latch?

○ 1

○ 0

2) d is 0, clk is 0, q is 1.
What is in the second latch?

○ 1

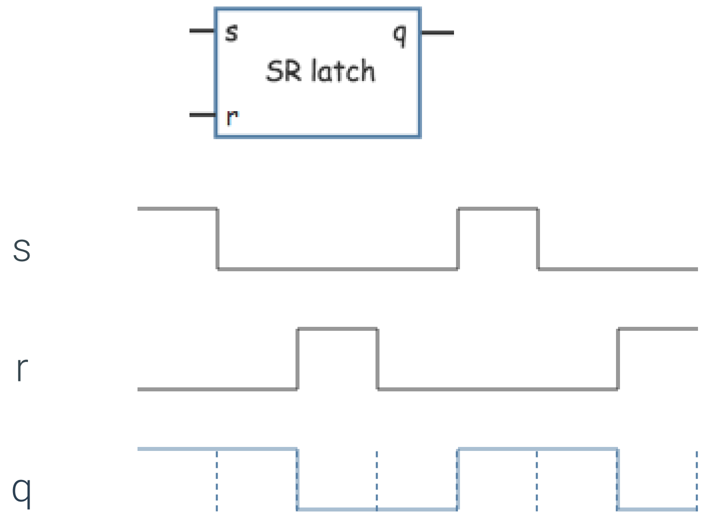
○

0

CHALLENGE ACTIVITY 7.7.1: Indicate q's value over time.

1
2
3
4

Start



1 2 3 4

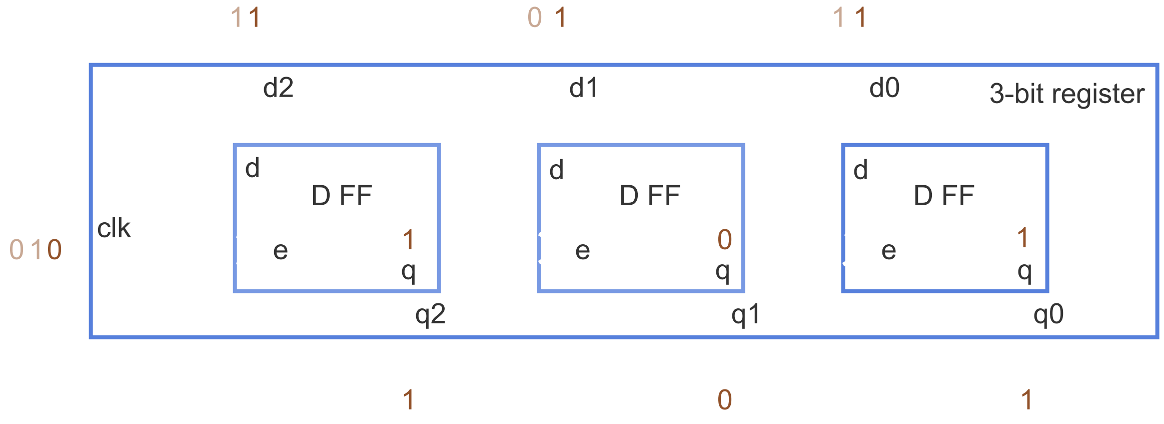
Check Next

Basic register

Bits are usually stored in groups. A ***register*** is a circuit that stores a group of bits; a 3-bit register stores three bits. On a risir bits are stored simultaneously. Storing bits in a register is known as ***loading*** the register. A common register implementatic

PARTICIPATION ACTIVITY 7.7.8: 3-bit register using 3 flip-flops: Inputs only stored on rising clk.

Start □ 2x speed



PARTICIPATION ACTIVITY 7.7.9: Basic register.

Given a 3-bit register with data inputs d2, d1, d0, clock input clk, and outputs q2, q1, q0.

1) d2d1d0 is 101, and q2q1q0 is 000.
clk rises. What does q2q1q0 become?

Check Show answer

2) d2d1d0 is 111, q2q1q0 is 000, clk rises

so q2q1q0 becomes 111.
Then d2d1d0 changes to 010. What does q2q1q0 become?

Check Show answer

Provide feedback on this section