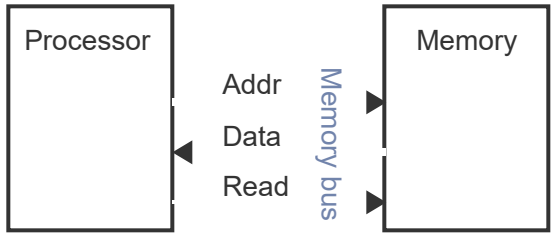
7.14 Buses

A ***bus*** is a collection of wires that carry out data transfer. The term can refer to a specific group of wires like an 8-bit addres data bus, as well as to a larger item like a memory bus having an address bus, data bus, and read control signal.

A ***bus protocol*** is the rules by which data is transferred over a bus.

PARTICIPATION ACTIVITY 7.14.1: Buses and protocols.

Start ☐ 2x speed



Protocol

Processor puts address on Addr bus

After 20ns, processor raises Read signal

Memory puts data on Data bus within 40 ns

Memory keeps data on Data bus until Processor lowers Read

PARTICIPATION ACTIVITY 7.14.2: Buses.

Consider the above animation.

1) The Addr bus is 1 wire.

○ True

- False

2) Read is a bus.
   - True
   - False

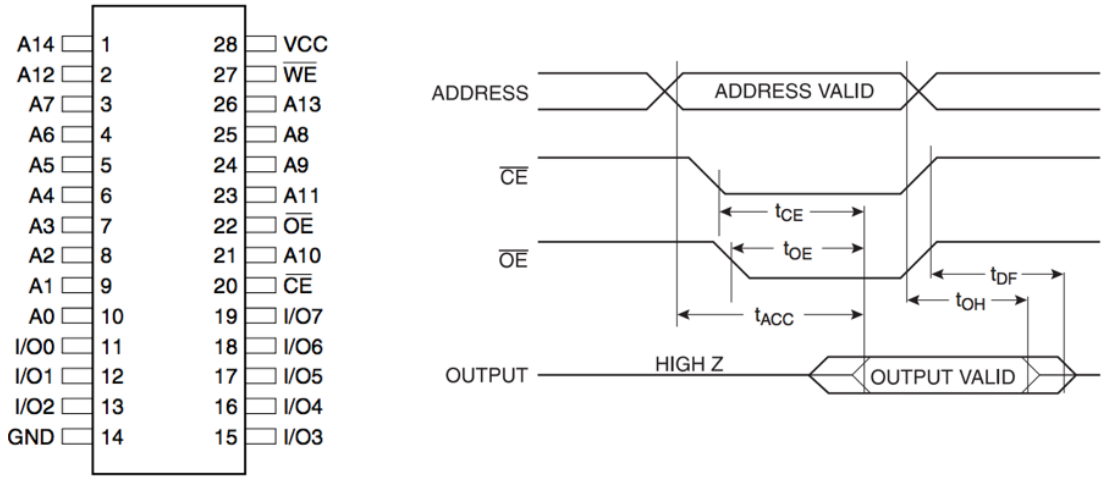
3) The Addr bus, Data bus, and Read signal are together considered the Memory bus.
   - True
   - False

4) The Memory bus protocol begins by putting data on the data bus.
   - True
   - False

A bus protocol example

Example 7.14.1: Bus protocol for a small memory chip.

The following timing diagram is from the datasheet for a small memory chip (an ATMEL 256K (32K x 8) EEPROM, AT28BV256), describing the bus protocol for reading data from the memory.



Source: Microchip/Atmel

The left side depicts the memory chip's top-view, showing the various input and output pins. 15 pins labeled A14 … A0 serve as the ADDRESS inputs. CE is a "chip enable" input that must be 0 to enable the chip. OE is an "output enable" input that serves as the read control signal, and must be 0 to perform a read. In the timing diagram, after a valid address is placed on ADDRESS and then OE is lowered, valid data output will appear on OUTPUT (8 pins labeled I/O7 … I/O0).

The timing diagram has several times listed. One is t_{OE}, indicating how long after OE is lowered will valid data appear at the output.

For many devices, due to electrical design reasons, a control signal may be ***active low***, meaning that a 0 causes the control action rather than a 1. An active low signal is commonly written with a bar across the top of the signal's name. OE is an active low signal (as is CE). To avoid confusion in the presence of active low and active high signals, a control signal is said to be ***asserted***, meaning set to 1 if active high or set to 0 if active low.

PARTICIPATION ACTIVITY 7.14.3: Memory bus and protocol example.

Consider the above memory bus and protocol example.

1) After a processor puts an address on the address bus, the processor should set _____ to start a memory read.
   - OE with 0
   - OE with 1
   - t_{OE} with 0

2) After the read signal is asserted, the memory will put the data on the OUTPUT bus within time _____ .
   - 5 ns
   - t_{OE}
   - t_{ACC}

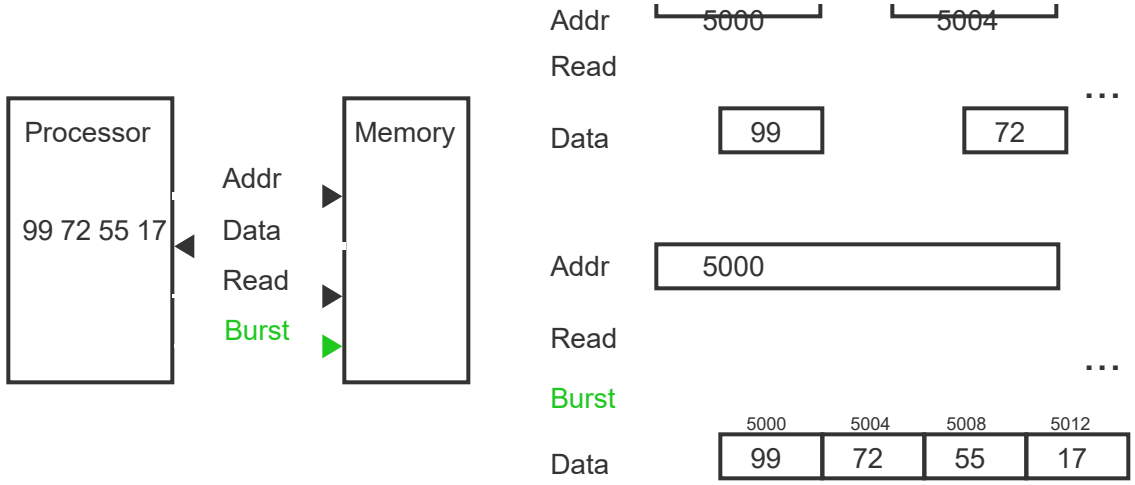
3) The memory bus uses a _____ protocol.
   - strobe
   - handshake

Burst protocols

Commonly, a bus is used to transfer data that appears sequentially in a memory or other device. Ex: A processor may want locations 5000, 5004, 5008, and 5012, perhaps to fill a cache line. A ***burst*** read protocol (aka ***burst mode***) automatically get data items without requiring separate read transactions for each item, thus saving time.

PARTICIPATION ACTIVITY 7.14.4: A burst protocol.

Start ☐ 2x speed



PARTICIPATION ACTIVITY 7.14.5: Burst bus protocol.

Consider the above burst protocol example.

1) If the read and burst signals are both high, the memory automatically reads out successive locations.
   - ○ True
   - ○ False

2) During a burst, the processor had to provide a sequence of addresses.
   - ○ True
   - ○ False

3) During a burst, the memory provides a

handshake acknowledge signal to indicate when new data has been put on the data bus.

- ○ True
- ○ False

4) Suppose 16 locations will be read. If independent read transactions take 2 clock cycles, how many cycles will the entire read require?

- ○ 16
- ○ 32

5) Suppose 16 locations will be read. If a burst read requires 2 cycles for the first read and 1 cycle for each additional, how many cycles will the entire read require?

- ○ 17
- ○ 33

6) Burst makes sense not just for reads, but also for writes.

- ○ True
- ○ False

Note: Modern bus protocols have become quite sophisticated, supporting numerous initiators, numerous responders, varic various priorities among different initiators (including interrupting a burst to let another burst proceed), and more. A popula AMBA, whose specification is hundreds of pages long.

Exploring further:

- AMBA (Wikipedia)
- AMBA (ARM)

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