

4.4 Multipliers (array-style)

Assuming unsigned binary numbers, an N-bit **multiplier** multiplies two N-bit numbers to yield a 2N-bit product. A multiplier by mimicking multiplication by hand. Each multiplier digit is multiplied with the multiplicand and appended with 0's based on location, yielding a partial product, all of which are summed to yield the product.

PARTICIPATION ACTIVITY

4.4.1: 4-bit array-style multiplier.

Start ☐ 2x speed

Note: ppx stands for partial product x

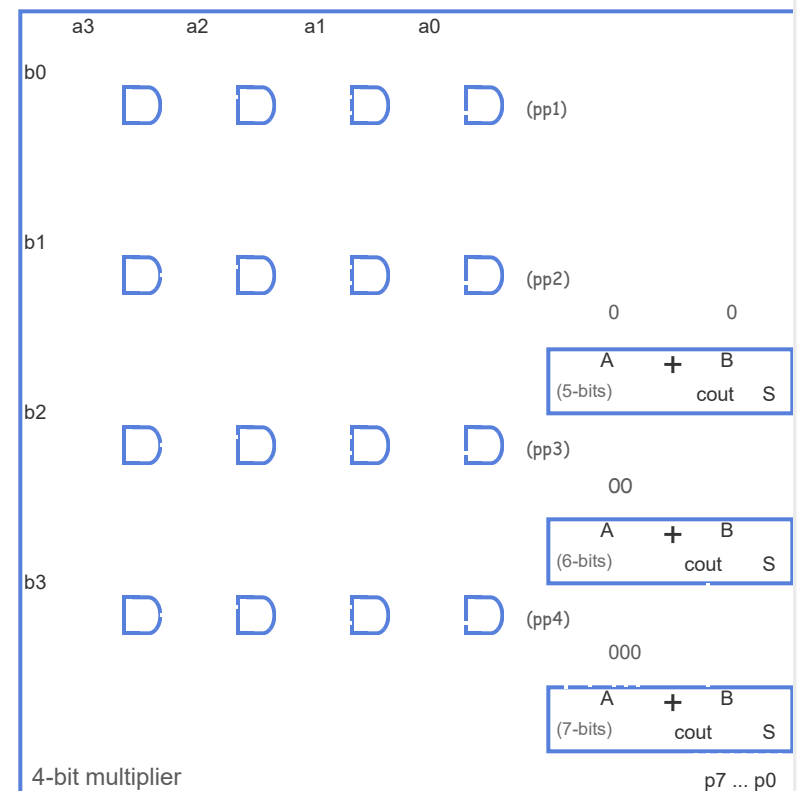
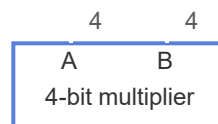
```

      0 1 1 0 (Multiplicand)
x     0 1 0 1 (Multiplier)
-----
      0 1 1 0
    0 0 0 0 0
  + 0 1 1 0 0 0
  + 0 0 0 0 0 0 0
  + 0 0 0 1 1 1 1 0 (Product)
  
```

```

      a3 a2 a1 a0
x     b3 b2 b1 b0
-----
    b0a3 b0a2 b0a1 b0a0 (pp1)
  b1a3 b1a2 b1a1 b1a0 0 (pp2)
 b2a3 b2a2 b2a1 b2a0 0 0 (pp3)
+ b3a3 b3a2 b3a1 b3a0 0 0 0 (pp4)
-----
p7 p6 p5 p4 p3 p2 p1 p0 (Product)
  
```

Block symbol



$\overline{\text{P}}$
8

**PARTICIPATION
ACTIVITY**

4.4.2: Multiplying binary numbers.

Multiply the following 3-bit values. Include any leading zeros.

010
x 110

1) pp1 = ???

Check[Show answer](#)

2) pp2 = ????

Check[Show answer](#)

3) pp3 = ?????

Check[Show answer](#)

4) product = ??????

Check

Show answer

**PARTICIPATION
ACTIVITY**

4.4.3: Multiplier.

Assume a 4-bit array-style multiplier. (Note: Assume every gate input requires 2 transistors and ignore inverters.)

1) Which component performs 1-bit multiplication?

- ☐ AND gate
- ☐ Adder

2) The product is the sum of partial products.

- ☐ True
- ☐ False

3) What is the size (in transistors) used to compute all partial products?

- ☐ 16
- ☐ 64

4) What is the size (in transistors) of a 5-bit carry-ripple adder built from full adders, if a full adder has 50 transistors?

- ☐ 100

☐ 250

5) What is close in size (in transistors) of a 4-bit array-style multiplier? Assume: 6-bit adder has 300 transistors, 7-bit adder has 350.

☐ 250

☐ 1000

6) What is the delay (in gate-delays) to compute all partial products?

☐ 1

☐ 4

7) What is the delay (in gate-delays) of a 5-bit carry-ripple adder built from full adders, assuming a full adder's delay is 2 gate-delays?

☐ 2

☐ 10

8) Which is closer to the total delay of a 4-bit array-style multiplier?

☐ 10

☐ 15

 **Provide feedback on this section**