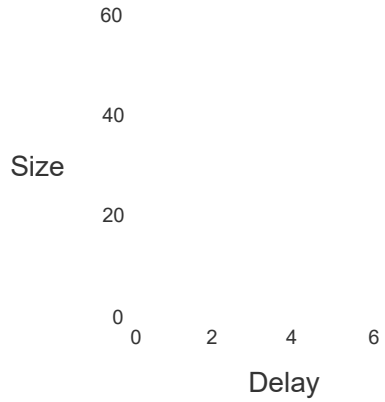
3.8 Tradeoffs

A particular desired behavior, like adding two 4-bit numbers, may have alternative circuit implementations. A ***tradeoff*** is a d that improves one implementation metric while worsening another. An implementation ***metric*** is a measurement of an imp goodness. A common circuit metric is a circuit's size, with smaller size being better. Another is circuit delay, with less delay Unfortunately, decreasing size usually increases delay, representing a tradeoff. Other common metrics include power and c

In contrast to a tradeoff, a design decision that improves some metric(s) without worsening any others is called an ***optimiz***

PARTICIPATION ACTIVITY 3.8.1: A behavior may have alternative implementations that trade off size and delay.

Start 2x speed



PARTICIPATION ACTIVITY 3.8.2: Tradeoffs.

Consider implementing a particular behavior. Indicate whether implementation B is a tradeoff compared to implementation A. (Units are intentionally omitted for this generic example).

1) A's size is 100, delay is 2.
   B's size is 60, delay is 4.
   - ○ Tradeoff
   - ○ Not a tradeoff

2) A's size is 100, delay is 2.
   B's size is 80, delay is 2.
   - ○ Tradeoff
   - ○ Not a tradeoff

Multiple approaches exist for determining circuit size. One approach estimates transistors, assuming every gate input requ transistors, and ignoring inverters for simplicity. A 2-input gate requires 2 inputs · 2 trans/input = 4 transistors. A 3-input ga 6 transistors. A 4-input gate: 8 transistors.

Wires also contribute to size, but ignoring wires as above is a common approximation.

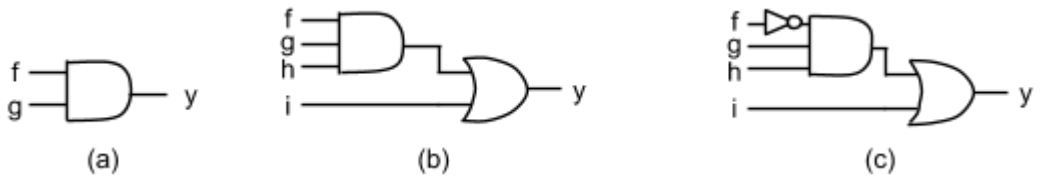
Although each gate may have a unique delay and wires also have delay, a quick approach for approximating circuit delay co number of gates from a circuit's inputs to output, known as ***gate delays***. Inverters are ignored for simplicity.

If multiple paths exist from inputs to output, the circuit's delay is the longest path, called the circuit's ***critical path***.

Real gates have differing delays. A 3-input gate has slightly longer delay than a 2-input gate. Wires also have delay. But cou as above is a common approximation.

PARTICIPATION ACTIVITY 3.8.3: Circuit size and delay.

Determine size in units of transistors, and delay in units of gate-delays.



1) Size of (a)

transistors

Check Show answer

2) Size of (b)

transistors

Check Show answer

3) Size of (c)

transistors

Check Show answer

4) Delay of (b)

gate-delays

Check Show answer

5) Delay of (c)

gate-delays

Check Show answer

Size and delay can be estimated directly from an equation. Ex: y = abc + def has a 3-input AND for abc, another 3-input AND input OR, so size is 3·2 + 3·2 + 2·2 = 16 transistors. The circuit has a column of AND gates followed by an OR, so delay is 2

PARTICIPATION ACTIVITY 3.8.4: Estimating size and delay from an equation.

1) y = a. Size = ___ transistors?
   - ○ 0
   - ○ 2

2) y = ab. Size = ___ transistors?
   - ○ 4
   - ○ 8

3) y = ab + bc. Size = ___ transistors?
   - ○ 8
   - ○ 12

4) y = ab + bc. Delay = ___ gate-delays?
   - ○ 1
   - ○ 2

5) y = a'b'. Size = ___ transistors?
   - ○ 4
   - ○ 6

6) y = ab + a'b'. Delay = ___ gate-delays?
   - ○ 2
   - ○ 3

7) y = a + bcd. Size = ___ transistors?

- 10
- 12

8) y = a + b + cd. Size = ___ transistors?

- 10
- 12

Provide feedback on this section