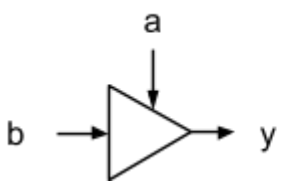
7.11 Register files

A ***three-state buffer*** is a component that outputs y = b if input a is 1, and outputs Z if a is 0. Z represents an electrical situa ***high impedance***. A wire with Z is akin to no wire. As such, three-state buffers support efficient combining of multiple wires will be seen when introducing register files below. Of course, only one connected wire can have a non-Z (0 or 1) value, else collide. Further details on three-state buffer and high impedance are beyond this material's scope.

Figure 7.11.1: Three-state buffer.



a	y
0	'Z' (high impedance)
1	b

PARTICIPATION ACTIVITY 7.11.1: Three-state buffer.

Given a three-state buffer with control input a, data input b, and data output y.

1) If a = 1 and b = 1, then y = ?
   - ○ 1
   - ○ 'Z'

2) If a = 1 and b = 0, then y = ?
   - ○ 1
   - ○ 0

3) If a = 0 and b = 0, then y = ?

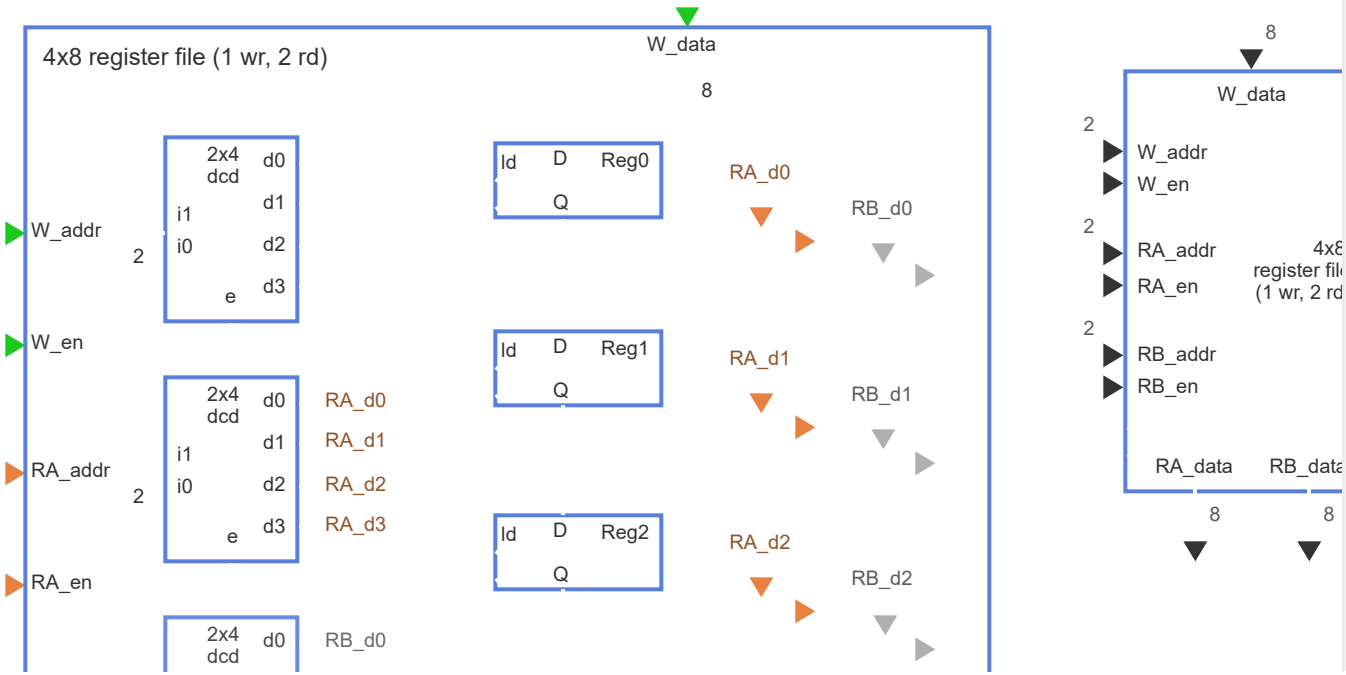
- 0
- 'Z'

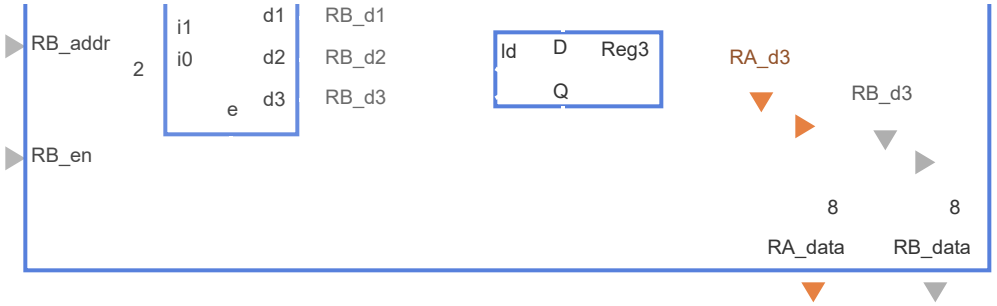
A three-state buffer is more commonly called a ***tri-state buffer***, but that name is trademarked. The term *three-state driver* (
is also used.

An NxM ***register file*** efficiently implements access to N M-bit registers. A 16x32 register file has 16 registers, each 32 bits
having 512 (16 times 32) wires connecting with those registers for loads, a register file consolidates loads through one 32-
course, the tradeoff is that only one register can be loaded at a time, as indicated by a 4-bit address input. Loading a registe
file is known as a ***write*** operation. The data input, address input, and load enable input for writing are together called a ***write***
a register file consolidates read wires into a single 32-bit data output, 4-bit address input, and enable input, forming a ***read***
port may use three-state buffers to efficiently connect the data wires.

PARTICIPATION ACTIVITY 7.11.2: 4x8 register file.

Start 2x speed





PARTICIPATION ACTIVITY 7.11.3: Register file.

1) A 32x8 register file consists of ____ registers.
   - 8
   - 32
   - 40

2) The write address, write enable control, and write data are collectively known as what?
   - Write port
   - Read port
   - Write decoder

3) W_en must be set to 1 to write to, or load, a register.
   - True

- False

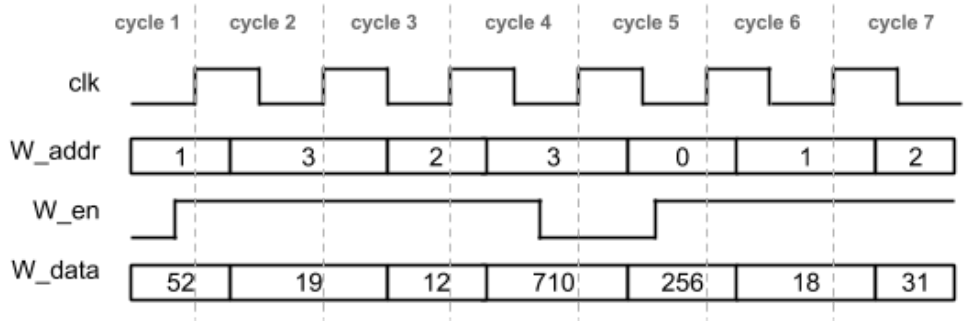
4) Given a 32x8 register file, how many bits is W_addr?
   - 2
   - 3
   - 5

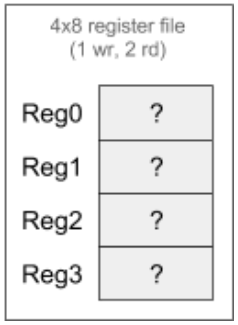
5) Assuming a register file with one write port and two read ports, write and read operations can occur simultaneously.
   - True
   - False

6) Assuming a register file with one write port and two read ports, two read operations can occur simultaneously.
   - True
   - False

PARTICIPATION ACTIVITY 7.11.4: Register files: Writing.

For the given values of W_addr, W_en, and W_data, indicate the register file's contents in a given clock cycle.





1) Reg1, cycle 2

Check Show answer

2) Reg1, cycle 6

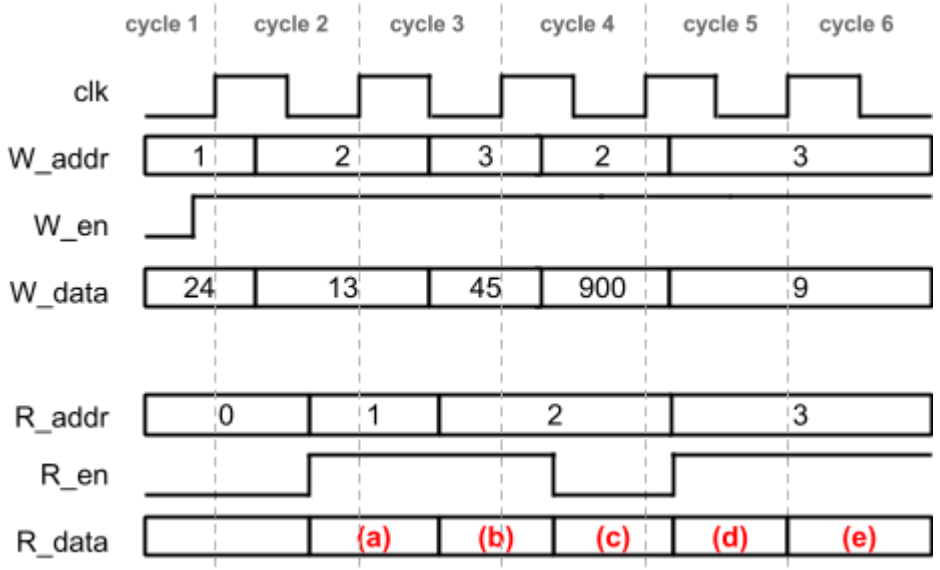
Check Show answer

3) Reg3, cycle 5

Check Show answer

PARTICIPATION ACTIVITY 7.11.5: Register files: Writing and reading.

Assume a 4x32 register file with one read port and one write port. Determine R_data's value at each indicated time. If appropriate, type: Z.



1) (a)

Check Show answer

2) (b)

Check Show answer

3) (c)

Check Show answer

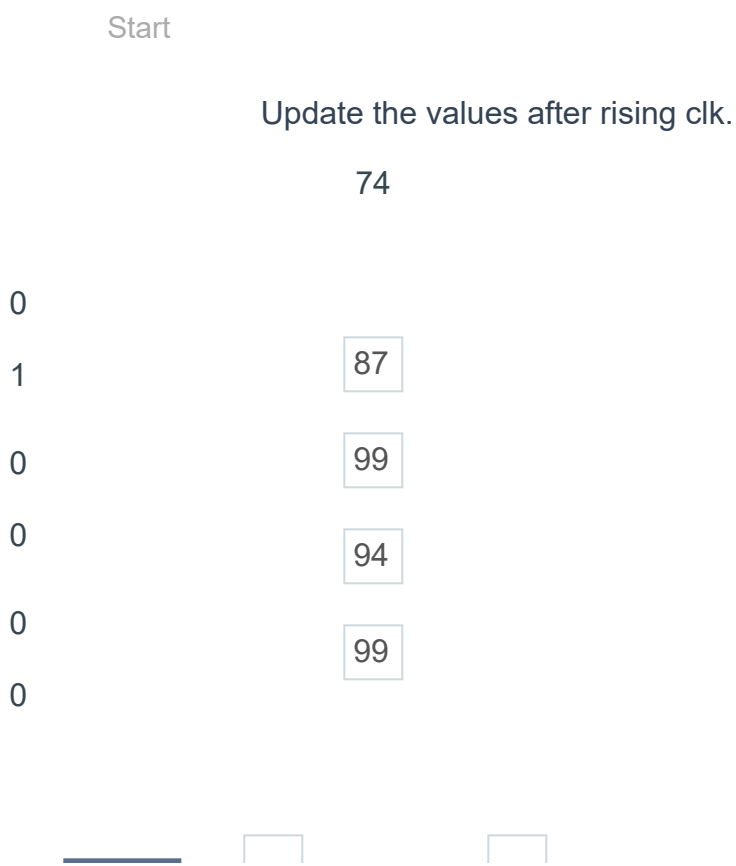
4) (d)

Check Show answer

5) (e)

Check Show answer

CHALLENGE ACTIVITY 7.11.1: Register file writing and reading.



Check Next

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