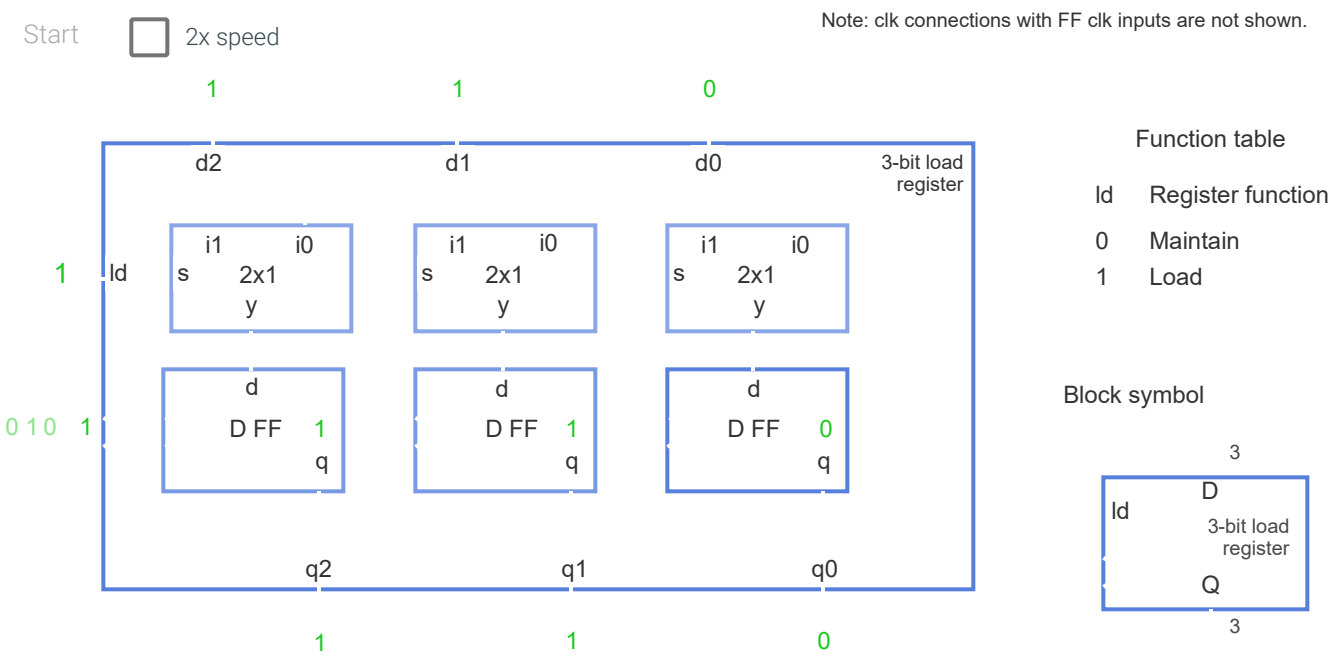
7.8 Load registers

Load register design

A designer may want to ***load*** a register only on certain clock cycles rather than on every clock cycle. Registers commonly c control input named "load" or "ld". Implementing such a load register can be done using 2x1 muxes.

PARTICIPATION ACTIVITY 7.8.1: 3-bit load register implemented with 3 flip-flops and muxes.

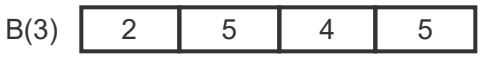


Many registers also come with a reset or clear input, to reset/clear the stored bits to 0's (described in another section).

PARTICIPATION ACTIVITY 7.8.2: Multi-bit data in a timing diagram.

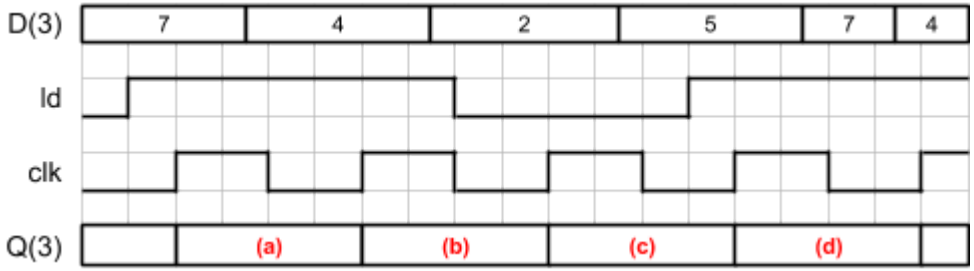
Start ☐ 2x speed

a



PARTICIPATION ACTIVITY 7.8.3: Trace a load register's behavior.

For the given values of D, ld, and clk, indicate the register's Q value.



1) (a)

Q =

Check Show answer

2) (b)

Q =

Check Show answer

3) (c)

Q =

Check Show answer

4) (d)

Q =

Check Show answer

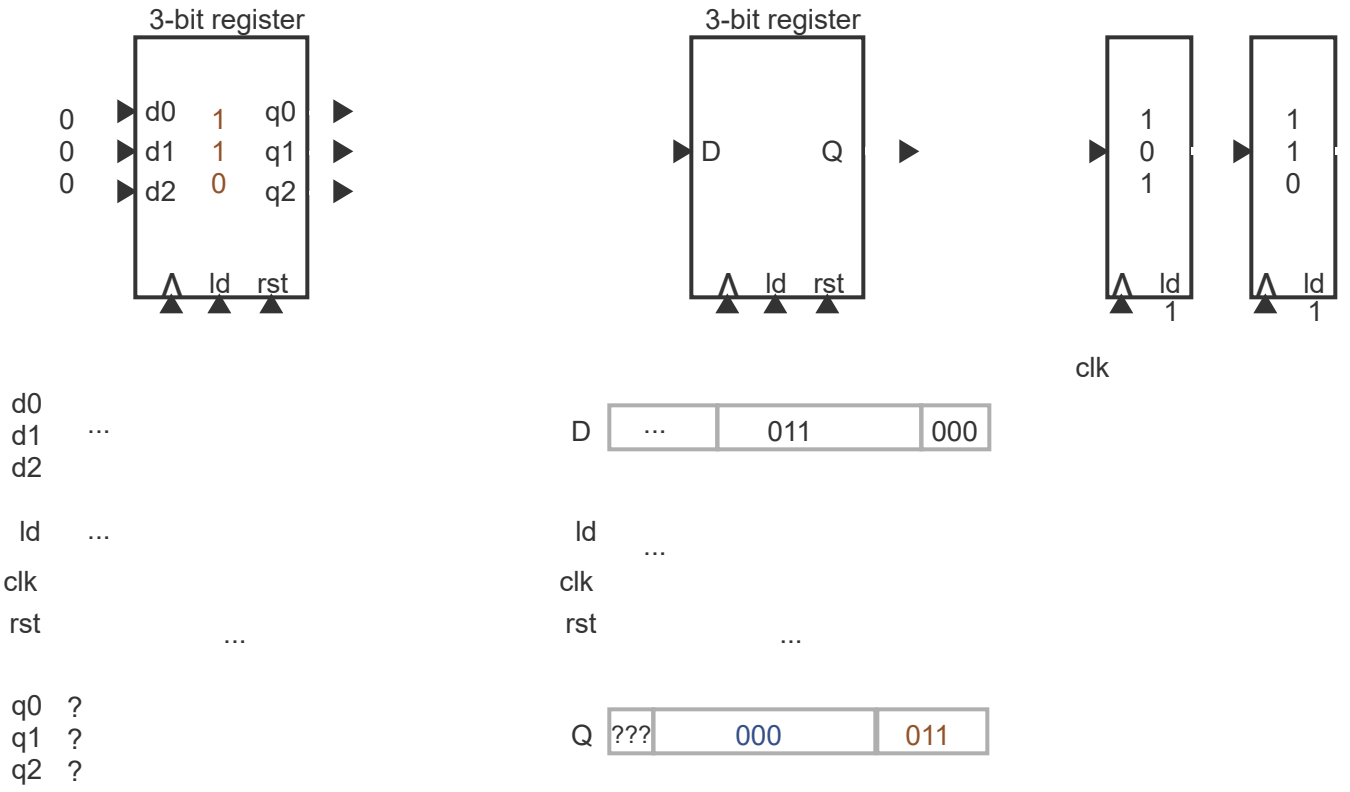
Load register behavior

An N-bit ***load register*** (such as an 8-bit load register or just 8-bit register) stores N bit values, loading new bit values when a if a load input is 1. A load input (ld) indicates when the register should be loaded. A reset input (rst) may exist that indicates register's bits should be reset to 0 (having priority over ld).

All a circuit's registers may share one ***clock*** signal, whose ***rising edge*** (the instant a 0 changes to 1) synchronizes loading c (like a drum beat synchronizes a marching band).

PARTICIPATION ACTIVITY 7.8.4: Registers.

Start 2x speed



PARTICIPATION ACTIVITY 7.8.5: Registers.

Consider the above 3-bit load register.

1) What are q2q1q0 when rst = 1 and ld = 1, assuming q2q1q0 were previously 110, and d2d1d0 are 111?

- 110
-

- 000
- 111
- Depends on clk's value

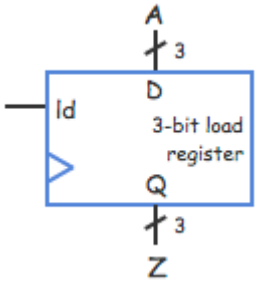
2) Assume rst = 0, ld = 1, d2d1d0 are 110, and q2q1q0 are 111. When a rising clock occurs, what do q2q1q0 become?
   - 111
   - 110
   - 000

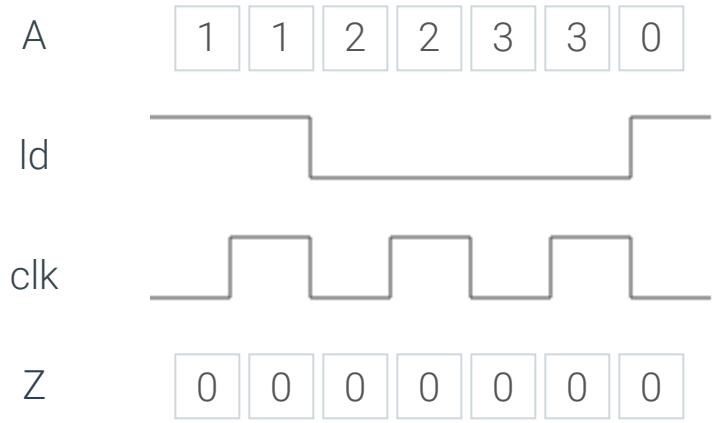
3) Assume rst = 0, ld = 0, d2d1d0 are 110, and q2q1q0 are 111. When a rising clock occurs, what do q2q1q0 become?
   - 111
   - 110
   - 000

4) Assume Y connects to register R1's inputs, and R1's outputs connect to R2's data inputs. On rising clock 1, Y was 100. On rising clock 2, Y was 000. On rising clock 3, Y was 111. What is now in R2?
   - 100
   - 000
   - 111

CHALLENGE ACTIVITY 7.8.1: Indicate Z's value over time.

Start





1 2 3 4 5 6

Check Next

Provide feedback on this section