3.22 Introduction to HDLs (Verilog)

A ***hardware description language*** is a textual language for describing digital systems, as Boolean functions, gate circuits, o Hardware description language is abbreviated as ***HDL***.

An HDL's key purpose is to support simulation. Given designer-provided test input values for particular times, ***simulation*** de output values a digital system would generate over time.

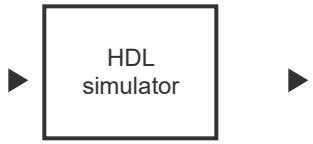
PARTICIPATION ACTIVITY 3.22.1: HDL simulator.

Start 2x speed

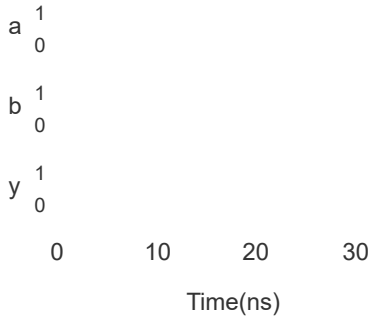
Digital_system:
Inputs: a, b
Outputs: y

y = a'b' + ab

Designer_provided_inputs:
0 ns: b = 0 a = 0
10 ns: b = 0 a = 1
20 ns: b = 1 a = 0
30 ns: b = 1 a = 1



Timing diagram



PARTICIPATION ACTIVITY 3.22.2: HDL Simulations.

Consider the above HDL simulator animation.

1) At time 25 ns, y is 0.
   - ○ True
   - ○ False

2) Input values are determined automatically by the HDL simulator.
   - ○ True
   - ○ False

3) Outputs values are determined automatically by the HDL simulator.
   - ○ True
   - ○ False

The two most common HDLs are Verilog and VHDL. ***VHDL*** is an HDL that was first published in 1987 as an IEEE standard, behest of the U.S. Dept. of Defense. The DoD wanted unambiguous simulatable models of chips being provided by supplie for VHSIC hardware description language, where VHSIC stands for Very High Speed Integrated Circuit. VHDL's syntax is bor from ***Ada***, an earlier DoD language for software programming.

Verilog is an HDL that originated in 1985 at a company called Gateway Design Automation (now Cadence). Verilog was als simulate (or verify) logic circuits. Verilog also became an IEEE standard in 1995. Verilog syntax comes largely from the C pr language.

In the 1990s, HDLs began being used not just for simulating existing circuits, but to specify desired circuit behavior. A ***synth*** automatically converts specified behavior into a circuit.

PARTICIPATION ACTIVITY 3.22.3: HDLs.

Verilog 1985 1987 C VHDL

Year that Verilog originated.

Year that VHDL was first published, as an IEEE standard.

An HDL developed by the U.S. Dept. of Defense.

An HDL developed by Gateway Design Automation, originally proprietary, but later published as an IEEE standard.

The popular programming language, known for conciseness, from which Verilog borrows much syntax.

Reset

Exploring further:

- Verilog (Wikipedia)
- VHDL (Wikipedia)

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