1.5 Signed binary numbers: Two's complement

Two's complement

Unsigned numbers involve only non-negative numbers, like 0 and 3. ***Signed numbers*** involve both positive and negative nur -3.

In binary, a ***signed-magnitude representation*** uses the left bit for the sign: 0 means positive, 1 means negative. Ex: For 4-bi is 3, and 1011 is -3. Signed-magnitude representation is rarely used, because calculations involving negative numbers, such require special circuits beyond an adder.

A more clever negative number representation exists that can use an adder for both positive and negative numbers. A ***com*** digit number is another number that yields a sum of 100...00 (with N 0's), and can be used to represent the negative of that

PARTICIPATION ACTIVITY 1.5.1: Two's complement signed number representation.

Start ☐ 2x speed

Base 10:

		Replace by:	
	5		5
-	3	+	7
	2		1 2 ignore carry

Base 2:

			Replace by:	
	0101	(5)		0101 (5)
-	0011	(3)	+	1101 (-3)
	0010	(2)		1 0010 (2) ignore carry

Why?

7 + 3 = 10; 7 is the complement of 3.

Thus 5 + 7 is 10 too much, so the carry can be ignored.

Complement: invert bits, add 1.

0011 (3) has complement: (0011)' + 1

1100 + 1

So -3 is: 1101

The above is called the ***two's complement representation***, which inverts every bit and adds 1. One's complement also exists used, and so is not discussed further. This material uses "complement" to mean two's complement.

The left bit indicates the sign. 0011 is +3. 1101 is a negative; complementing yields the positive version: 0010 + 1 = 0011, w 1101 is -3.

Given a negative number like 1110, the value can be obtained by complementing, so 0001 + 1 = 0010, and negating, so -00 -2.

PARTICIPATION ACTIVITY 1.5.2: Two's complement signed number representation.

1) In base ten , what is the complement of 33 (two digits)?

Check Show answer

2) In base two , what is the complement of 0010 (four bits)?

Check Show answer

3) What is -2 in four-bit two's complement representation?

Check Show answer

Check Show answer

4) What is -7 in four-bit two's complement representation?

Check Show answer

5) Assuming four-bit two's complement representation, is 1011 positive or negative?

Check Show answer

6) Assuming two's complement representation, what base ten number does 1111 represent?

Check Show answer

7) Assuming two's complement representation, what base ten number does 1001 represent?

Check Show answer

8) In base two, for four bits, what is the complement of 0000?

Check Show answer

9) What is -3 in eight-bit two's complement representation?

Check Show answer

Note: This section uses 4-bit numbers for ease of example; wider numbers like 8 or 32 bits are more typical.

Subtracting by adding

Two's complement representation has the benefit of allowing an adder to be used even when dealing with negative numbe just 0101(5) + 1101(-3) = 10010, or 0010(2) after ignoring the carry. No extensive special circuitry for negative numbers is r

PARTICIPATION ACTIVITY 1.5.3: Two's complement arithmetic.

Assume four-bit two's complement representation.

1) 6 + 2 is 0110 + ?

Check Show answer

2) 6 + -2 is 0110 + ?

Check Show answer

3) 3 + -4 is 0011 + 1100 = ?

Check Show answer

4) 2 - 3 is 0010 + ?

Check Show answer

5) -3 + 2 is ? + 0010

Check Show answer

Overflow

The largest positive four-bit two's complement number is 0111, or 7. The smallest negative is 1000, or -8 (0111 + 1 = 1000, 8). Adding two positives, or adding two negatives, may yield a value that can't be represented in the given number of bits, a as ***overflow***. Ex: 0101 (5) + 0011 (3) incorrectly yields 1000, which is -8 in two's complement.

PARTICIPATION ACTIVITY 1.5.4: Overflow.

Start 2x speed

Adding two positives May overflow	Adding two negatives May overflow	Adding positive and negative Cannot overflow
0010 + 0011 = 0101 (ok) 2 + 3 = 5	1111 + 1111 = (1)1110 (ok) -1 + -1 = -2	1000 + 0111 = 1111 (ok) -8 + 7 = -1

0111 + 0001 = 1000 (overflow)
7 + 1 = -8

1000 + 1111 = (1)0111 (overflow)
-8 + -1 = 7

0010 + 1000 = 1010 (ok)
2 + -8 = -6

As seen above, overflow occurs if the numbers being added have the same sign bit but the sum's sign bit differs. In other w
occurs if two positives sum to a negative (clearly wrong), or two negatives sum to a positive (clearly wrong).

Adding a positive number and negative number (or vice-versa) cannot result in overflow. The sum always has a smaller ma
or both of the numbers, so clearly can fit in the same number of bits. Ex: 7 + -2 = 5, and 5's magnitude is smaller than 7.

PARTICIPATION ACTIVITY 1.5.5: Overflow.

All numbers are in four-bit two's complement representation.

1) 0011 + 0010 results in overflow.
   - ○ True
   - ○ False

2) 0111 + 0110 results in overflow.
   - ○ True
   - ○ False

3) 0001 + 1111 results in overflow.
   - ○ True
   - ○ False

4) 1011 + 1110 results in overflow.
   - ○ True
   - ○

False

5) Number A's sign bit is 0. Number B's sign bit is 0. The sum's sign bit is 1. The addition resulted in overflow.

- True
- False

6) Number A's sign bit is 1. Number B's sign bit is 0. The sum's sign bit is 0. The addition resulted in overflow.

- True
- False

CHALLENGE ACTIVITY 1.5.1: Two's complement.

Start

Note: Answer with 1 digit.

Decimal complement of 4 is Ex: 9

1	2	3	4	5	6

Check Next

1 2 3 4 5 6

Provide feedback on this section