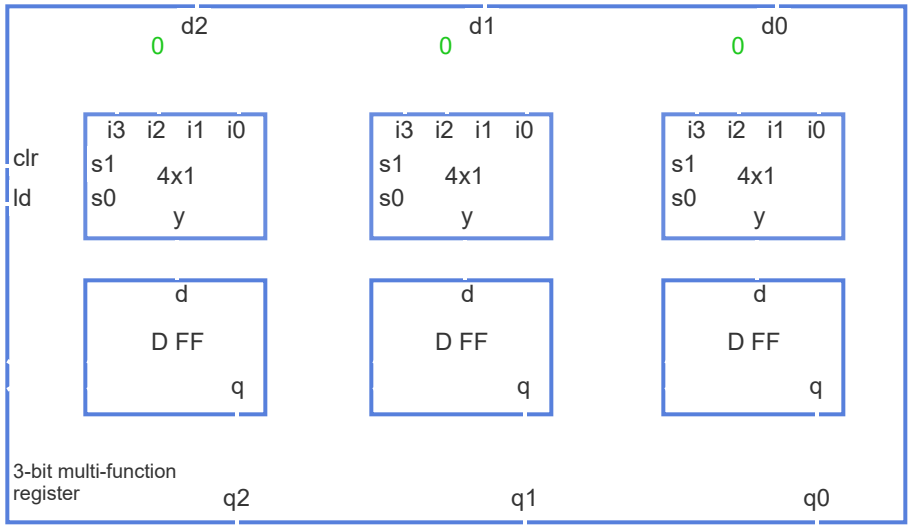
7.9 Multi-function registers

A designer commonly wants to ***clear*** a register, meaning to load 0's. Registers commonly come with a control input named register with clear and load control inputs can be implemented using 4x1 muxes. A register with multiple functions, like clear called a ***multi-function register***.

PARTICIPATION ACTIVITY 7.9.1: Multi-function register with load and clear.

Start 2x speed

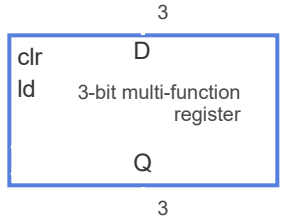
Note: clk connections with FF clk inputs are not shown.



Function table

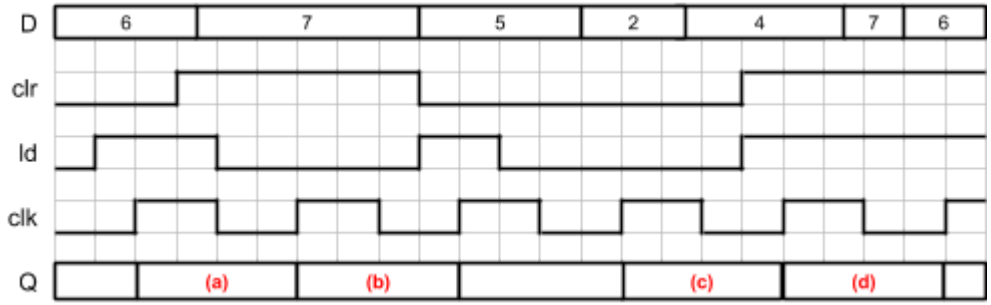
clr	ld	Register function
0	0	Maintain
0	1	Load
1	0	Clear
1	1	Maintain

Block symbol



PARTICIPATION ACTIVITY 7.9.2: Trace a register's behavior: Load and clear.

For the given values of D, clr, ld, and clk, indicate the register's Q value.



1) (a)

Q =

Check Show answer

2) (b)

Q =

Check Show answer

3) (c)

Q =

Check Show answer

4) (d)

Q =

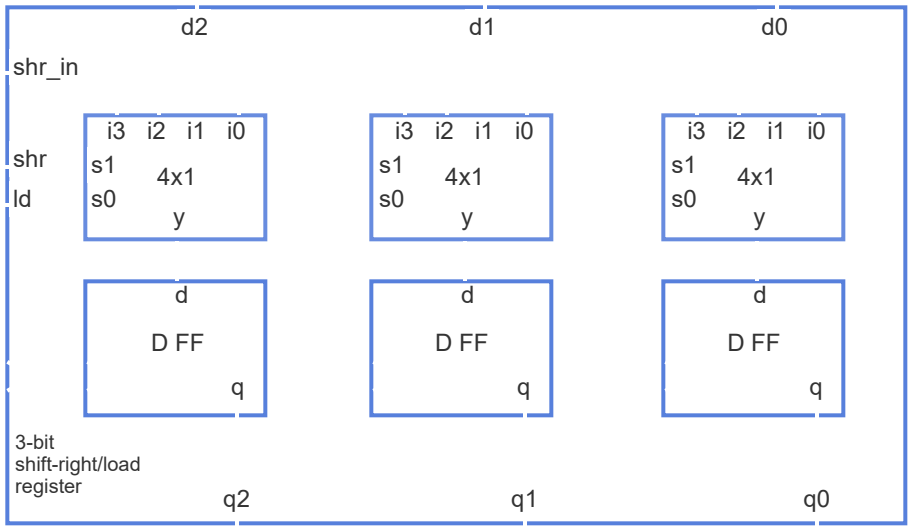
Check Show answer

A ***shift register*** shifts contents by one position, shifting in a new bit too. Ex: A 4-bit right-shift register holding 1100 become shift, assuming the shifted-in bit is 0; the rightmost bit (0) is discarded.

PARTICIPATION ACTIVITY 7.9.3: A register with shift-right and load.

Start 2x speed

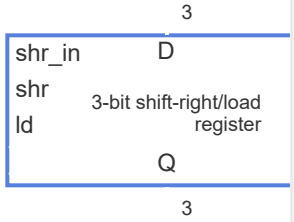
Note: clk connections with FF clk inputs are not shown.



Function table

shr	ld	Register function
0	0	Maintain
0	1	Load
1	0	Shift-right
1	1	Maintain

Block symbol



PARTICIPATION ACTIVITY 7.9.4: Register with shift right and load.

For the given values of D, shr, shr_in, ld, and clk, indicate the register's Q value.

1) D is 111, shr_in is 0, shr is 0, ld is 0, and Q is 101.
clk rises. What does Q become?

Check Show answer

2) D is 111, shr_in is 0, shr is 0, ld is 1, and Q is 101.
clk rises. What does Q become?

Check Show answer

3) D is 111, shr_in is 0, shr is 1, ld is 0, and Q is 101.
clk rises. What does Q become?

Check Show answer

4) D is 111, shr_in is 1, shr is 1, ld is 0, and Q is 101.
clk rises. What does Q become?

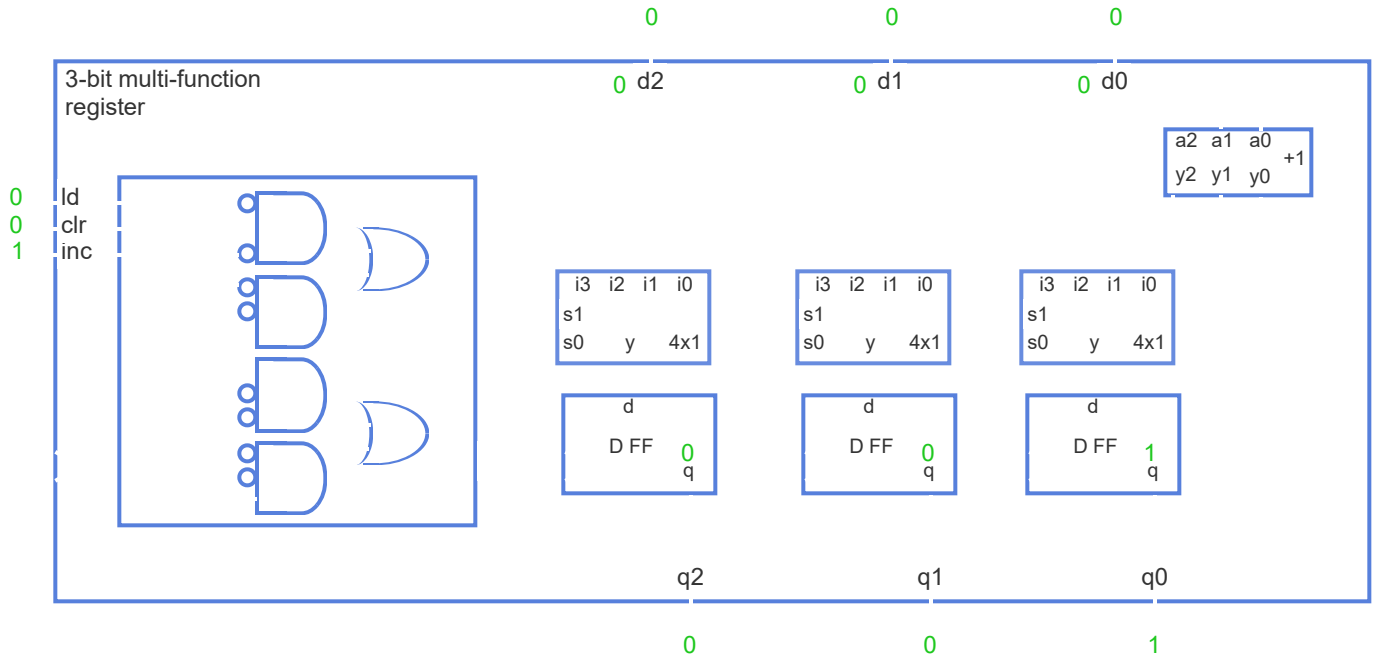
Check Show answer

A register can have various combinations of functions, such as load, clear, and increment. Some simple combinational logi
the control signals to mux select lines.

PARTICIPATION ACTIVITY 7.9.5: Register with load, clear, and increment.

Start 2x speed

Note: clk connections with FF clk inputs are not shown

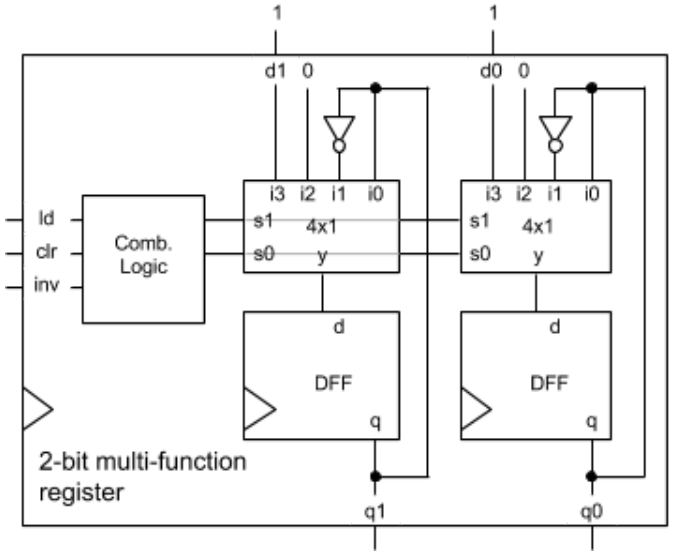


inc	clr	ld	s1	s0	Register function
0	0	0	0	0	Maintain
0	0	1	0	1	Load
0	1	0	1	0	Clear
0	1	1	0	0	(Maintain)
1	0	0	1	1	Increment
1	0	1	0	0	(Maintain)
1	1	0	0	0	(Maintain)
1	1	1	0	0	(Maintain)

$s1 = inc' \cdot clr \cdot ld' + inc \cdot clr' \cdot ld'$

$s0 = inc' \cdot clr' \cdot ld + inc \cdot clr' \cdot ld'$

PARTICIPATION ACTIVITY 7.9.6: Multi-function registers: Load, clear, invert.



ld	clr	inv	s1	s0	Register function
0	0	0	0	0	Maintain
0	0	1	(F)		Invert bits
0	1	0	(G)		Clear
0	1	1	0	0	(Maintain)
1	0	0	(H)		Load
1	0	1	0	0	(Maintain)
1	1	0	0	0	(Maintain)
1	1	1	0	0	(Maintain)

1) (F)

- ○ s1s0 = 00
- ○ s1s0 = 01
- ○ s1s0 = 10

2) (G)

- ○ s1s0 = 00
- ○ s1s0 = 10
- ○ s1s0 = 11

3) (H)

- ○ s1s0 = 11
- ○ s1s0 = 10

- s1s0 = 01

Provide feedback on this section