3.24 Identifiers (Verilog)

An ***identifier*** is a designer-defined name used for items such as modules, inputs, and outputs. An identifier must start with or underscore (_), followed by any number of letters (A-Z, a-z), digits (0-9), underscores (_), or dollar signs ($). Identifiers are meaning upper and lower case letters differ. So testEn and testEN are different.

A ***keyword*** is a word that is part of the language, like the words module and input. A designer cannot use a keyword as an i of keywords appears at this section's end.

PARTICIPATION ACTIVITY 3.24.1: Identifier validator.

Try an identifier: Validate

Awaiting your input...

PARTICIPATION ACTIVITY 3.24.2: Valid identifiers.

Which are valid identifiers?

1) SensorA
   - ○ Valid
   - ○ Invalid

2) red_led
   - ○ Valid
   - ○ Invalid

3) first!motor
   - Valid
   - Invalid

4) fsm input a
   - Valid
   - Invalid

5) _REGISTER_LOAD_
   - Valid
   - Invalid

6) 1_MuxSel
   - Valid
   - Invalid

7) MuxSel_19
   - Valid
   - Invalid

8) always
   - Valid
   - Invalid

Table 3.24.1: Verilog keywords.

always	end	ifnone	not	rnmos	tri
and	endcase	incdir	notif0	rpmos	tri0

assign	endconfig	include	notif1	rtran	tri1
automatic	endfunction	initial	or	rtranif0	triand
begin	endgenerate	inout	output	rtranif1	trior
buf	endmodule	input	parameter	scalared	trireg
bufif0	endprimitive	instance	pmos	showcancelled	unsigned
bufif1	endspecify	integer	posedge	signed	use
case	endtable	join	primitive	small	vectored
casex	endtask	large	pull0	specify	wait
casez	event	liblist	pull1	specparam	wand
cell	for	library	pulldown	strong0	weak0
cmos	force	localparam	pullup	strong1	weak1
config	forever	macromodule	pulsestyle_ondetect	supply0	while
deassign	fork	medium	pulsestyle_onevent	supply1	wire
default	function	module	rcmos	table	wor
defparam	generate	nand	real	task	xnor
design	genvar	negedge	realtime	time	xor
disable	highz0	nmos	reg	tran	
edge	highz1	nor	release	tranif0	
else	if	noshowcancelled	repeat	tranif1	

Provide feedback on this section