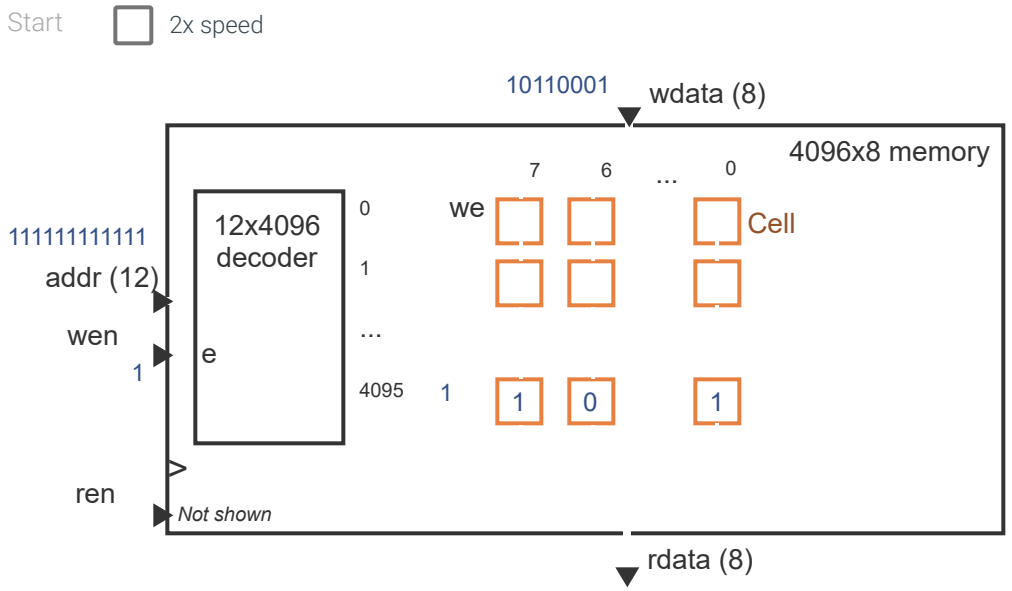
7.12 RAM design

SRAM

An NxM SRAM consists of N locations each M bits wide. An SRAM could be built from N M-bit registers, with a decoder co register's load input for writes, and the decoder controlling a large mux for reads, but such a design has excessive wiring ar large RAMs. Instead, each SRAM location is typically built from an array of cells, with each cell passing a word enable line a through.

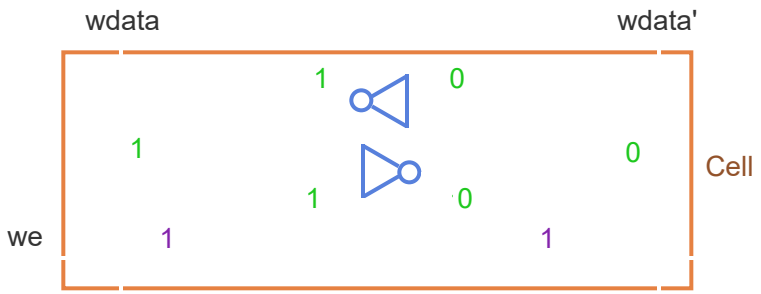
PARTICIPATION ACTIVITY 7.12.1: SRAM design: Array of cells, and decoder.



A common ***SRAM cell*** design uses two inverters to store a bit, and two transistors to let a 1 or 0 into that loop. Because ea transistors, each cell has six transistors.

PARTICIPATION ACTIVITY 7.12.2: SRAM 6-transistor cell basics.

Start 2x speed



Reads use an electrical technique beyond this section's scope. In short, when read-enable (ren) is 1, both data lines are set also set with 1, so the transistors on both sides conduct, causing either the left or right data line's voltage to be pulled dow special "sense amplifier" circuit detects which side was slightly pulled down, to determine whether a 0 or 1 was stored.

PARTICIPATION ACTIVITY 7.12.3: SRAM design.

Consider the above SRAM design.

1) How many cells exist in one word?

Check Show answer

2) How many total cells exist?

Check Show answer

3) For one cell, how many data lines enter from the top?

Check Show answer

4) In the animation, for one cell, a word enable (we) line enters from the left, and exits from the _____.

Check Show answer

5) For a cell, we is 1 and wdata is 1, causing 1 to pass through the left transistor and enter the left side of the inverter loop. What value will appear on the right side of the inverter loop?

Check Show answer

6) we is 1, wdata is 1, and 1 is on the left side of the inverter loop, and 0 on the right. Then we and wdata are set with 0.

What value is on the left side of the inverter loop?

Check Show answer

7) A cell has 0 on the left and 1 on the right of the inverter loop, with we = 0. What value is presently stored in the cell?

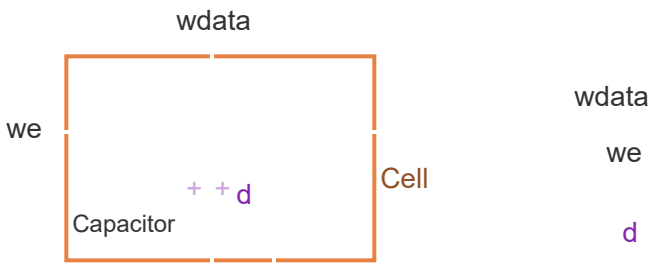
Check Show answer

DRAM

A ***DRAM cell*** stores a bit as a charge on a capacitor, with one transistor that can pass current to the capacitor. With only 1 t capacitor, a DRAM cell is much smaller than an SRAM cell. But the capacitor in a DRAM cell leaks, requiring repeated reads ***refresh*** the cell, which is one reason DRAM access is slower than SRAM.

PARTICIPATION ACTIVITY 7.12.4: DRAM 1-transistor 1-capacitor cell basics.

Start 2x speed



PARTICIPATION ACTIVITY 7.12.5: DRAM cells.

1) How many transistors are in a DRAM cell?
   - ○ 1
   - ○ 2

2) Where is a 1 stored in a DRAM cell?
   - ○ Transistor
   - ○ Capacitor

3) To prevent a stored bit from leaking completely away, a DRAM repeatedly reads and then writes each cell, called a _____.
   - ○ replenish
   - ○ refresh

4) A DRAM is non-volatile.
   - ○ True
   - ○ False

5) A DRAM requires a controller to handle refreshes.
   - ○ True
   - ○ False

Variations of SRAM and DRAM cells exist, such as SRAM cells with 4 transistors and two resistors, but the above are the m
forms.

Exploring further:

- SRAM (Wikipedia)
- DRAM (Wikipedia)

Provide feedback on this section