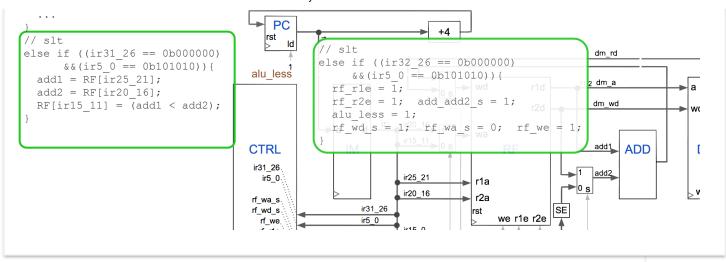
7.19 Base MIPSzy + slt

A designer can extend the base MIPSzy to support the slt instruction. The designer might first modify the behavioral descriptorion opcode 000000 and function code 101010, with the actions being to set the first operand register with 1 if second register third, else setting the first register with 0.

The designer can then modify the processor circuit to carry out those actions. The designer can extend the ADD componer input signal indicating that the component should perform a less-than comparison rather than an addition, outputting 1 if ir than input B, else outputting 0 (the 1 and 0 are actually 32 bits: 00..01 and 00..00). Because the component now does more the designer might name the component ALU. An **ALU** (**arithmetic-logic unit**) is a combinational component that performs arithmetic and logic operations needed by a processor, like add, subtract, compare, AND, etc. This ALU only does add and c

Finally, the designer would update the control logic to feed the two RF registers to the ALU and set alu_less = 1, and write the RF (the paths for those reads and write already exist to support the very similar add instruction).





PARTICIPATION ACTIVITY

7.19.2: Extending the base MIPSzy to support the slt instruction.

1) If add1 is less than add2, what does the ALU output? Type one digit.

Check Show answer

2) The control logic actions for slt are nearly identical to those for add. Type the statement that was added for slt.

Check

Show answer

3) If add1 is not less than add2 (being equal or greater), a 0 will be written into the register specified by which ir bits?

Type answer as: ir5_0

