7.23 Base MIPSzy + beq/bne

A designer can extend the base MIPSzy to support the beq (branch on equal) instruction. The designer might first modify th description to detect opcode 000100, with the actions being to load PC with the target address if the instruction's two RF re equal values.

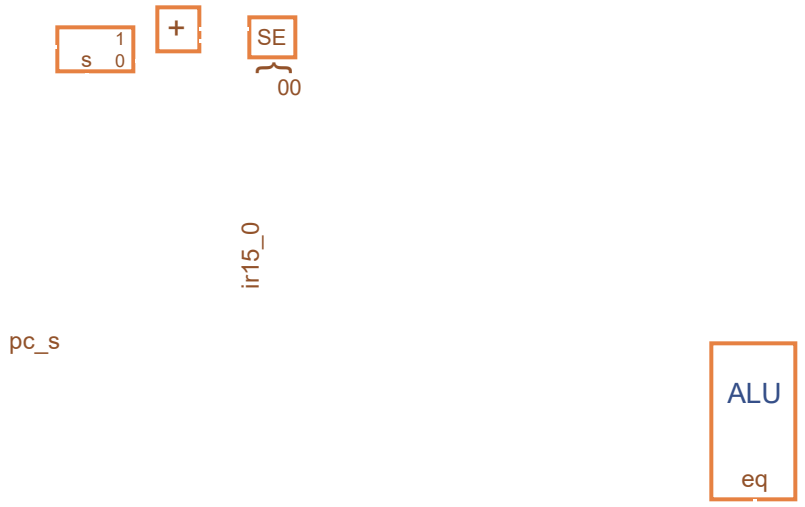
The designer can then modify the processor circuit to carry out those actions. The designer would extend the ADD compor output signal indicating whether the component's two data inputs are equal. Because the component now does more than designer might name the component ALU. An ***ALU*** (***arithmetic-logic unit***) is a combinational component that performs the arithmetic and logic operations needed by a processor, like add, subtract, compare, AND, etc. This ALU only does add and c equality.

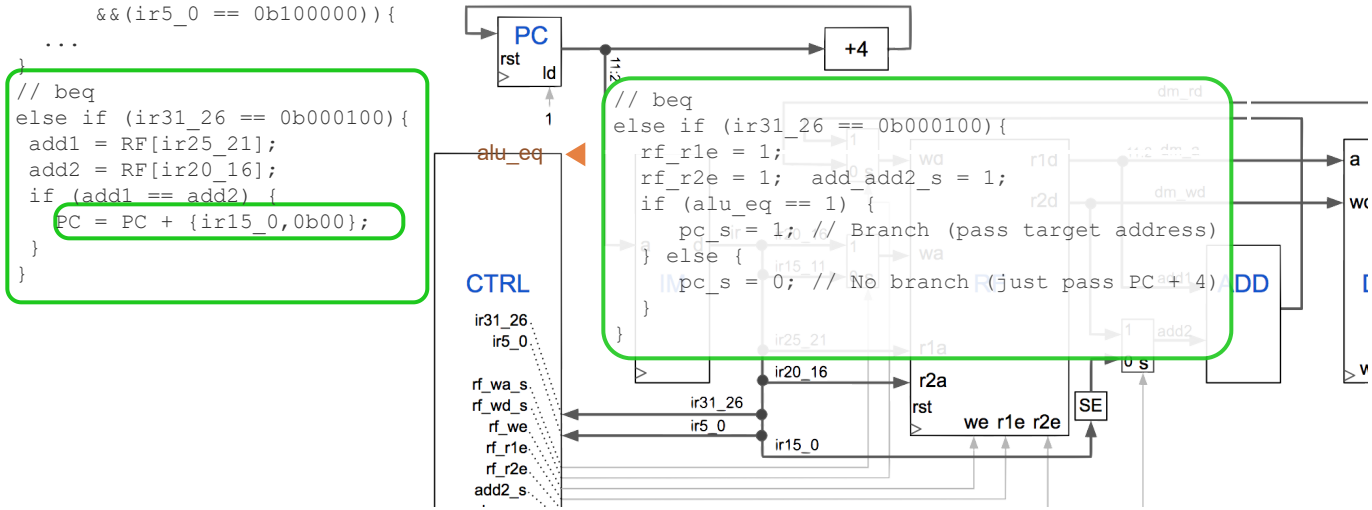
The designer would also add a mux in front of the PC, with the new value coming from ir15_0 with 00 appended and summ Finally, the designer would update the control logic to feed the two RF registers to the ALU, then control the PC mux based alu_equal.

PARTICIPATION ACTIVITY 7.23.1: Extending the base MIPSzy for the beq instruction.

Start 2x speed

```
ir = IM[PC/4];
PC = PC + 4;
// Assume ir31_26... extracted
// lw
if (ir31_26 == 0b100011)  {
  ...
}
// sw
else if (ir31_26 == 0b101011){
  ...
}
// addi
else if (ir31_26 == 0b001000){
  ...
}
// add
else if ((ir31_26 == 0b000000)
```





The bne (branch on not equal) is nearly identical, but with opcode 000101 (rather than 000100), and with comparison alu_e than 1). No changes to the processor circuit are required; only the behavioral and control logic actions change.

PARTICIPATION ACTIVITY 7.23.2: Extending the base MIPSzy to support beq and bne instructions.

Consider the base MIPSzy extended to support beq and bne.

1) In the processor circuit, if the two register values being input to the ALU are 27 and 13, the ALU's eq output is ___.
   - ○ 0
   - ○ 1

2) In the processor circuit, the beq (and bne) instruction forms the offset by appending's two 0's to ir15_0, and sign extending to ___ bits total.
   - ○

18

- 32

3) In the processor circuit, the offset is added with ___.
   - PC + 4
   - the ALU's output

4) If the two registers of a *beq* instruction have equal values, then alu_eq coming into the control logic will be 1. The control logic will thus set pc_s with ___.
   - 0
   - 1

5) If the two registers of a *bne* instruction have equal values, then alu_eq coming into the control logic will be 1. The control logic will thus set pc_s with ___.
   - 0
   - 1

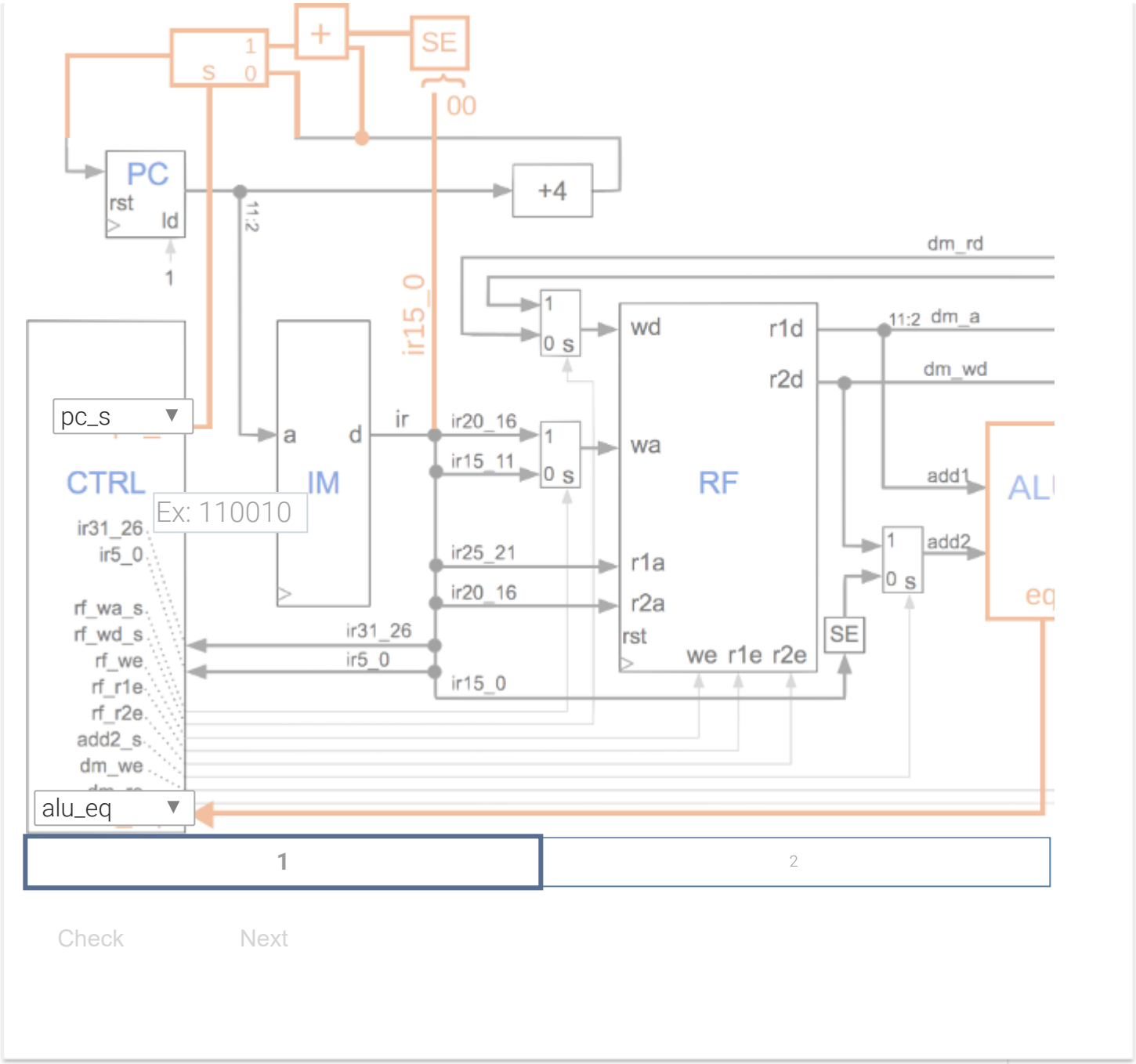
CHALLENGE ACTIVITY 7.23.1: beq/bne extension in MIPSzy.

Start

1

2

Enter the bits for each item if $t1 and $t6 are different.
asm: beq $t1, $t6, LABEL
ir: 000100 01001 01110 0000000000111011



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