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# Measurement errors in the scanning of piezoresistive sensors arrays

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**Abstract**

Arrays of piezoresistive sensors (PRS), which are often used for tactile sensing, suffer from crosstalk between adjacent elements that can alter the readings of the force applied. In this paper, the sources of errors, with specific reference to crosstalk and electronic circuitry used to scan the array, are examined. The solutions presented in the literature are discussed, evaluating their performance and errors. From this analysis, some guidelines can be derived for the use of scanning circuits. 

*Keywords:* Piezoresistive sensors; Arrays; Crosstalk; Scanning electronics

## 1. Introduction

Artificial tactile sensors aim at reproducing some of the basic functions of the biological tactile system, such as texture detection, shape discrimination, or evaluation of the force needed for a correct grasp [1–4]. These sensors are widely used in robotics, ergonomics and rehabilitation. The task is very often to measure the (normal) components of the force with adequate spatial resolution.

For the above mentioned task different kinds of sensors (such as resistive, capacitive, strain gage, etc.) have been proposed. Piezoresistive sensors (PRS) (sometimes referred to as Force Sensing Resistors, FSR) are among the most widely used. In this way, discrete sensors, and arrays of sensors with resolution of a millimetre can be easily made.

PRS sensors can be realised using a conductive polymer allocated between a film conductive grid, and have been widely used to build arrays. The transduction mechanism is based on the variation of the polymer-grid resistance when the sensor is pressed. An electronic circuit measures the voltage drop across (or the current through) this resistance so that, by means of a suitable calibration, the applied force can be determined.

In despite of their widespread application, PRS sensors suffer from some problems due to their transduction mechanism, such as non linearity, hysteresis, and creep. These problems have often been addressed in the literature.

Moreover, when using arrays, there are other aspects which need to be considered, such as the crosstalk between adjacent elements. Crosstalk is due to the presence of parasitic parallel paths that, when attempting to read the voltage corresponding to a taxel (tactile pixel), alter the value of the resistance read. This aspect has also been addressed in literature, and some circuits have been proposed in order to eliminate this problem. However, the circuits used are normally discussed in a very schematic way, without a careful examination of the errors due to the electronics used, while a comparative evaluation of the performance of the various circuits is still lacking.

The aim of this paper is therefore to examine the performance of the circuits most often encountered in the literature for the scanning of piezoresistive arrays, evaluate and compare the errors that they can introduce, and determine some guidelines for their use.

## 2. The plastic film sensor array

For the realisation of PRS sensors, two main structures can be identified. In the first one, a resistive polymer is inserted between two plastic films, each one carrying rows of parallel conductive strips in contact with the resistive film. The conductive strips are placed orthogonal to another, thus building a matrix of sensors, where the sensitive area corresponds to the portion of the resistive poly-

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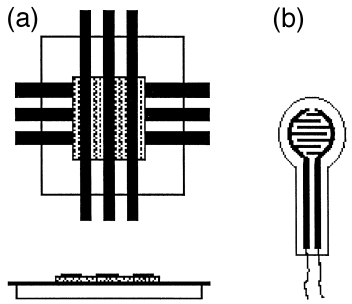


Fig. 1. In (a) a schematic of a matrix of piezoresistive sensors with the sandwich structure; in (b) a discrete sensor with interdigitated structure and longitudinal reading.

mer under the crossing of two $x$–$y$ conductive strips (Fig. 1a). When a force (pressure) is applied to the sensor, the resistance between conductive strips and polymer varies, thus allowing measurement of the force itself. In the other structure, the conductors are allocated on the same side of the polymer (Fig. 1b), so that the resistance of the longitudinal path is read through the same mechanism described above. The two structures can be used for the implementation of arrays.

The curve pressure vs. resistance of piezoresistive sensors is approximately linear in a log $P$ vs. log $R$ plot, while the resistance values range typically from 200 Ω to 300 kΩ, depending on how the sensors are made and on the pressure exerted on them. For example, sensors made by means of silicon resins loaded with graphite show a resistance ranging from 50 Ω to 50 kΩ, while other sensors, based on resistive inks or on polymer sheets, have values ranging from 1 kΩ to 300 kΩ. Moreover, the pressure exerted (and therefore the resistance) depends on the application: in cases where the measure of a grasp is involved, the pressure is more limited, typically between 1 N and 20 N, and the resistance values are comparatively higher; however, in cases where these sensors are used for gait analysis, the maximum pressure on a single sensor can reach and exceed 0.4 MPa, and resistances can be as low as 200–400 Ω [5–8].

## 3. Materials and methods

One of the most notable effects when dealing with arrays is the presence of crosstalk between adjacent elements, since the response of each sensitive area also depends on the presence of the surrounding resistive elements which introduce parallel paths.

In order to understand the crosstalk effects, we will refer to Fig. 2a, where, for simplicity, only a small portion of an array is presented.

When we try to read the value of resistor $R_{ij}$, other parasitic paths of different lengths and resistance, such as the path composed of the three resistances $R_{im}$, $R_{sm}$ and $R_{sj}$ in series, appear in parallel to $R_{ij}$ (Fig. 2b). They cause errors in the reading of the voltage and thus of the force acting on $R_{ij}$. In the case of sensors made by a single polymer sheet, also the paths due to the bulk conductivity of the sheet, schematised by the parasitic resistances $R_{is} = R_{rr}$ and $R_{jm} = R_{cc}$ (row–row and column–column couplings) are present. Their magnitude depends on the materials and dimensions of the array and also on the pressure map. They can be eliminated either by using non isotropic polymer sheets with on plane resistance much higher than through plane resistance, or (more commonly) by means of scanning circuits which try to counteract this effect (see next paragraphs).

In order to avoid crosstalk, the logic which scans the array by rows and columns must connect only one row and one column (that is, one sensitive element) at a time to the A/D converter, all other rows and columns being (electronically) disconnected. The various circuits proposed [6–14] aim at completely eliminating crosstalk, even if their performance with respect to the errors which can affect the measurement are different, and therefore must be carefully analysed.

Obviously, crosstalk is less important when the piezoresistances are higher but, as reported in Section 2, for the wide range of resistances and pressures involved, different errors in different point of the pressure–resistance characteristics can be present, so that an analysis of the errors, valid in any condition, is necessary.

### *3.1. Analysis of the errors introduced by the scanning electronics*

The circuits proposed for the scanning of piezoresistive arrays can be subdivided in two main categories: the ones

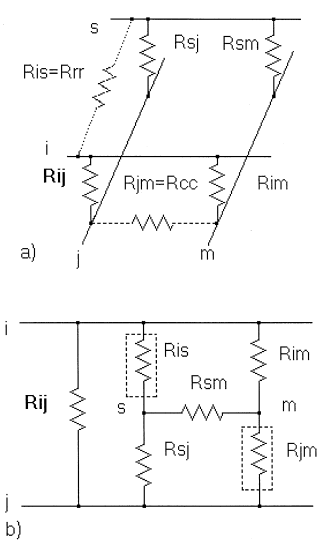


Fig. 2. In (a) the portion of the matrix. From the scheme in (b), there emerges a path composed of three resistances ($R_{im}$, $R_{sm}$ and $R_{sj}$) which, being in parallel to $R_{ij}$, alters its value. If also $R_{is}$ and $R_{jm}$ are present, other parallel paths must be included.

which counteract crosstalk by introducing a feedback loop [10–14] and the ones which use grounding [6–9]. In the following, examples of these two circuits, together with their performance, will be examined.

*3.1.1. Circuits using a feedback loop*

The performance of this class of circuit will be discussed with reference to the scheme of Fig. 3 (Circuit A, adapted from [12]). Multiplexers $\text{mux}_1$ and $\text{mux}_3$ connect $R_{ij}$ in the partition circuit composed by $V_{cc}$, $R_p$, $R_{\text{mux}_1}$ (the on resistance of $\text{mux}_1$), $R_{ij}$, buffer $i$ and $\text{mux}_3$, while $V_{out}$ is read through $\text{mux}_2$ and buffer 1. The unwanted effects due to crosstalk are reduced by including the loop formed by the buffers on the rows and the switches on the columns. In fact, the buffers impose the output voltage on all the rows, except row $i$, while the switch connects the columns not active to $V_{out}$, so that all the terminals of the resistances of the array other than $R_{ij}$ are at the same potential and (in ideal conditions) no current flows across them.

The presence of $\text{mux}_2$ on the columns is necessary to virtually eliminate the effects of $R_{\text{mux}_1}$ on the readings of the $R_{ij}$. If $\text{mux}_2$ were not present (see for instance Refs. [10,11]) and $V_{out}$ were measured at node A, $V_{out}$ would include both the voltage drop across $R_{ij}$ and the one across $R_{\text{mux}_1}$, so that the voltage applied to the rows other than $i$th would differ from $V_{out}$ and the parasitic paths would not be completely cancelled. In fact, even if $R_{\text{mux}_1}$ is low (50–100 Ω), its effect can be noticeable. Moreover, the level of reduction of the crosstalk would depend on the resistances surrounding $R_{ij}$, that is on the pressure map.

The current in the buffers need also to be considered in the design of the electronics. In fact, if $R_{ij}$ is to be read, buffer $i$ must supply the sum of the currents which cross $R_{ij}$ and the other resistances $R_{ik}$ ($k = 1, 2, \ldots, N$, $k \neq j$) allocated between the columns (referred at voltage $V_{out}$) and row $i$ (at ground potential). This current, which can be

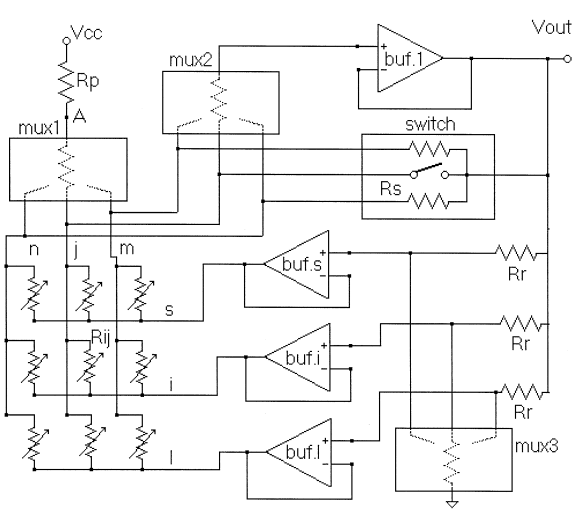


Fig. 3. Circuit based on the feedback (Circuit A): the buffers and the switch apply the output voltage on the rows and on the columns respectively in order to counteract crosstalk and the effect of $R_{rr}$ and $R_{cc}$.

calculated with reference to the voltage divider composed of $V_{out}$, the on resistance of the switch $R_{sw}$, $R_{ik}$ and buffer $i$, can be high when $R_{ij}$ (and thus, $V_{out}$) is high, and the $R_{ik}$ are low. In fact, if $R_{ik} = 200\ \Omega$ ($k = 1, 2, \ldots, N$, $k \neq j$), the current $I_i$ that buffer $i$ must supply is:

$$I_i = \frac{V_{out}}{R_{ij}} + (N-1)\frac{V_{out}}{R_{ik}} \tag{1}$$

For instance, if $V_{out} = 5$ V, this current can reach $(N-1) \times 25$ mA, a value that buffer $i$ cannot supply, with a consequent degradation of the performance of the circuit. This circuit is therefore not suited for use when taxel resistances can assume low values and/or the array is large.

The current is also affected by $R_{rr}$, which constitutes a direct path between row $i$ and the adjacent rows, and that, even if not altering $V_{out}$, increases the current that flows in buffer $i$ by the quantity $\Delta I_i$:

$$\Delta I_i = \frac{V_{out}}{R_{ris}} + \frac{V_{out}}{R_{rik}} \tag{2}$$

where $R_{rik}$ and $R_{ris}$ are the resistances between row $i$ and the two adjacent rows (the other rows are at the same voltage $V_{out}$ and do not affect this current). $R_{cc}$ can alter the value of $V_{out}$ (in Fig. 2 it would give rise to the path composed of $R_{jm}$ and $R_{im}$, in parallel to $R_{ij}$) but through the presence of the switch on the columns, its effect on $V_{out}$ and on the currents is counteracted, and only $R_{ij}$ is read.

For a more realistic evaluation of the errors of this circuits, the effect of some parasitic parameters, such as the offset and bias of the op-amps used, and the on resistances of the mux and of the switch must be considered. This will be done in Section 4.

Another circuit, based on the feedback, has been outlined in Ref. [13], where buffers are inserted both on the rows and on the columns not active. In Fig. 4, a slightly modified circuit (Circuit B) is proposed. It includes both the characteristics of the double mux (which compensates for the resistance of the switch), as in Circuit A, and the buffers on rows and columns, as in Ref. [13]. Therefore, it shows improved performance with respect to the two above mentioned circuits. However, the complexity of the electronics increases. The problems concerning this circuit are similar to those of Circuit A, and will be discussed in Section 4.

*3.1.2. Circuits based on grounding*

The second class of circuits has been reported in some papers [6–8], even if there are slight differences among them. Fig. 5 depicts a structure, Circuit C, which can be used for the discussion.

It is based on a reading by means of amplifiers, so that:

$$V_{out} = -V_i \frac{R_r}{R_{ij}} \tag{3}$$

and eliminates the crosstalk by interposing a buffer on

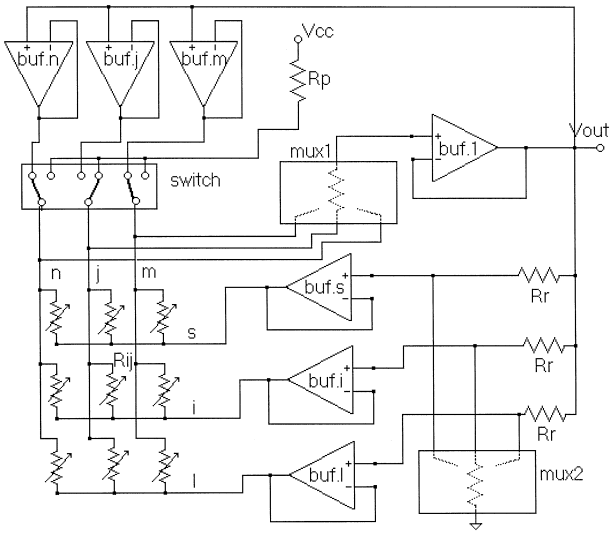


Fig. 4. Circuit based on the feedback (Circuit B). The circuit is similar to Circuit A, but the crosstalk is counteracted by buffers inserted both on rows and on columns.

every column and a trans-resistance amplifier on every row. In this way, a difference of potential which must be as much as possible close to zero is imposed across the elements not read, thus counteracting the effect of the parasitic paths, and also of resistances $R_{rr}$ and $R_{cc}$.

This scheme can be considered as derived from the circuit proposed in [9] where only one trans-resistance amplifier is included after a mux which addresses the columns. However, in this circuit the resistance of the mux, in series with $R_{ij}$, alters the reading of $V_{\text{out}}$, while the effect of $R_{rr}$ and $R_{cc}$ is not eliminated. Therefore, this circuit will not be discussed in detail here. In Circuit C, the use of an amplifier on every column (followed by the mux) improves the performance of the circuits, but with an obvious increase in complexity.

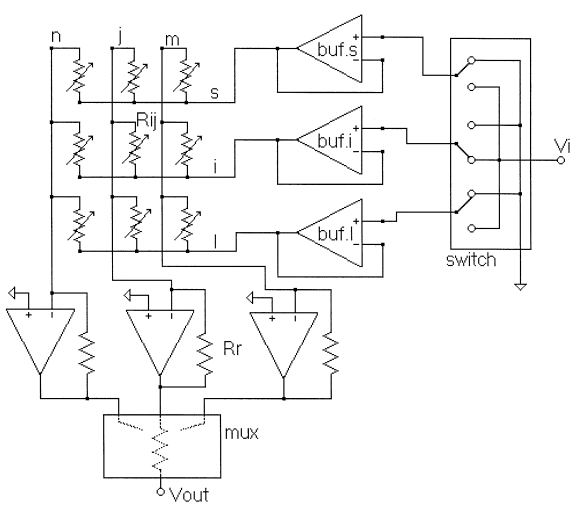


Fig. 5. Circuit based on grounding (Circuit C). Every row is driven, through independent buffers, by a constant voltage source ($V_i$), while the input of the trans-resistance amplifiers acts as a virtual ground so that the columns not active are grounded. The gain of the amplifiers can be varied in order to fit to the desired voltage range.

Also for this circuit the performance with respect to parasitic parameters, mainly bias and offset, needs to be analysed, while care must be devoted to the maximum allowable current, as for Circuits A and B. A limitation on the maximum current of the op-amps arises if the array is uniformly pressed along a row, say row $i$. In this case, the resistances of all the sensors on this row $R_{ij}$ ($j = 1, \ldots, N$) would be in parallel, so that buffer $i$ must supply a current $N$ times larger than that due to a single resistance. For instance, if $V_i = 1$ V and $R_{ij} = 200\ \Omega$, $j = 1, \ldots, N$, the total current drawn from buffer $i$ would be $N \times 5$ mA. In order to reduce this problem, the supply voltage must be held at a low value. In the same way as for Circuits A and B, the net effect of $R_{rr}$ (which is a shunt between row $i$ and the adjacent rows) is that of increasing the current that the row buffers must withstand. Also in this case, the current is lower when the taxel resistances are high.

## 4. Simulations results and discussion

In the following the results of some Montecarlo simulations will be reported, which can be useful not only to validate the theoretical results but also to determine the behaviour of the various circuits in real conditions; that is, by also taking into account the spread in circuit parameters. In fact, in evaluating the performance of the circuits, a statistical approach can be more useful than a deterministic, or worst case, one.

The simulations have been used to evaluate the performance of the circuits with respect to different parameters, that is the mux and switch resistance, the bias and offset of the op-amps, the effect of the row–row and column–column resistances.

The parameters that have been considered as indicative of the performance of the different circuits are the errors on the voltage read in correspondence to the selected resistance $R_{ij}$, and the current that buffer $i$ (the most stressed) had to supply. Finally, the complexity of the circuit can be evaluated through the number of op-amps and of mux.

The percentage error on the value of the voltage read has been evaluated as follows:

$$e\% = \frac{V_{\text{id}} - V_{\text{out}}}{V_{\text{id}}} * 100 \qquad (4)$$

where $V_{\text{id}}$ is the voltage which would be read in ideal conditions, that is in the absence of parasitic parameters, and $V_{\text{out}}$ is the voltage effectively read at the output. The comparison has been made on the basis of a similar range for the output voltage, that is 0–10 V for the three circuits.

For the simulations, a matrix of $5 \times 5$ elements was considered, and the performance of the electronics was simulated by means of the Spice® program. When considering the effect of a single parameter in the simulations, the effect of the other parameters in the Spice model was put to zero. Here, only the results obtained with a pressure

map where the resistance of the central element is to be read, and all the 24 surrounding elements are set at values which can vary randomly in a pre-defined range, will be reported. The use of this simulated map allows determining a mean value of the errors, and making a comparison between the different circuits. In order to have a single figure depicting the performance of the circuits, the values obtained for the errors and the currents have been averaged over 40 Montecarlo trials.

The values of the resistances have been made to vary in the range 200–20 kΩ and in a higher range (500–200 kΩ) while the value of the central element to be read varies correspondingly in the range 200 Ω–20 kΩ (or 500 Ω–200 kΩ). The mean values for the offset voltage and the bias current of the op amps have been respectively assumed as 1 mV and 100 nA, with random variations within a range of ±30%. These values can easily be found in commercial devices. The mux and switch resistances have been assumed as randomly varying between 50 and 100 Ω, which can also be considered as typical.

The effect of the coupling resistances $R_{rr}$ has been summarised by introducing a resistance between rows $i$ and $s$, and rows $i$ and $l$: the other rows (not indicated in the figures) have no effect because they are all at the same voltage ($V_{out}$ or ground). In a similar way, the presence of column–column resistances has been depicted with resistances placed between columns $j$ and $n$, and $j$ and $m$. Moreover, the coupling resistances have been assumed as randomly varying in the same range as the array resistances.

For brevity, only the results for the case of lower resistance range, and of presence of $R_{rr}$ and $R_{cc}$, which is more critical, will be reported in detail below.

In Figs. 6 and 7 the mean value of the errors for the three circuits, evaluated according to Eq. (4), and of the currents supplied by the most stressed buffer have been reported, respectively. From Fig. 6, it emerges that Circuit B and C have an almost similar performance, while Circuit A gives greater errors because of mux and switch resistances. Moreover, Circuit A performs proportionally better for higher values of the central resistance, while the other two have lower errors for lower resistance values.

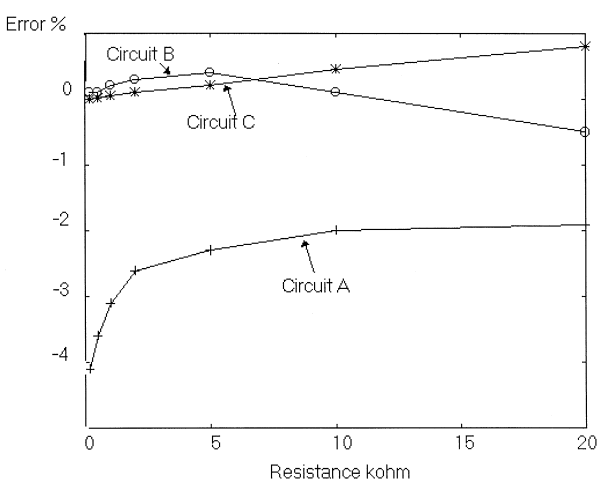


Fig. 6. Average errors of the three circuits in the reading of a central element of a 5×5 array when the resistance of the surrounding elements varies randomly in the prefixed range (200 Ω–20 kΩ).

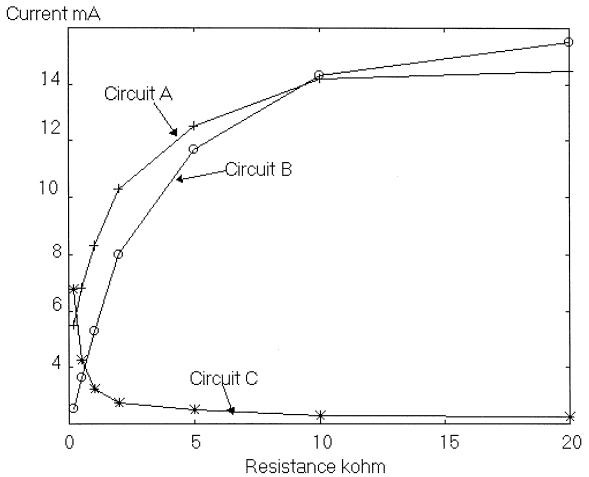


Fig. 7. Average current supplied in the three circuits by the $i$th buffer, for a 5×5 elements array and a resistance range of 200 Ω–20 kΩ. Circuit C has the lower value of the current.

The three circuits show different values for the maximum current. Fig. 7 shows that the values of the current in buffer $i$ are on average lower for Circuit C, while in Circuits A and B the $i$th buffer is more stressed.

The spread in the values of errors and currents has also been evaluated. It was found that while the ratio between the standard deviation and the mean value of the error is low (typically 1%), the currents in the three circuits show a much higher spread. Therefore, attention must be devoted to current values in practical circuits.

From other simulations, where the values of coupling resistances have been made to vary in a lower range, it emerged that errors in Circuits B and C are almost insensitive to this variation, while Circuit A shows an increase in errors. Moreover, while the current in Circuit C does not vary, currents in Circuit A and B increase by 10–15%.

For the three circuits, simulations where the mux and switches resistances are varied have been performed. It was found that Circuit A has the greatest sensitivity to these parameters. In fact, for the errors in Circuit A to be reduced below 1.5%, the mux and switches resistances have to be lower than 15 Ω, which is a value not easily found in commercial devices. Circuits B and C do not have this sensitivity because of the absence of the switch and because mux resistances are either counteracted by the presence of double mux in Circuit B or allocated after the op-amps in Circuit C.

As for complexity, Circuit A has the lowest complexity, that is $(N+1)$ op-amps and 4 mux, while the other two

have almost the same complexity, that is $(2N + 1)$ op-amps and 3 mux in Circuit B, and $2N$ op-amps and 2 mux in Circuit C.

In conclusion, each one of the three circuits can be considered as a good choice for the scanning of piezoresistive arrays, even if they show different errors and differently stress the op-amps on the rows. In any case, when piezoresistance values are higher, the errors and the currents supplied are lower. Among the three circuits, Circuit C is the most versatile with lower errors and currents, and with a performance that is less sensitive to parasitic parameters and dimensions of the array.

A choice within these three circuits can therefore be made according to the dimensions of the array, the range of resistance, the errors acceptable and the complexity of the circuits.

## 5. Conclusions

In this paper, the sources of errors in piezoresistive sensors arrays, with specific reference to errors due to crosstalk and to the scanning electronics have been discussed. These problems were previously only qualitatively dealt with in the literature. The electronic circuits reported in the literature for the scanning of the circuits have been analysed in detail and their advantages and limitations highlighted. The results presented in this paper can therefore be useful also for a choice between different circuits to be used for the scanning of piezoresistive arrays.

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