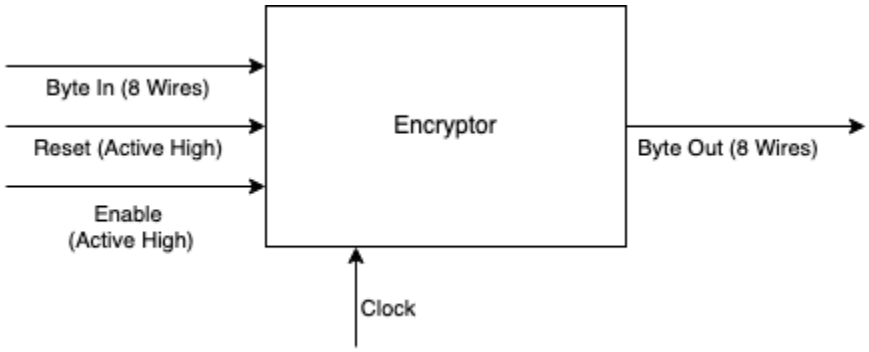
FPGA Design Document #1337-69
Reference: EoaC (Exfil-On-A-Chip) v2.0.2.3

Change Log:
28 Apr 2018 - Initial Release
11 Dec 2018 - Fixed Key Rollover Bug
30 Mar 2019 - Changed Key Values
14 Feb 2020 - Removed Encryptor Design Discussion (Need To Know Only)
25 Nov 2020 - Added Design Obfuscation

Module Design Discussion:
REMOVED

Module Block Diagram:



Verilog Module Example Instantiation:

```
reg clock;
reg reset;
reg enable;
reg [7:0] data_in;
wire [7:0] data_out;

encryptor m0 (
    .clock(clock),
    .reset(reset),
    .enable(enable),
    .in(data_in),
    .out(data_out)
);
```