A Reconfigurable Memristive Dynamic Adaptive Neural Network Array

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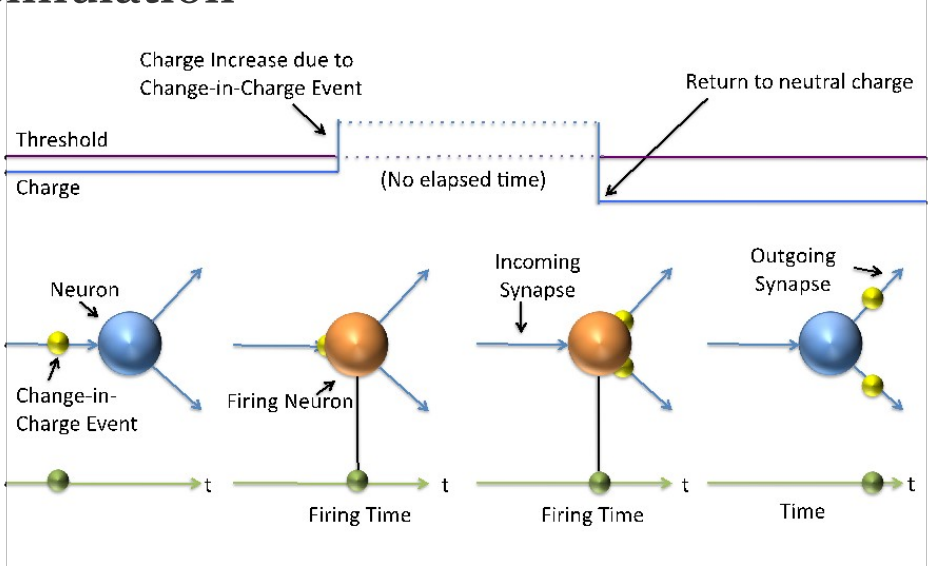
BIG ORANGE. BIG IDEAS.®

NIDA:
Neuro-Inspired Dynamic Architecture

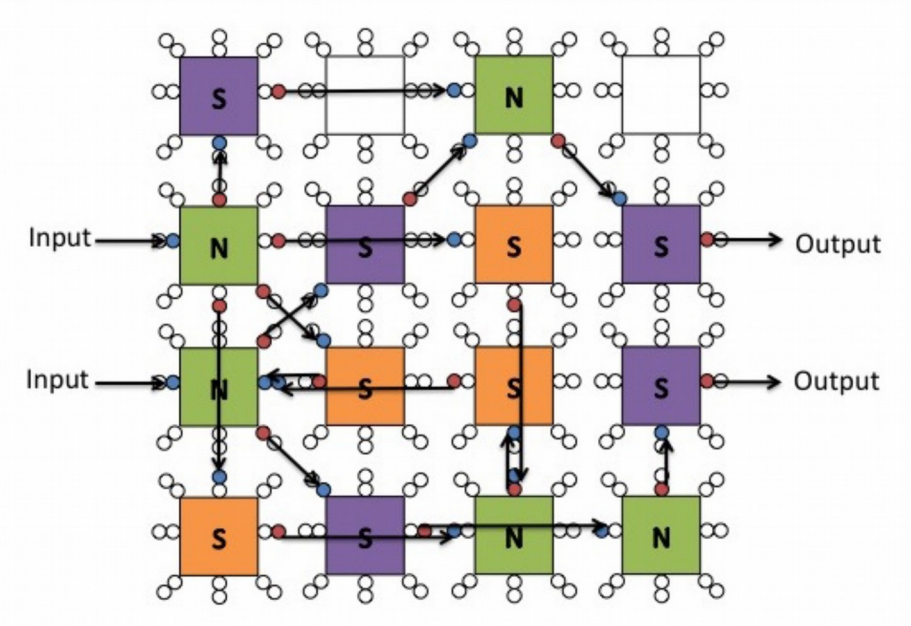
- Spiking neural network modeled in 3D space
- Simple neuron and synapse design: 2 parameters per element
- Evolutionary optimization (EO) used to *compile/synthesize* networks
- Discrete event simulation



Ref.: C. Schuman, J.D. Birdwell, and M. Dean, "Neuroscience-Inspired Dynamic Architectures," BSEC, 2014.

Dynamic Adaptive Neural Network Array (DANNA)

- Array of programmable neural network elements
- Each element can be connected to up to 16 other elements
- Have implemented using FPGA
- Hardware-accurate simulator available – used for offline evolutionary optimization



Ref.: M. Dean, C. Schuman, and J.D. Birdwell, “Dynamic Adaptive Neural Network Array,” Springer, 2014.

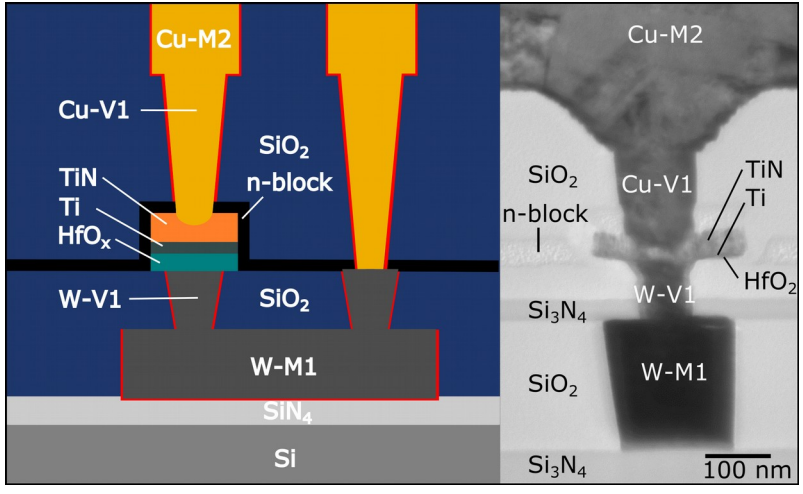
Toward a Memristive DANNA (mrDANNA)

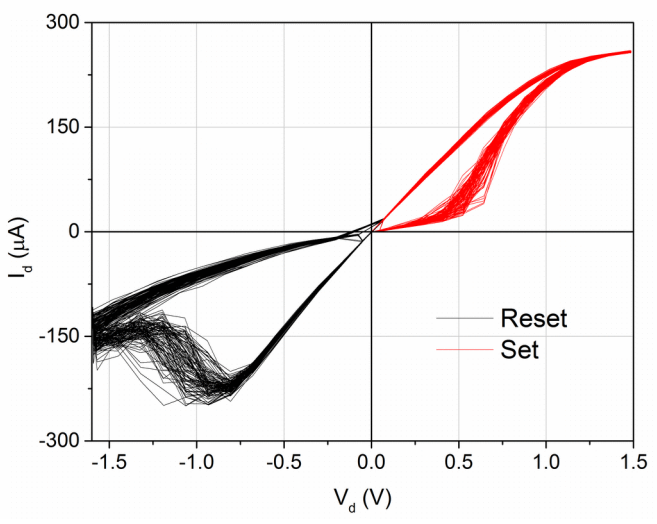
- Maintain salient features of NIDA/DANNA architecture:
  - Configurable hardware: structure & weights optimized offline
  - Dynamic adaptation via LTD/LTP mechanism
  - Simple neuron and synapse design
    - Neurons: programmable threshold & refractory period
    - Synapses: programmable delay & synaptic weights
- Leverage metal-oxide memristors for synapses
  - High density synaptic arrays
  - Potential for low-power operation

Goal: A memristor-based neuromorphic system with reconfigurable structure, parameter initialization and dynamic adaptability.

Hafnium-Oxide Memristors

- SUNY Polytechnic—CNSE fabricating HfO_2 memristors
- Complete hybrid CMOS/memristor process
  - Memristors in via layer between metal1 and metal2

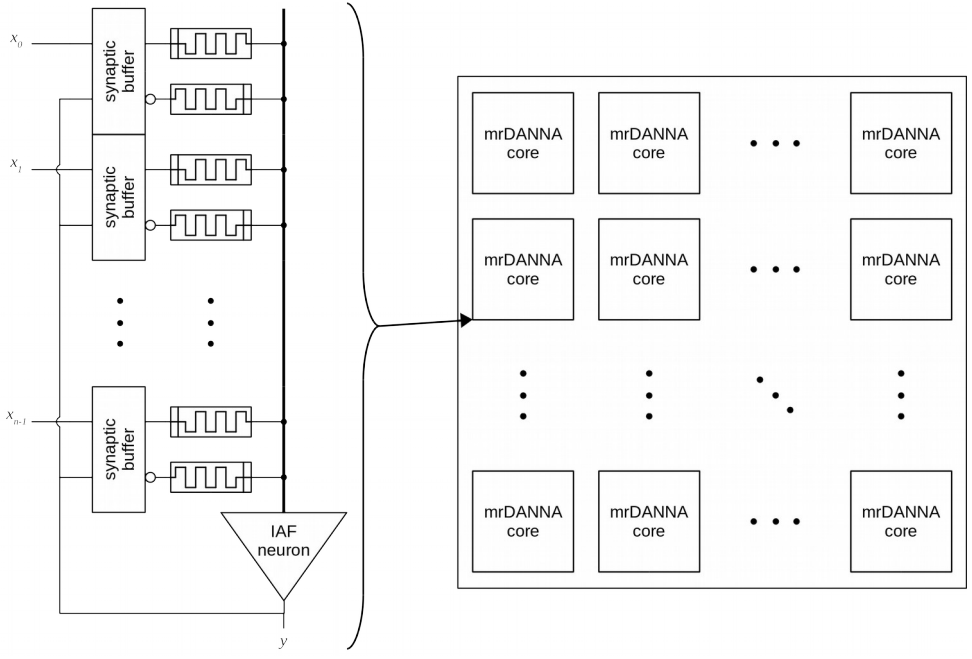




Ref.: N. Cady, et al., "Towards Memristive Dynamic Adaptive Neural Network Arrays," GOMAC, March 2016.

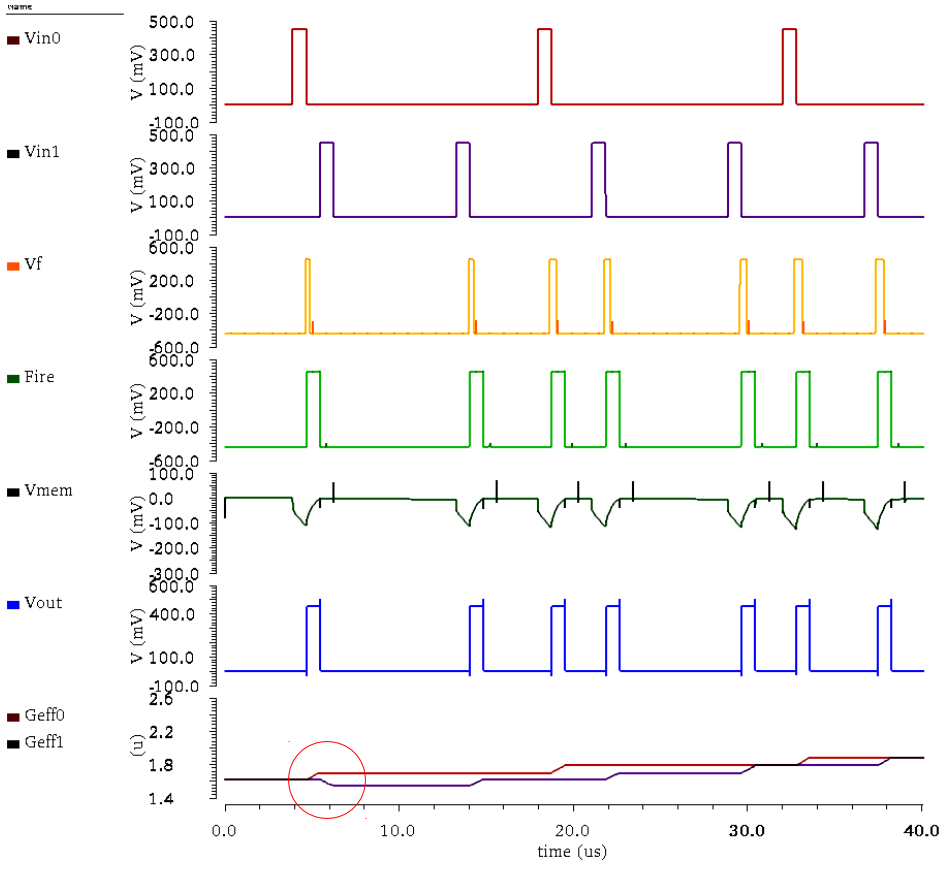
mrDANNA Circuit Elements

- Memristor pairs implement synaptic weights
  - weight proportional to effective conductance of pair
- Synaptic buffers provide delay and complementary drive signals for memristor pairs
- Integrate & fire (IAF) neurons
- Feedback from IAF neurons to synaptic buffers used for on-chip adaptation



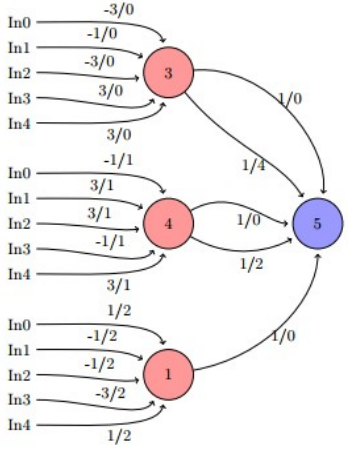
LTP and LTD in mrDANNA System

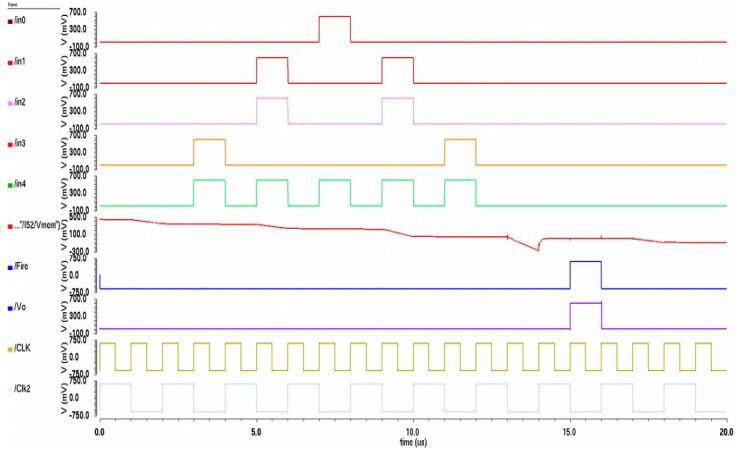
- Implemented NIDA rule for LTP/LTD
- LTP: Increase weight for synapse causing a post-synaptic neuron firing event
- LTD: Decrease weight for synapse that fires simultaneous to post-synaptic neuron firing event
- Integrate & Fire neurons – integrates until threshold reached, charge resets upon firing event

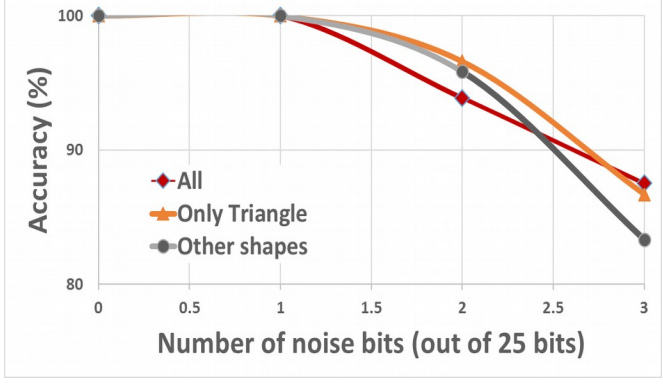


Simulation Results

- Each column of weight matrix denotes the weights of each neuron
- Optimization of number of neurons reduces the structure complexity
- Threshold calculation consistent with maximum and minimum synaptic weights







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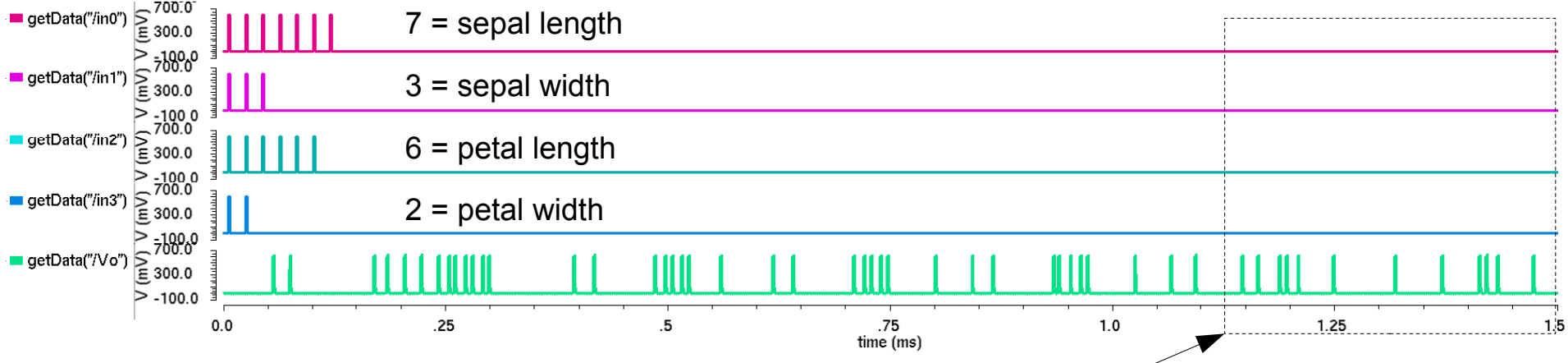
Spike Encoding – Iris Dataset Example

- Simulated NIDA Iris network translated to mrDANNA
  - Length and width values rounded up for this example
- Example shown: Result identifying versicolor Iris



12 fires in final 50 cycles
versicolor (type 1)

Concluding Thoughts

- Build better understanding of constraints for memristive circuits
  - Guide algorithmic refinement
- Hardware interfaces and software
  - Developing FPGA-based DANNA in parallel – improved interfaces
  - Evolutionary optimization used to *compile* or *synthesize* networks
  - mrDANNA model and simulator – used for verification & EO
  - Commander and other tools for interfacing with the system
- Strike a balance: offline network initialization vs. online training
- Will fabricate mrDANNA test chip in collaboration with AFRL & CNSE

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