Digital Design Project

QUESTION 1a

ASHISH BAGHUDANA 2011B1A7575G

ANSHU AVIRAL 2011B5A7289G

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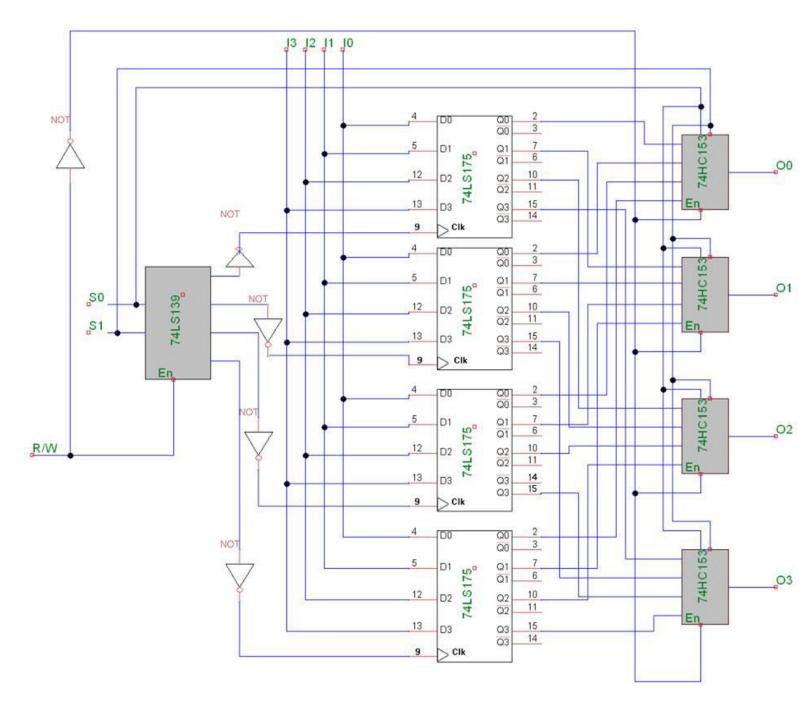
SAJIDUR RAHAMAN 2011B5A7496G

B.N.M. PREETAM 2011B5A7501G

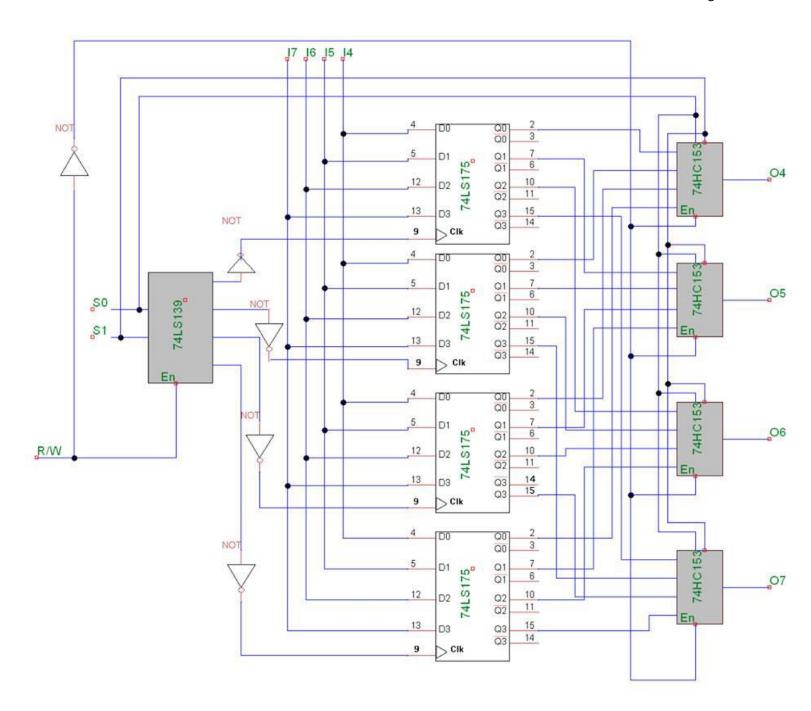
ABHISHEK DESAI 2012A7B4065G

Two 4X4 Memory Blocks

Circuit Diagram:



Block - 1



Block - 2

ICs used (Total circuit):

8 X 74LS175 Quad-D flip-flops (Pos. edge triggered)

4X74HC153 Dual 4to 1 multiplexer

1 X 74LS139 2 X4 Decoder

1X 7404 Hex inverter

(Note: Decoder, multiplexer and inverter ICs are common in both the blocks. Separate D flip-flop ICs are used for different blocks.)