

TITLE	Page
Cover Sheet Block Diagram	1,2
CPU-Memory	3,
CPU-Control/MISC/CFG/Audio	4
CPU-PEG/Display/GND/POWER	5,6,7
DDR4 Slot-DIMM1~4, POWER/GND	8,9,10,11
PCH-Audio/Display/Clock	12
PCH-USB/PCIE/DMI/SATA	13
PCH-GPIO/USB OC#/SATASTRAP	14
PCH-LPC/SPI/SMBUS/MISC	15
PCH-Power/GND/Strap	16,17,18
PCI E Slot-X16/X1/X4/X8	19,20,21,22
SATA Connector	23
M.2 Card SLOT	24
USB POWER/USB2.0/PS2/USB3.0/TYP E C	25,26,27,28,29
LAN RTL8111H	30
VGA/DVI/HDMI Connector	31,32,33
AUDIO ALC1150	34,35
SIO-NTC6793D	36,37
CPU FAN &SYS FAN	38,39
ATX Power/F_Panel	40
ACPI-UPI Power	41
OV-NCT3933	42
+12VIN/VRM_EN&PGD	43
PWM-ISL95856 V CORE+VGT	44
V CORE MOS-PHASE 1~4,VGT 1!3	45,46,47
CPU PWR_VCCIO/ST/PLL/SA	48,49,50
DDR4 Power/Vpp25	51,52
PCH Core Power-UP1540Q	53
BIOS &Clear CMOS	54
Manual parts	55

# MS-7998

ATX  
Ver: 1.1

## Intel -Skylake plamform Z170 /C236

### CPU:

Skylake-S

### System Chipset:

Z170 Colay C236

### Onboard Chip:

HD Audio Codec:ALC1150

LAN:RTL8111H

SIO:Nuvoton 6793D

Flash ROM: SPI 128MB

### Main Memory:

DDRIV (800/1066/1333/1600/2133MHz) \* 4 (Dual Channel)

### ACPI:

NIKO/UPI

### PWM:

RT3606BC

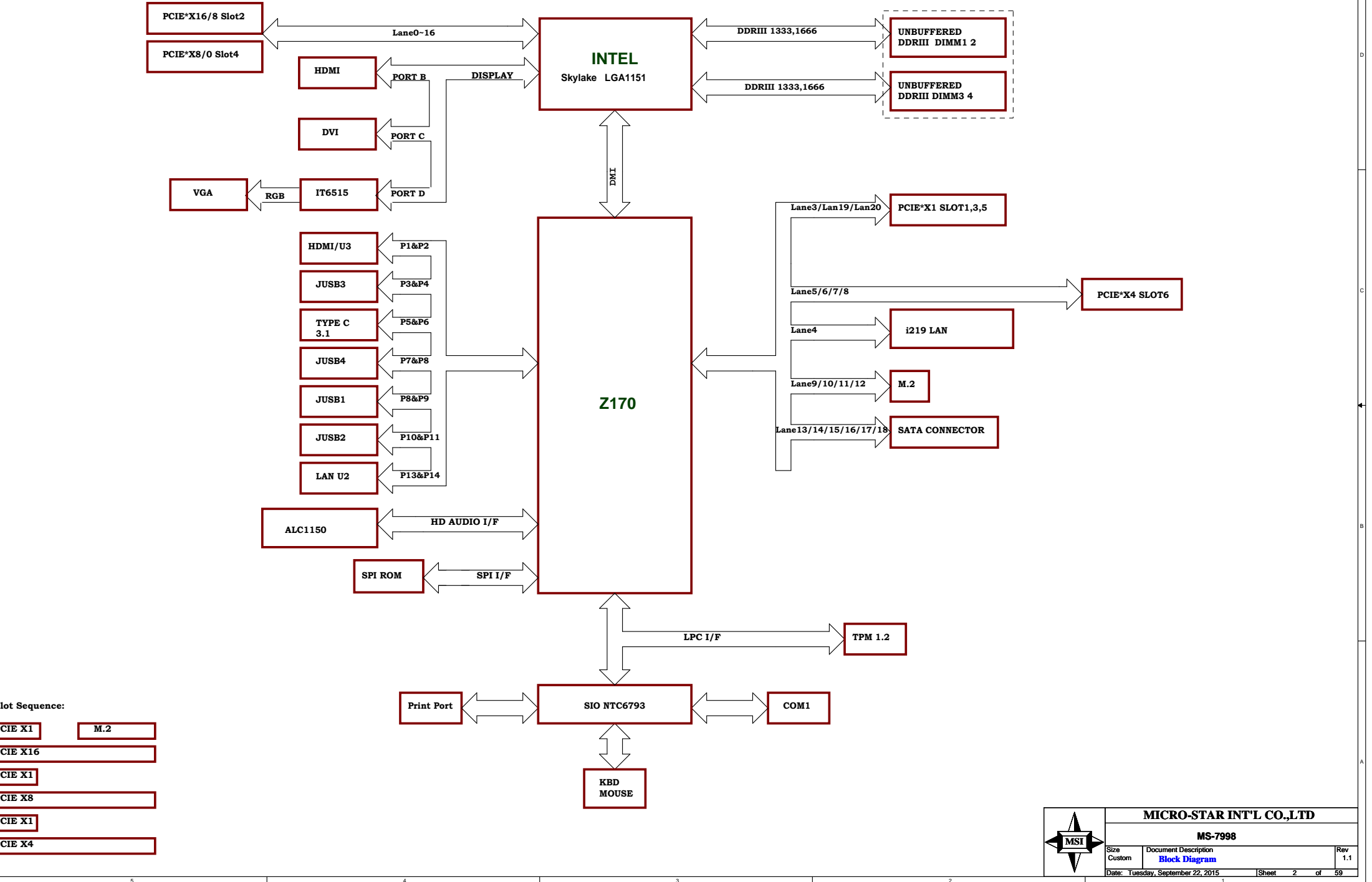
### Expansion Slots:

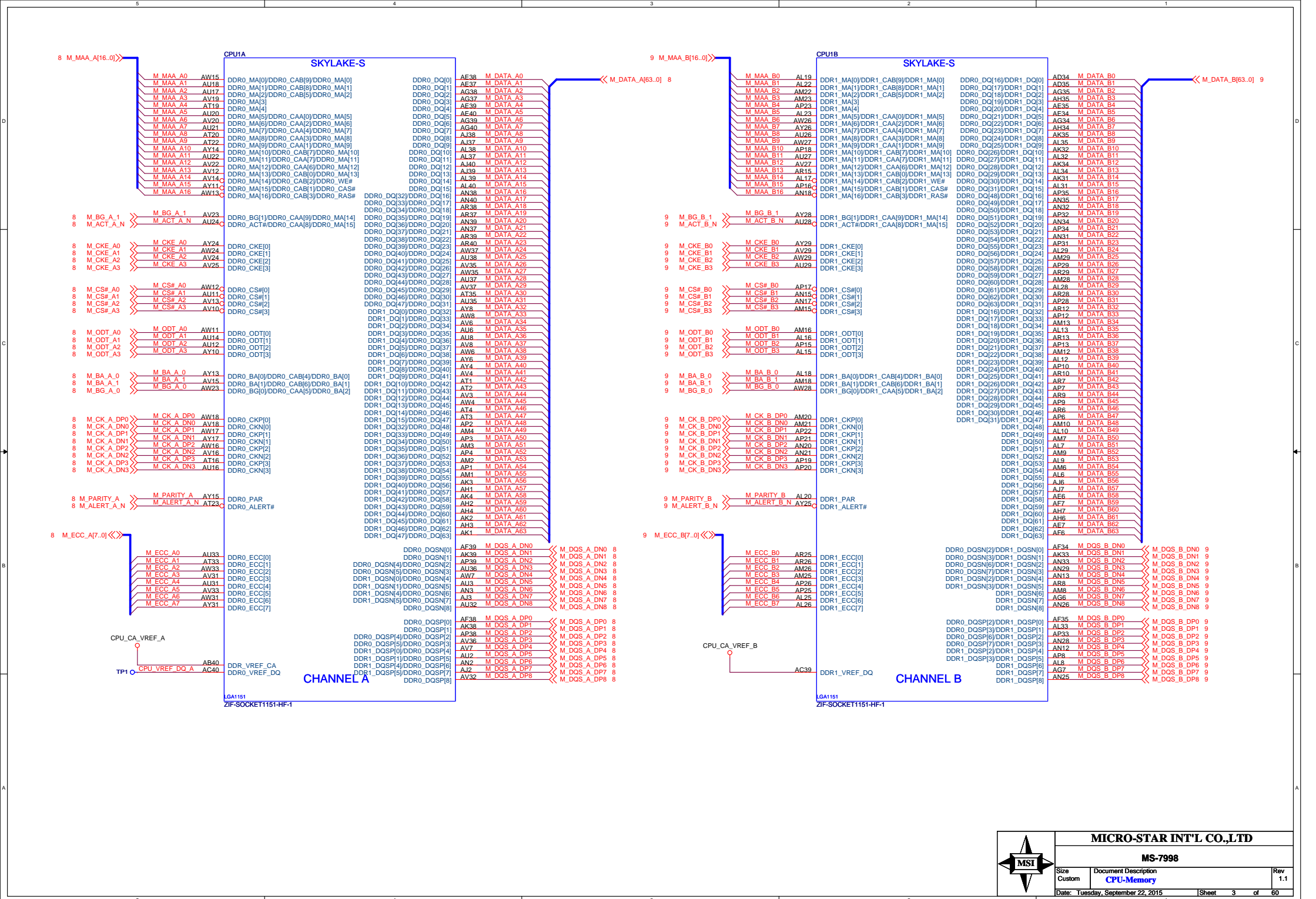
PCI Express (X16) Slot \*1  
PCI Express (X8) Slot \*1  
PCI Express (X4) Slot \* 1  
PCI Express (X1 ) Slot \* 3  
M2 \* 1

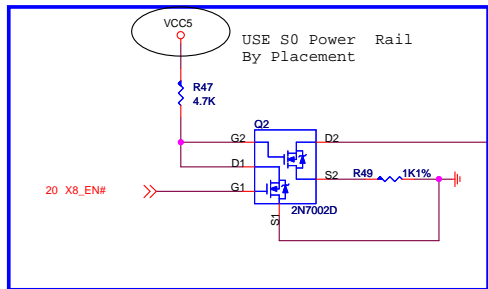
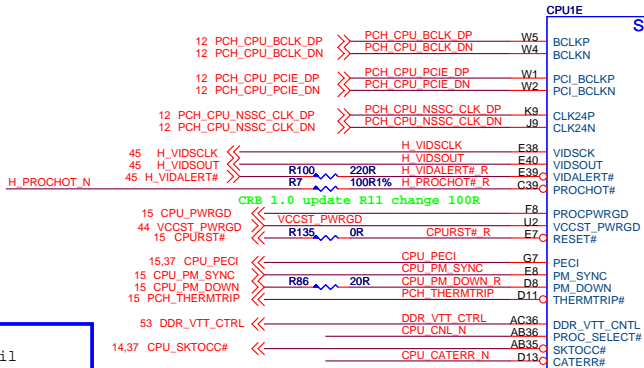
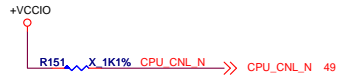
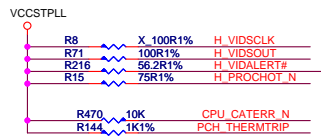
### Other:

SATA3.0 x6 (PCH)  
FRONT USB2.0 \*4  
FRONTUSB3.0 \*4  
REAR USB3.0 \*4  
REAR USB2.0 \*2

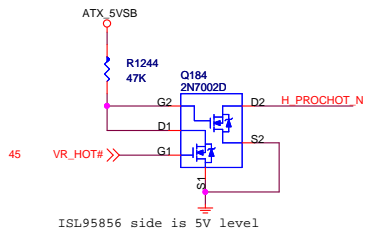
MS-7998 Block Diagram



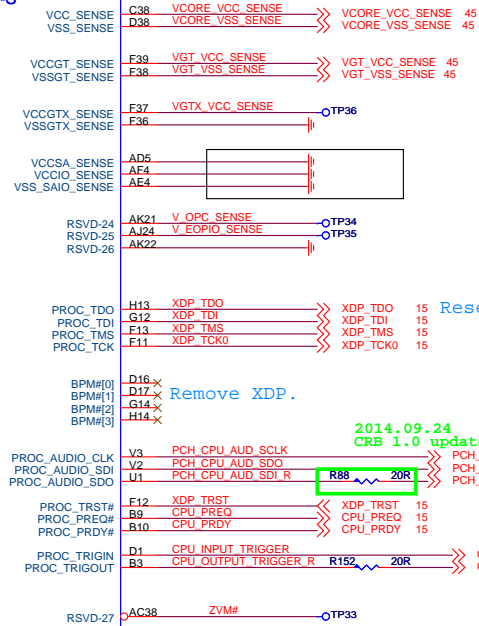




X8 Ctrl		
ENABLE#	SLOT2	SLOT4
0	X8	X8
1	X16	X0



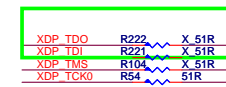
SKYLAKE-S



## CFG Strap

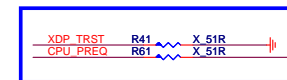
CFG Table			
	HIGH	LOW	DESCRIPTION
0	No Lock	Lock	PCU PLL lock
1		RSVD	RSVD
2	NORM	REVERSE	PEG_LANE_REVERSAL
3		RSVD	RSVD
4	DISABLE	ENABLE	eDP
5	DISABLE	ENABLE	PEG0CPGSEL[0]
6	DISABLE	ENABLE	PEG0CPGSEL[1]
7	RESET#	BIOS REQ	PEG_DEFER_TRAINING
8		RSVD	RSVD
9		RSVD	RSVD
10		RSVD	RSVD
11		RSVD	RSVD
12		RSVD	RSVD
13		RSVD	RSVD
14	RSVD		RSVD
15	RSVD		RSVD

2014.09.29 remove



Close CPU <1100 mil

1000 mil < CPU\_XDP\_MBP0~1 < 6000 mil



Reserve for DCI.

2014.09.24  
CRB 1.0 update R29 change 20R



- CFG[0]
- CFG[1]
- CFG[2]
- CFG[3]
- CFG[4]
- CFG[5]
- CFG[6]
- CFG[7]
- CFG[8]
- CFG[9]
- CFG[10]
- CFG[11]
- CFG[12]
- CFG[13]
- CFG[14]
- CFG[15]

- CFG[17]
- CFG[16]
- CFG[19]
- CFG[18]

CFG\_RCOMP

LGA1151  
ZIF-SOCKET1151-HF-1

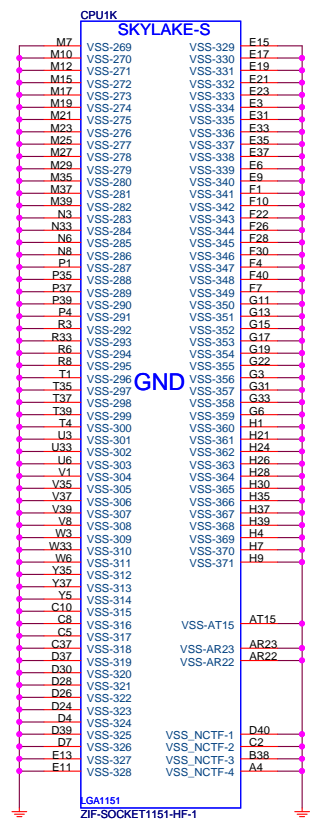
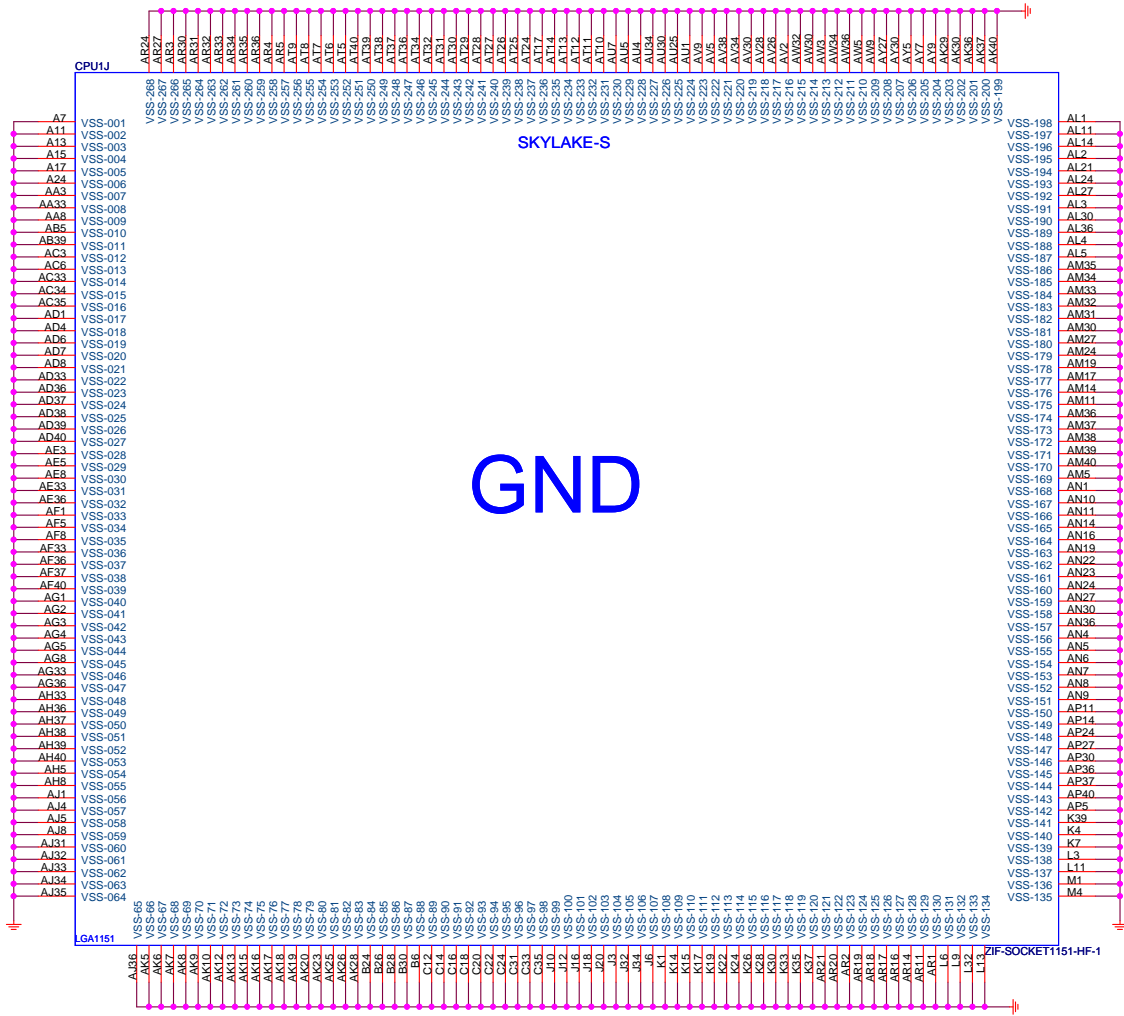


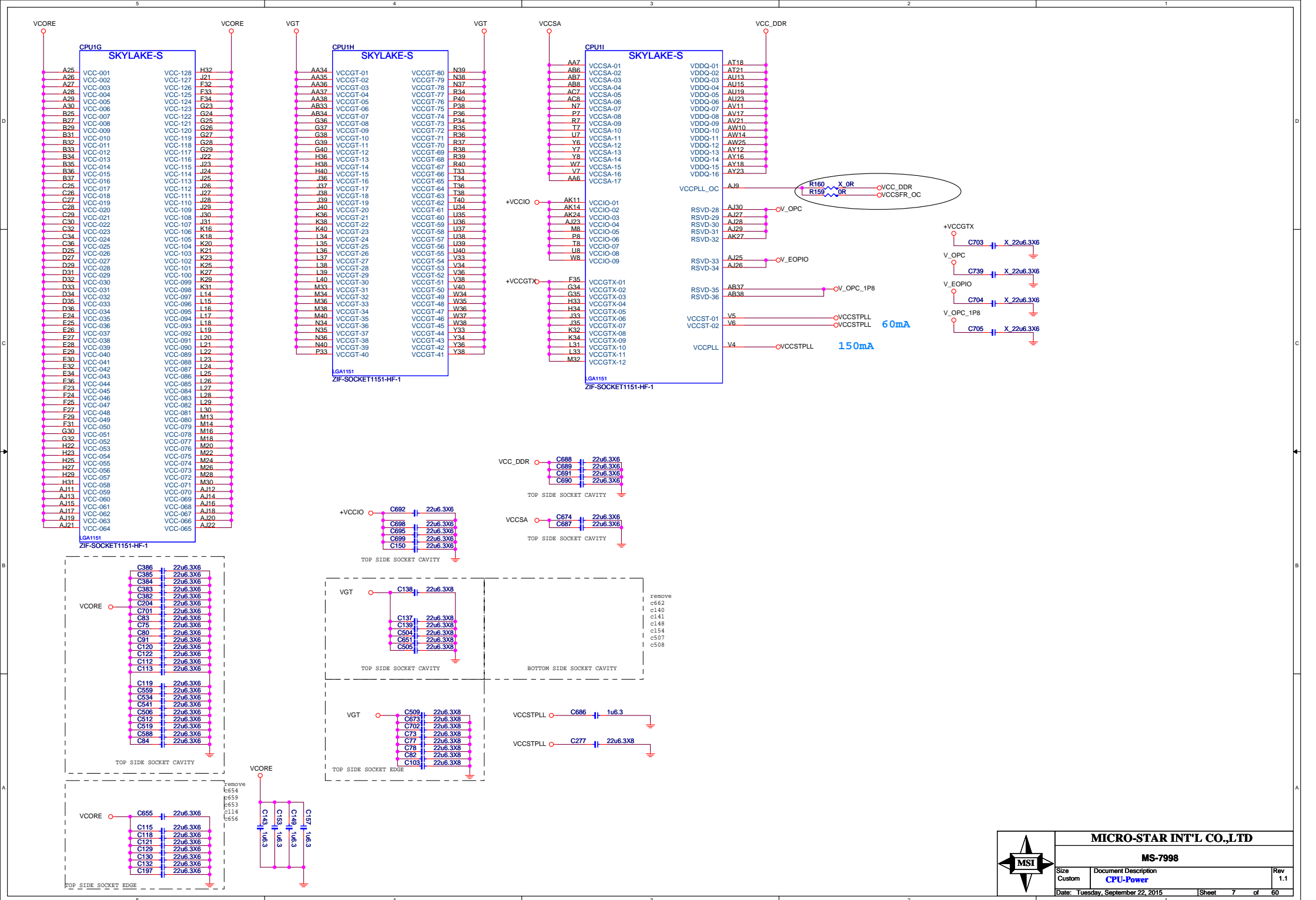
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MS-7998

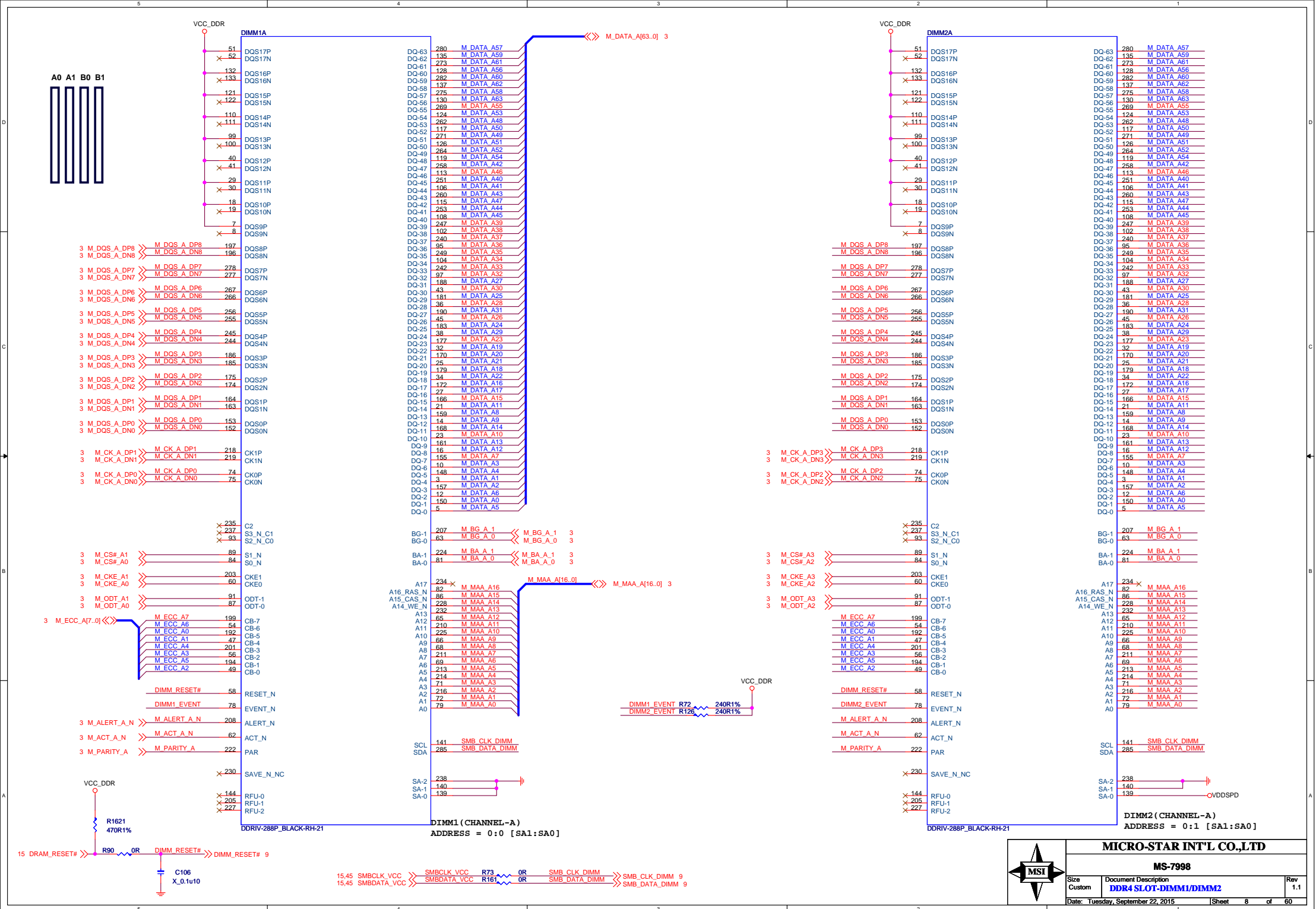
Size	Document Description	Rev
Custom	CPU-Control/MISC/CFG/Audio	1.1
Date:	Tuesday, September 22, 2015	Sheet 4 of 60



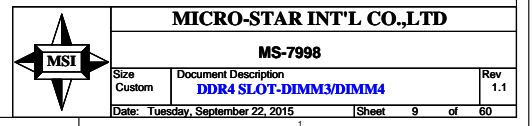


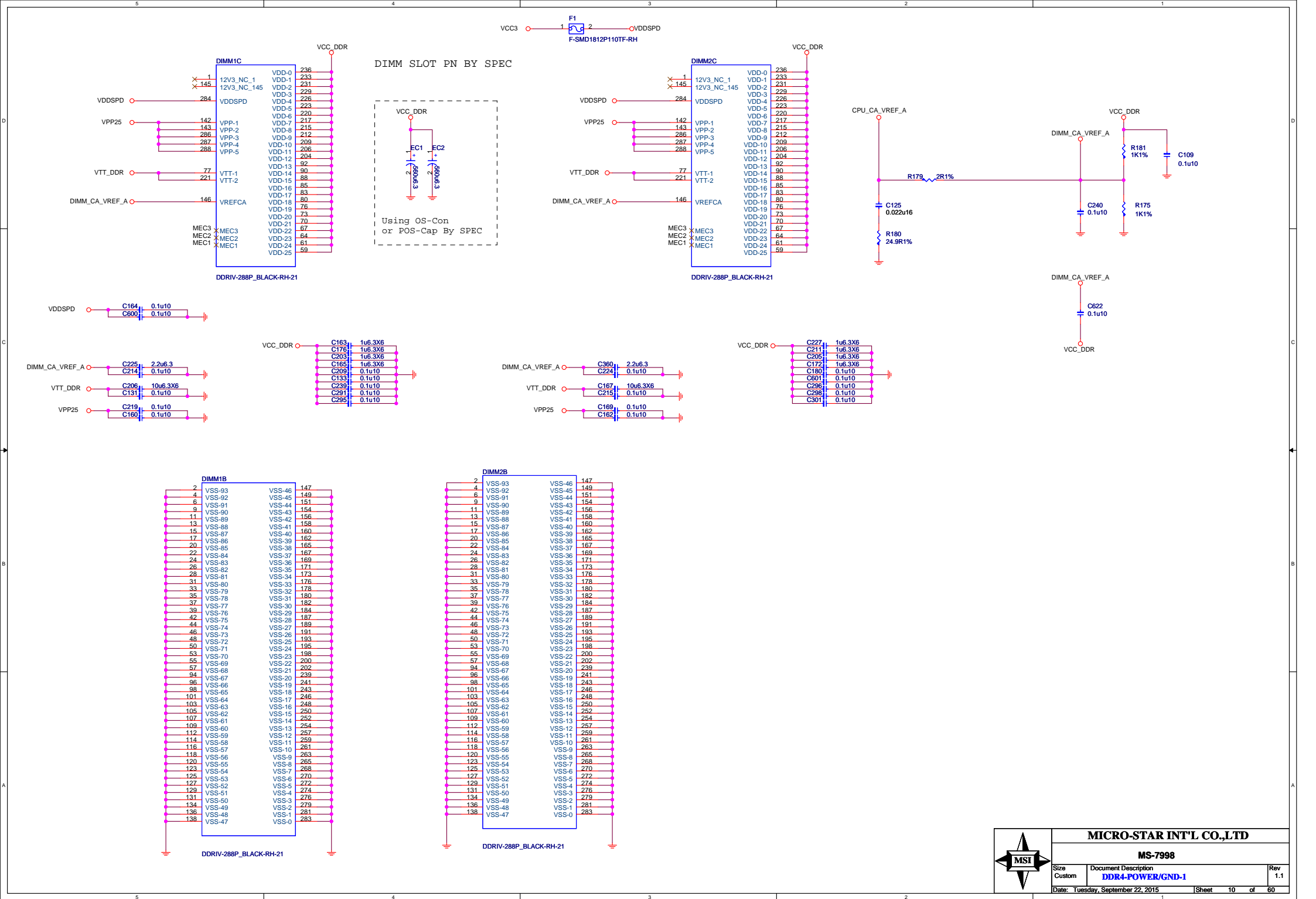


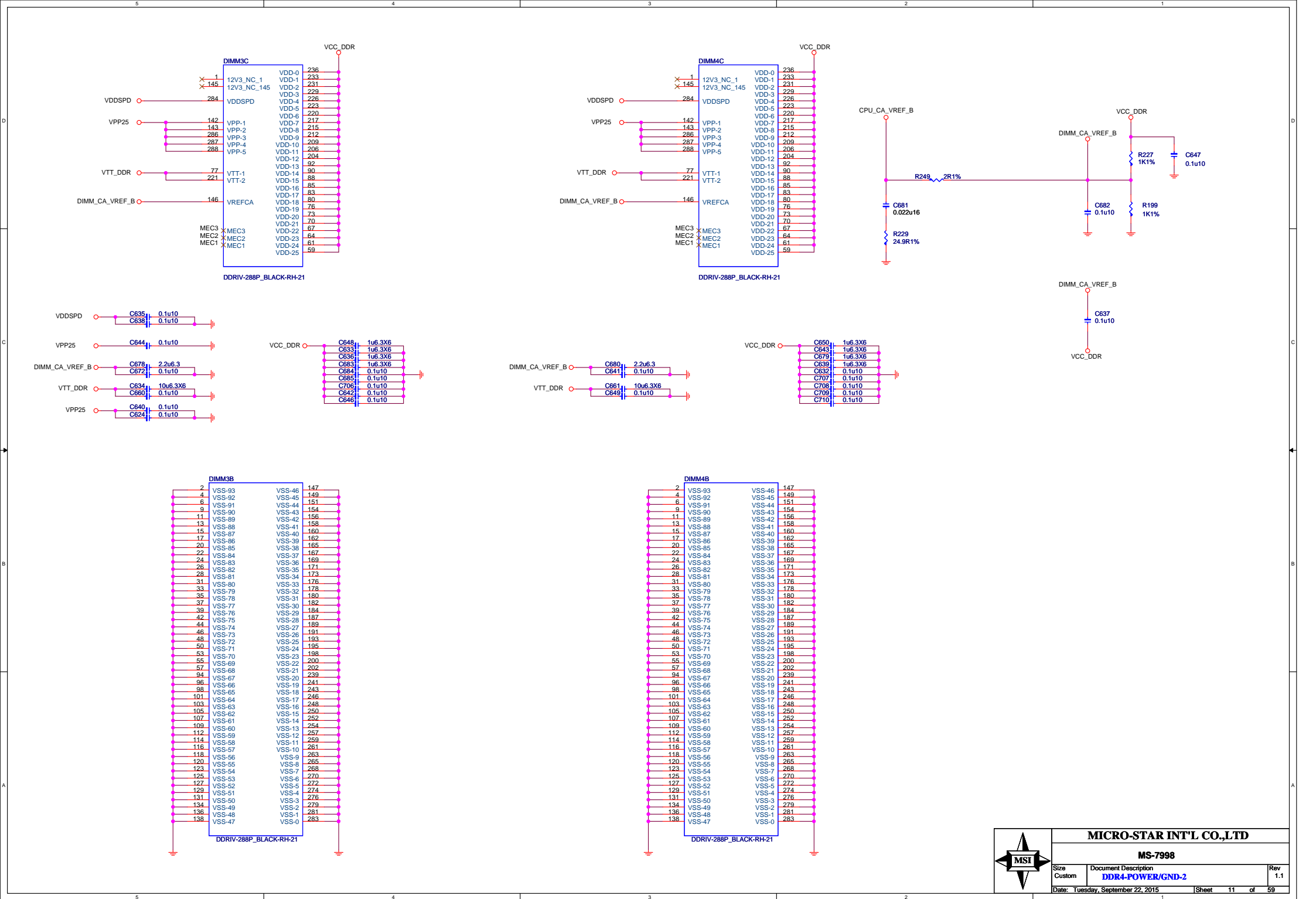


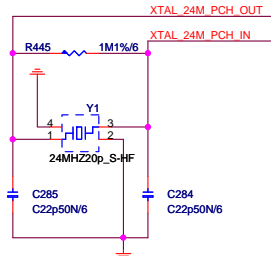
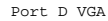


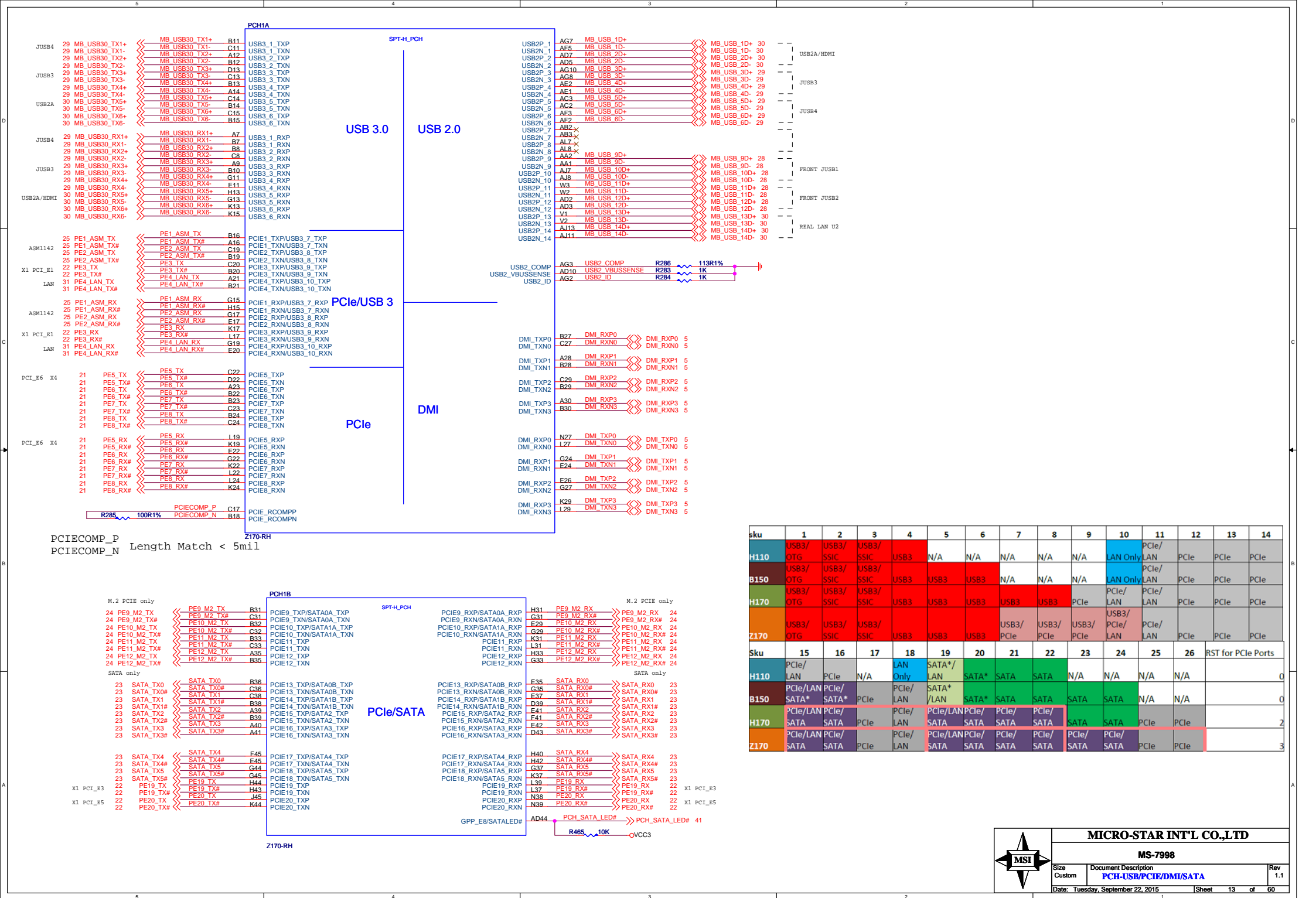






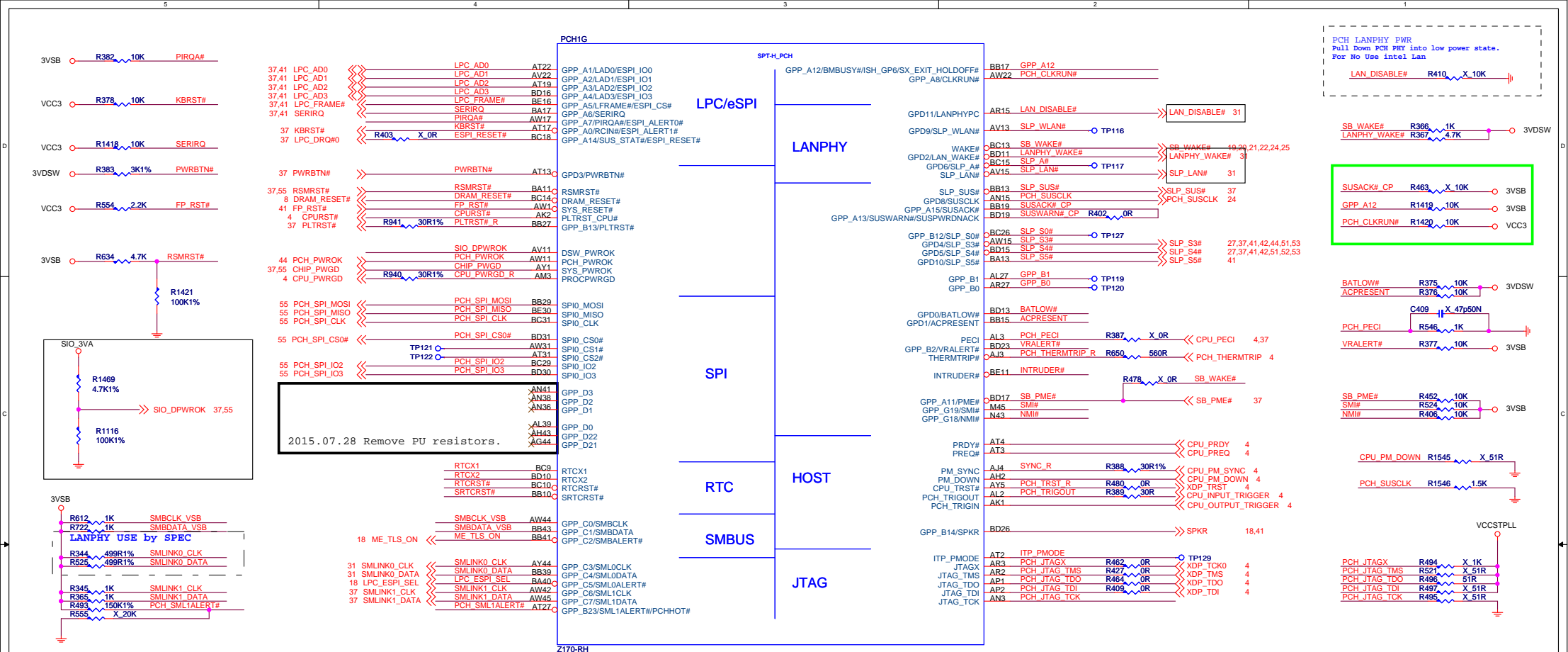




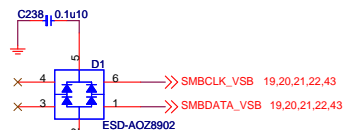








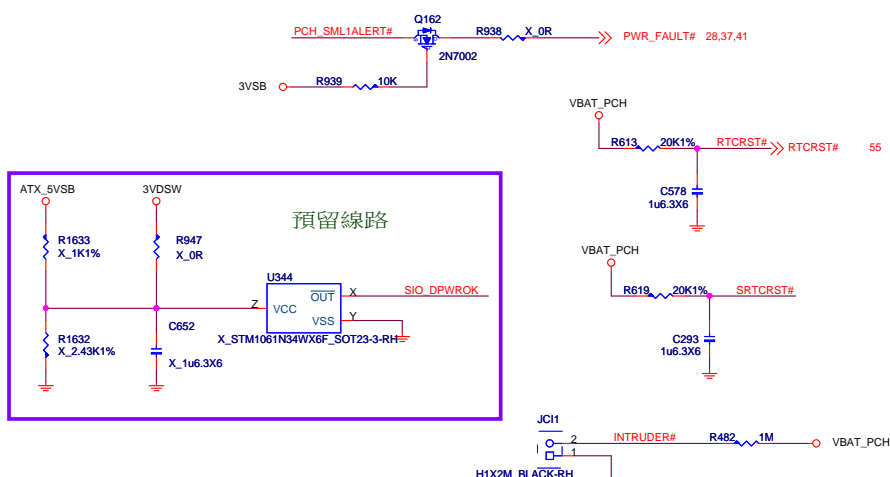
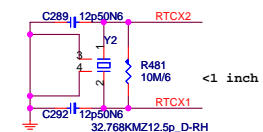
## SMBUS ESD



By Placement

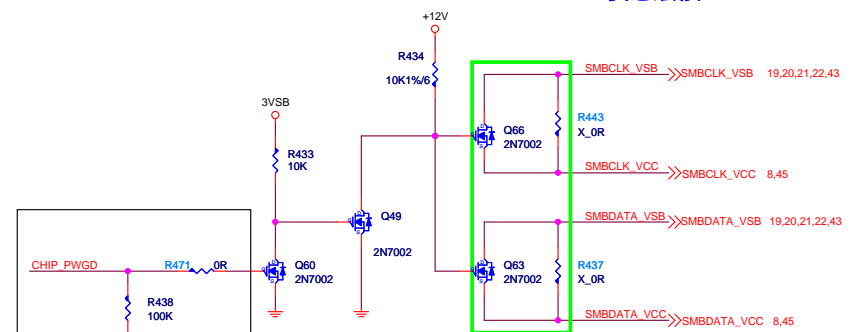
## RTC Block

Close to PCH



SMBUS隔離線路(PCH接出來是PULL HIGH 3VSB)  
需要再S3/S5底下動作的接SMBCLK\_VSB/SMBDATA\_VSB  
不需要的接SMBCLK\_VCC/SMBDATA\_VCC

基本上PCIE的SLOT要接  
3VSB的,CPU的PWM IC/DDR  
要接VCC3的其他的請注意  
要怎麼接

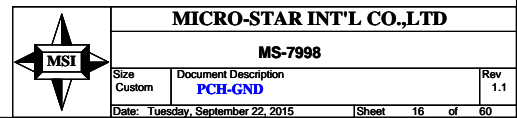


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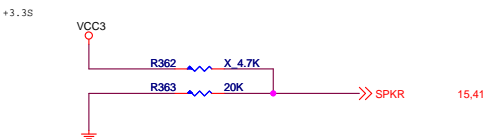
Size	Document Description	Rev
Custom	PCH-LPC/SPI/SMBUS/MISC	1.1
Date: Tuesday, September 22, 2015	Sheet 15 of 60	





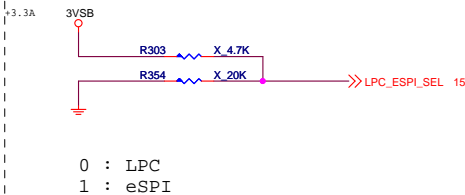


# TOP Swap



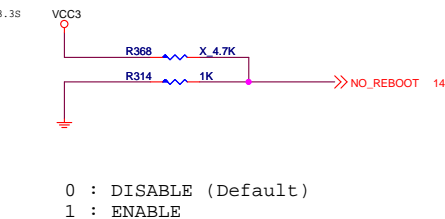
Internal pull-down is disabled after PLTRST#

# LPC eSPI Mode



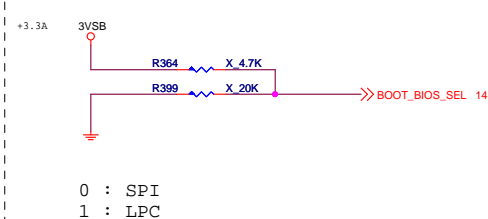
Internal pull-down is disabled after RSMRST

# No Reboot



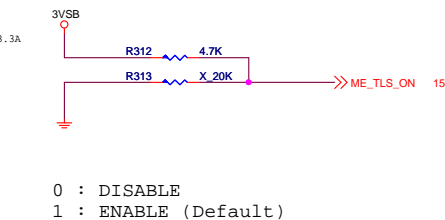
Internal pull-down is disabled after PLTRST#

# Boot BIOS



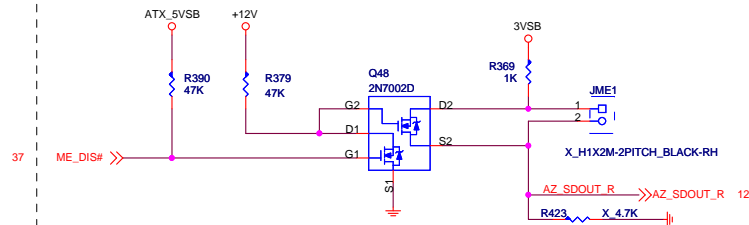
Internal pull-down is disabled after PLTRST#

# AMT and SBA with confidentiality

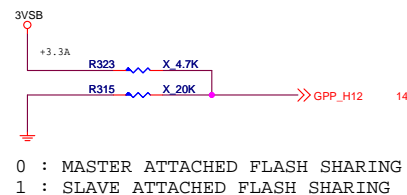


Internal pull-down is disabled after RSMRST

# HDA\_SDO



# ESPI FLASH SHARING MODE



Internal pull-down is disabled after RSMRST

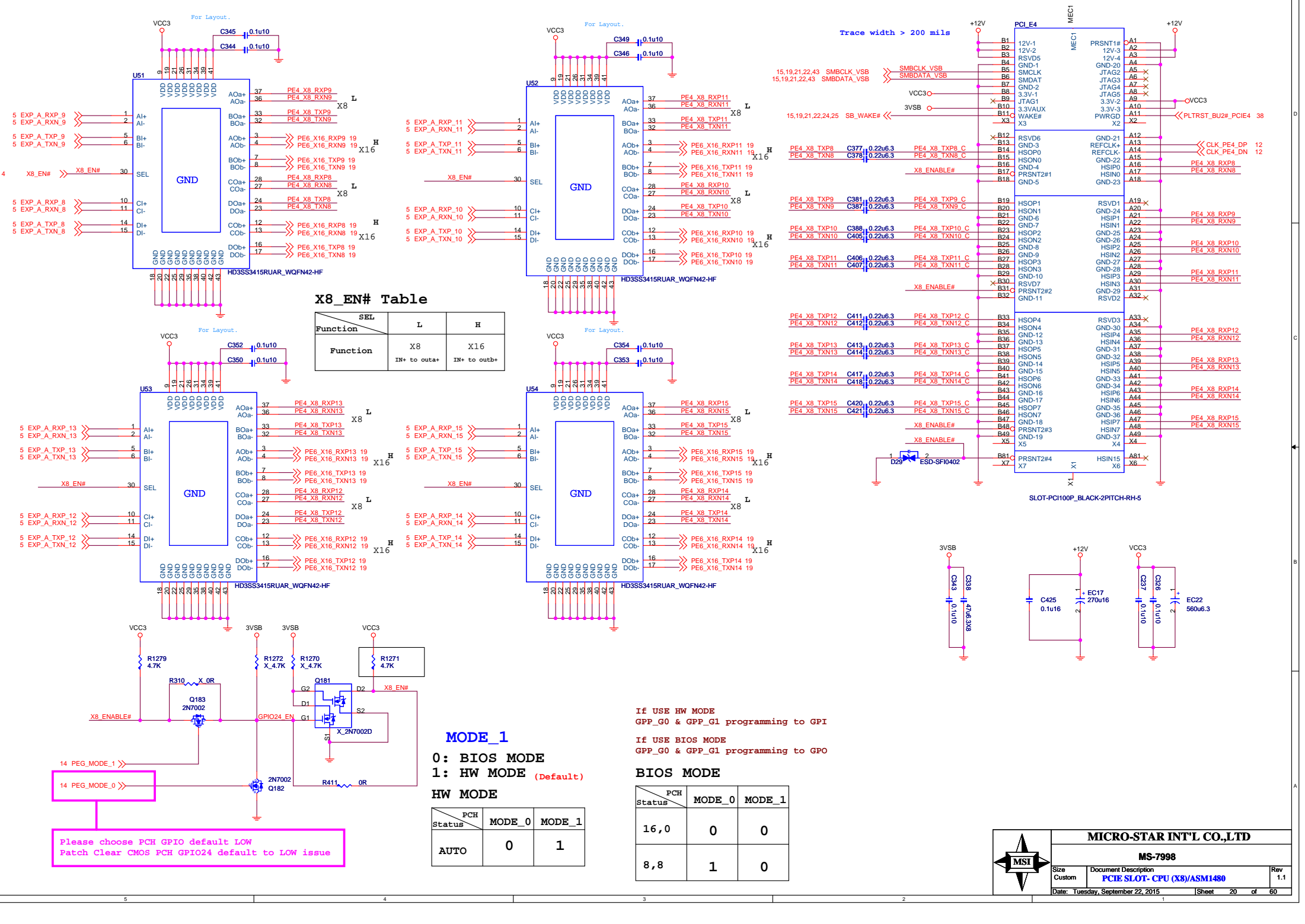


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MS-7998

Size	Document Description	Rev
Custom	PCH-Strap	1.1
Date: Tuesday, September 22, 2015	Sheet 18 of 60	





X8\_EN# Table

Function	SEL	L	H
Function		X8	X16
		IN+ to outa+	IN+ to outb+

MODE\_1  
0: BIOS MODE  
1: HW MODE (Default)

PCH Status	MODE_0	MODE_1
AUTO	0	1

If USE HW MODE  
GPP\_G0 & GPP\_G1 programming to GPI  
  
If USE BIOS MODE  
GPP\_G0 & GPP\_G1 programming to GPO

PCH Status	MODE_0	MODE_1
16,0	0	0
8,8	1	0

Please choose PCH GPIO default LOW  
Patch Clear CMOS PCH GPIO24 default to LOW issue

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**MS-7998**

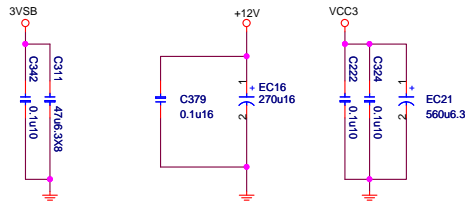
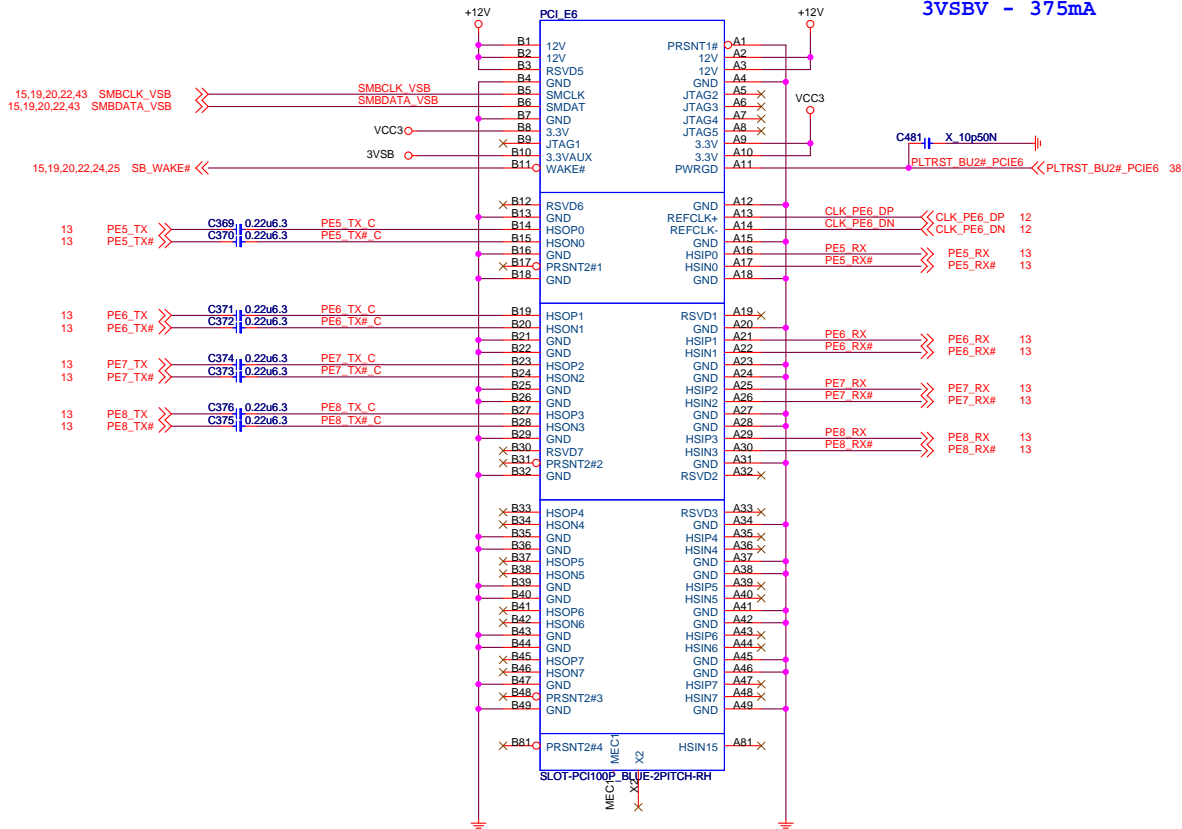
Size Custom	Document Description <b>PCIe SLOT- CPU (X8)/ASM1480</b>	Rev 1.1
Date: Tuesday, September 22, 2015	Sheet 20	of 60

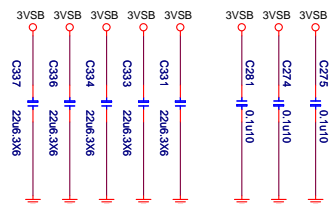
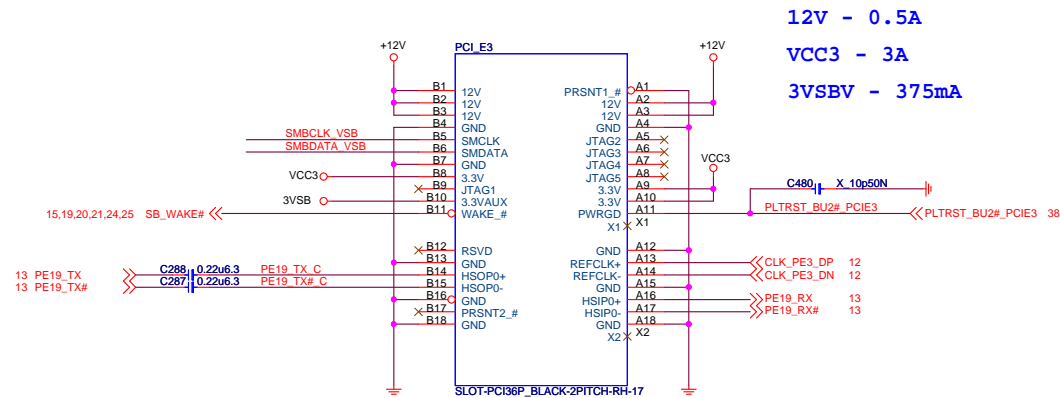
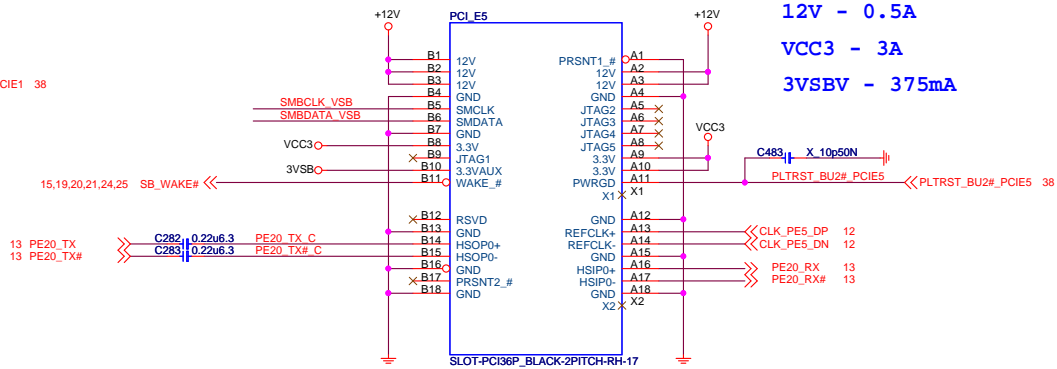
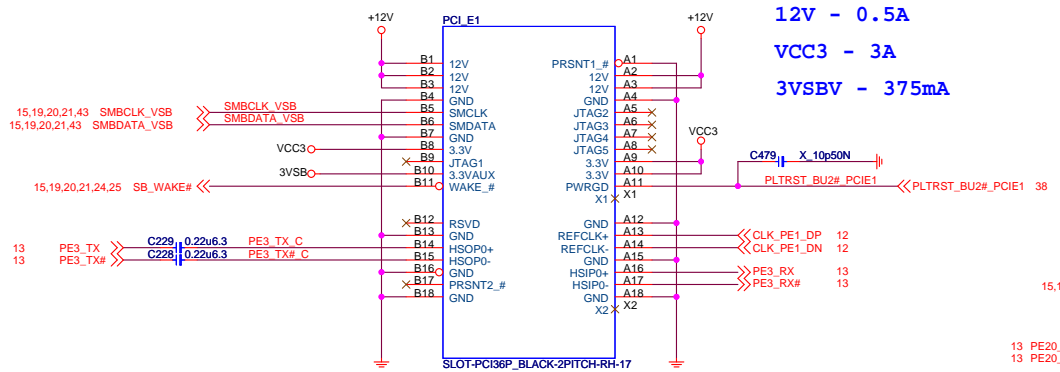
# PCI\_Express X4 Slot

12V - 2.1A

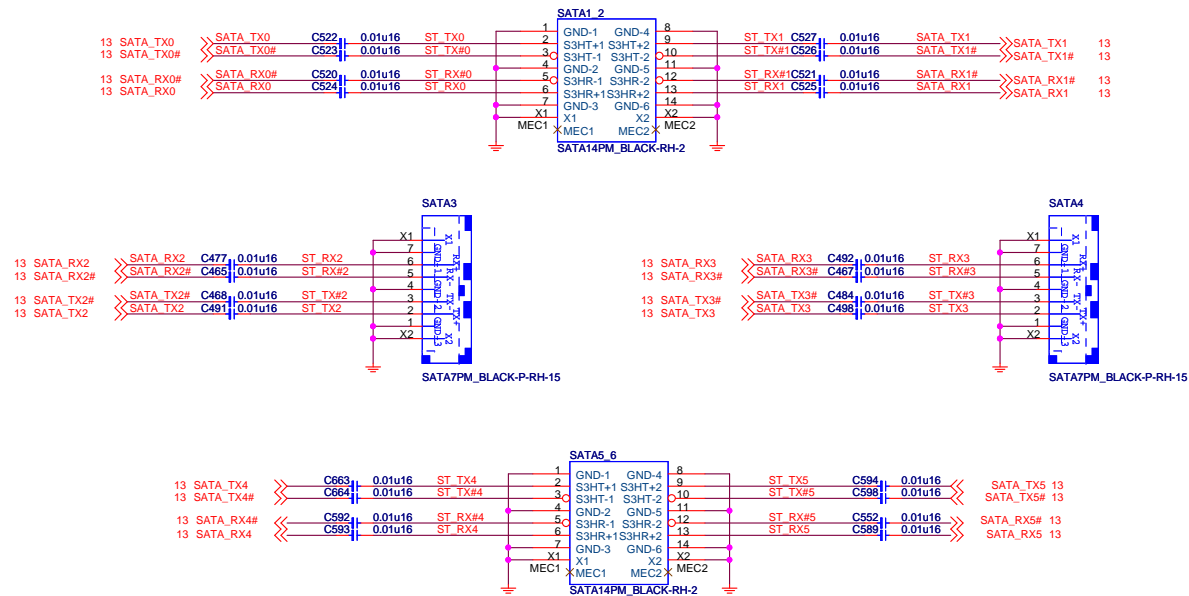
VCC3 - 3A

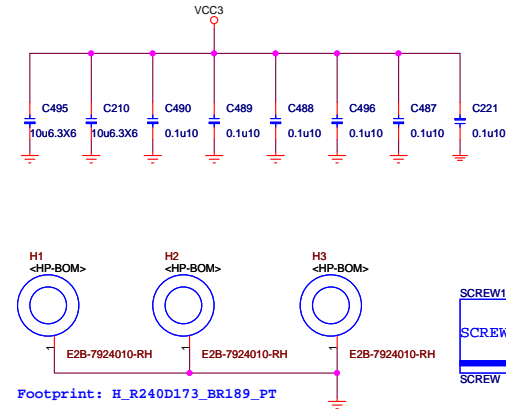
3VSBV - 375mA



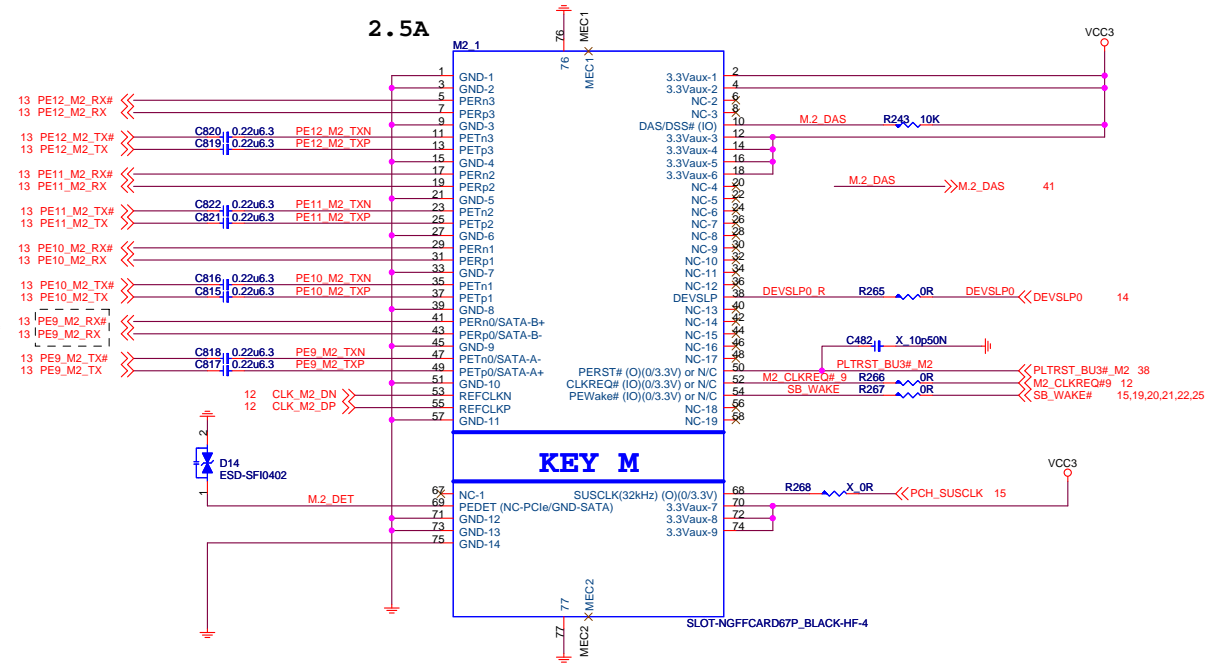








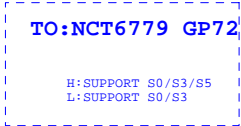
SATA 要反接



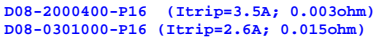




## USB PORT POWER



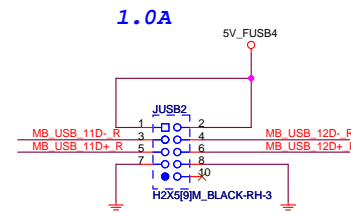
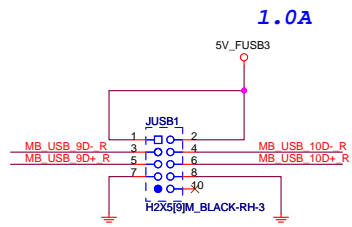
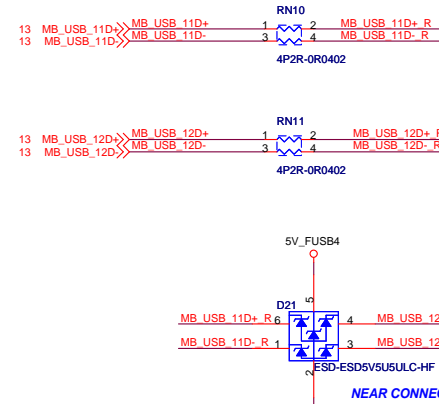
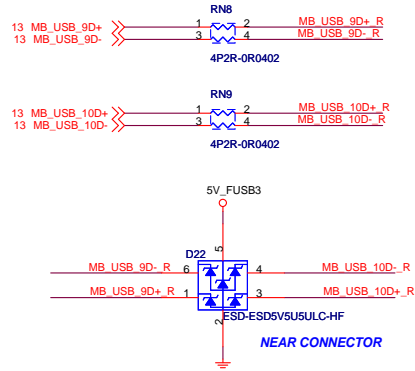
5VDRV2, 5VSBDRV2 width 12mil,  
Do NOT route near the edge of a board.



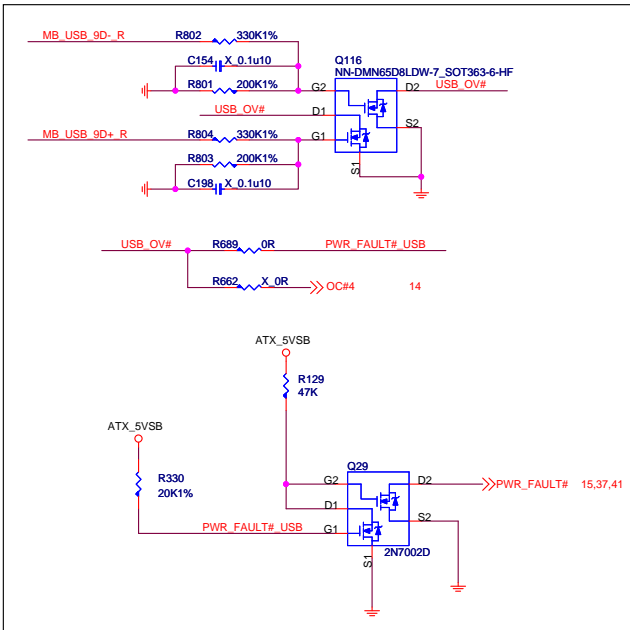
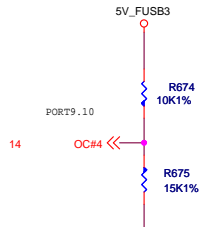
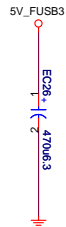
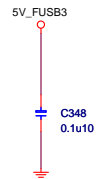
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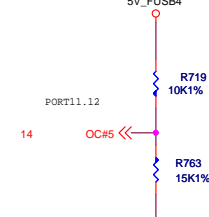
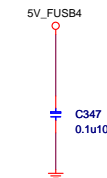
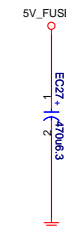
Size Custom	Document Description <b>USB POWER UP7501</b>	Rev 1.1
Date: Tuesday, September 22, 2015		Sheet 27 of 60



EMI Cap near Connector.



EMI Cap near Connector.



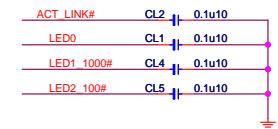
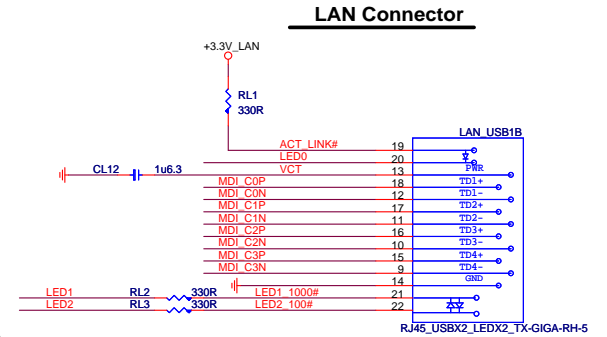
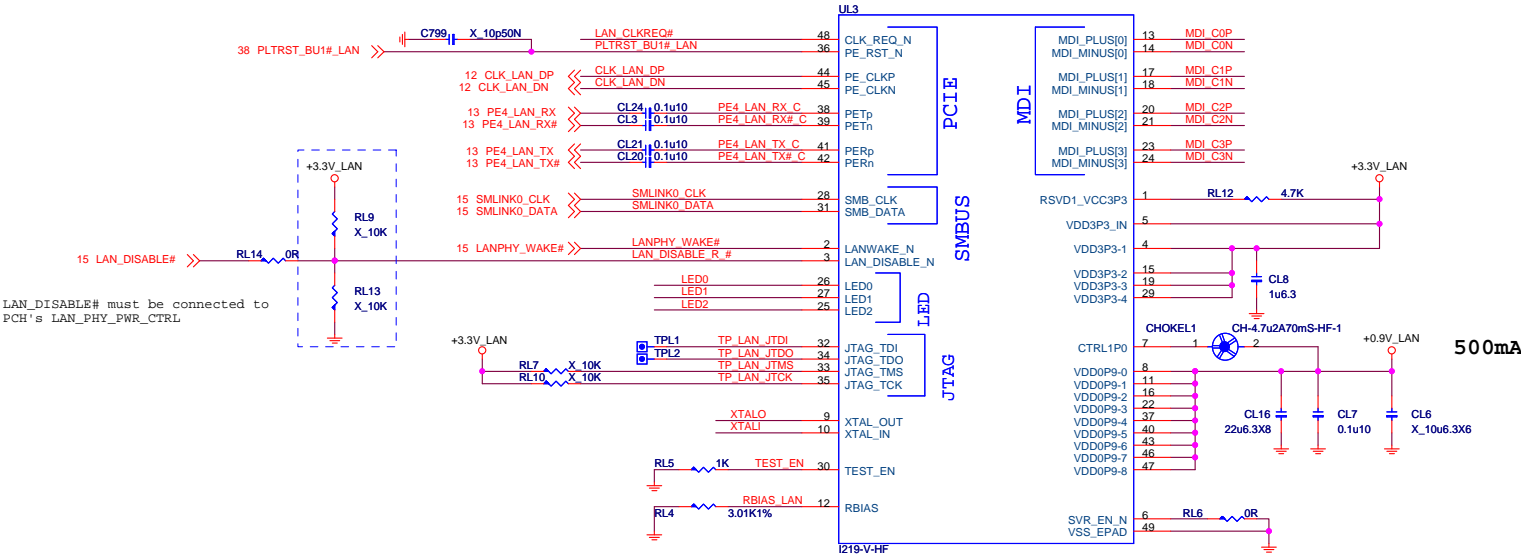




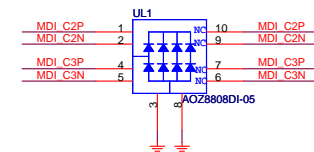
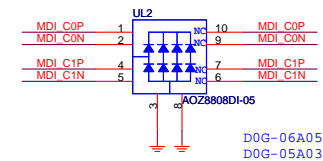


# Intel Lan- i219

8111H:B06-08111CC-R09  
8111G:B06-081116C-R09

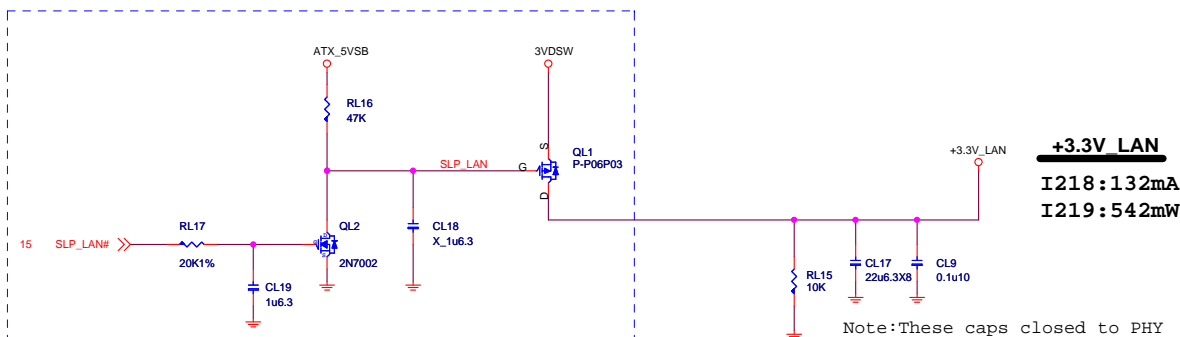


UL2&UL3 close to connector

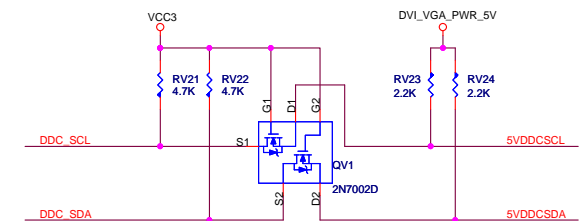
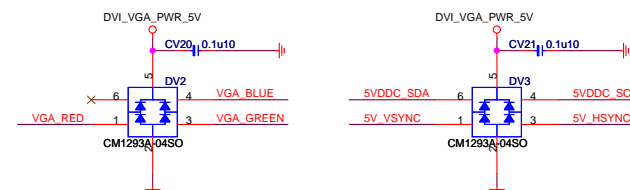
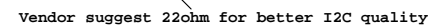
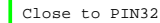


The 10Kohm pull-up resistor (RL18) of CLK\_REQ\_N is connected to 3.3V Suspend/Core/etc. power well, depending on the power well of PCH's input PCIE<CLKREQ#> buffer.

support WOL from Deep Sx:  
Power source from 3VA (DSW power) & make sure MAX current is enough to support i218/i219.



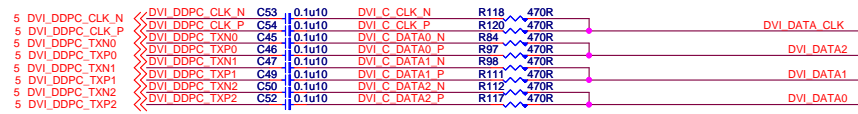
If connect to eDP port,must confirm whether it support hot plug detection HPD and re-auxtraining



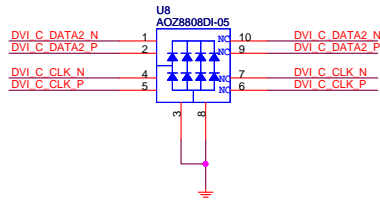
MS-7998

Size Custom	Document Description <b>VGA Connector</b>	Rev 1.1
Date: Tuesday, September 22, 2015		Sheet 32 of 60

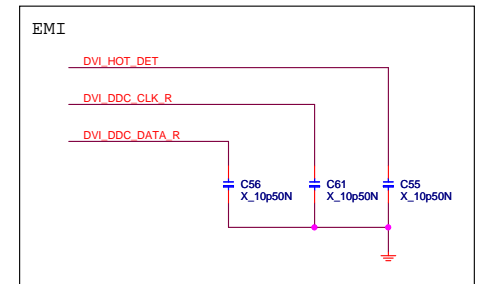
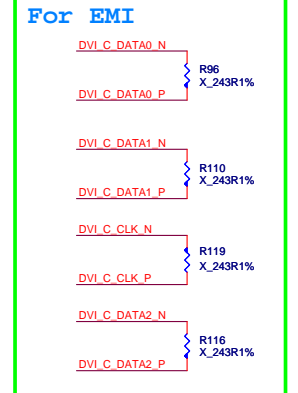
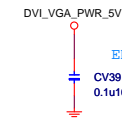
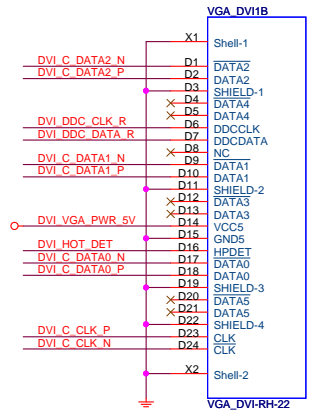
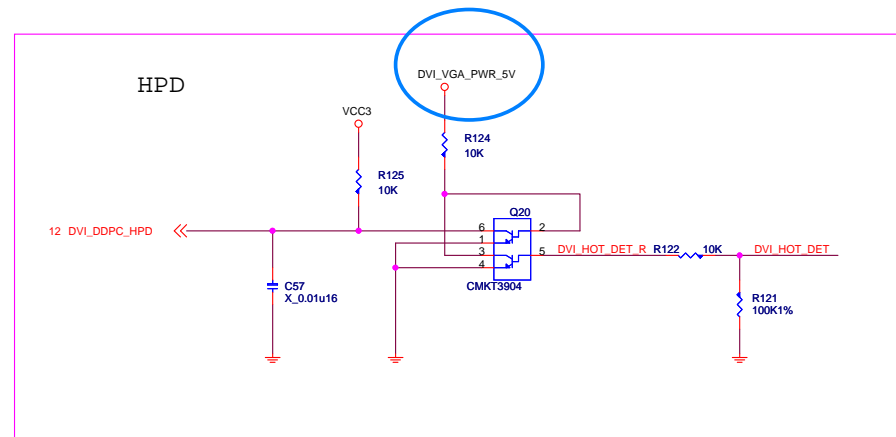
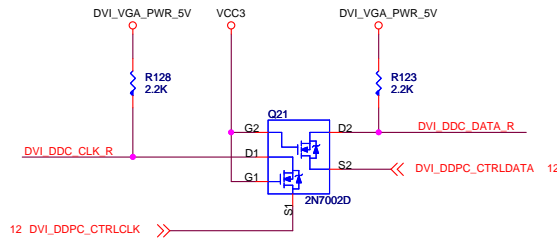
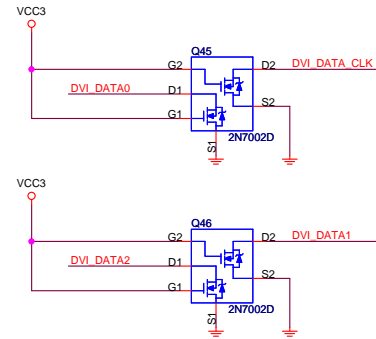
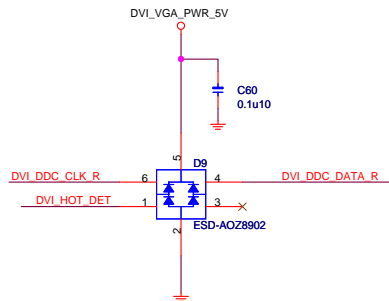
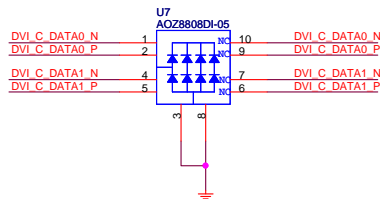
VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)



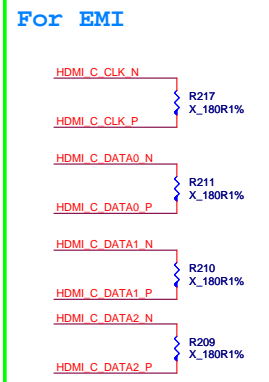
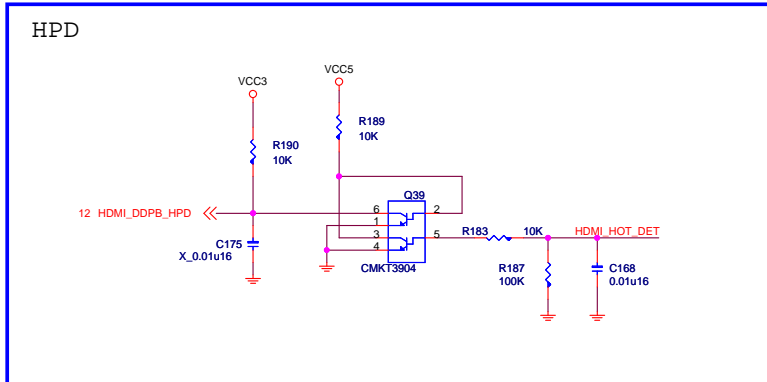
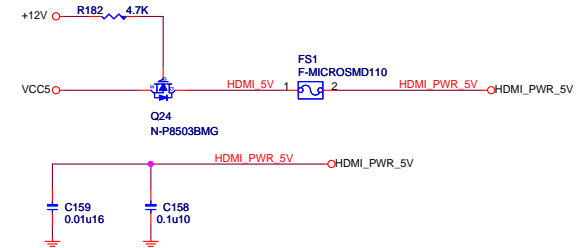
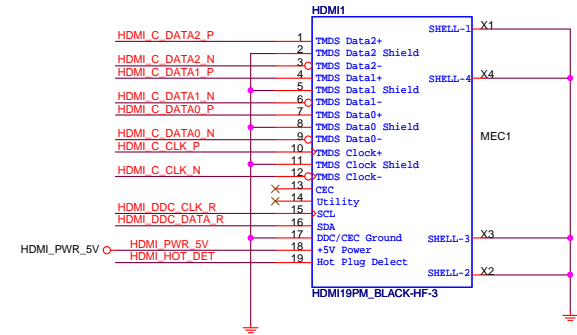
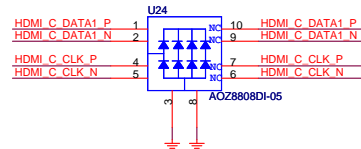
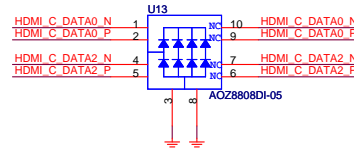
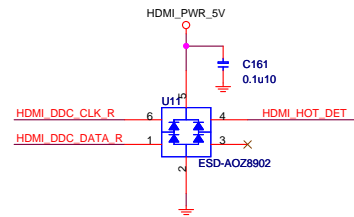
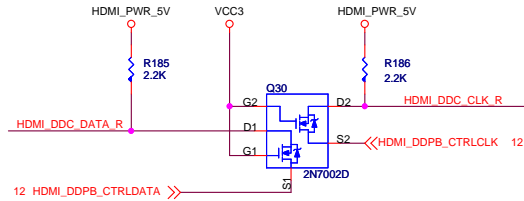
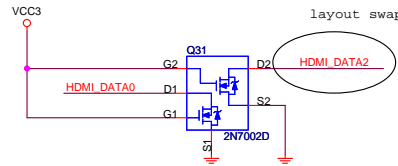
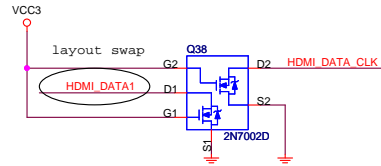
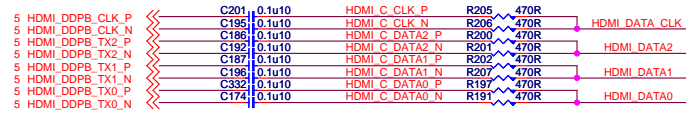
U26 AVL:D0G-05A050C-005  
D0G-06A050C-A68

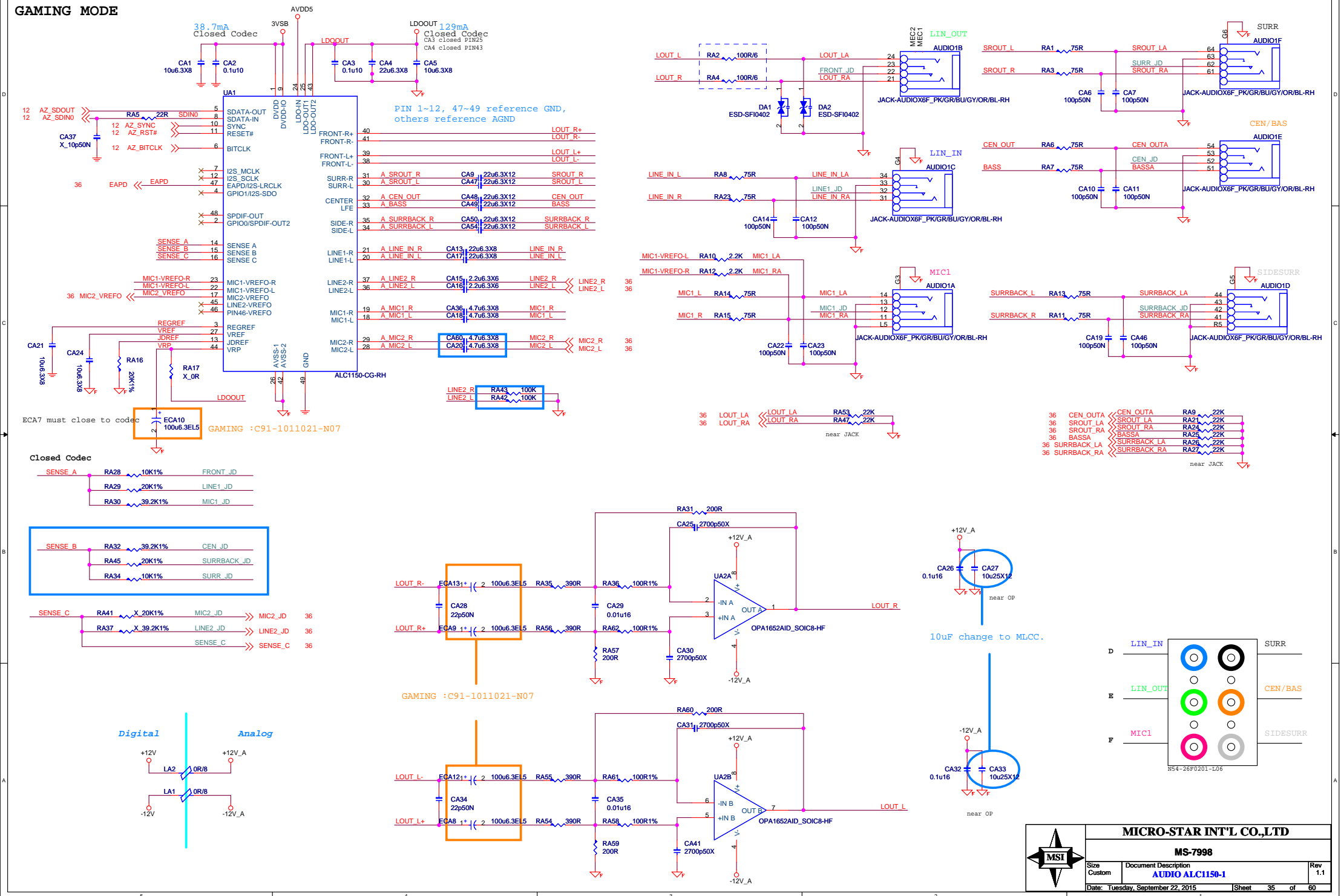


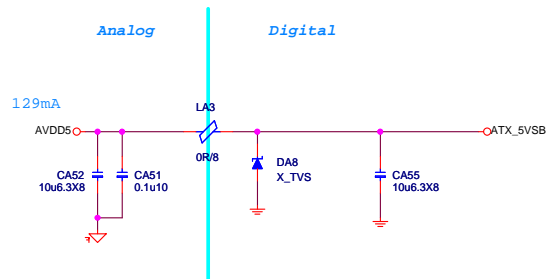
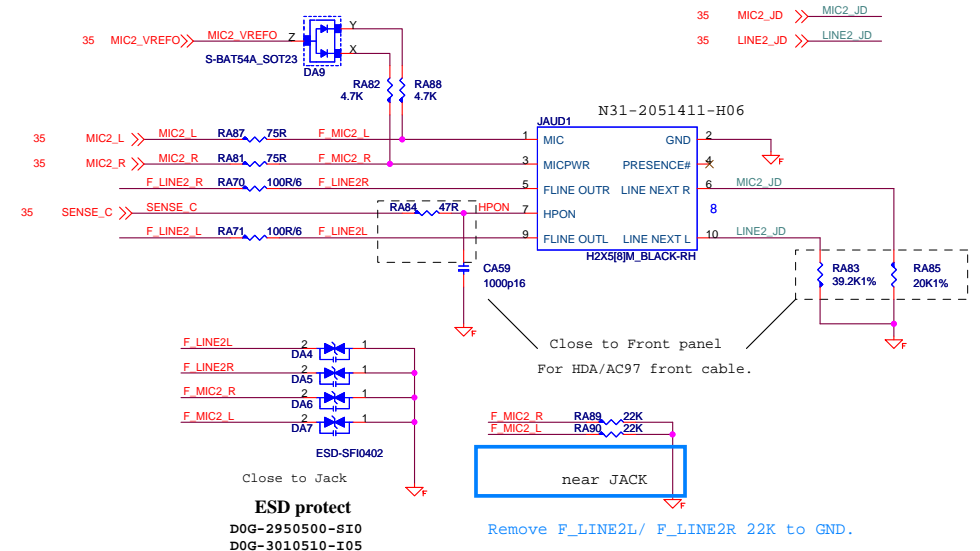
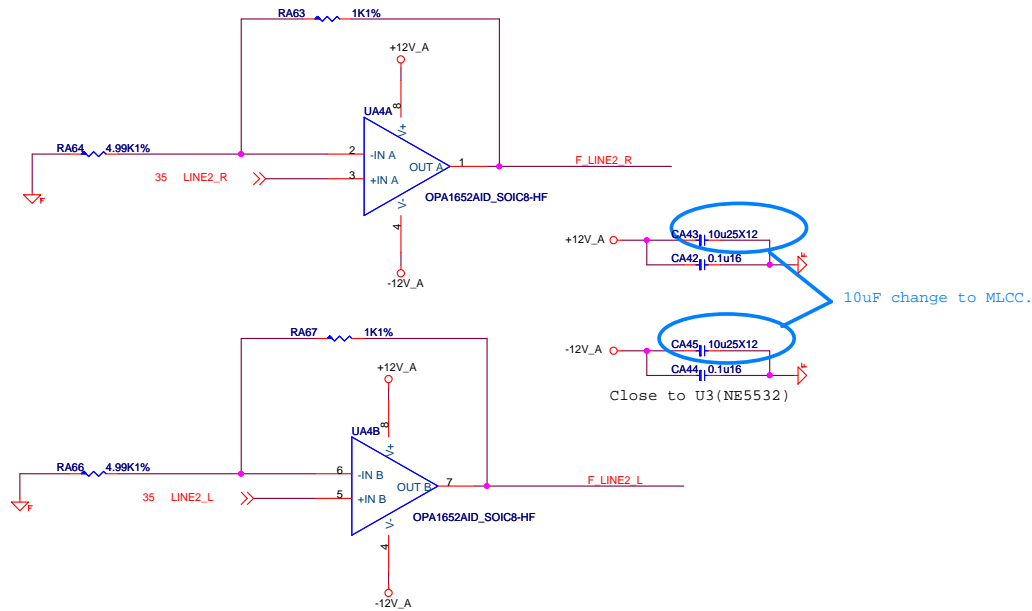
U27 AVL:D0G-05A050C-005  
D0G-06A050C-A68



HDMI, DVI : 1920x1200 at 60 Hz (16:10 WUXGA)



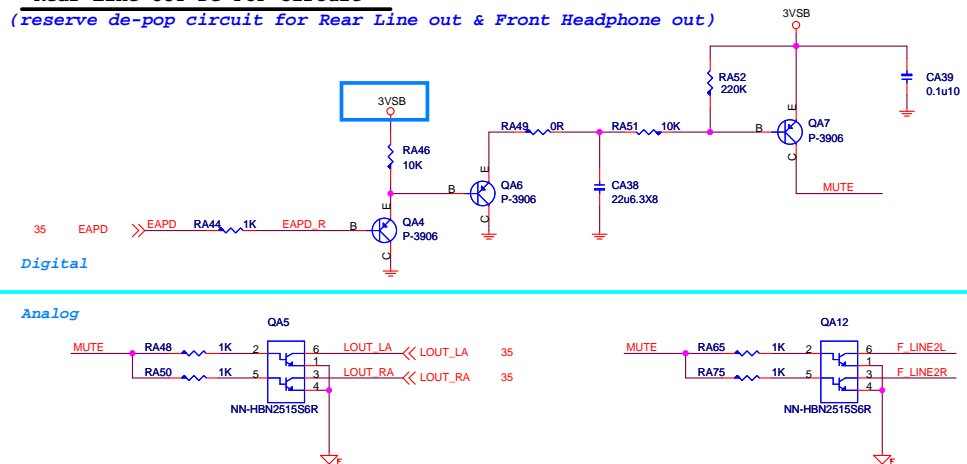
ALC1150  
GAMING MODE



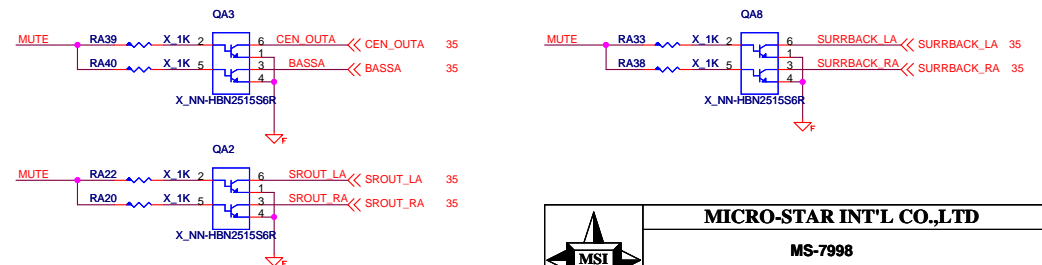
EMI



### Rear Line OUT De-POP circuit (reserve de-pop circuit for Rear Line out & Front Headphone out)

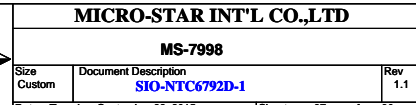
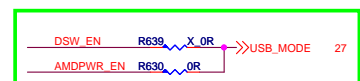


(add de-pop circuit by PM spec or customer request,  
NOTE: add de-pop circuit need to change CA6, CA7, CA12, CA13, CA23, CA24 to TVS)



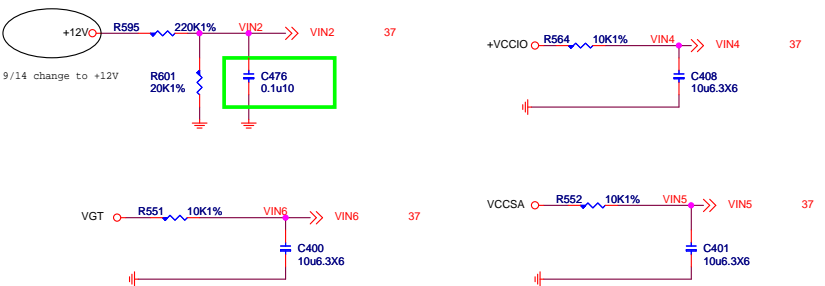
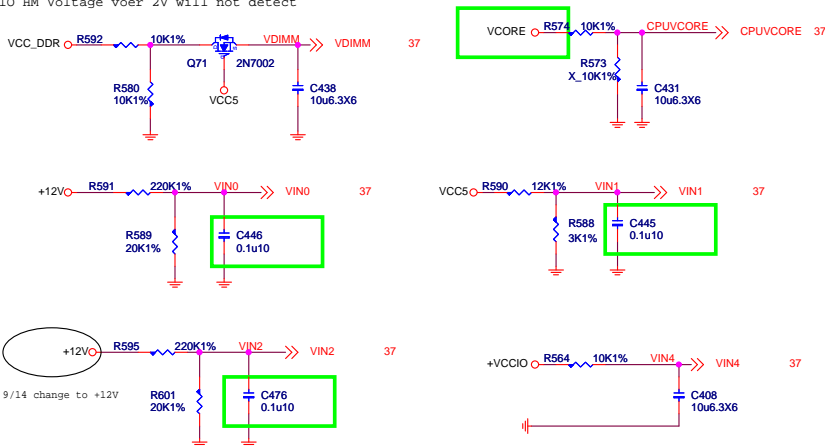
	MICRO-STAR INT'L CO.,LTD		
	MS-7998		
Size	Document Description	Rev	
Custom	AUDIO ALC1150-2	1.1	
Date: Tuesday, September 22, 2015	Sheet	36	of 60



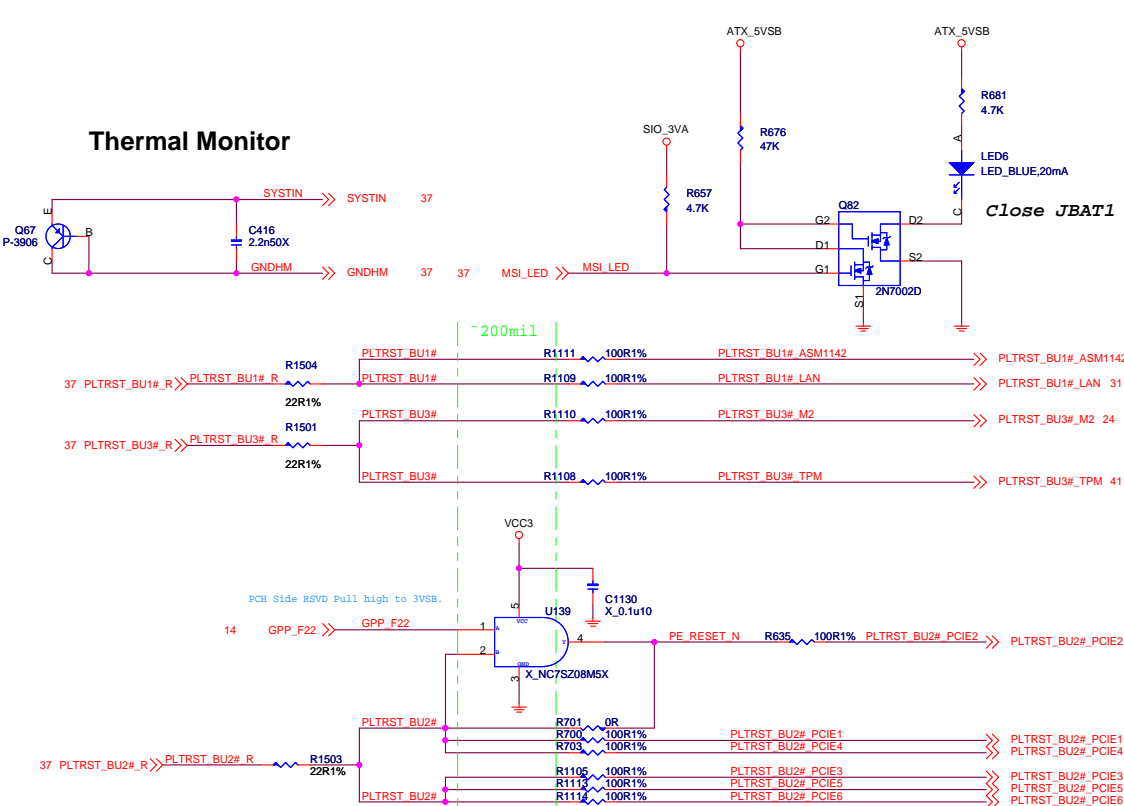


## HW Monitor - Voltage

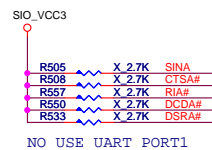
SIO HM Voltage voer 2V will not detect



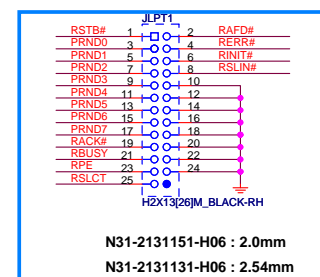
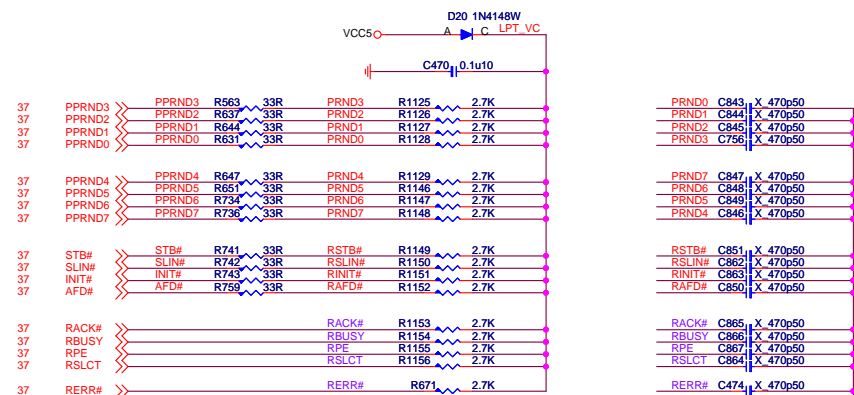
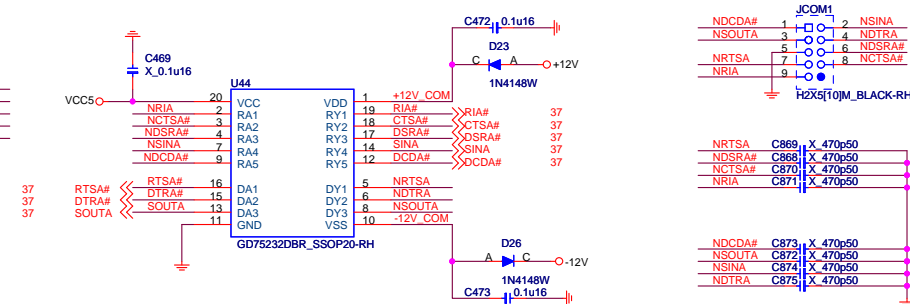
## Thermal Monitor



## SERIAL PORT 1



## PARALLAL PORT

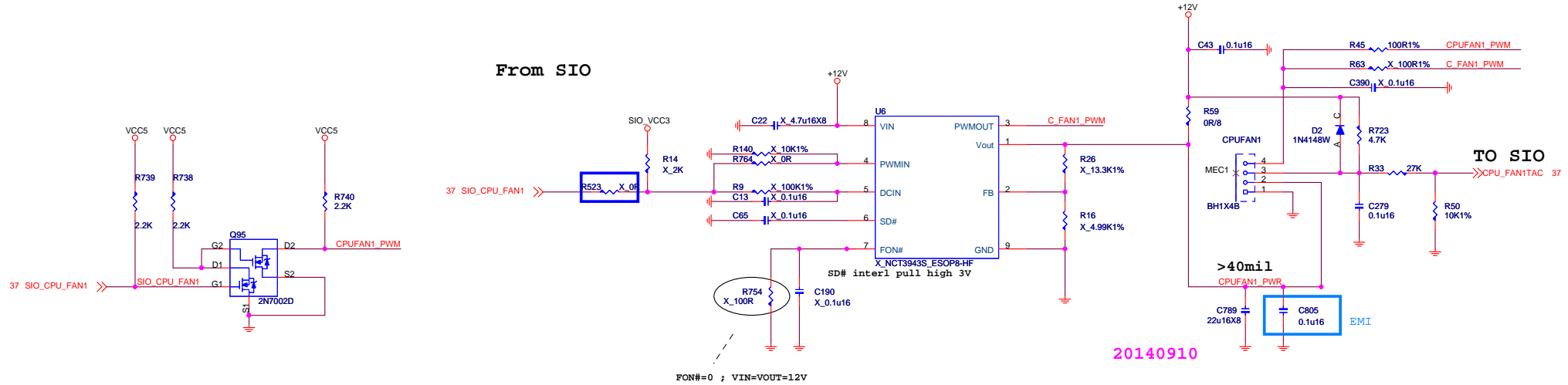


**MICRO-STAR INT'L CO.,LTD**

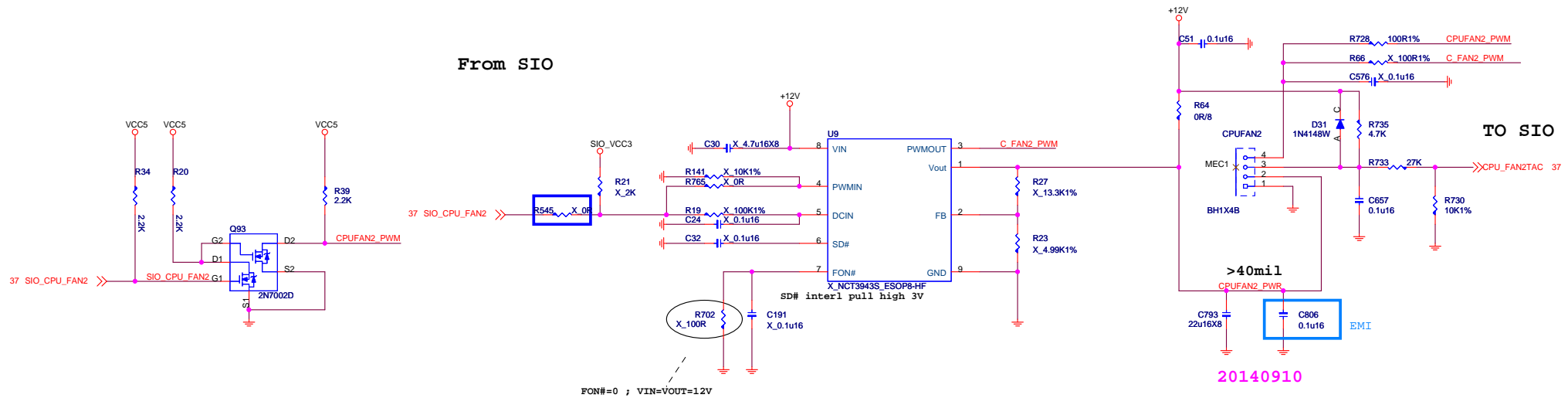
**MS-7998**

Size Custom	Document Description <b>SIO-NTC6792D-2</b>	Rev 1.1
Date: Tuesday, September 22, 2015		Sheet 38 of 60

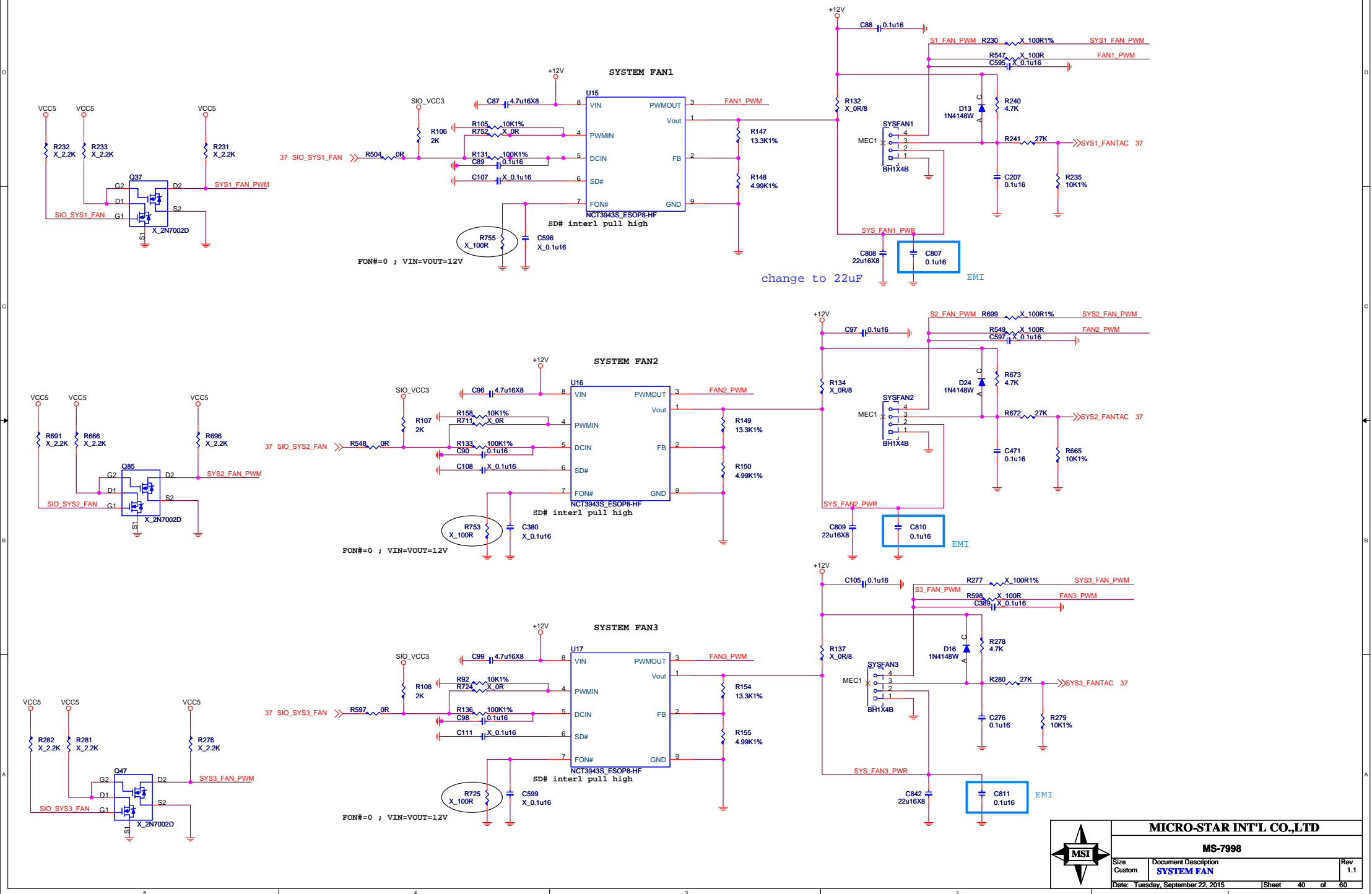
# FAN TYPE G WITH CUT POWER (Default 使用SIO的PWM MODE控制FAN的第4PIN)



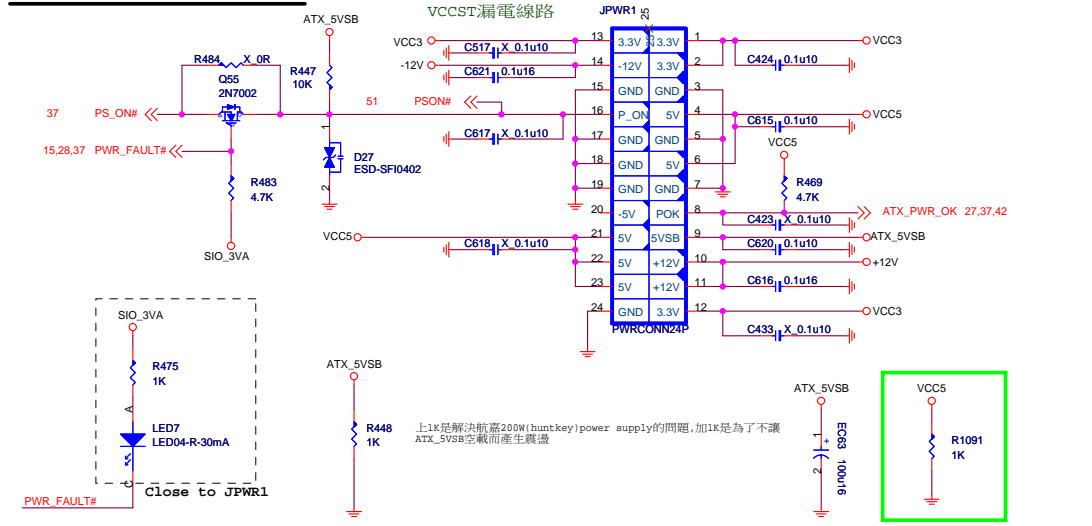
# FAN TYPE G WITH CUT POWER (Default 使用SIO的PWM MODE控制FAN的第4PIN)



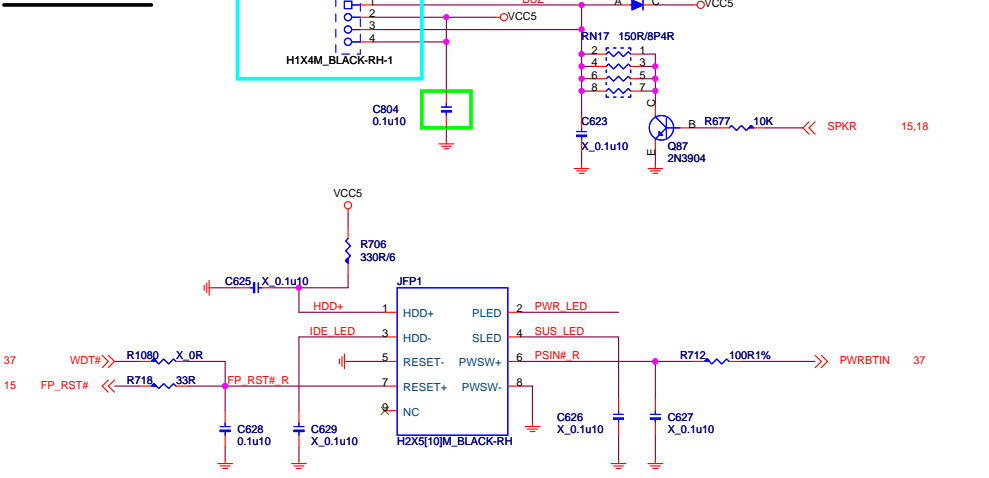
# Type H : 4 PIN SYSTEM FAN FROM SIO (Smart Fan/PWM MODE ) (FOR NCT6776/5533)



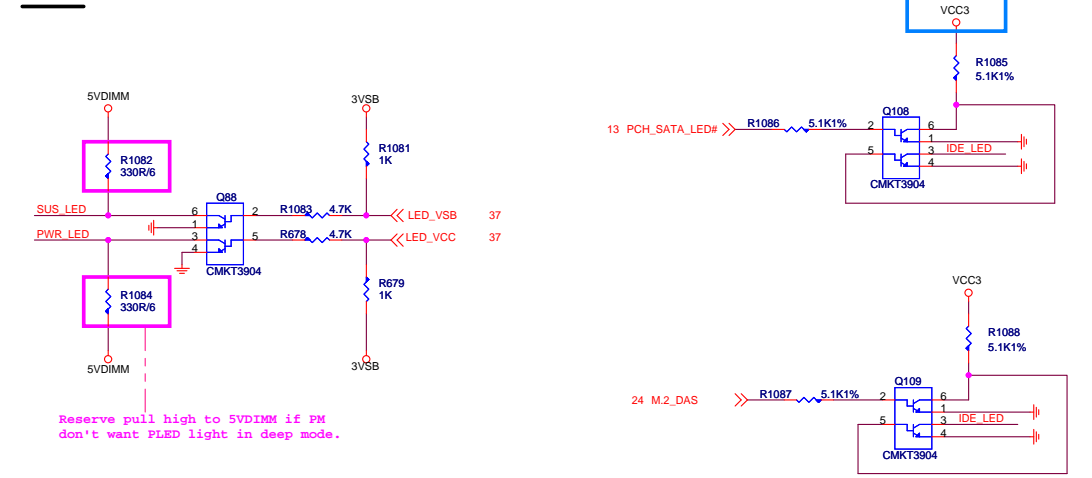
ATX POWER CONNECTOR



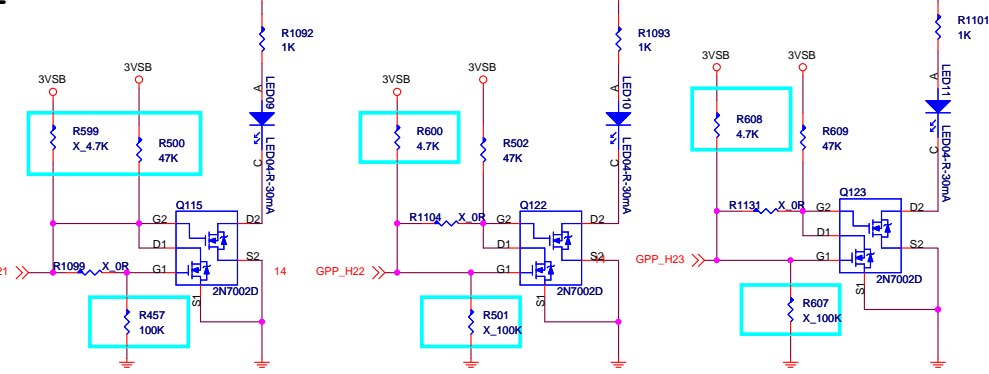
Front Panel



LED

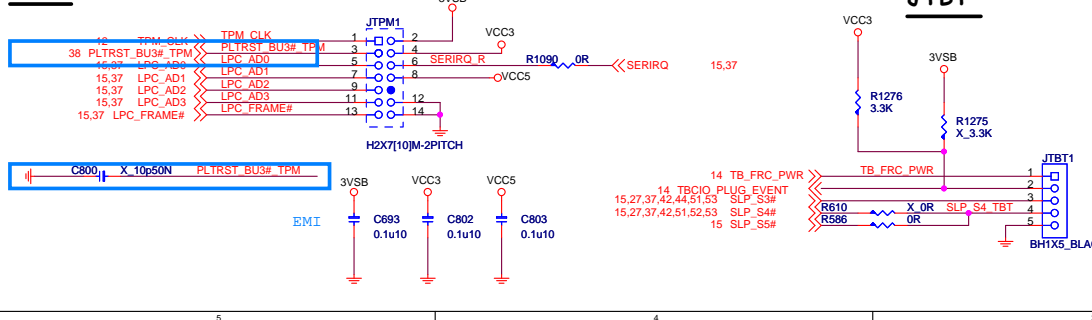


LED

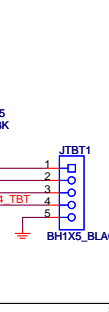


關機斷電狀態下，3個LED先維持default全暗，開機通電後：  
1. 首先進行CPU checkCPU LED 亮，check PASS後則CPU LED減掉。  
2. 接著依序進行Memory /memory LED亮check PASS後則memory LED減掉。  
3. VGA的check/VGA LED亮，check PASS後則VGA LED減掉。  
4. 因此最後正常順利開機後，三個LED燈都是減掉的。(系統重啟或其他原因造成系統重開機，則LED仍按上進行為動作)

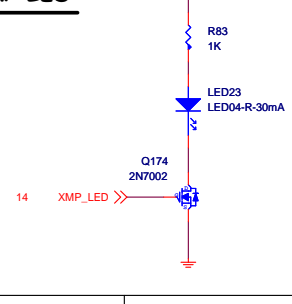
TPM



JTBT



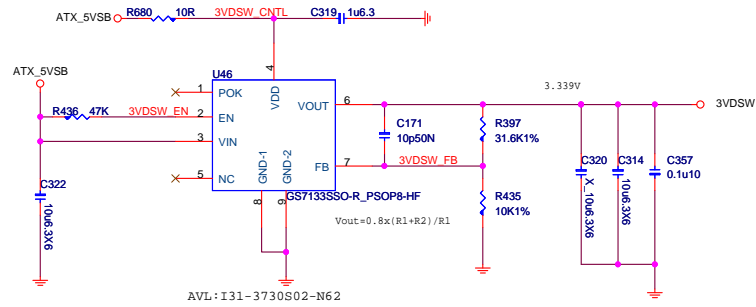
XMP LED



GPIO LED	GPP_H21	GPP_H22	GPP_H23
亮	GPI PULL HIGH	GPO PO LOW	GPO PO LOW
滅	GPO PO LOW	GPO HIGH (default HIGH)	GPO HIGH (default HIGH)

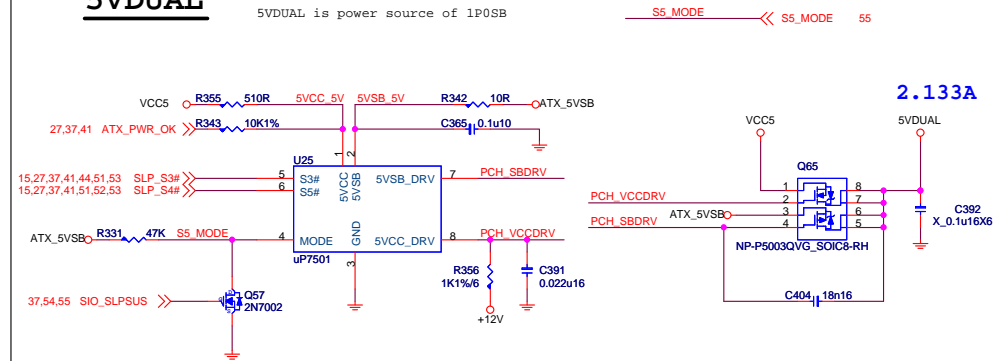
**MICRO-STAR INT'L CO.,LTD**  
**MS-7998**  
Size Custom Document Description **ATX Power/F\_Panel** Rev 1.1  
Date: Tuesday, September 22, 2015 Sheet 41 of 60

## 3VDSW

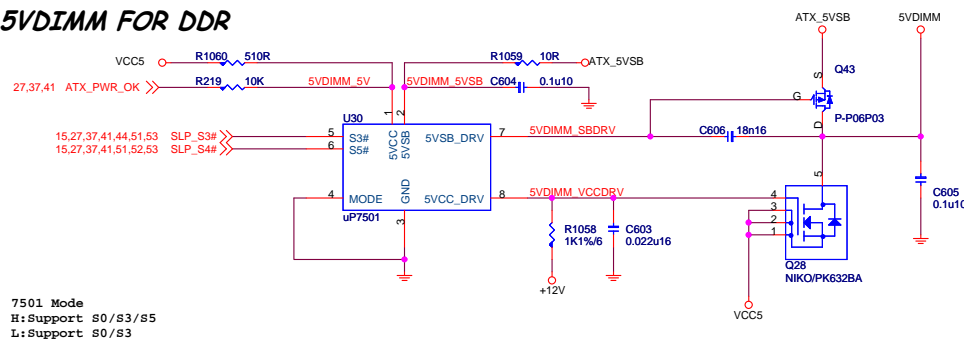


## 5VDUAL

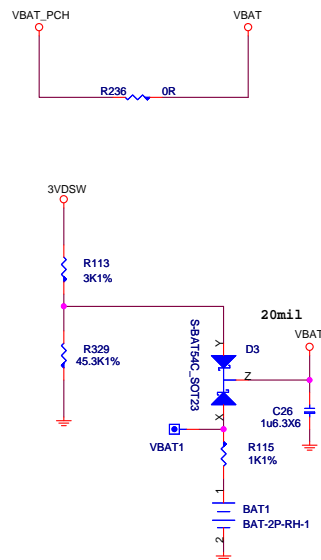
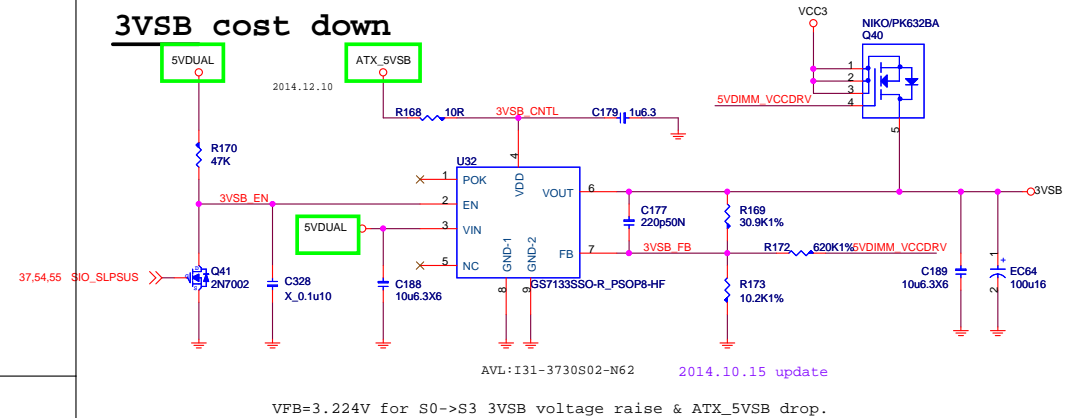
5VDUAL is power source of 1P0SB



## 5VDIMM FOR DDR

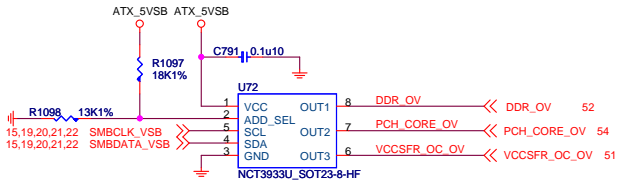


## 3VSB cost down



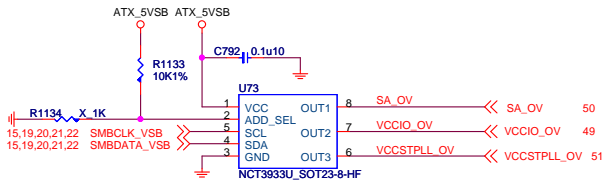
UPI VOLTAGE CONSOLE

0x26:RH=18K,RL=1.3K



ADDRESS	0x2A	0X28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%

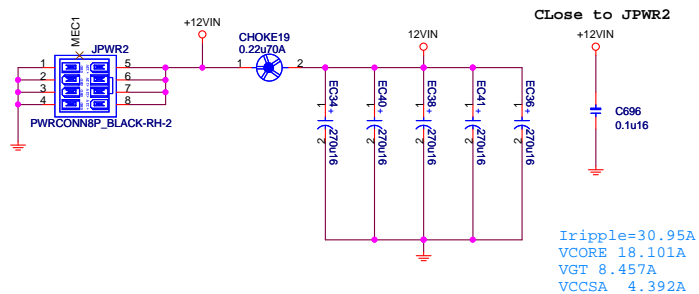
0x20:RH=10K,RL=OPEN



MICRO-STAR INT'L CO.,LTD

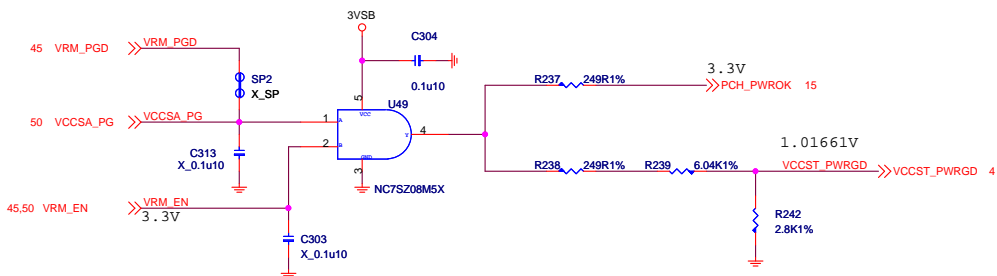
MS-7998

Size	Document Description	Rev
Custom	OV-NCT3933/GPIO-NCT5605	1.1
Date:	Tuesday, September 22, 2015	Sheet 43 of 60

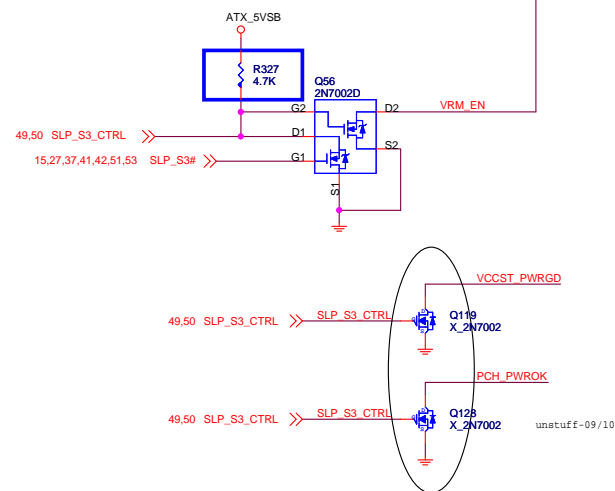
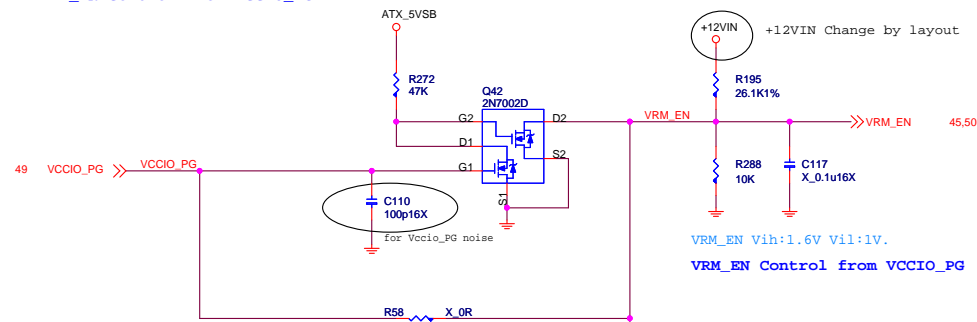


PCH\_PWROK Control from VCCIO\_PG&VCCSA  
VCCST\_PWRGD Control from VRM\_PG

VCCSA&Vcore use same PWM IC, pull up VCC3  
VCCSA&Vcore use different PWM IC,pull up VCCSA  
VCCST\_PWRGD can assert before or equal to PCH\_PWROK, but must never lag it.

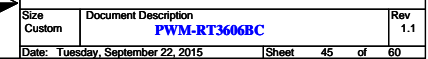


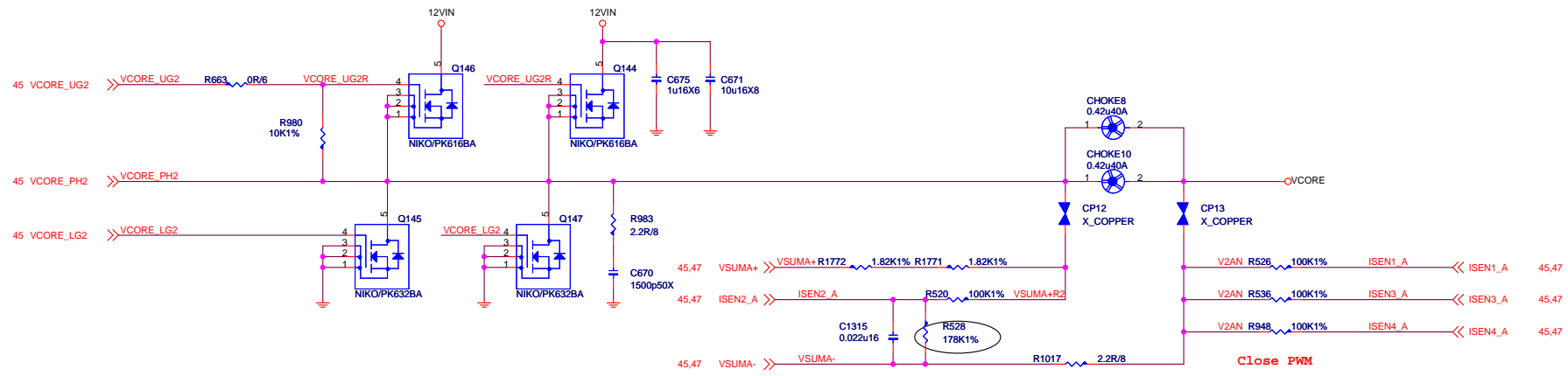
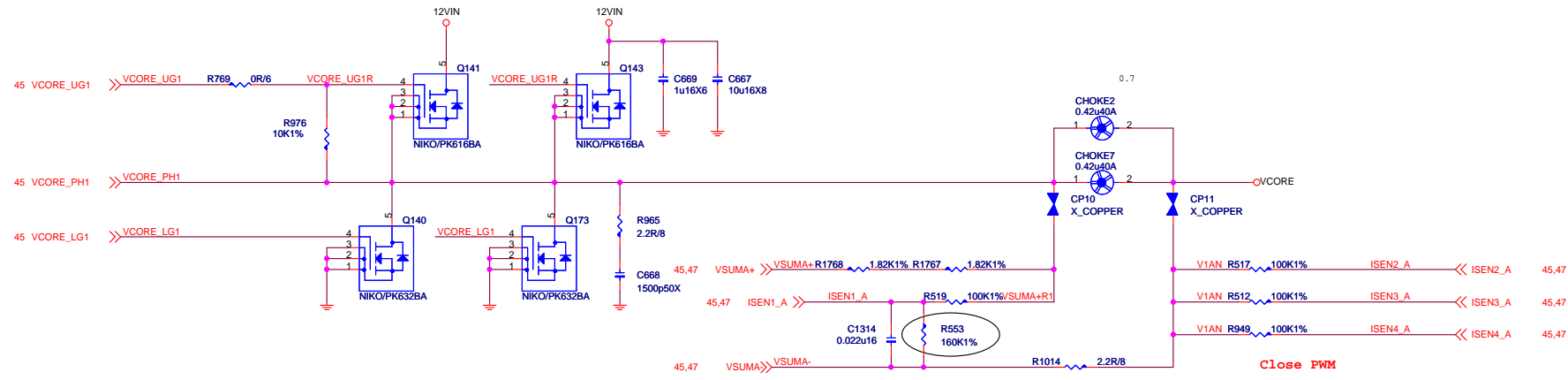
VRM\_EN Control from VCCIO\_PG



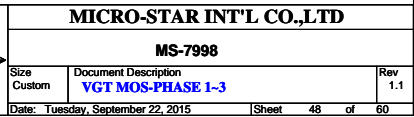
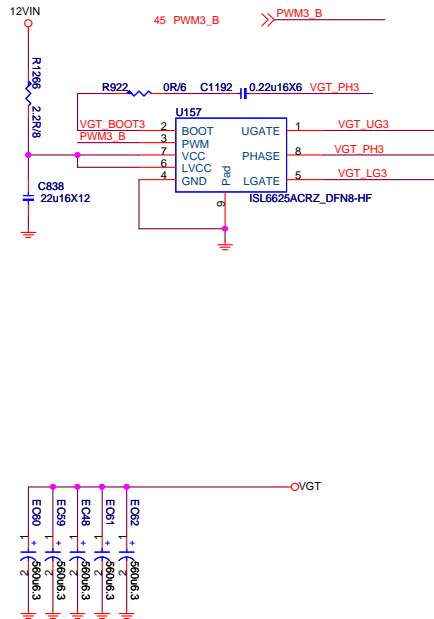
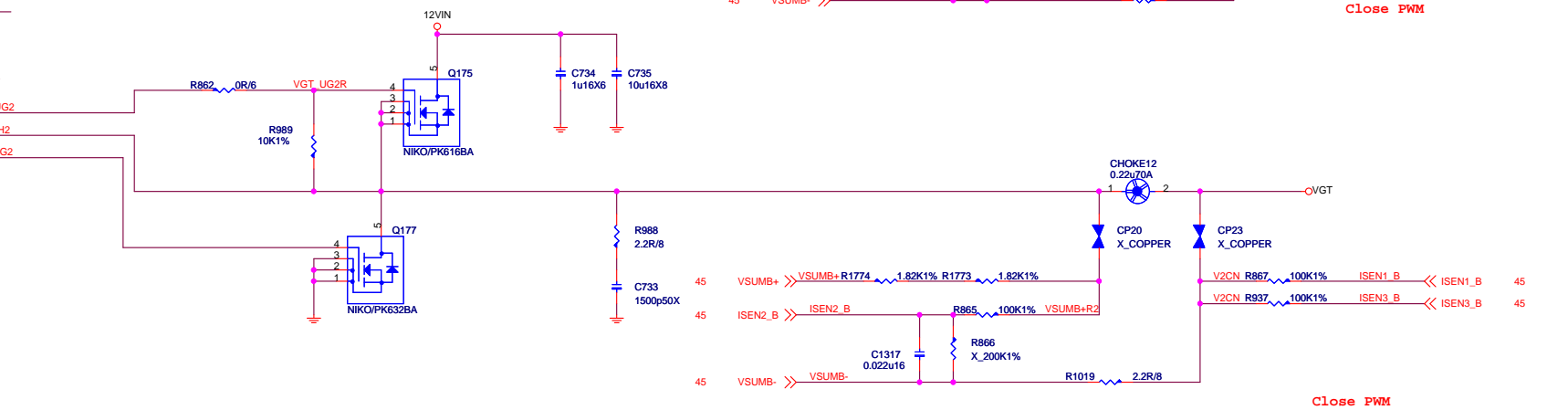


```
Constraint: 5/10/15
SVID Addr 00h : VCORE
SVID Addr 01h : VGT
SMBus Addr: XXh
```



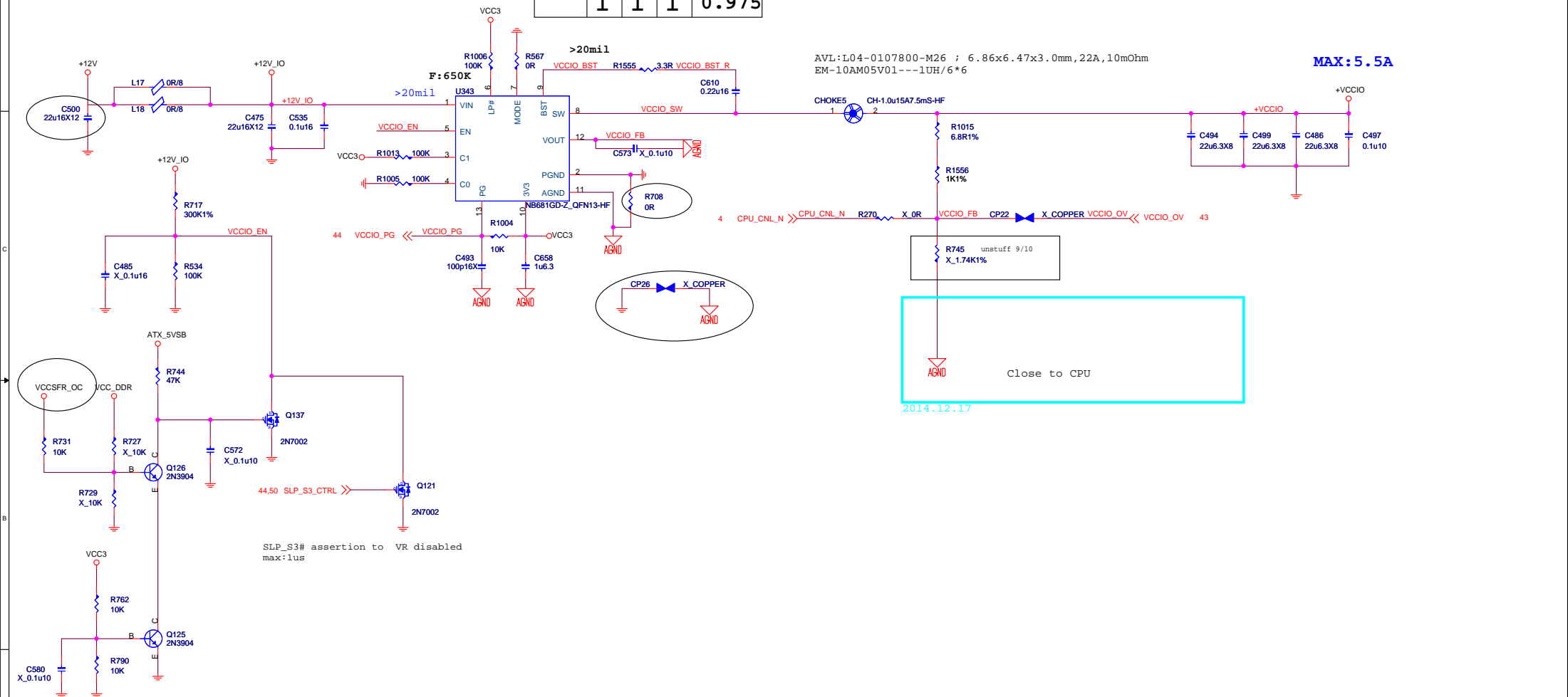






**VCCIO**  
 0.95V; 5.5A  
 I<sub>MAX</sub> 6A  
 I<sub>LIMIT</sub>=8.5~9A

	LP#	C1	C0	VOUT(V)
VCCIO	0	X	X	0
	1	0	0	0.85
	1	0	1	0.875
	1	1	0	0.95
	1	1	1	0.975



# SA Power:1.05V,11.1A

$$OCP = 11.1A * 1.4 = 15.54A$$

$$Rocs(R417) = OCP * Rdson(Low\ side) [3.4mohm] / 10uA$$

$$= 15.54 * (3.4mohm) / 10uA$$

$$= 5.2836Kohm$$

Rocs: 5.2836K, OCP:

D03-4C05N03-005 : 15.76A

D03-632BA0C-N03 : 16.24A

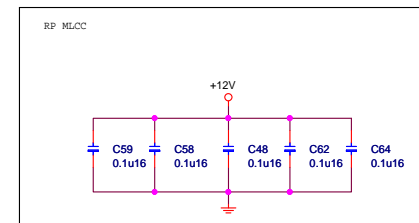
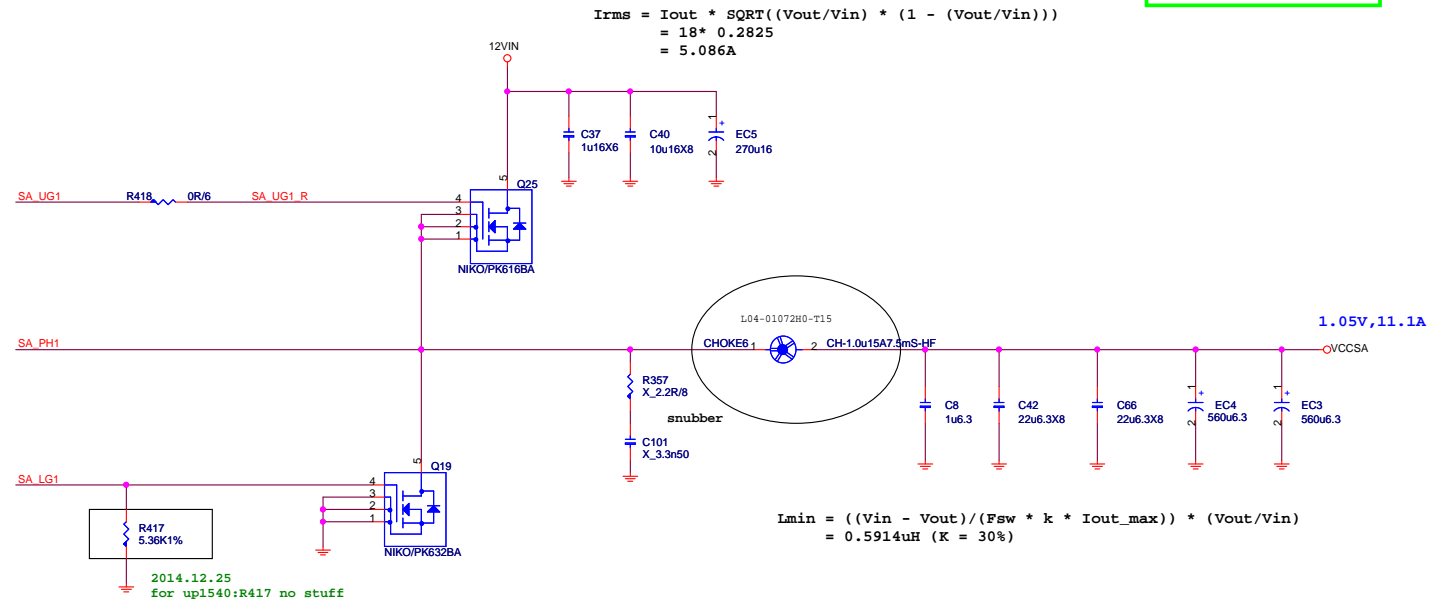
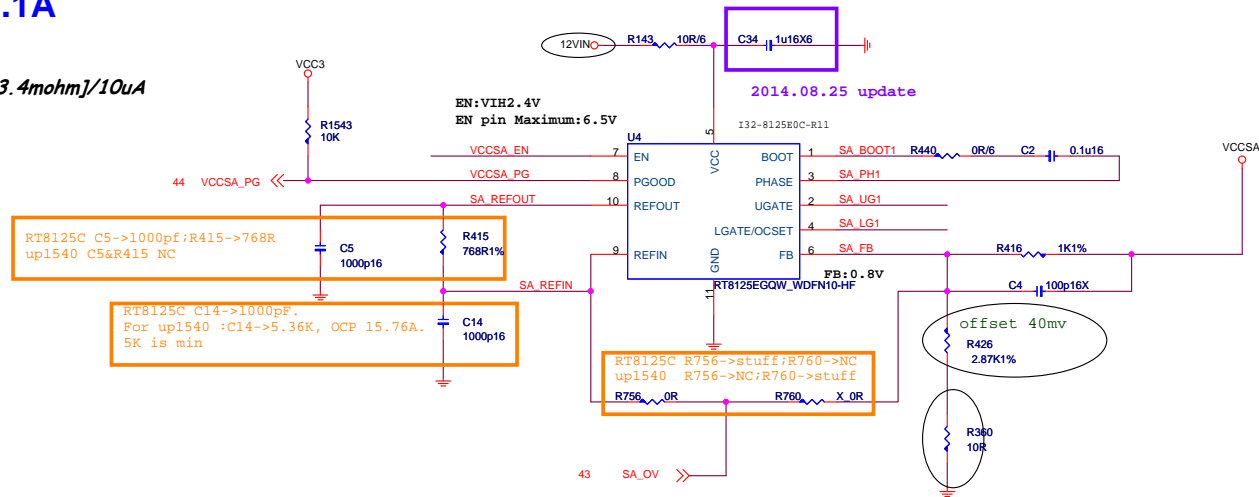
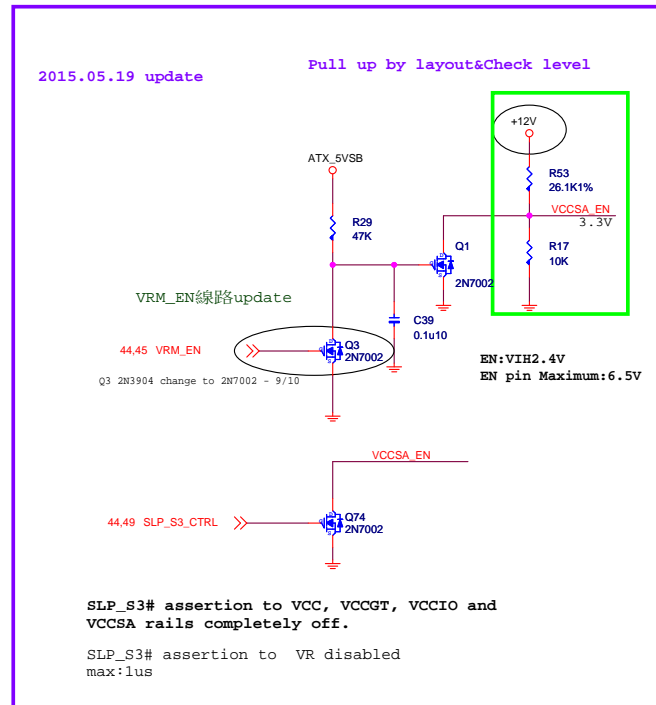
use UBIQ MOS need Check

Rdson(Low) 10V

D03-4C05N03-005 : 3.4mohm

D03-632BA0C-N03 : 3.3mohm

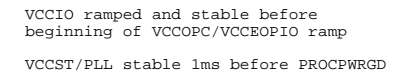
D03-3056M00-U47 : 4.2mohm



MICRO-STAR INT'L CO.,LTD			
MS-7998			
Size	Document Description	Rev	
Custom	CPU PWR_SA-RT8125C	1.1	
Date:	Tuesday, September 22, 2015	Sheet	50 of 60

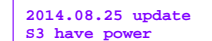
*for Gaming3/5, Classic, ECO  
and H110*

For Cost down VCCST&VCCPLL merge



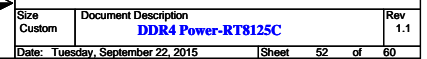
1.2V; 110mA

EN:VIH1.2V  
EN pin Maximum:VIN+0.3V



MS-7998

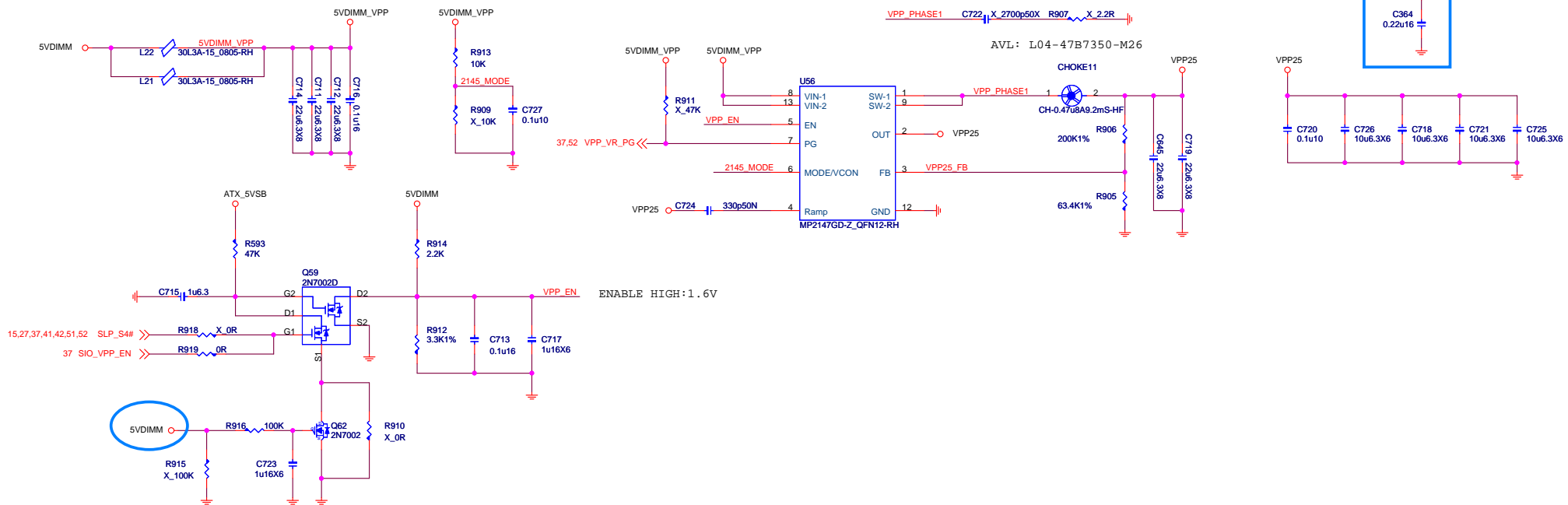
Size Custom	Document Description <b>CPU PWR_ST/PLL</b>	Rev 1.1
Date: Tuesday, September 22, 2015		Sheet 51 of 60





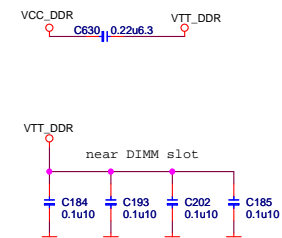
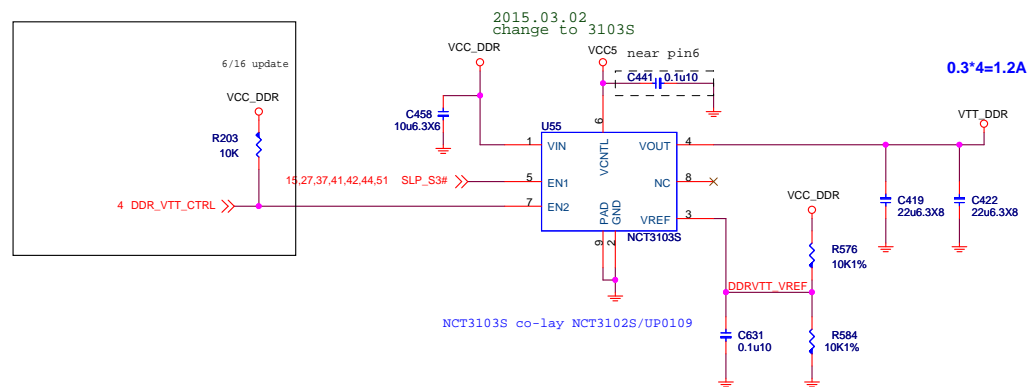
4DIMM :2.24A FOR DDR VPP2.5V

**VPP25 Power**  
**2.5V; 2.24A**



To make sure VPP EN after 5VDIMM stable

### DDR VTT Power



**MICRO-STAR INT'L CO.,LTD**

MS-7998

Size Custom	Document Description <b>DDR4 Power-VPP25</b>	Rev 1.1
Date: Tuesday, September 22, 2015		Sheet 53 of 60

# PCH\_1VSB

1.0V; 11A

OCp = 16.21A

Rocset =  $1.5 * I_{max} * R_{dson(LOW)} / I_{ocset}$   
 =  $1.5 * 10.664 * 5\text{mohm} / 10\text{uA}$   
 = 7.998K

Rocs: 7.87K, OCP:

D03-4C05N03-005 : 15.74A

D03-632BA0C-N03 : 17.1A

use UBIQ MOS need Check

Rdson(LOW) 4.5V

D03-3116M00-U47 : 3.6 mohm

D03-632BA0C-N03 : 4.6mohm

D03-3056M00-U47 : 6.2mohm

1504 change to 8125 I32-8125E0C-R11

$$I_{rms} = I_{out} * \sqrt{(V_{out}/V_{in}) * (1 - (V_{out}/V_{in}))}$$

$$= 10.664 * 0.4$$

$$= 4.2656A < 5000mA$$

L04-47B7730-T15 for OC, Gaming 10, 9, 7, 5  
 L04-12A7321-L65 for Gaming 3, SLI, ECO  
 L04-12A7721-T15 for cost down

MAX: 10.664A  
 7.088A

$$L_{min} = ((V_{in} - V_{out}) / (F_{sw} * k * I_{out\_max})) * (V_{out}/V_{in})$$

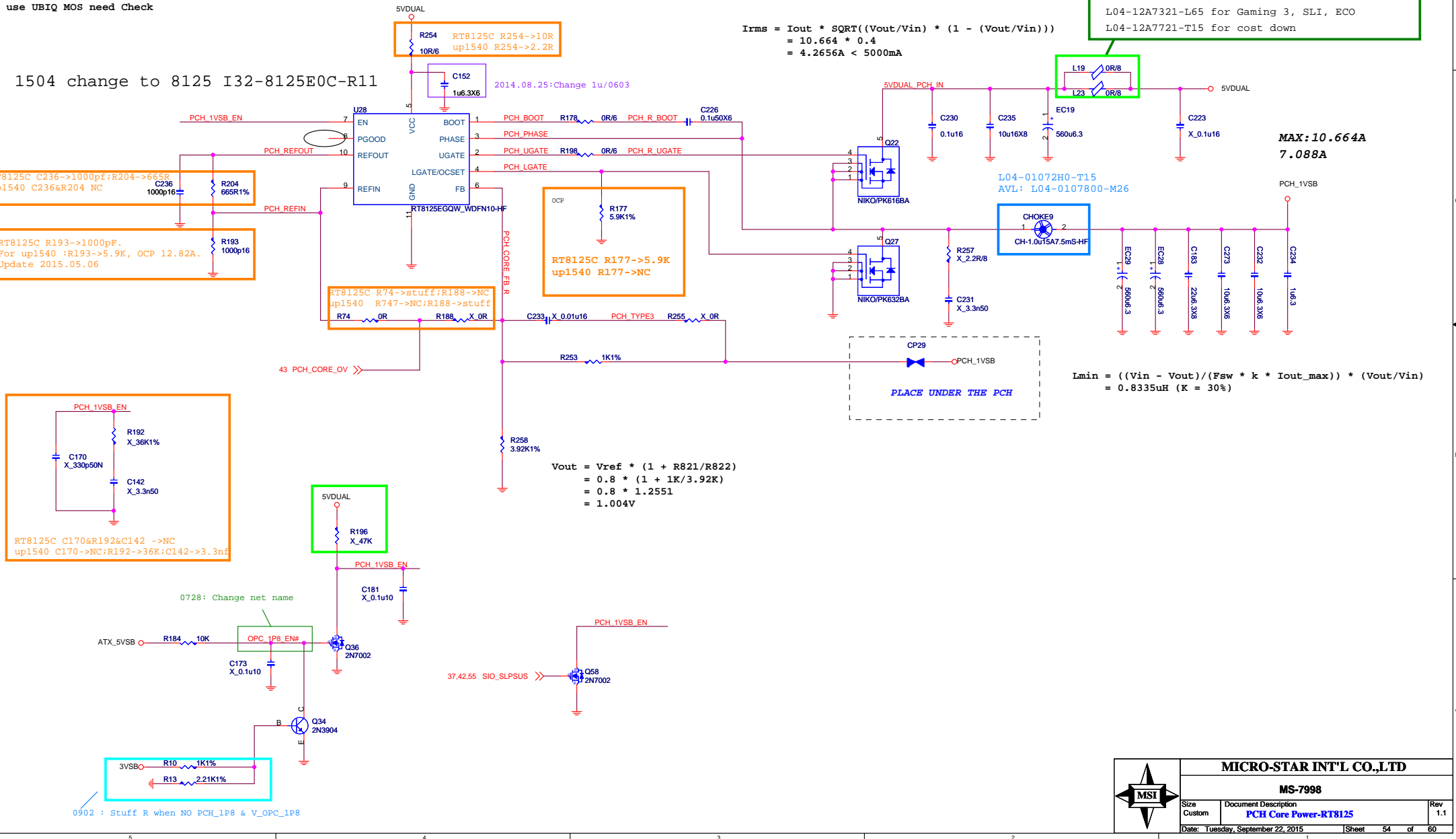
$$= 0.8335\text{uH} (K = 30\%)$$

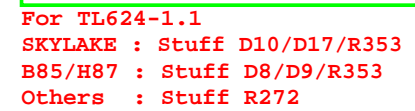
$$V_{out} = V_{ref} * (1 + R_{821}/R_{822})$$

$$= 0.8 * (1 + 1K/3.92K)$$

$$= 0.8 * 1.2551$$

$$= 1.004V$$

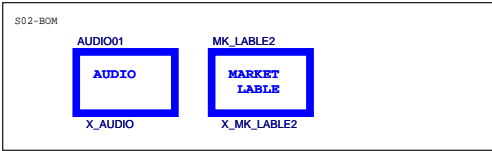


Rev  
1.1

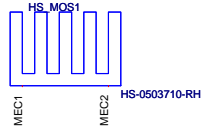
PCB



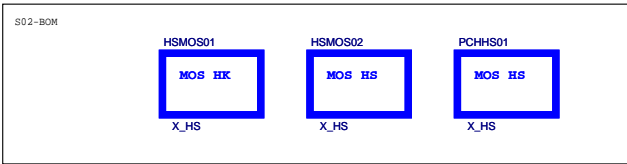
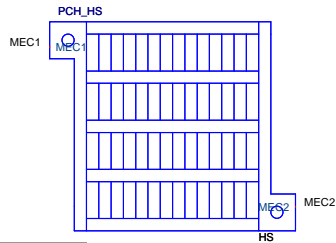
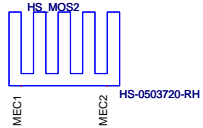
PD0-0799810-G37  
PD0-0799810-E48



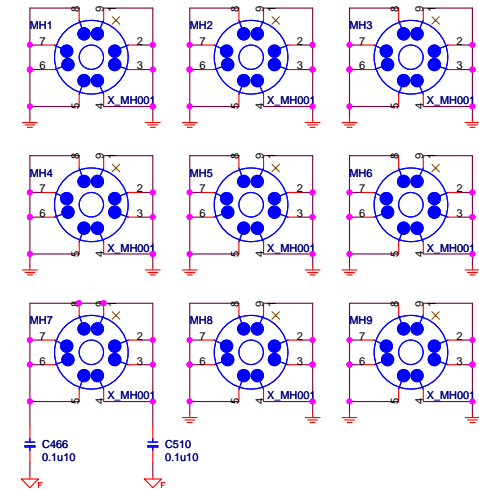
MOS1 Heatsink



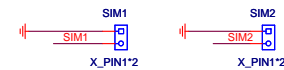
MOS2 Heatsink



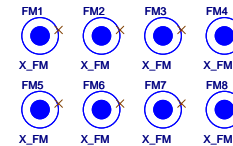
Mounting Holes



Simulation



Optical Fiducial Marks-120



Test point

