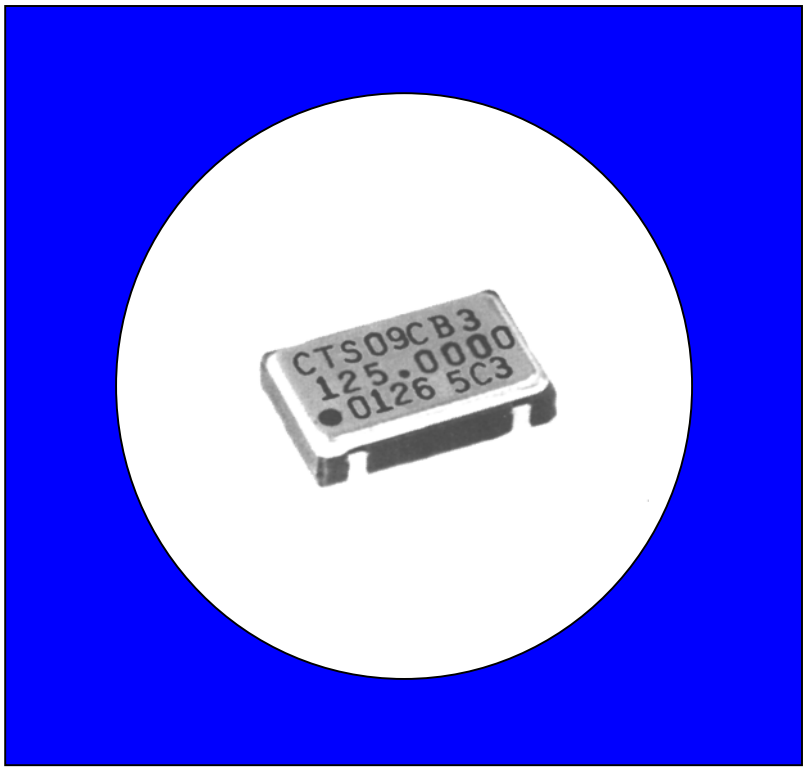
# Model CB3 & CB3LV

## HCMOS/TTL CLOCK OSCILLATOR

### FEATURES

- Standard 7.5x5.0mm Surface Mount Footprint
- HCMOS/TTL Compatible
- Fundamental and 3rd Overtone Crystals
- Frequency Range 1.5 – 160 MHz
- Frequency Stability, ±50 ppm Standard (±25 ppm and ±20 ppm available)
- +3.3Vdc or +5.0Vdc Operation
- Operating Temperature to –40°C to +85°C
- Output Enable Standard
- Tape & Reel Packaging
- **RoHS/Green Compliant**




### DESCRIPTION

The CB3/CB3LV is a ceramic packaged Clock oscillator offering reduced size and enhanced stability. The small size means it is perfect for any application. The enhanced stability means it is the perfect choice for today's communications applications that require tight frequency control.

### ORDERING INFORMATION

CB3 ☐ - ☐☐ - M

**SUPPLY VOLTAGE**
LV = +3.3Vdc
Blank = +5.0Vdc

**FREQUENCY STABILITY**
6 = ± 20 ppm *
5 = ± 25 ppm
7 = ± 32 ppm
3 = ± 50 ppm (standard)

**FREQUENCY IN MHz**
M - indicates MHz and decimal point. Frequency is recorded with minimum 4 significant digits to the right of the "M".

**OPERATING TEMPERATURE RANGE**
C = -20°C to +70°C (standard)
I = -40°C to +85°C *

* Consult factory for 6I availability.

Example Part Number: CB3LV-3C-32M7680 or CB3-3I-32M7680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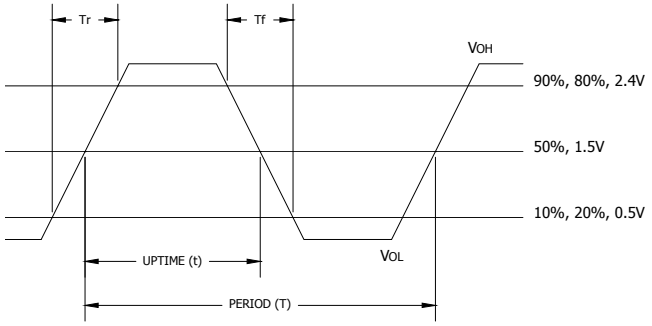
• • • www.ctscorp.com • • •

## ELECTRICAL CHARACTERISTICS

| | PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| Absolute Maximums | Maximum Supply Voltage | $V_{CC}$ | - | -0.5 | - | 7.0 | V |
| | Storage Temperature | $T_{STG}$ | - | -55 | - | 125 | °C |
| | Frequency Range | | | | | | |
| | $V_{CC}$ = 5.0V | $f_O$ | - | 1.5 | - | 107 | MHz |
| | $V_{CC}$ = 3.3V | | - | 1.5 | - | 160 | |
| | Frequency Stability (See Note 1 and Ordering Information) | $\Delta f/f_O$ | - | - | - | 20,25 or 50 | ± ppm |
| | Operating Temperature | | | | | | |
| | Commercial | $T_A$ | - | -20 | 25 | 70 | °C |
| | Industrial | | | -40 | | 85 | |
| Electrical and Waveform Parameters | Supply Voltage | | ± 10 % | | | | |
| | CB3 | $V_{CC}$ | | 4.5 | 5.0 | 5.5 | V |
| | CB3LV | | | 3.0 | 3.3 | 3.6 | |
| | Supply Current | | | | | | |
| | CB3 | | 1.5 MHz to 20 MHz $C_L$=50pF | - | 10 | 25 | mA |
| | | | 20.1 MHz to 80 MHz $C_L$=50pF | - | 30 | 50 | |
| | | $I_{CC}$ | 80.1 MHz to 160 MHz $C_L$=15pF | - | 40 | 100 | |
| | CB3LV | | 1.5 MHz to 20 MHz $C_L$=15pF | - | 7 | 12 | |
| | | | 20.1 MHz to 80 MHz $C_L$=15pF | - | 20 | 40 | |
| | | | 80.1 MHz to 160 MHz $C_L$=15pF | - | 30 | 60 | |
| | Output Load | | 1.5 MHz to 50 MHz | - | - | 50 | pF |
| | | $C_L$ | 50.1 MHz to 80 MHz | - | - | 30 | |
| | | | 80.1 MHz to 160 MHz | - | - | 15 | |
| | Output Voltage Levels | | | | | | |
| | Logic '1' Level | $V_{OH}$ | CMOS Load | 0.9*$V_{CC}$ | - | - | V |
| | | | 10 TTL LOAD | $V_{CC}$-0.6V | | | |
| | Logic '0' Level | $V_{OL}$ | CMOS | - | - | 0.1*$V_{CC}$ | |
| | | | TTL Load | | | 0.4 | |
| | Output Current | | | | | | |
| | Logic '1' Level | $I_{OH}$ | $V_{OH}$ = 3.9V/2.2V $V_{CC}$ = 4.5V/3.0V | - | - | -16/-8 | mA |
| | Logic '0' Level | $I_{OL}$ | $V_{OL}$ = 0.4V $V_{CC}$ = 4.5V/3.0V | - | - | +16/+8 | |
| | Output Duty Cycle | SYM | @ 50% Level | 45 | - | 55 | % |
| | Rise and Fall Time | | @ 10% - 90% Levels | | | | |
| | CB3 | | 1.5 MHz to 20 MHz $C_L$=50pF | - | 8 | 10 | ns |
| | | | 20.1 MHz to 80 MHz $C_L$=50pF | - | 4 | 8 | |
| | | $T_R$, $T_F$ | 80.1 MHz to 160 MHz $C_L$=15pF | - | 2.5 | 5 | |
| | CB3LV | | 1.5 MHz to 20 MHz $C_L$=15pF | - | 6 | 8 | |
| | | | 20.1 MHz to 80 MHz $C_L$=15pF | - | 3 | 4 | |
| | | | 80.1 MHz to 160 MHz $C_L$=15pF | - | 1.5 | 3 | |
| | Start Up Time | $T_S$ | Application of $V_{CC}$ | - | - | 10 | ms |
| | Enable Function (See Note 2) | | | | | | V |
| | Enable Input Voltage | $V_{IH}$ | Pin 1 Logic '1', Output Enabled | 2.0 | - | - | |
| | Disable Input Voltage | $V_{IL}$ | Pin 1 Logic '0', Output Disabled | - | - | 0.8 | |
| | Enable Time | | Pin 1 Logic '1' | | | | |
| | CB3 | $T_{PLZ}$ | | - | - | 100 | ns |
| | CB3LV | | | - | - | 10 | ms |
| | Phase Jitter | tjms | Bandwidth 12 kHz - 20 MHz | - | - | 1 | ps RMS |

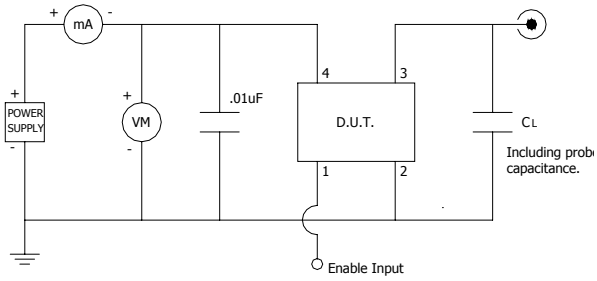
Notes:
1. Inclusive of initial tolerance at time of shipment, changes in supply voltage, load, temperature and first year aging at an average operating temperature of +40 °C.
2. Reference CTS Application Note 014-0002-0.

### CMOS/TTL OUTPUT WAVEFORM




DUTY CYCLE = t/T x 100 (%)

### TEST CIRCUIT, CMOS LOAD




### ENABLE TRUTH TABLE

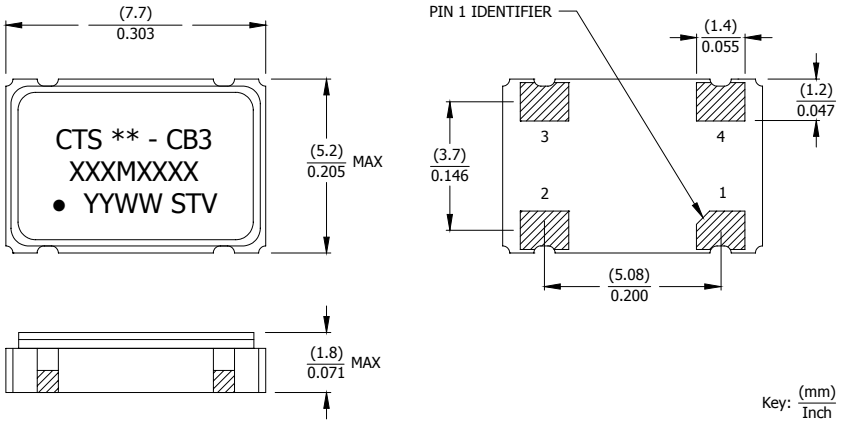
| PIN 1 | PIN 3 |
|---|---|
| Logic '1' | Output |
| Open | Output |
| Logic '0' | High Imp. |

### D.U.T. PIN ASSIGNMENTS

| PIN | SYMBOL | DESCRIPTION |
|---|---|---|
| 1 | EOH | Enable Input |
| 2 | GND | Circuit & Package Ground |
| 3 | Output | RF Output |
| 4 | $V_{CC}$ | Supply Voltage |

## MECHANICAL SPECIFICATIONS

### PACKAGE DRAWING



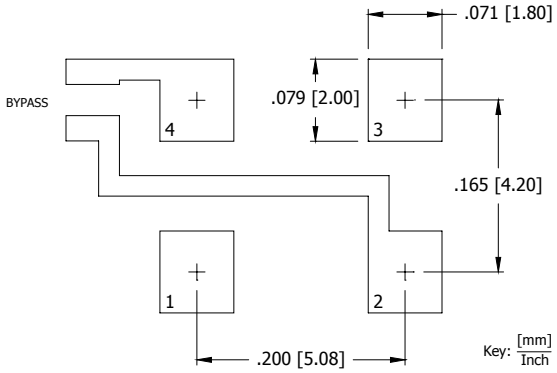

### MARKING INFORMATION

1. ** - Manufacturing Site Code.
2. XXXMXXXX - Frequency marked with 4 significant digits after the 'M'.
3. YYWW – Date code, YY – year, WW – week.
4. ST – Frequency stability/temperature code. (Reference Ordering Information.)
5. V – Voltage code. 3 = 3.3V, 5 = 5.0V.

### NOTES

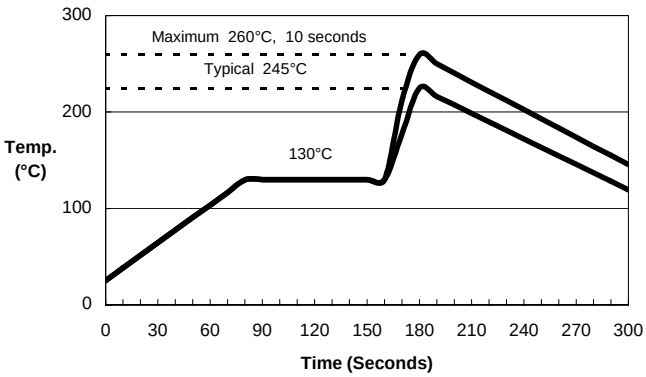
1. Termination pads (e4), barrier-plating is nickel (Ni) with gold (Au) flash plate.
2. Reflow conditions per JEDEC J-STD-020.

### SUGGESTED SOLDER PAD GEOMETRY

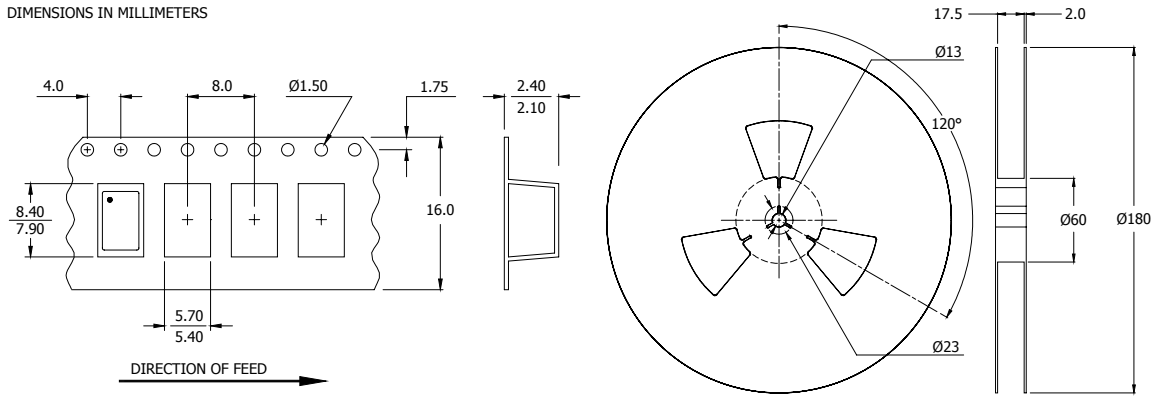



$C_{BYPASS}$ should be ≥ 0.01 uF.

### SUGGESTED REFLOW PROFILE



## TAPE AND REEL INFORMATION




Device quantity is 1,000 pieces per 180mm reel.

## ENVIRONMENTAL SPECIFICATIONS

| | |
|---|---|
| Temperature Cycle: | 400 cycles from –55°C to +125°C, 10 minute dwell at each temperature, 1 minute transfer time between temperatures. |
| Mechanical Shock: | 1,500g's, 0.5mS duration, ½ sinewave, 3 shocks each direction along 3 mutually perpendicular planes (18 total shocks). |
| Sinusoidal Vibration: | 0.06 inches double amplitude, 10 to 55 Hz and 20g's, 55 to 2,000 Hz, 3 cycles each in 3 mutually perpendicular planes (9 times total). |
| Gross Leak: | No leak shall appear while immersed in an FC40 or equivalent liquid at +125°C for 20 seconds. |
| Fine Leak: | Mass spectrometer leak rates less than $2x10^{-8}$ ATM cc/sec air equivalent. |
| Resistance to Solder Heat: | Product must survive 3 reflows of +260°C peak, 10 seconds maximum. |
| High Temperature Operating Bias: | 2,000 hours at +125°C, maximum bias, disregarding frequency shift. |
| Frequency Aging: | 1,000 hours at +85°C, full bias, less than ±5 ppm shift. |
| Moisture Sensitivity Level: | Level 1 per JEDEC J-STD-020. |

## QUALITY AND RELIABILITY

Quality systems meet or exceed the requirements of ISO 9000:2000 standards.