



XAPP453 (v1.1.1) June 23, 2008

The 3.3V Configuration of Spartan-3 FPGAs

Summary

This application note provides an approach to configure Spartan®-3 FPGAs from a 3.3V interface. It provides a set of proven connection diagrams for each configuration mode. These diagrams are complete, ready-to-implement solutions.

The same approach can be applied to the Spartan-3E family, although pin names and banks are different. The Spartan-3A/3AN/3A DSP families allow V_{CCAUX} to be 3.3V, simplifying the interface. See [UG332](#) for details on configuration for these families.

Introduction

The configuration process programs FPGAs with a user-specific design by writing bitmap data to a Configuration port. Associated with the port are several configuration signals. The simplest, most direct interface possible employs signals with 2.5V swing (i.e., *standard* configuration using LVCMOS25). This interface requires the fewest possible external components.

FPGAs can be programmed not only through the Configuration port but through the JTAG (Boundary-Scan) port as well. The simplest JTAG interface also uses 2.5V signals (i.e., LVCMOS25).

Devices on many of today's boards, such as PROMs or microcontrollers, may only be able to drive 3.3V signals to the FPGA's configuration and JTAG ports. In such cases, configuration with 3.3V signals is easy to achieve, requiring only a few additional external resistors.

Configuration and JTAG Pins

Configuration pins fall into one of two categories, *Dedicated* or *Dual-Purpose*. Each Dedicated pin carries one kind of signal devoted to a special purpose. Each Dual-Purpose pin carries a specialized signal during configuration; once in User mode, the pin functions as an I/O. All JTAG pins are Dedicated.

The Dedicated configuration pins are PROG_B, HSWAP_EN (HSWAP in the Spartan-3E family), CCLK, DONE, and M0-M2. The Dedicated JTAG pins are TDI, TMS, TCK, and TDO. All these pins use the V_{CCAUX} lines to power their associated internal circuits.

The Dual-Purpose configuration pins are INIT_B, DOUT, BUSY, RDWR_B, CS_B, and DIN/D0-D7. Each pin, according to its bank placement, uses the V_{CCO} rails for either Bank 4 (V_{CCO_4}) or Bank 5 (V_{CCO_5}). All the pins used in the serial configuration modes (INIT_B, DOUT, and DIN) rely on V_{CCO_4} power. Pins used in the parallel configuration and Readback modes not only use V_{CCO_4} to power the D0-D3 and BUSY pins, but also require V_{CCO_5} for the D4-D7, RDWR_B, and CS_B pins.

In Spartan-3E FPGAs, the Dual-Purpose configurations pins are supplied by the V_{CCO_2} rail, plus V_{CCO_1} in BPI mode.

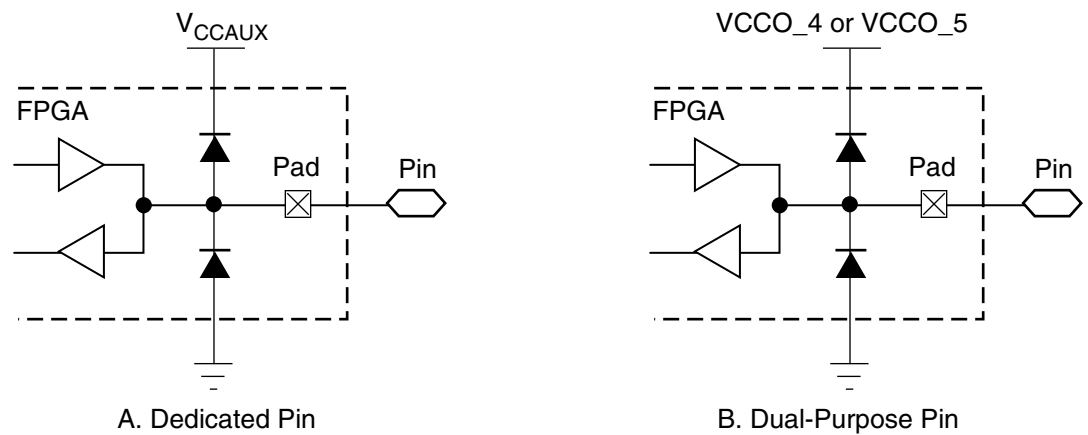
Table 1 lists the configuration and JTAG pins by category as well as indicating the associated power rails.

Table 1: Dedicated and Dual-Purpose Pins

Pin	Bank	V _{CCAUX}	V _{CCO}		V _{REF}
			Output Driver	Input Stage	
Dedicated Pins					
PROG_B	-	2.5V	-	-	-
HSWAP_EN	-	2.5V	-	-	-
TDI	-	2.5V	-	-	-
TMS	-	2.5V	-	-	-
TCK	-	2.5V	-	-	-
TDO	-	2.5V	-	-	-
CCLK	-	2.5V	-	-	-
DONE	-	2.5V	-	-	-
M0-M2	-	2.5V	-	-	-
Dual-Purpose Pins					
INIT_B	4	-	-	VCCO_4	-
DOUT	4	-	VCCO_4	-	-
BUSY	4	-	VCCO_4	-	-
DIN	4	-	-	VCCO_4	-
D0-D3	4	-	VCCO_4 for readback	VCCO_4 for configuration	-
D4-D7	5	-	VCCO_5 for readback	VCCO_5 for configuration	-
RDWR_B	5	-	-	VCCO_5	-
CS_B	5	-	-	VCCO_5	-

Idealized Circuit Structure for Dedicated and Dual-Purpose Pins

The main difference between the internal I/O structures of Dedicated and Dual-Purpose pins concerns the rail that provides power. Figure 1 shows idealized bidirectional I/O circuits for each category of pin. As described in the preceding section, V_{CCAUX} powers the Dedicated pins (A), whereas V_{CCO} (Bank 4 or 5) powers the Dual-Purpose pins (B). Pins providing only the input function lack the driver portion of the circuit. Pins providing only the output function lack the receiver portion. An open-drain pin, such as INIT_B or DONE (when so configured), has a driver for sinking Low logic levels as well as a receiver for sensing the signal state.



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Figure 1: Idealized I/O Circuits for Dedicated and Dual-Purpose Pins

By design, all of the FPGA's signal-carrying pins can handle 3.3V signals. A pair of diodes is associated with every such pin. The upper or Power diode is connected between the power rail and the I/O pad. The lower or GND diode lies between the pad and GND. These diodes are present for every signal standard, all of the time.

During normal operation, these diodes are always off; therefore, they are effectively invisible. The V_{IN} specification in the Absolute Maximum Ratings table of the Spartan-3 FPGA Data Sheet requires that the I/O pad voltage (V_{IN}) be less than or equal to the rail voltage (V_{CCAUX} or V_{CCO}) plus the diode turn-on voltage ($\sim 0.5V$). The Power diode is off whenever the applicable condition below is met:

- ◆ For Dedicated pins:

$$V_{IN} \leq V_{CCAUX} + 0.5V \quad (1)$$

- ◆ For Dual-Purpose pins:

$$V_{IN} \leq V_{CCO} + 0.5V \quad (2)$$

When performing 3.3V configuration, it is possible for Power diodes to turn on whenever the applicable condition above is not met. For example, a 3.3V signal applied directly to the I/O pin when the rail voltage (V_{CCAUX} or V_{CCO}) is 2.5V gives rise to a Power diode current that our application solutions must address.

Standard Configuration Interfaces

The *standard* configuration interface uses LVCMOS25 (2.5V swing, 12 mA drive and Fast slew rate) for all signals. It uses a supply voltage of 2.5V for the V_{CCAUX} rail as well as the V_{CCO_4} and V_{CCO_5} rails. The Spartan-3 FPGA Data Sheet discusses standard configuration at length, with a functional description and connection diagrams in Module 2 as well as timing specifications in Module 3. The data sheet for Xilinx Platform Flash PROMs provides additional connection diagrams.

The standard configuration interface only requires 2.5V on the V_{CCO_4} and V_{CCO_5} rails from power-on to the end of configuration. After completing configuration, it may be possible to switch to a supply voltage permitting signal swings other than 2.5V, depending on the requirements of the application in question. Such an approach permits a standard interface during configuration, then enables Dual-Purpose I/Os to handle 3.3V signals in the User mode.

The standard JTAG interface uses LVCMOS25 for all four of its signals. In this case, the associated V_{CCAUX} rail is at 2.5V, as usual. The data sheet for Xilinx Platform Flash PROMs provides connection diagrams for the standard JTAG interface.

Approach to a 3.3V Configuration Interface

The solutions presented in this application note are useful when it is necessary to configure Spartan-3 FPGAs using 3.3V signals. This requirement can arise for the following reasons:

1. External devices can only provide 3.3V configuration signals to the FPGA. Signals with 2.5V swing are not possible.
2. When Dual-Purpose pins need to function as 3.3V I/Os in User mode, it may be undesirable to switch the VCCO_4 and VCCO_5 rail voltages from 2.5V to 3.3V after the configuration process is complete.

The recommended approach for achieving a 3.3V-tolerant configuration interface treats Dedicated and Dual-Purpose pins and their associated power rails differently.

Dual-Purpose Pins

To power the Dual-Purpose pins, apply 3.3V to the FPGA's VCCO_4 and (if needed) the VCCO_5 rails. Using this higher voltage, rather than the standard 2.5V, scales up the High logic level of the Dual-Purpose outputs, while at the same time, proportionately increasing the switching thresholds of the inputs.

The Dual-Purpose outputs DOUT, BUSY, and D0-D7 (during Readback) now switch from GND to 3.3V. Connect these outputs as needed directly to the inputs of any 3.3V, compatible external device. Here, the noise margin is fully suitable for 3.3V signals.

The Dual-Purpose INIT_B pin is an open-drain output. An internal pull-up resistor from the INIT_B pin to the VCCO_4 rail permits a High logic level. As a standard recommendation, tie an external 4.7K Ω pull-up resistor from the INIT_B pin to the VCCO_4 rail (at 3.3V) as well. When configuring multiple FPGAs, tie together all INIT_B pins. In this last case, connect a *single* external pull-up resistor between the common node and the VCCO_4 rail.

The Dual-Purpose inputs INIT_B (the sensing function), DIN, D0-D7 (during configuration), RDWR_B, and CS_B can accept 3.3V signals directly from external devices. With the V_{CCO} rails at 3.3V, the V_{IN} condition for Dual-Purpose pins (see equation 2 on page 3) is satisfied and the power diodes are off.

Dedicated Pins

To power the Dedicated pins, apply 2.5V to the FPGA's V_{CCAUX} rail, as specified in the Spartan-3 Family Data Sheet.

With the V_{CCAUX} rails at 2.5V, the Dedicated outputs TDO, DONE (with BitGen option **DriveDone = Yes**), and CCLK (in the master configuration modes) switch from GND to 2.5V. Connect these outputs as needed directly to the inputs of any 3.3V compatible external device. The High logic level, V_{OH}, for the LVCMOS25 standard at the FPGA's Dedicated outputs is 2.5V, whereas V_{IH} min. at an external receiver's 3.3V LVCMOS inputs is 2.0V. The resulting noise margin of 500mV is reasonable for configuration purposes.

The Dedicated DONE pin becomes an open-drain output when the BitGen option **DriveDone** is set to **No**. In this case, tie an external 330 Ω pull-up resistor from the DONE pin to the V_{CCAUX} rail (at 2.5V). When configuring multiple FPGAs, tie together all DONE pins. In this last case, connect a *single* external pull-up resistor between the common node and the V_{CCAUX} rail. The open-drain option has its uses; however, in many applications, a DONE pin with full totem pole drive (**DriveDone = Yes**) is preferable, if only because it permits a faster transition time.

With a 2.5V V_{CCAUX} rail and 3.3V signals applied to Dedicated inputs, the V_{IN} condition is not satisfied. As a result, internal Power diodes turn on, causing *reverse currents* to flow from the inputs to the V_{CCAUX} rail. A resistor (R_{SER}) in series with the input is recommended to limit the current. Choose the value of the resistor to keep the current at or under 10 mA. Worst-case load-line analysis using IBIS models indicates that a 5% resistor with a 68 Ω value keeps the input current just under 10 mA. Put these resistors in series with the Dedicated inputs PROG_B, TDI, TMS, TCK, and CCLK (in the slave configuration modes) as needed. The

remaining Dedicated inputs, HSWAP_EN and M0-M2, are usually static. Connect these inputs directly to either GND or V_{CCAUX} , according to the application's requirements.

Managing Reverse Current

As explained in the previous section, applying 3.3V signals to any of the Dedicated inputs PROG_B, TDI, TMS, TCK, and CCLK (slave modes) causes reverse current to flow into the V_{CCAUX} rail.

Figure 2 shows that the total reverse current (I_{REV}) is the cumulative result of all the input current contributions (I_{IN}).

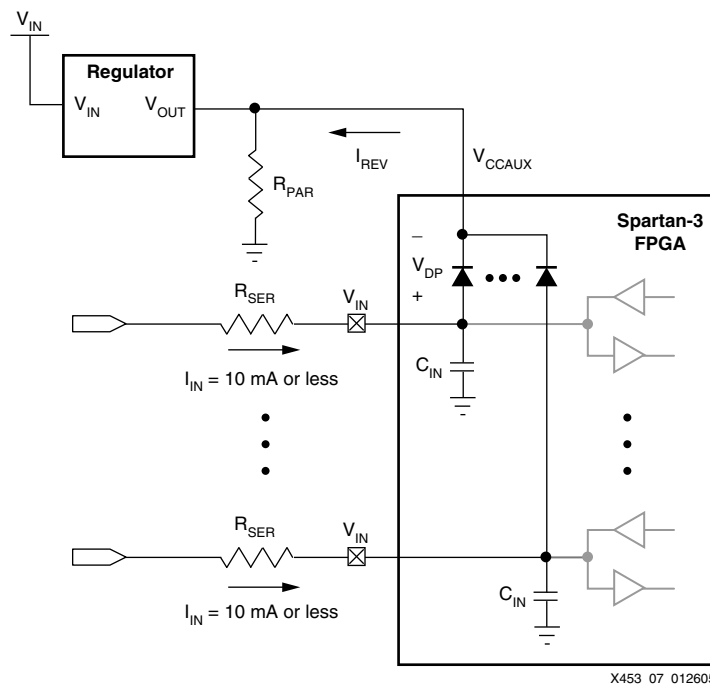


Figure 2: Reverse Current Solution for Regulator

For N Dedicated inputs with Power diodes on, I_{REV} is the sum of the I_{IN} currents:

$$I_{REV} = \sum_{i=1}^N I_{IN} \quad (3)$$

If series resistors (R_{SER}) limit each diode current to 10 mA, then

$$I_{REV} = N (10\text{mA}) \quad (4)$$

The reverse current does not interfere with FPGA operation. Still, care must be taken to ensure proper regulation of the V_{CCAUX} voltage. There are two ways to make sure that the V_{CCAUX} regulator works correctly:

1. Use a regulator specified to maintain its intended output voltage while sinking the anticipated reverse current.
2. Add a shunt resistor (R_{PAR}) from the regulator output to GND (Figure 2). Choose R_{PAR} to carry a current equal to I_{REV} , as follows:

$$R_{PAR} = \frac{V_{CCAUX \text{ min}}}{I_{REV}} \quad (5)$$

Use the *standard* resistor value for R_{PAR} equal to or just under the value predicted by equation 5.

Several inputs with Power diodes on can result in a large I_{REV} value, so that equation 5 yields a rather low R_{PAR} value. In such cases, it is possible to increase R_{PAR} by raising R_{SER} above 68Ω . The higher R_{SER} value slows the signal transitions as it reduces the I_{IN} current. Make sure the transition time is not too long.

Contact your preferred vendor of power solutions for more information on the two methods for managing reverse current.

Connection Diagrams for 3.3V Configuration

The schematics below show how to connect the Dedicated and Dual-Purpose pins for the 3.3V configuration of Spartan-3 devices. A schematic is provided for each of the configuration modes.

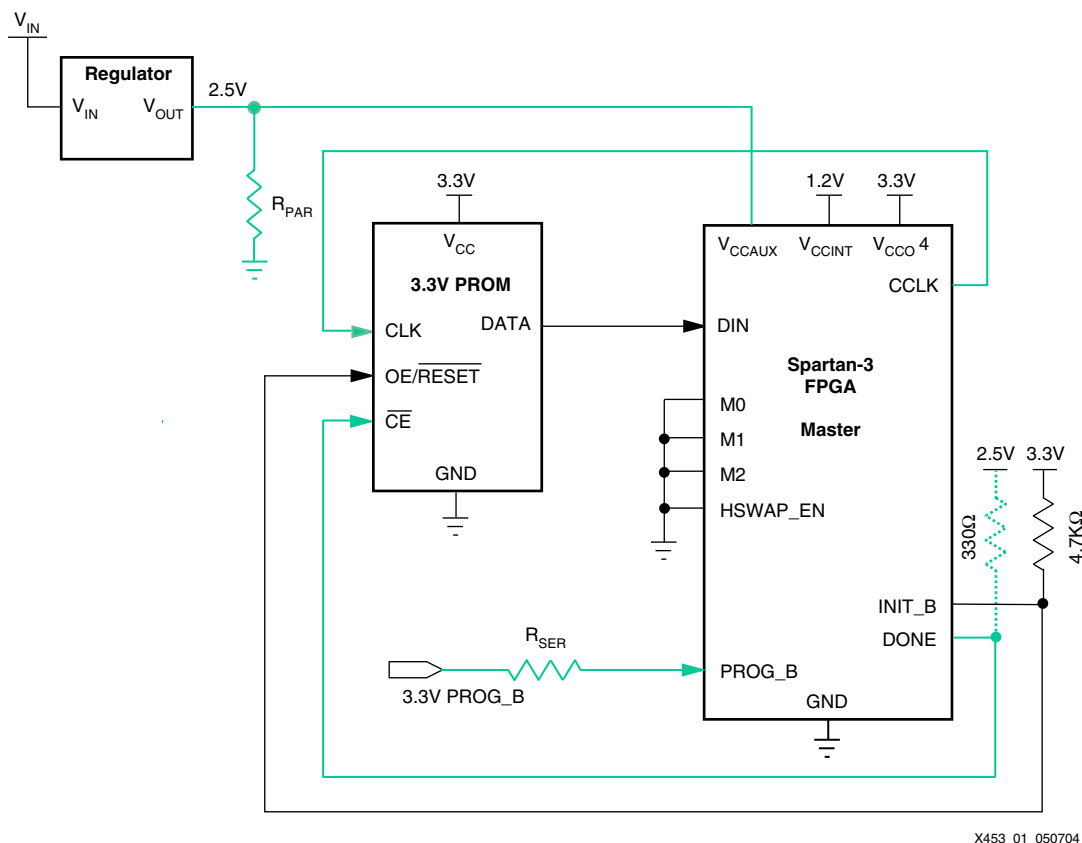
In each schematic, the solid black lines represent signal paths that remain the same as those in the standard 2.5V version of the interface. As part of a 3.3V interface, these lines need no special consideration.

The solid gray lines (green when viewed on a monitor) indicate signal paths for which specific measures are taken to achieve 3.3V tolerance. These lines show where the resistors R_{SER} and R_{PAR} are added, the former to limit current entering Dedicated inputs and the latter to ensure proper power regulation. Solid gray lines can also indicate the reduced noise margin associated with Dedicated outputs. For more information on noise margin and the resistors, see [“Approach to a 3.3V Configuration Interface.”](#)

The dotted gray line (green as seen from a monitor) shows the pull-up resistor tied to the open-drain DONE pin. This resistor is only added when the BitGen option `DriveDone = No`. The DONE output exhibits reduced noise margin when the pull-up resistor is connected to the 2.5V rail. The same is true when `DriveDone = Yes` and no pull-up resistor is present.

3.3V Master Serial Configuration

Figure 3 shows the connections for 3.3V Master Serial configuration.



Notes:

1. With HSWAP_EN Low, the internal pull-up resistors connected to all I/Os are enabled. To disable these resistors, tie HSWAP_EN High.

Figure 3: Connection Diagram for 3.3V Master Serial Mode

Calculate the resistor values as follows:

- $R_{SER} = 68\Omega$ limits the current entering each Input to 9.5 mA
- $N = 1$ input has a diode on

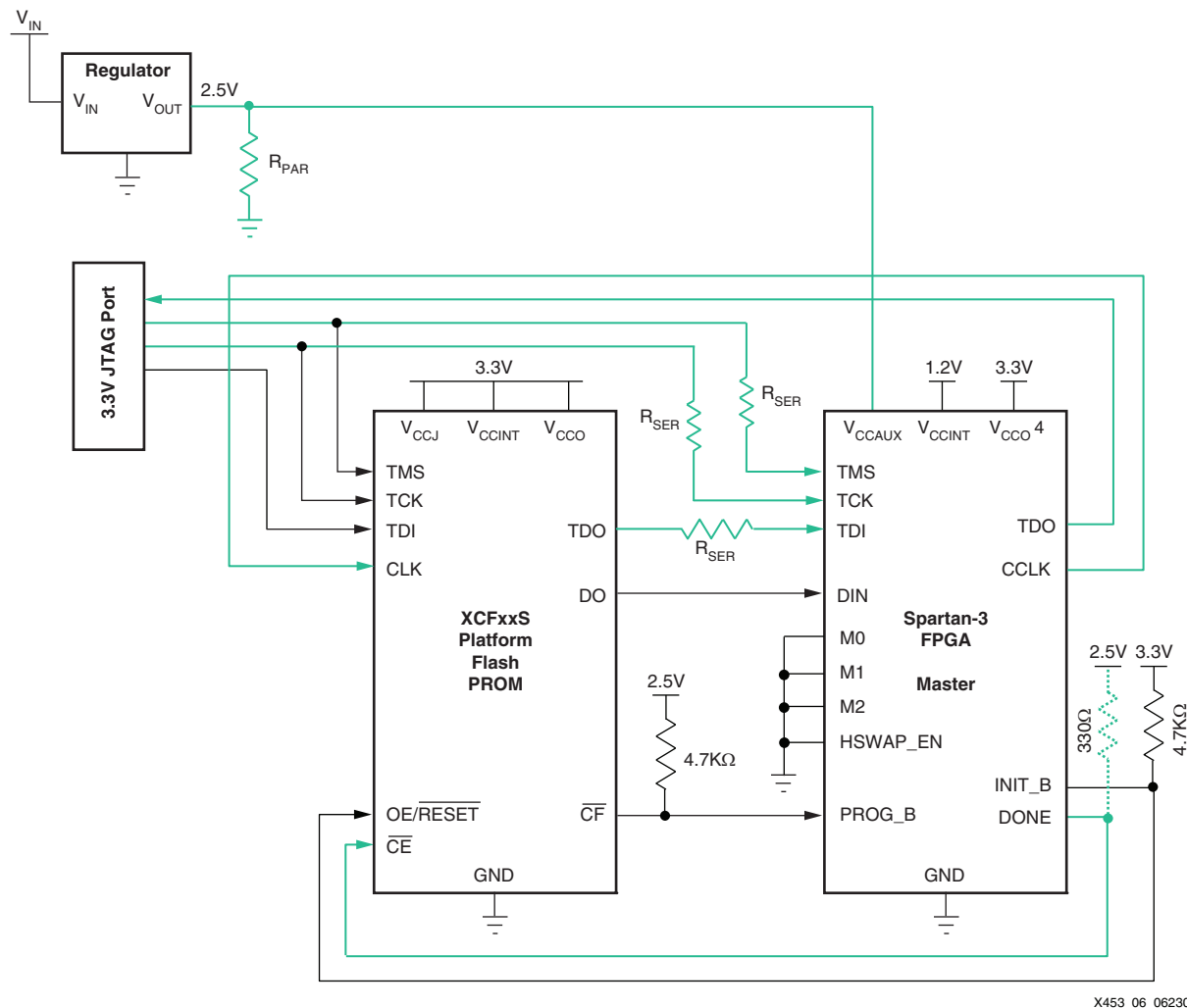
$$R_{PAR} = \frac{V_{CCAUX} \min}{NI_{IN}}$$

$$= \frac{2.375V}{(1)(9.5mA)}$$

$R_{PAR} = 250\Omega$ or 240Ω for a standard value 5% resistor

3.3V Master Serial Configuration with Platform Flash PROM

Figure 4 shows the connections for 3.3V Master Serial configuration with a Platform Flash PROM.



Notes:

1. With HSWAP_EN Low, the internal pull-up resistors connected to all I/Os are enabled. To disable these resistors, tie HSWAP_EN High.

Figure 4: Connection Diagram for 3.3V Master Serial Mode with Platform Flash PROM

Calculate the resistor values as follows:

- $R_{SER} = 68\Omega$ limits the current entering each Input to 9.5 mA
- $N = 3$ inputs have diodes on

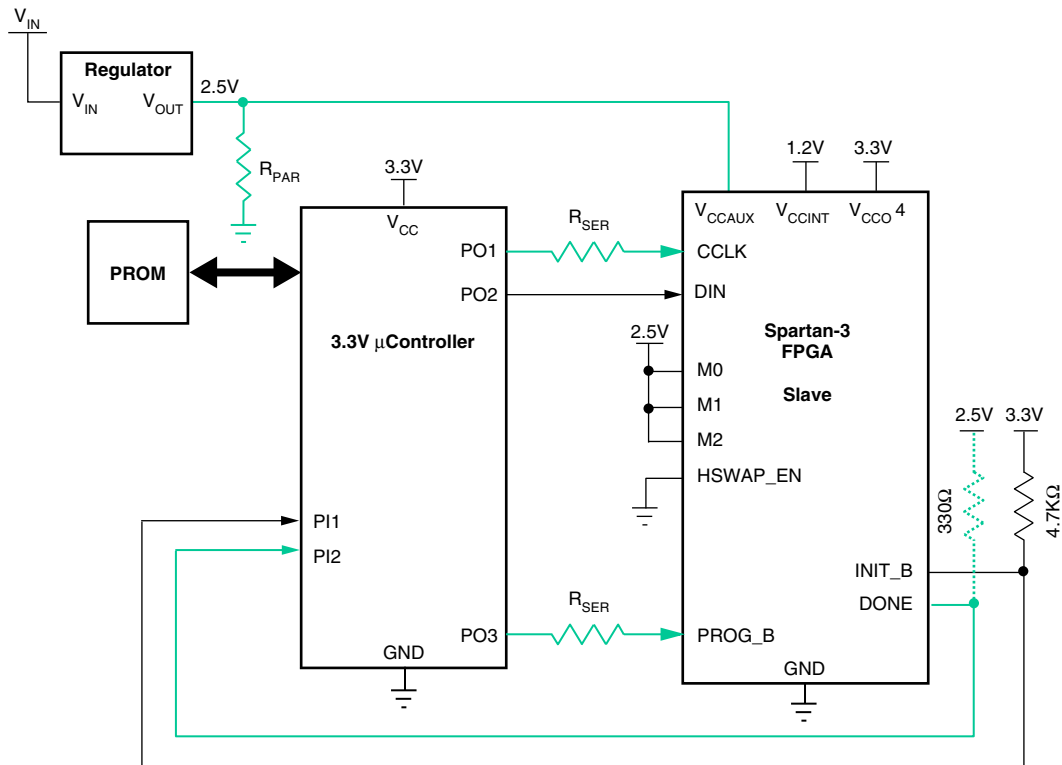
$$R_{PAR} = \frac{V_{CCAUX \min}}{NI_{IN}}$$

$$= \frac{2.375V}{(3)(9.5mA)}$$

$R_{PAR} = 83\Omega$ or 82Ω for a standard value 5% resistor

3.3V Slave Serial Configuration

Figure 5 shows the connections for 3.3V Slave Serial configuration.



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Notes:

1. With HSWAP_EN Low, the internal pull-up resistors connected to all I/Os are enabled. To disable these resistors, tie HSWAP_EN High.

Figure 5: Connection Diagram for 3.3V Slave Serial Mode

Calculate the resistor values as follows:

- PI_n and PO_n are programmable I/Os
- $R_{SER} = 68\Omega$ limits the current entering each Input to 9.5 mA
- $N = 2$ inputs have diodes on

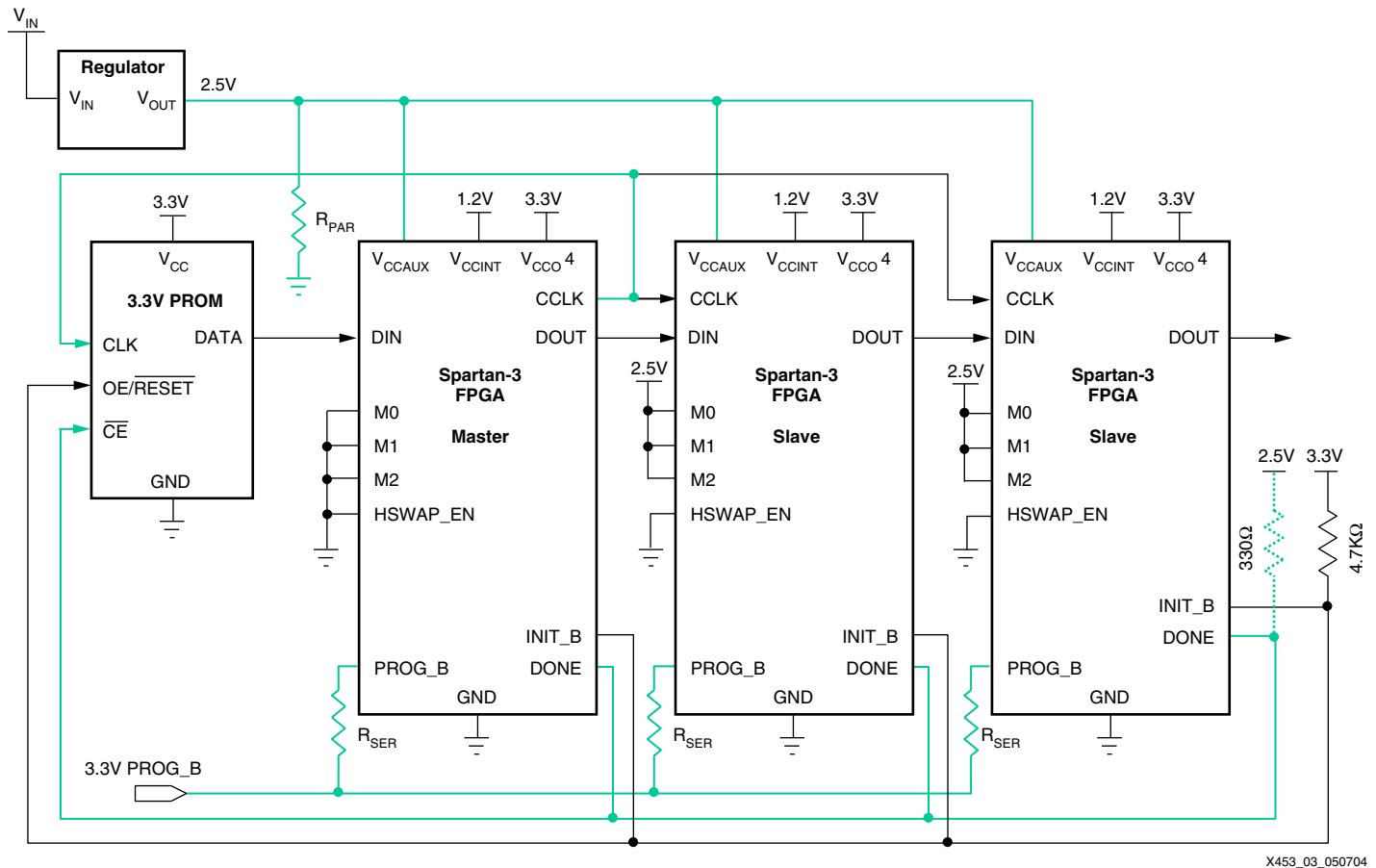
$$R_{PAR} = \frac{V_{CCAUX \text{ min}}}{NI_{IN}}$$

$$= \frac{2.375V}{(2)(9.5mA)}$$

$$R_{PAR} = 125\Omega \text{ or } 120\Omega \text{ for a standard value 5\% resistor}$$

3.3V Daisy-Chain Configuration

Figure 6 shows the connections for Daisy-Chain configuration.



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Notes:

1. With HSWAP_EN Low, the internal pull-up resistors connected to all I/Os are enabled. To disable these resistors, tie HSWAP_EN High.

Figure 6: Connection Diagram for 3.3V Daisy-Chain Configuration

Calculate the resistor values as follows:

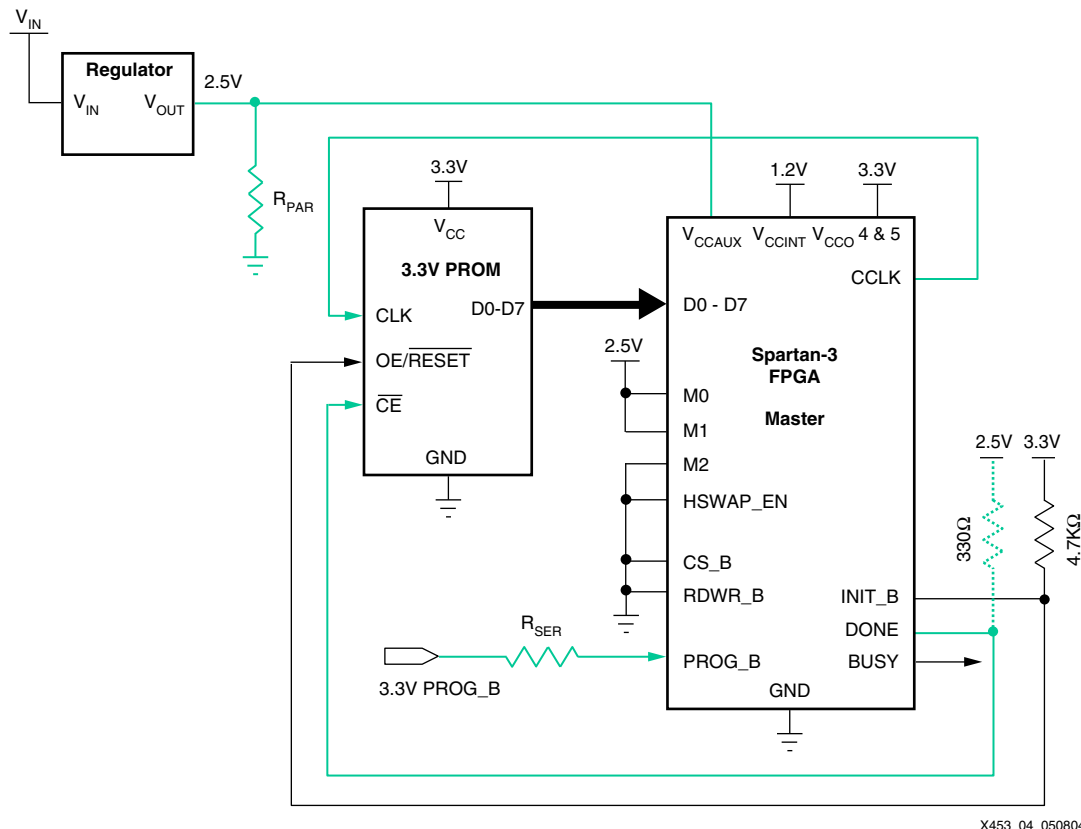
- $R_{SER} = 68\Omega$ limits the current entering each Input to 9.5 mA
- $N = 3$ inputs have diodes on

$$R_{PAR} = \frac{V_{CCAUX \min}}{N I_{IN}} = \frac{2.375V}{(3)(9.5mA)}$$

$R_{PAR} = 83\Omega$ or 82Ω for a standard value 5% resistor

3.3V Master Parallel Configuration

Figure 7 shows the connections for 3.3V Master Parallel configuration.



Notes:

1. With HSWAP_EN Low, the internal pull-up resistors connected to all I/Os are enabled. To disable these resistors, tie HSWAP_EN High.

Figure 7: Connection Diagram for 3.3V Master Parallel Mode

Calculate the resistor values as follows:

- $R_{SER} = 68\Omega$ limits the current entering each Input to 9.5 mA
- $N = 1$ input has a diode on

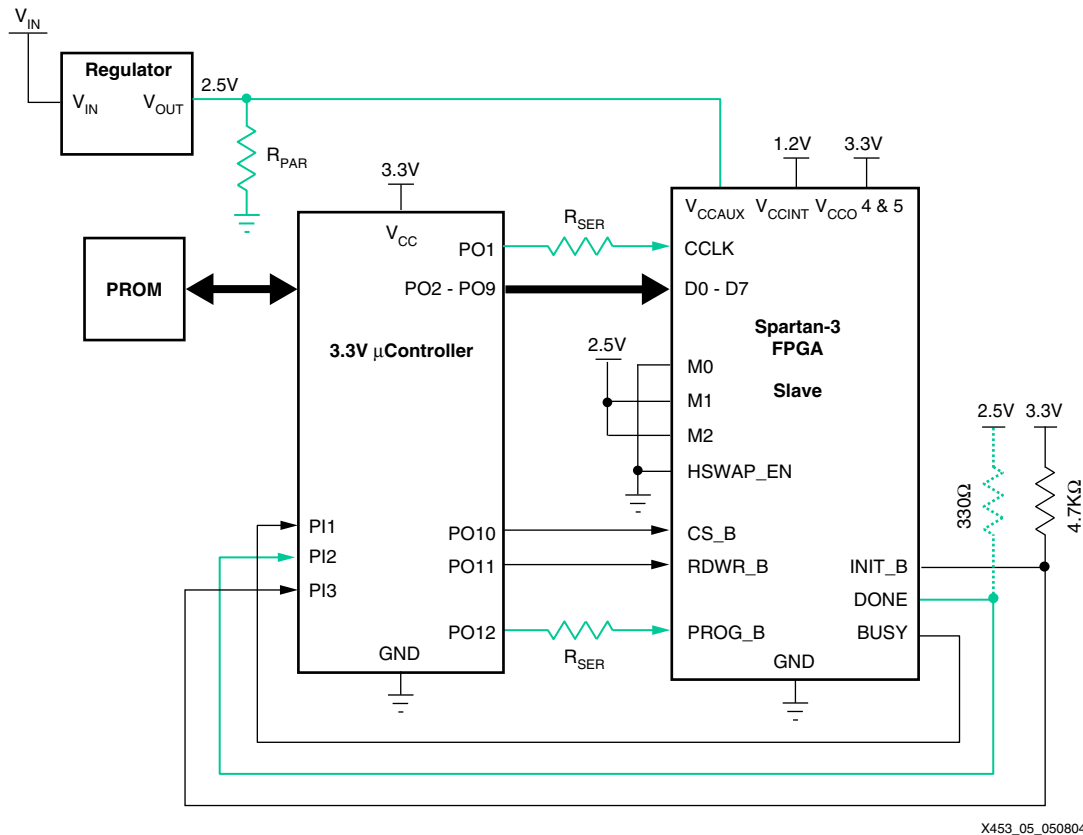
$$R_{PAR} = \frac{V_{CCAUX \min}}{NI_{IN}}$$

$$= \frac{2.375V}{(1)(9.5mA)}$$

$R_{PAR} = 250\Omega$ or 240Ω for a standard value 5% resistor

3.3V Slave Parallel Configuration

Figure 8 shows the connections for 3.3V Slave Parallel configuration.



Notes:

1. With HSWAP_EN Low, the internal pull-up resistors connected to all I/Os are enabled. To disable these resistors, tie HSWAP_EN High.

Figure 8: Connection Diagram for 3.3V Slave Parallel Mode

Calculate the resistor values as follows:

- PI_n and PO_n are programmable I/Os
- $R_{SER} = 68\Omega$ limits the current entering each Input to 9.5 mA
- $N = 2$ inputs have diodes on

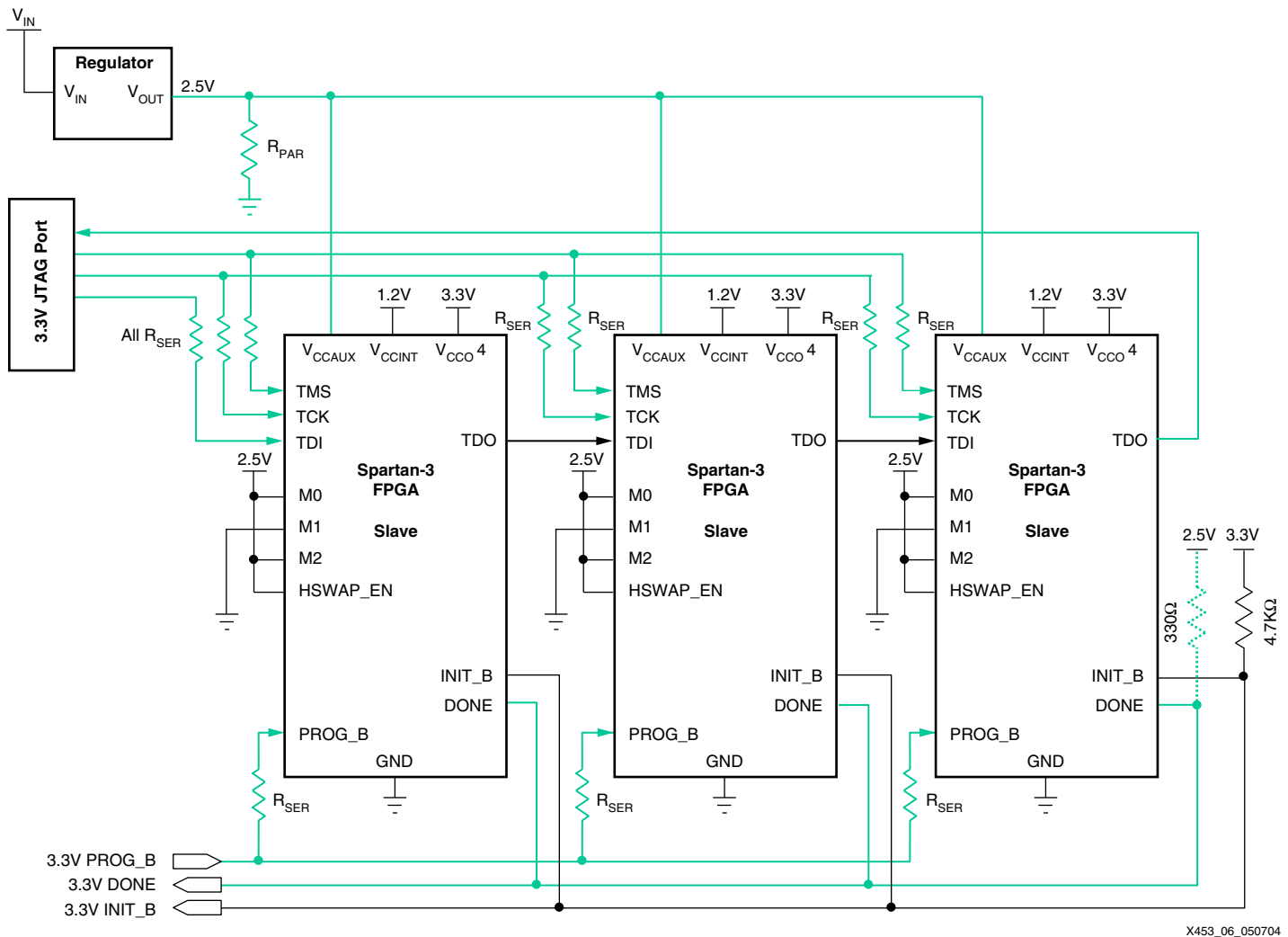
$$R_{PAR} = \frac{V_{CCAUX} \min}{NI_{IN}}$$

$$= \frac{2.375V}{(2)(9.5mA)}$$

$R_{PAR} = 125\Omega$ or 120Ω for a standard value 5% resistor

3.3V JTAG Configuration

Figure 9 shows the connections for JTAG configuration.



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Notes:

- With HSWAP_EN High, the internal pull-up resistors connected to all I/Os are disabled. To enable these resistors, tie HSWAP_EN Low.

Figure 9: Connection Diagram for 3.3V Boundary-Scan (JTAG) Mode

Calculate the resistor values as follows:

- $R_{SER} = 68\Omega$ limits the current entering each Input to 9.5 mA
- $N = 10$ inputs have diodes on

$$R_{PAR} = \frac{V_{CCAUX} \min}{NI_{IN}}$$

$$= \frac{2.375V}{(10)(9.5mA)}$$

$R_{PAR} = 25\Omega$ or 24Ω for a standard value 5% resistor. Because this multiple-FPGA example has as many as 10 I_{IN} currents contributing to the total reverse current, R_{PAR} is low. An application with fewer FPGAs would use a higher R_{PAR} value. See the end of “Managing Reverse Current,” page 5 for a method to increase this resistance.

Conclusion

Configuration of Spartan-3 FPGAs takes place through either the Configuration port or the JTAG port. The standard interface uses 2.5V signals; however, some applications need 3.3V signals instead. Configuration using 3.3V signals is easy to achieve, requiring the addition of only a few external resistors. The connection diagrams included in this application note provide complete 3.3V solutions for all modes of configuration.

References

The following Xilinx documents provide supplemental material useful with this application note:

- *Spartan-3 FPGA Family Data Sheet*, [DS099](#)
- *Platform Flash In-System Programmable Configuration PROMs Data Sheet*, [DS123](#)
- *Powering and Configuring Spartan-3 Generation FPGAs in PCI Compliant Applications*, [XAPP457](#)
- *Eliminating I/O Coupling Effects When Interfacing Large-Swing Single-Ended Signals to User I/O Pins on Spartan-3 Generation FPGAs*, [XAPP459](#)
- *Spartan-3 Generation Configuration User Guide*, [UG332](#)

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
02/02/05	1.0	Initial Xilinx release.
04/03/06	1.1	Updated resistor values to reflect the Spartan-3 IBIS file, revision 3.4.
06/23/08	1.1.1	Updated families referenced. Updated links.