A Quick JTAG ISP Checklist

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Summary

Most Xilinx CPLDs, PROMs, and FPGAs have an IEEE Standard 1149.1 (JTAG) port. Xilinx devices with a JTAG port are in-system programmable (ISP) through the JTAG port. The ISP feature is beneficial for fast prototype development. This application note describes a short list of considerations needed to get the best performance from your ISP designs. The list of considerations generally applies to all Xilinx ISP device families. Special considerations for Xilinx CPLDs are highlighted.

Families

XC9500/XL/XV CPLDs, CoolRunner™ CPLDs, CoolRunner-II CPLDs, Spartan™ FPGA families, Virtex™ FPGA families, XC18V00 PROMs, and Platform Flash XCF00S/XCF00P PROMs.

Overview

All JTAG-capable devices on a board can be connected in a single JTAG device daisy-chain enabling JTAG software to control multiple devices through a single JTAG cable connection. Thus, the Xilinx iMPACT software can in-system program all Xilinx CPLDs, PROMs, and FPGAs on a board through a Xilinx JTAG cable.

Careful design practices for the JTAG connections are essential for ensuring the integrity of the JTAG chain and for maximizing potential in-system programming performance.

In-system programmable PROMs and CPLDs contain sophisticated circuits for programming internal, non-volatile configuration memories. Internal charge pumps create high voltages for programming the memories. The charge pumps require a modest amount of care in the design of the board-level power supply delivery system. The voltages to which the pumps must rise are directly derived from the external voltage supplied to the VCCINT pins on the CPLDs or ISP PROMs. Because these elevated voltages must be within their prescribed values to properly program the CPLD or ISP PROM, the supply voltages must be clean (noise free) and within the specified range.

The following are key JTAG design and usage rules for in-system programming Xilinx devices:

- Make sure V_{CC} is within the range specified in the device data sheet.
- For CPLDs and PROMs, provide both 0.1 µF and 0.01 µF capacitors at every V_{CC} point of the chip, attached directly to the nearest ground. For FPGAs, see the FPGA family's user guide or FPGA family's PCB designer's guide for decoupling capacitor recommendations.

JTAG specifications do require pull-up resistance to be supplied internally to the TDI and TMS pins by the chips, but no particular value is required. Not specifying a value lets vendors supply whatever they choose and still remain in full compliance. Because of this, very long JTAG chains or chains using parts from multiple vendors can present significant loading to the ISP drive cable. In these cases, it is wise to:

- Use the latest Xilinx download cables and their ribbon cable connectors.
- Consider including buffers on TMS or TCK signals interleaved at various points on your JTAG circuitry to account for unknown device impedance. The signal integrity of the TCK signal is critical because all JTAG operations for all devices in a JTAG chain are synchronous to the TCK clock. Use the necessary design practices for routing and ensuring the integrity of the TCK clock signal.

The Xilinx iMPACT downloading software is continuously being improved. With this in mind, it is appropriate to:

- Always be certain to use the latest version of the Xilinx iMPACT software.

In some cases, XC9500/XL/XV designs appear to experience erase time or programming time extension as the design progresses — particularly for long chains. This extension is probably due to the fact that parts being reprogrammed have a large number of switching signals arriving at its inputs, which differs from the initial case where a blank part is being programmed. If this situation occurs, there is a way to lower the noise:

- Put the rest of the JTAG chain into HIGHZ when programming a troublesome part. HIGHZ is a JTAG instruction that tristates the device I/O pins. Within iMPACT, set the "Use HIGHZ instead of BYPASS" configuration preference in the **Edit** → **Preferences** dialog box.

  Setting this preference limits the number of additional signals presented both to the system and frequently to a troublesome part (because parts within a given chain tend to be connected amongst themselves).
- If free running clocks are delivered into the ISP CPLD, it might be necessary to disconnect or disable the clocks in order to avoid clock noise during CPLD programming.

  The best way to disable the clock input is to use a commercially available clock generation device with an output enable/disable feature.

  Note: The IEEE Standard 1149.1 does not specify an operating voltage level for the JTAG port. The JTAG ports on different devices can operate at different voltage levels.
- Match the download cable V_{CC}/V_{REF} power supply to the JTAG I/O levels supported in the ISP devices.
- Ensure compatible signal levels for all JTAG I/Os. When devices permit operation of JTAG pins at one of many possible voltage levels, set all devices in the same chain to operate their JTAG ports at the same voltage level. Otherwise, when devices of different JTAG operating voltages are in the same JTAG chain, ensure the JTAG I/Os are compatible or tolerant of the JTAG signal levels on the board or use level translators to ensure compatible JTAG signal connections.

Checklist

- Make sure V_{CC} is within the range specified by the device data sheet.
- For CPLDs and PROMs, provide both 0.1 µF and 0.01 µF capacitors at every V_{CC} point of the device, attached directly to the nearest ground. For FPGAs, see the FPGA family's user guide or FPGA family's PCB designer's guide for decoupling capacitor recommendations.
- Use the latest Xilinx download cables and their ribbon cable connectors.
- Consider including buffers on TCK and TMS interleaved at various points on the application's JTAG circuitry to account for unknown device impedance. The signal integrity of the TCK signal is critical. Use the necessary design practices for routing and ensuring the integrity of the TCK clock signal.
- Always use the latest version of the Xilinx iMPACT software.
- Put the rest of the JTAG chain into HIGHZ when programming a troublesome device.
- Disable free-running clocks in order to minimize switching noise during programming.
- Match the download cable V_{CC}/V_{REF} power supply to the JTAG I/O voltage levels supported in the ISP devices.
- Ensure compatible signal levels for all JTAG I/Os. Set device JTAG operating voltages appropriately or use level translators when necessary.

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
04/14/00	1.0	Initial Xilinx release.
04/10/02	2.0	Revised.
06/07/02	2.1	Added Virtex Series FPGAs and Virtex-II Series Platform FPGAs to the Summary.
12/03/07	3.0	• Updated template. • Update "Families," page 1 with new devices families. • Completed various text fixes and updates.
12/20/07	3.0.1	• Correct typo of mF to µF on page 1.

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