

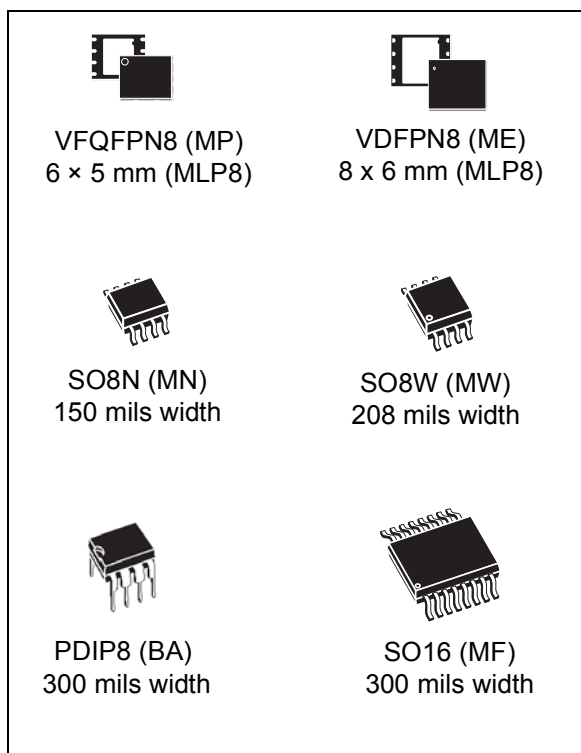
---

**16 Mbit, serial Flash memory, 75 MHz SPI bus interface**

---

**Features**

- n 16 Mbit of Flash memory
- n Page Program (up to 256 bytes) in 0.64 ms (typical)
- n Sector Erase (512 Kbit) in 0.6 s (typical)
- n Bulk Erase (16 Mbit) in 13 s (typical)
- n 2.7 V to 3.6 V single supply voltage
- n SPI bus compatible serial interface
- n 75 MHz Clock rate (maximum)
- n Deep Power-down mode 1  $\mu$ A (typical)
- n Electronic signatures
  - JEDEC standard two-byte signature (2015h)
  - Unique ID code (UID) with 16 bytes read-only, available upon customer request
  - RES instruction, one-byte, signature (14h), for backward compatibility
- n More than 100,000 Erase/Program cycles per sector
- n Hardware Write Protection: protected area size defined by three non-volatile bits (BP0, BP1 and BP2)
- n More than 20 year data retention
- n Packages
  - RoHS compliant





# Contents

<b>1</b>	<b>Description .....</b>	<b>7</b>
<b>2</b>	<b>Signal description .....</b>	<b>9</b>
2.1	Serial Data output (Q) .....	9
2.2	Serial Data input (D) .....	9
2.3	Serial Clock (C) .....	9
2.4	Chip Select ( $\overline{S}$ ) .....	9
2.5	Hold ( $\overline{HOLD}$ ) .....	9
2.6	Write Protect ( $\overline{W}$ ) .....	9
2.7	V <sub>CC</sub> supply voltage .....	10
2.8	V <sub>SS</sub> ground .....	10
<b>3</b>	<b>SPI modes .....</b>	<b>11</b>
<b>4</b>	<b>Operating features .....</b>	<b>13</b>
4.1	Page programming .....	13
4.2	Sector Erase and Bulk Erase .....	13
4.3	Polling during a Write, Program or Erase cycle .....	13
4.4	Active Power, Standby Power and Deep Power-down modes .....	13
4.5	Status Register .....	14
4.6	Protection modes .....	14
4.7	Hold condition .....	15
<b>5</b>	<b>Memory organization .....</b>	<b>17</b>
<b>6</b>	<b>Instructions .....</b>	<b>19</b>
6.1	Write Enable (WREN) .....	20
6.2	Write Disable (WRDI) .....	21
6.3	Read Identification (RDID) .....	22
6.4	Read Status Register (RDSR) .....	23
6.4.1	WIP bit .....	23
6.4.2	WEL bit .....	23
6.4.3	BP2, BP1, BP0 bits .....	23

6.4.4	SRWD bit	24
6.5	Write Status Register (WRSR)	25
6.6	Read Data Bytes (READ)	27
6.7	Read Data Bytes at Higher Speed (FAST_READ)	28
6.8	Page Program (PP)	29
6.9	Sector Erase (SE)	31
6.10	Bulk Erase (BE)	32
6.11	Deep Power-down (DP)	33
6.12	Release from Deep Power-down and Read Electronic Signature (RES)	34
<b>7</b>	<b>Power-up and power-down</b>	<b>36</b>
<b>8</b>	<b>Initial delivery state</b>	<b>37</b>
<b>9</b>	<b>Maximum rating</b>	<b>38</b>
<b>10</b>	<b>DC and AC parameters</b>	<b>39</b>
<b>11</b>	<b>Package mechanical</b>	<b>47</b>
<b>12</b>	<b>Part numbering</b>	<b>54</b>
<b>13</b>	<b>Revision history</b>	<b>55</b>

## List of tables

Table 1.	Signal names . . . . .	7
Table 2.	Protected area sizes . . . . .	15
Table 3.	Memory organization . . . . .	18
Table 4.	Instruction set . . . . .	20
Table 5.	Read Identification (RDID) data-out sequence . . . . .	22
Table 6.	Status Register format . . . . .	23
Table 7.	Protection modes . . . . .	26
Table 8.	Power-up timing and $V_{WI}$ threshold . . . . .	37
Table 9.	Absolute maximum ratings . . . . .	38
Table 10.	Operating conditions . . . . .	39
Table 11.	Data retention and endurance . . . . .	39
Table 12.	AC measurement conditions . . . . .	39
Table 13.	Capacitance . . . . .	39
Table 14.	DC characteristics . . . . .	40
Table 15.	AC characteristics (T9HX technology) . . . . .	41
Table 16.	AC characteristics (25 MHz operation) . . . . .	43
Table 17.	VFQFPN8 (MLP8) 8-lead very thin fine pitch quad flat package no lead, 6 × 5 mm, package mechanical data . . . . .	48
Table 18.	VDFPN8 (MLP8) 8-lead very thin dual flat package no lead, 8 × 6 mm, package mechanical data . . . . .	49
Table 19.	SO8N – 8 lead plastic small outline, 150 mils body width, package mechanical data . . . . .	50
Table 20.	SO8 wide – 8 lead plastic small outline, 208 mils body width, package mechanical data . . . . .	51
Table 21.	SO16 wide – 16-lead plastic small outline, 300 mils body width, mechanical data . . . . .	52
Table 22.	PDIP8 – 8 lead Plastic Small Outline, 300 mils body width, package mechanical data . . . . .	53
Table 23.	Ordering information scheme . . . . .	54
Table 24.	Document revision history . . . . .	55

## List of figures

Figure 1.	Logic diagram . . . . .	7
Figure 2.	SO8, VFQFPN, VDFPN, and PDIP8 connections . . . . .	8
Figure 3.	SO16 connections . . . . .	8
Figure 4.	Bus master and memory devices on the SPI bus . . . . .	11
Figure 5.	SPI modes supported . . . . .	12
Figure 6.	Hold condition activation . . . . .	16
Figure 7.	Block diagram . . . . .	17
Figure 8.	Write Enable (WREN) instruction sequence . . . . .	20
Figure 9.	Write Disable (WRDI) instruction sequence . . . . .	21
Figure 10.	Read Identification (RDID) instruction sequence and data-out sequence . . . . .	22
Figure 11.	Read Status Register (RDSR) instruction sequence and data-out sequence . . . . .	24
Figure 12.	Write Status Register (WRSR) instruction sequence . . . . .	25
Figure 13.	Read Data Bytes (READ) instruction sequence and data-out sequence . . . . .	27
Figure 14.	Read Data Bytes at Higher Speed (FAST_READ) instruction sequence and data-out sequence . . . . .	28
Figure 15.	Page Program (PP) instruction sequence . . . . .	30
Figure 16.	Sector Erase (SE) instruction sequence . . . . .	31
Figure 17.	Bulk Erase (BE) instruction sequence . . . . .	32
Figure 18.	Deep Power-down (DP) instruction sequence . . . . .	33
Figure 19.	Release from Deep Power-down and Read Electronic Signature (RES) instruction sequence and data-out sequence . . . . .	35
Figure 20.	Release from Deep Power-down (RES) instruction sequence . . . . .	35
Figure 21.	Power-up timing . . . . .	37
Figure 22.	AC measurement I/O waveform . . . . .	39
Figure 23.	Serial input timing . . . . .	44
Figure 24.	Write Protect setup and hold timing during WRSR when SRWD = 1 . . . . .	45
Figure 25.	Hold timing . . . . .	45
Figure 26.	Output timing . . . . .	46
Figure 27.	VFQFPN8 (MLP8) 8-lead very thin fine pitch quad flat package no lead, 6 × 5 mm, package outline . . . . .	47
Figure 28.	VDFPN8 (MLP8) 8-lead very thin dual flat package no lead, 8 × 6 mm, package outline . . . . .	49
Figure 29.	SO8N – 8 lead plastic small outline, 150 mils body width, package outline . . . . .	50
Figure 30.	SO8W – 8 lead plastic small outline, 208 mils body width, package outline . . . . .	51
Figure 31.	SO16 wide – 16-lead plastic small outline, 300 mils body width, package outline . . . . .	52
Figure 32.	PDIP8 – 8 lead Plastic Small Outline, 300 mils body width, package outline . . . . .	53

# 1 Description

The M25P16 is a 16 Mbit (2 Mbit × 8) serial Flash memory, with advanced write protection mechanisms, accessed by a high speed SPI-compatible bus.

The memory can be programmed 1 to 256 bytes at a time, using the Page Program instruction.

The memory is organized as 32 sectors, each containing 256 pages. Each page is 256 bytes wide. Thus, the whole memory can be viewed as consisting of 8192 pages, or 2 097 152 bytes.

The whole memory can be erased using the Bulk Erase instruction, or a sector at a time, using the Sector Erase instruction.

Figure 1. Logic diagram

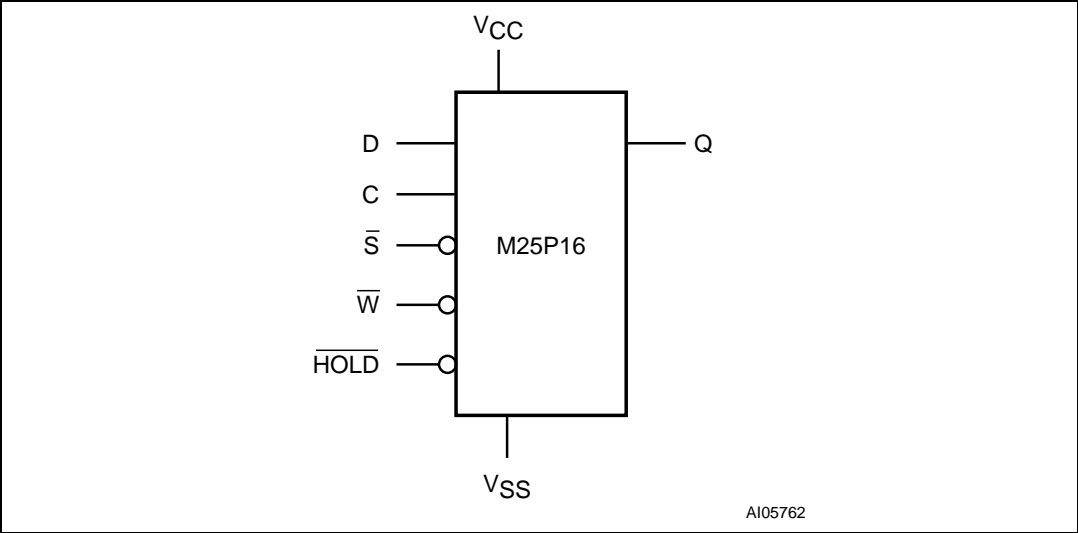
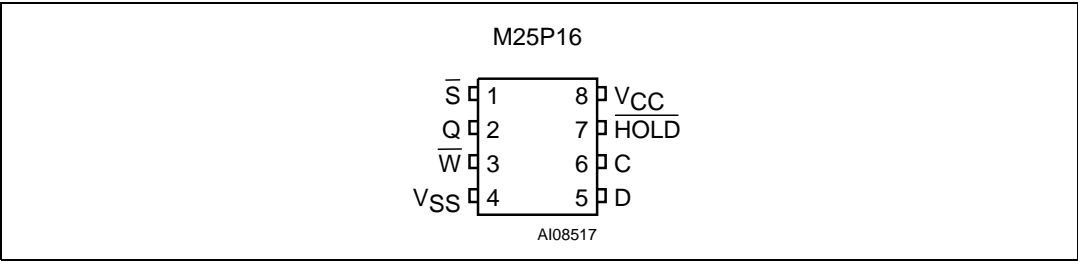


Table 1. Signal names

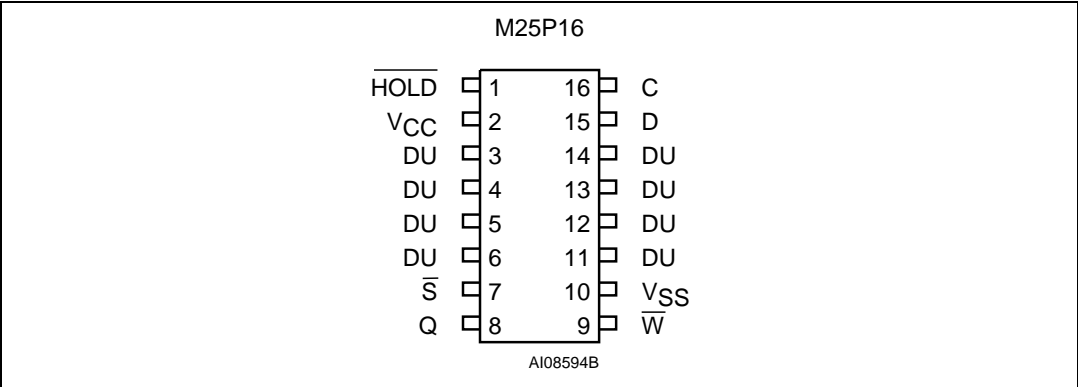
Signal name	Function	Direction
C	Serial Clock	Input
D	Serial Data input	Input
Q	Serial Data output	Output
$\overline{S}$	Chip Select	Input
$\overline{W}$	Write Protect	Input
$\overline{HOLD}$	Hold	Input
V <sub>CC</sub>	Supply voltage	
V <sub>SS</sub>	Ground	

Figure 2. SO8, VFQFPN, VDFPN, and PDIP8 connections



1. There is an exposed central pad on the underside of the VFQFPN package. This is pulled, internally, to VSS, and must not be allowed to be connected to any other voltage or signal line on the PCB.
2. See [Package mechanical](#) section for package dimensions, and how to identify pin-1.

Figure 3. SO16 connections



1. DU = Don't use
2. See [Package mechanical](#) section for package dimensions, and how to identify pin-1.



## 2 Signal description

### 2.1 Serial Data output (Q)

This output signal is used to transfer data serially out of the device. Data is shifted out on the falling edge of Serial Clock (C).

### 2.2 Serial Data input (D)

This input signal is used to transfer data serially into the device. It receives instructions, addresses, and the data to be programmed. Values are latched on the rising edge of Serial Clock (C).

### 2.3 Serial Clock (C)

This input signal provides the timing of the serial interface. Instructions, addresses, or data present at Serial Data input (D) are latched on the rising edge of Serial Clock (C). Data on Serial Data output (Q) changes after the falling edge of Serial Clock (C).

### 2.4 Chip Select ( $\overline{S}$ )

When this input signal is High, the device is deselected and Serial Data output (Q) is at high impedance. Unless an internal Program, Erase or Write Status Register cycle is in progress, the device will be in the Standby mode (this is not the Deep Power-down mode). Driving Chip Select ( $\overline{S}$ ) Low selects the device, placing it in the Active Power mode.

After power-up, a falling edge on Chip Select ( $\overline{S}$ ) is required prior to the start of any instruction.

### 2.5 Hold ( $\overline{HOLD}$ )

The Hold ( $\overline{HOLD}$ ) signal is used to pause any serial communications with the device without deselecting the device.

During the Hold condition, the Serial Data output (Q) is high impedance, and Serial Data input (D) and Serial Clock (C) are Don't care.

To start the Hold condition, the device must be selected, with Chip Select ( $\overline{S}$ ) driven Low.

### 2.6 Write Protect ( $\overline{W}$ )

The main purpose of this input signal is to freeze the size of the area of memory that is protected against program or erase instructions (as specified by the values in the BP2, BP1 and BP0 bits of the Status Register).

## 2.7 **$V_{CC}$ supply voltage**

$V_{CC}$  is the supply voltage.

## 2.8 **$V_{SS}$ ground**

$V_{SS}$  is the reference for the  $V_{CC}$  supply voltage.

### 3 SPI modes

These devices can be driven by a microcontroller with its SPI peripheral running in either of the two following modes:

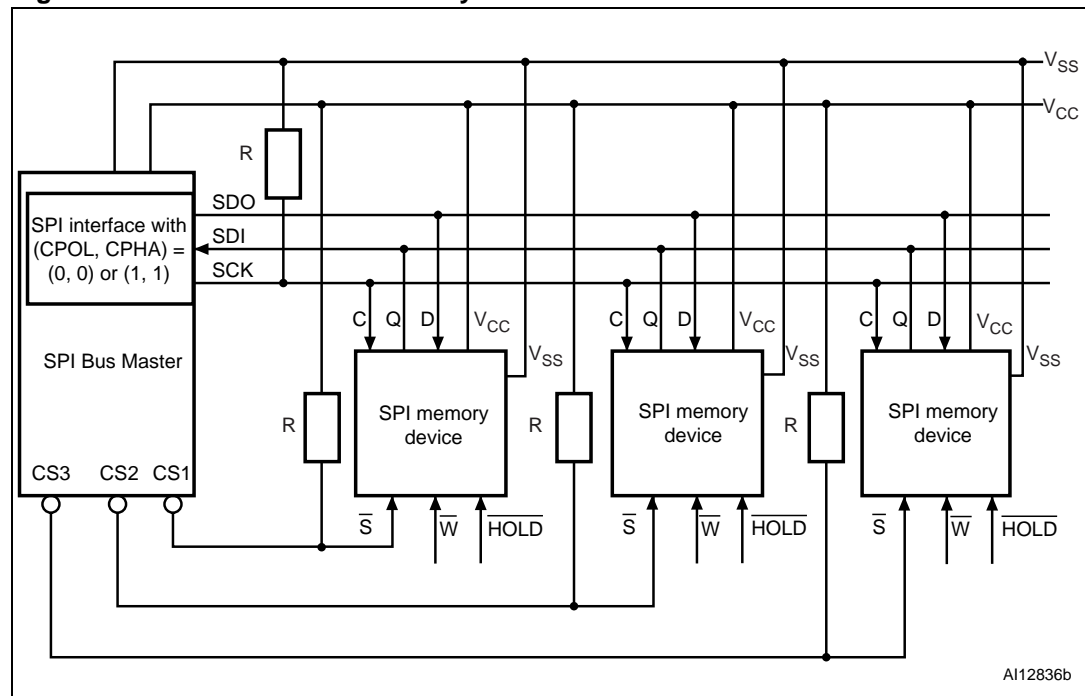
- ```
1    CPOL=0, CPHA=0
1    CPOL=1, CPHA=1
```

For these two modes, input data is latched in on the rising edge of Serial Clock (C), and output data is available from the falling edge of Serial Clock (C).

The difference between the two modes, as shown in [Figure 5](#), is the clock polarity when the bus master is in Standby mode and not transferring data:

- 1 C remains at 0 for (CPOL=0, CPHA=0)  
1 C remains at 1 for (CPOL=1, CPHA=1)

**Figure 4. Bus master and memory devices on the SPI bus**

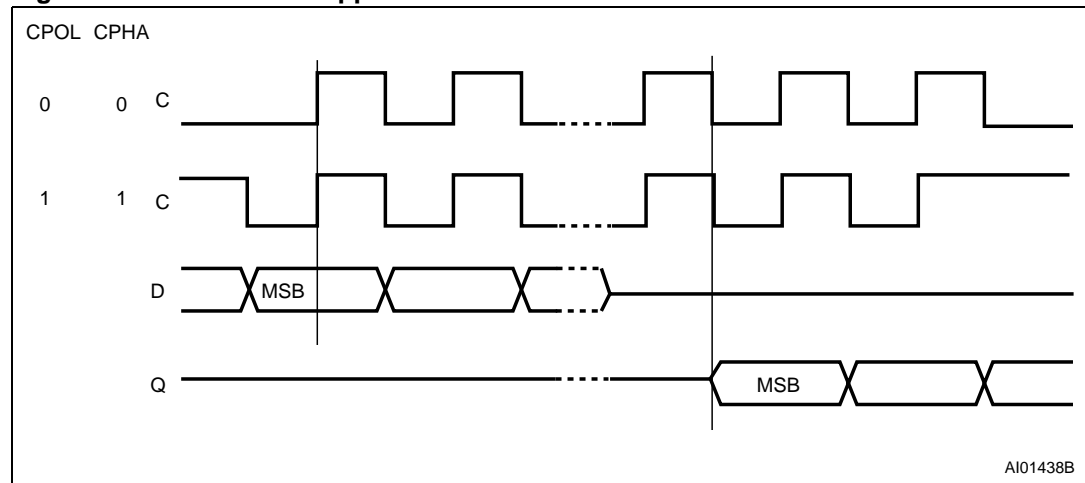


1. The Write Protect ( $\overline{W}$ ) and Hold ( $\overline{HOLD}$ ) signals should be driven, High or Low as appropriate.

**Figure 4** shows an example of three devices connected to an MCU, on an SPI bus. Only one device is selected at a time, so only one device drives the Serial Data output (Q) line at a time, the other devices are high impedance. Resistors R (represented in **Figure 4**) ensure that the M25P16 is not selected if the Bus Master leaves the  $\bar{S}$  line in the high impedance state. As the Bus Master may enter a state where all inputs/outputs are in high impedance at the same time (for example, when the Bus Master is reset), the clock line (C) must be connected to an external pull-down resistor so that, when all inputs/outputs become high impedance, the  $\bar{S}$  line is pulled High while the C line is pulled Low (thus ensuring that  $\bar{S}$  and C do not become High at the same time, and so, that the  $t_{SHCH}$  requirement is met). The typical value of R is 100 k $\Omega$ , assuming that the time constant  $R \cdot C_p$  ( $C_p$  = parasitic capacitance of the bus line) is shorter than the time during which the Bus Master leaves the SPI bus in high impedance.

**Example:**  $C_p = 50 \text{ pF}$ , that is  $R \cdot C_p = 5 \text{ } \mu\text{s} \Leftrightarrow$  the application must ensure that the Bus Master never leaves the SPI bus in the high impedance state for a time period shorter than  $5 \text{ } \mu\text{s}$ .

**Figure 5. SPI modes supported**



## 4 Operating features

### 4.1 Page programming

To program one data byte, two instructions are required: Write Enable (WREN), which is one byte, and a Page Program (PP) sequence, which consists of four bytes plus data. This is followed by the internal Program cycle (of duration  $t_{PP}$ ).

To spread this overhead, the Page Program (PP) instruction allows up to 256 bytes to be programmed at a time (changing bits from 1 to 0), provided that they lie in consecutive addresses on the same page of memory.

For optimized timings, it is recommended to use the Page Program (PP) instruction to program all consecutive targeted bytes in a single sequence versus using several Page Program (PP) sequences with each containing only a few bytes (see [Page Program \(PP\)](#)).

### 4.2 Sector Erase and Bulk Erase

The Page Program (PP) instruction allows bits to be reset from 1 to 0. Before this can be applied, the bytes of memory need to have been erased to all 1s (FFh). This can be achieved either a sector at a time, using the Sector Erase (SE) instruction, or throughout the entire memory, using the Bulk Erase (BE) instruction. This starts an internal Erase cycle (of duration  $t_{SE}$  or  $t_{BE}$ ).

The Erase instruction must be preceded by a Write Enable (WREN) instruction.

### 4.3 Polling during a Write, Program or Erase cycle

A further improvement in the time to Write Status Register (WRSR), Program (PP) or Erase (SE or BE) can be achieved by not waiting for the worst case delay ( $t_W$ ,  $t_{PP}$ ,  $t_{SE}$ , or  $t_{BE}$ ). The Write In Progress (WIP) bit is provided in the Status Register so that the application program can monitor its value, polling it to establish when the previous Write cycle, Program cycle or Erase cycle is complete.

### 4.4 Active Power, Standby Power and Deep Power-down modes

When Chip Select ( $\overline{S}$ ) is Low, the device is selected, and in the Active Power mode.

When Chip Select ( $\overline{S}$ ) is High, the device is deselected, but could remain in the Active Power mode until all internal cycles have completed (Program, Erase, Write Status Register). The device then goes in to the Standby Power mode. The device consumption drops to  $I_{CC1}$ .

The Deep Power-down mode is entered when the specific instruction (the Deep Power-down (DP) instruction) is executed. The device consumption drops further to  $I_{CC2}$ . The device remains in this mode until another specific instruction (the Release from Deep Power-down and Read Electronic Signature (RES) instruction) is executed.

While in the Deep Power-down mode, the device ignores all Write, Program and Erase instructions (see [Deep Power-down \(DP\)](#)). This can be used as an extra software protection mechanism, when the device is not in active use, to protect the device from inadvertent Write, Program or Erase instructions.

## 4.5 Status Register

The Status Register contains a number of status and control bits that can be read or set (as appropriate) by specific instructions. See [Section 6.4: Read Status Register \(RDSR\)](#) for a detailed description of the Status Register bits.

## 4.6 Protection modes

The environments where non-volatile memory devices are used can be very noisy. No SPI device can operate correctly in the presence of excessive noise. To help combat this, the M25P16 features the following data protection mechanisms:

- 1 Power on reset and an internal timer ( $t_{PUW}$ ) can provide protection against inadvertent changes while the power supply is outside the operating specification
- 1 Program, Erase and Write Status Register instructions are checked that they consist of a number of clock pulses that is a multiple of eight, before they are accepted for execution
- 1 All instructions that modify data must be preceded by a Write Enable (WREN) instruction to set the Write Enable Latch (WEL) bit. This bit is returned to its reset state by the following events:
  - Power-up
  - Write Disable (WRDI) instruction completion
  - Write Status Register (WRSR) instruction completion
  - Page Program (PP) instruction completion
  - Sector Erase (SE) instruction completion
  - Bulk Erase (BE) instruction completion
- 1 The Block Protect (BP2, BP1, BP0) bits allow part of the memory to be configured as read-only. This is the software protected mode (SPM)
- 1 The Write Protect ( $\overline{W}$ ) signal allows the Block Protect (BP2, BP1, BP0) bits and Status Register Write Disable (SRWD) bit to be protected. This is the hardware protected mode (HPM)
- 1 In addition to the low power consumption feature, the Deep Power-down mode offers extra software protection, as all Write, Program and Erase instructions are ignored.

**Table 2. Protected area sizes**

| Status Register content |         |         | Memory content                         |                                                  |
|-------------------------|---------|---------|----------------------------------------|--------------------------------------------------|
| BP2 bit                 | BP1 bit | BP0 bit | Protected area                         | Unprotected area                                 |
| 0                       | 0       | 0       | none                                   | All sectors <sup>(1)</sup> (32 sectors: 0 to 31) |
| 0                       | 0       | 1       | Upper 32nd (Sector 31)                 | Lower 31/32nds (31 sectors: 0 to 30)             |
| 0                       | 1       | 0       | Upper sixteenth (2 sectors: 30 and 31) | Lower 15/16ths (30 sectors: 0 to 29)             |
| 0                       | 1       | 1       | Upper eighth (4 sectors: 28 to 31)     | Lower seven-eighths (28 sectors: 0 to 27)        |
| 1                       | 0       | 0       | Upper quarter (8 sectors: 24 to 31)    | Lower three-quarters (24 sectors: 0 to 23)       |
| 1                       | 0       | 1       | Upper half (16 sectors: 16 to 31)      | Lower half (16 sectors: 0 to 15)                 |
| 1                       | 1       | 0       | All sectors (32 sectors: 0 to 31)      | none                                             |
| 1                       | 1       | 1       | All sectors (32 sectors: 0 to 31)      | none                                             |

1. The device is ready to accept a Bulk Erase instruction if, and only if, all Block Protect (BP2, BP1, BP0) are 0.

## 4.7 Hold condition

The Hold ( $\overline{\text{HOLD}}$ ) signal is used to pause any serial communications with the device without resetting the clocking sequence. However, taking this signal Low does not terminate any Write Status Register, Program or Erase cycle that is currently in progress.

To enter the Hold condition, the device must be selected, with Chip Select ( $\overline{\text{S}}$ ) Low.

The Hold condition starts on the falling edge of the Hold ( $\overline{\text{HOLD}}$ ) signal, provided that this coincides with Serial Clock (C) being Low (as shown in [Figure 6](#)).

The Hold condition ends on the rising edge of the Hold ( $\overline{\text{HOLD}}$ ) signal, provided that this coincides with Serial Clock (C) being Low.

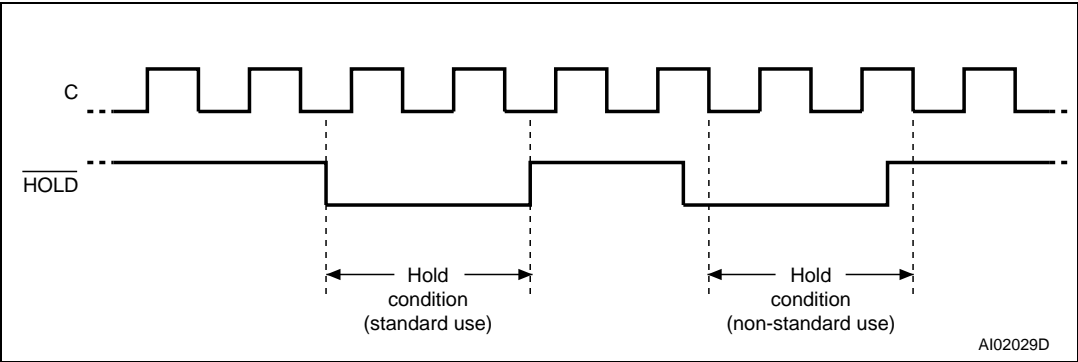
If the falling edge does not coincide with Serial Clock (C) being Low, the Hold condition starts after Serial Clock (C) next goes Low. Similarly, if the rising edge does not coincide with Serial Clock (C) being Low, the Hold condition ends after Serial Clock (C) next goes Low (this is shown in [Figure 6](#)).

During the Hold condition, the Serial Data output (Q) is high impedance, and Serial Data input (D) and Serial Clock (C) are Don't care.

Normally, the device is kept selected, with Chip Select ( $\overline{\text{S}}$ ) driven Low, for the whole duration of the Hold condition. This is to ensure that the state of the internal logic remains unchanged from the moment of entering the Hold condition.

If Chip Select ( $\overline{\text{S}}$ ) goes High while the device is in the Hold condition, this has the effect of resetting the internal logic of the device. To restart communication with the device, it is necessary to drive Hold ( $\overline{\text{HOLD}}$ ) High, and then to drive Chip Select ( $\overline{\text{S}}$ ) Low. This prevents the device from going back to the Hold condition.

Figure 6. Hold condition activation





## 5 Memory organization

The memory is organized as:

- 1 2 097 152 bytes (8 bits each)
- 1 32 sectors (512 Kbits, 65536 bytes each)
- 1 8192 pages (256 bytes each).

Each page can be individually programmed (bits are programmed from 1 to 0). The device is sector or bulk erasable (bits are erased from 0 to 1) but not page erasable.

**Figure 7. Block diagram**

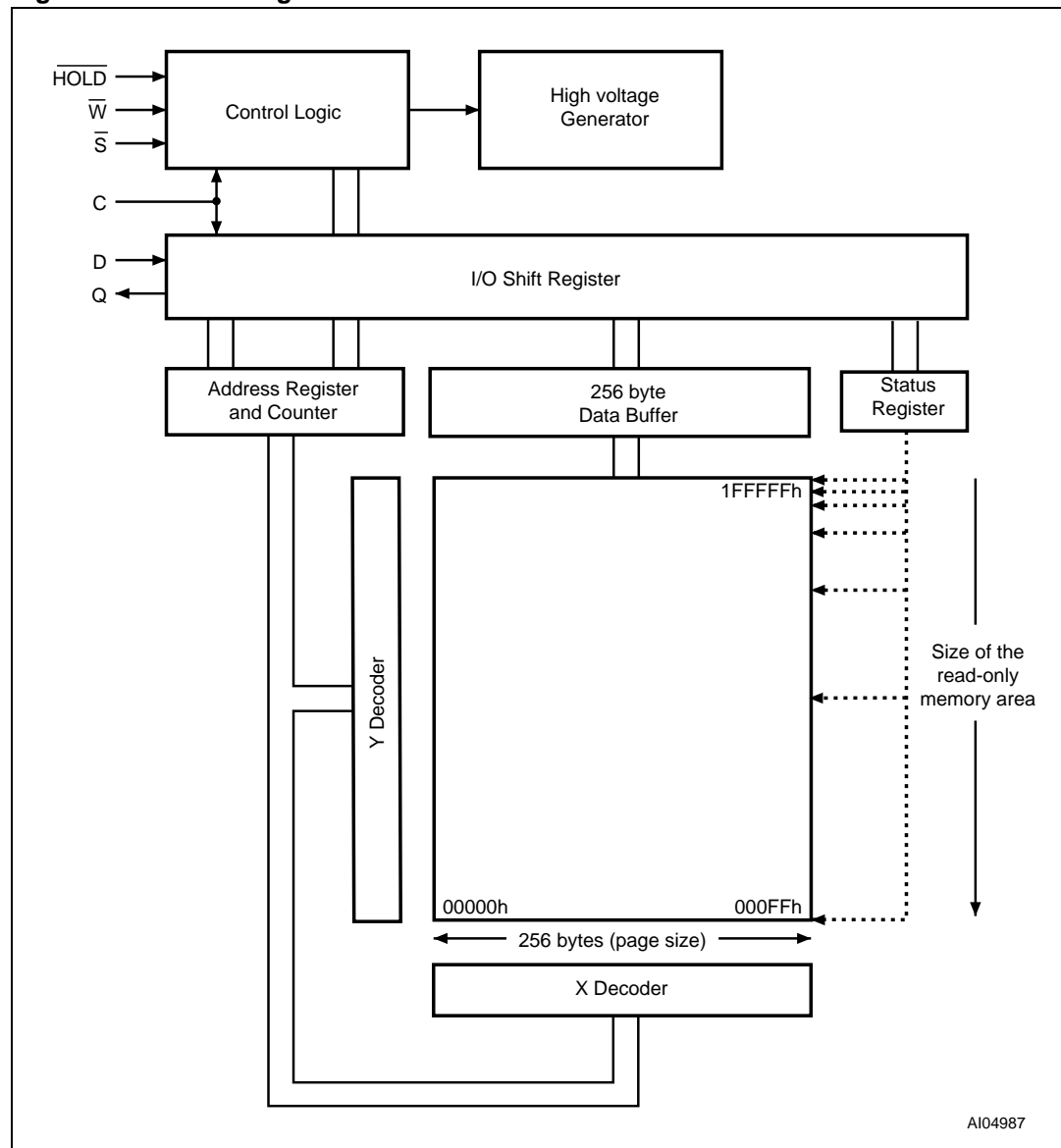


Table 3. Memory organization

| Sector | Address range |           |
|--------|---------------|-----------|
| 31     | 1F0000h       | 1FFFFFFh  |
| 30     | 1E0000h       | 1EFFFFFFh |
| 29     | 1D0000h       | 1DFFFFFFh |
| 28     | 1C0000h       | 1CFFFFFFh |
| 27     | 1B0000h       | 1BFFFFFFh |
| 26     | 1A0000h       | 1AFFFFFFh |
| 25     | 190000h       | 19FFFFFFh |
| 24     | 180000h       | 18FFFFFFh |
| 23     | 170000h       | 17FFFFFFh |
| 22     | 160000h       | 16FFFFFFh |
| 21     | 150000h       | 15FFFFFFh |
| 20     | 140000h       | 14FFFFFFh |
| 19     | 130000h       | 13FFFFFFh |
| 18     | 120000h       | 12FFFFFFh |
| 17     | 110000h       | 11FFFFFFh |
| 16     | 100000h       | 10FFFFFFh |
| 15     | 0F0000h       | 0FFFFFFh  |
| 14     | 0E0000h       | 0EFFFFFFh |
| 13     | 0D0000h       | 0DFFFFFFh |
| 12     | 0C0000h       | 0CFFFFFFh |
| 11     | 0B0000h       | 0BFFFFFFh |
| 10     | 0A0000h       | 0AFFFFFFh |
| 9      | 090000h       | 09FFFFFFh |
| 8      | 080000h       | 08FFFFFFh |
| 7      | 070000h       | 07FFFFFFh |
| 6      | 060000h       | 06FFFFFFh |
| 5      | 050000h       | 05FFFFFFh |
| 4      | 040000h       | 04FFFFFFh |
| 3      | 030000h       | 03FFFFFFh |
| 2      | 020000h       | 02FFFFFFh |
| 1      | 010000h       | 01FFFFFFh |
| 0      | 000000h       | 00FFFFFFh |

## 6 Instructions

All instructions, addresses and data are shifted in and out of the device, most significant bit first.

Serial Data input (D) is sampled on the first rising edge of Serial Clock (C) after Chip Select ( $\bar{S}$ ) is driven Low. Then, the one-byte instruction code must be shifted in to the device, most significant bit first, on Serial Data input (D), each bit being latched on the rising edges of Serial Clock (C).

The instruction set is listed in [Table 4](#).

Every instruction sequence starts with a one-byte instruction code. Depending on the instruction, this might be followed by address bytes, or by data bytes, or by both or none.

In the case of a Read Data Bytes (READ), Read Data Bytes at Higher Speed (FAST\_READ), Read Status Register (RDSR), Read Identification (RDID) or Release from Deep Power-down, and Read Electronic Signature (RES) instruction, the shifted-in instruction sequence is followed by a data-out sequence. Chip Select ( $\bar{S}$ ) can be driven High after any bit of the data-out sequence is being shifted out.

In the case of a Page Program (PP), Sector Erase (SE), Bulk Erase (BE), Write Status Register (WRSR), Write Enable (WREN), Write Disable (WRDI) or Deep Power-down (DP) instruction, Chip Select ( $\bar{S}$ ) must be driven High exactly at a byte boundary, otherwise the instruction is rejected, and is not executed. That is, Chip Select ( $\bar{S}$ ) must be driven High when the number of clock pulses after Chip Select ( $\bar{S}$ ) being driven Low is an exact multiple of eight.

All attempts to access the memory array during a Write Status Register cycle, Program cycle or Erase cycle are ignored, and the internal Write Status Register cycle, Program cycle or Erase cycle continues unaffected.

*Note: Output Hi-Z is defined as the point where data out is no longer driven.*

Table 4. Instruction set

| Instruction | Description                                                 | One-byte instruction code |     | Address bytes | Dummy bytes | Data bytes |
|-------------|-------------------------------------------------------------|---------------------------|-----|---------------|-------------|------------|
| WREN        | Write Enable                                                | 0000 0110                 | 06h | 0             | 0           | 0          |
| WRDI        | Write Disable                                               | 0000 0100                 | 04h | 0             | 0           | 0          |
| RDID        | Read Identification                                         | 1001 1111                 | 9Fh | 0             | 0           | 1 to 20    |
| RDSR        | Read Status Register                                        | 0000 0101                 | 05h | 0             | 0           | 1 to ∞     |
| WRSR        | Write Status Register                                       | 0000 0001                 | 01h | 0             | 0           | 1          |
| READ        | Read Data Bytes                                             | 0000 0011                 | 03h | 3             | 0           | 1 to ∞     |
| FAST_READ   | Read Data Bytes at Higher Speed                             | 0000 1011                 | 0Bh | 3             | 1           | 1 to ∞     |
| PP          | Page Program                                                | 0000 0010                 | 02h | 3             | 0           | 1 to 256   |
| SE          | Sector Erase                                                | 1101 1000                 | D8h | 3             | 0           | 0          |
| BE          | Bulk Erase                                                  | 1100 0111                 | C7h | 0             | 0           | 0          |
| DP          | Deep Power-down                                             | 1011 1001                 | B9h | 0             | 0           | 0          |
| RES         | Release from Deep Power-down, and Read Electronic Signature | 1010 1011                 | ABh | 0             | 3           | 1 to ∞     |
|             | Release from Deep Power-down                                |                           |     | 0             | 0           | 0          |

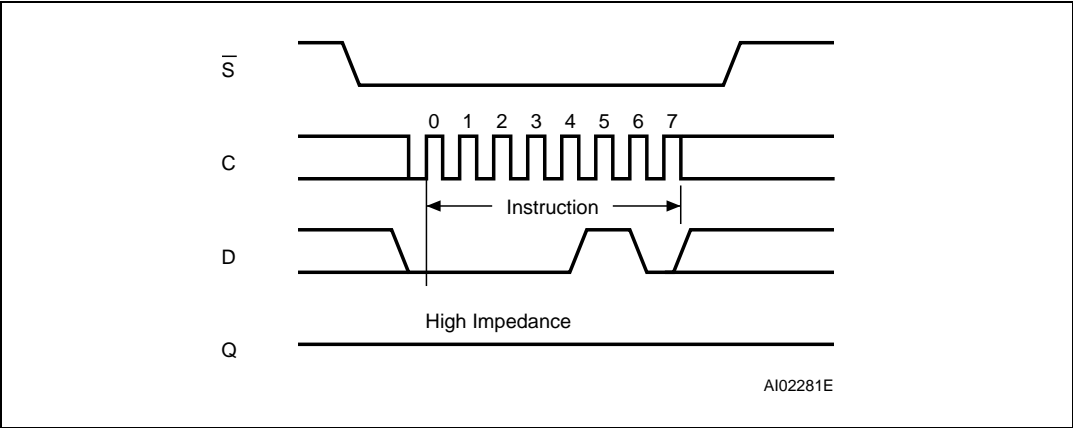
6.1 Write Enable (WREN)

The Write Enable (WREN) instruction ([Figure 8](#)) sets the Write Enable Latch (WEL) bit.

The Write Enable Latch (WEL) bit must be set prior to every Page Program (PP), Sector Erase (SE), Bulk Erase (BE) and Write Status Register (WRSR) instruction.

The Write Enable (WREN) instruction is entered by driving Chip Select ( $\overline{S}$ ) Low, sending the instruction code, and then driving Chip Select ( $\overline{S}$ ) High.

Figure 8. Write Enable (WREN) instruction sequence



## 6.2 Write Disable (WRDI)

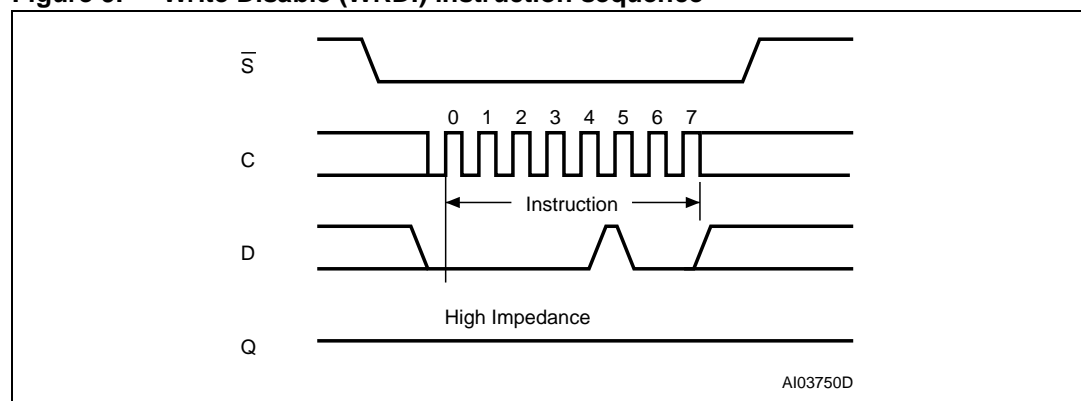
The Write Disable (WRDI) instruction ([Figure 9](#)) resets the Write Enable Latch (WEL) bit.

The Write Disable (WRDI) instruction is entered by driving Chip Select ( $\overline{S}$ ) Low, sending the instruction code, and then driving Chip Select ( $\overline{S}$ ) High.

The Write Enable Latch (WEL) bit is reset under the following conditions:

- 1 Power-up
- 1 Write Disable (WRDI) instruction completion
- 1 Write Status Register (WRSR) instruction completion
- 1 Page Program (PP) instruction completion
- 1 Sector Erase (SE) instruction completion
- 1 Bulk Erase (BE) instruction completion

**Figure 9. Write Disable (WRDI) instruction sequence**



6.3 Read Identification (RDID)

The Read Identification (RDID) instruction allows to read the device identification data:

- 1 Manufacturer identification (1 byte)
- 1 Device identification (2 bytes)
- 1 A Unique ID code (UID) (17 bytes, of which 16 available upon customer request).

The manufacturer identification is assigned by JEDEC, and has the value 20h for Numonyx. The device identification is assigned by the device manufacturer, and indicates the memory type in the first byte (20h), and the memory capacity of the device in the second byte (15h). The UID contains the length of the following data in the first byte (set to 10h), and 16 bytes of the optional Customized Factory Data (CFD) content. The CFD bytes are read-only and can be programmed with customers data upon their request. If the customers do not make requests, the devices are shipped with all the CFD bytes programmed to zero (00h).

*Note:* See [Section 12: Part numbering on page 54](#) for CFD programmed devices.

Any Read Identification (RDID) instruction while an Erase or Program cycle is in progress, is not decoded, and has no effect on the cycle that is in progress.

The device is first selected by driving Chip Select ( $\overline{S}$ ) Low. Then, the 8-bit instruction code for the instruction is shifted in. After this, the 24-bit device identification, stored in the memory, the 8-bit CFD length followed by 16 bytes of CFD content will be shifted out on Serial Data output (Q). Each bit is shifted out during the falling edge of Serial Clock (C).

The instruction sequence is shown in [Figure 10](#).

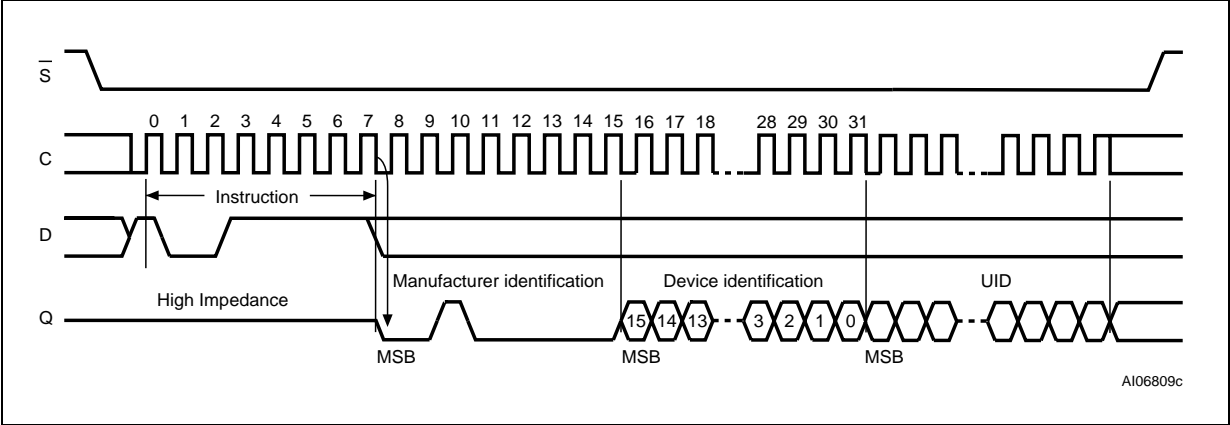
The Read Identification (RDID) instruction is terminated by driving Chip Select ( $\overline{S}$ ) High at any time during data output.

When Chip Select ( $\overline{S}$ ) is driven High, the device is put in the Standby Power mode. Once in the Standby Power mode, the device waits to be selected, so that it can receive, decode and execute instructions.

Table 5. Read Identification (RDID) data-out sequence

| Manufacturer identification | Device identification |                 | UID        |             |
|-----------------------------|-----------------------|-----------------|------------|-------------|
|                             | Memory type           | Memory capacity | CFD length | CFD content |
| 20h                         | 20h                   | 15h             | 10h        | 16 bytes    |

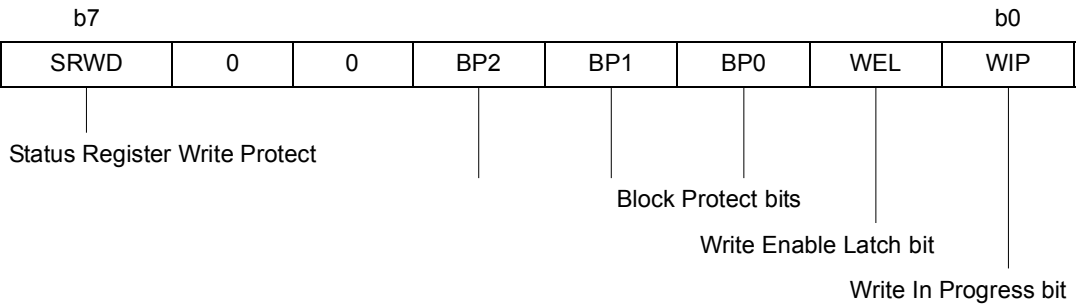
Figure 10. Read Identification (RDID) instruction sequence and data-out sequence



### 6.4 Read Status Register (RDSR)

The Read Status Register (RDSR) instruction allows the Status Register to be read. The Status Register may be read at any time, even while a Program, Erase or Write Status Register cycle is in progress. When one of these cycles is in progress, it is recommended to check the Write In Progress (WIP) bit before sending a new instruction to the device. It is also possible to read the Status Register continuously, as shown in [Figure 11](#).

**Table 6. Status Register format**



The status and control bits of the Status Register are as follows:

#### 6.4.1 WIP bit

The Write In Progress (WIP) bit indicates whether the memory is busy with a Write Status Register, Program or Erase cycle. When set to '1', such a cycle is in progress, when reset to '0' no such cycle is in progress.

#### 6.4.2 WEL bit

The Write Enable Latch (WEL) bit indicates the status of the internal Write Enable Latch. When set to '1' the internal Write Enable Latch is set, when set to '0' the internal Write Enable Latch is reset and no Write Status Register, Program or Erase instruction is accepted.

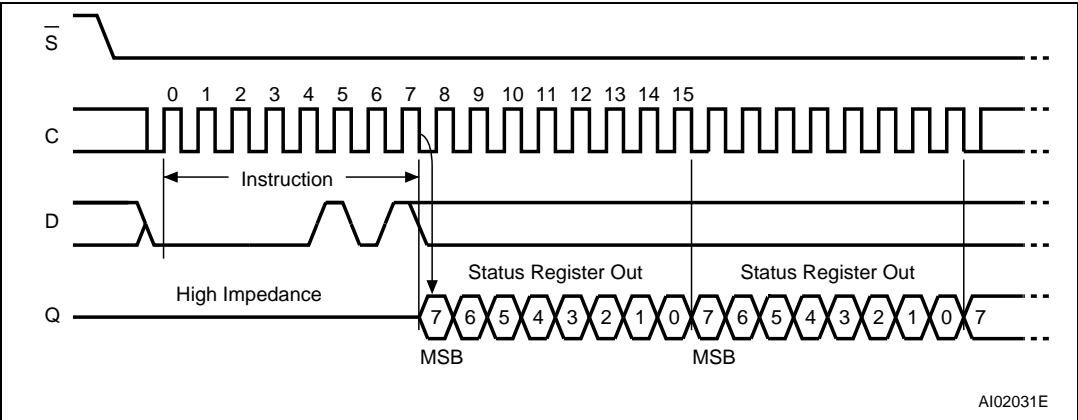
#### 6.4.3 BP2, BP1, BP0 bits

The Block Protect (BP2, BP1, BP0) bits are non-volatile. They define the size of the area to be software protected against Program and Erase instructions. These bits are written with the Write Status Register (WRSR) instruction. When one or more of the Block Protect (BP2, BP1, BP0) bits is set to '1', the relevant memory area (as defined in [Table 2](#)) becomes protected against Page Program (PP) and Sector Erase (SE) instructions. The Block Protect (BP2, BP1, BP0) bits can be written provided that the Hardware Protected mode has not been set. The Bulk Erase (BE) instruction is executed if, and only if, all Block Protect (BP2, BP1, BP0) bits are 0.

6.4.4 SRWD bit

The Status Register Write Disable (SRWD) bit is operated in conjunction with the Write Protect ( $\overline{W}$ ) signal. The Status Register Write Disable (SRWD) bit and Write Protect ( $\overline{W}$ ) signal allow the device to be put in the Hardware Protected mode (when the Status Register Write Disable (SRWD) bit is set to '1', and Write Protect ( $\overline{W}$ ) is driven Low). In this mode, the non-volatile bits of the Status Register (SRWD, BP2, BP1, BP0) become read-only bits and the Write Status Register (WRSR) instruction is no longer accepted for execution.

Figure 11. Read Status Register (RDSR) instruction sequence and data-out sequence





## 6.5 Write Status Register (WRSR)

The Write Status Register (WRSR) instruction allows new values to be written to the Status Register. Before it can be accepted, a Write Enable (WREN) instruction must previously have been executed. After the Write Enable (WREN) instruction has been decoded and executed, the device sets the Write Enable Latch (WEL).

The Write Status Register (WRSR) instruction is entered by driving Chip Select ( $\overline{S}$ ) Low, followed by the instruction code and the data byte on Serial Data input (D).

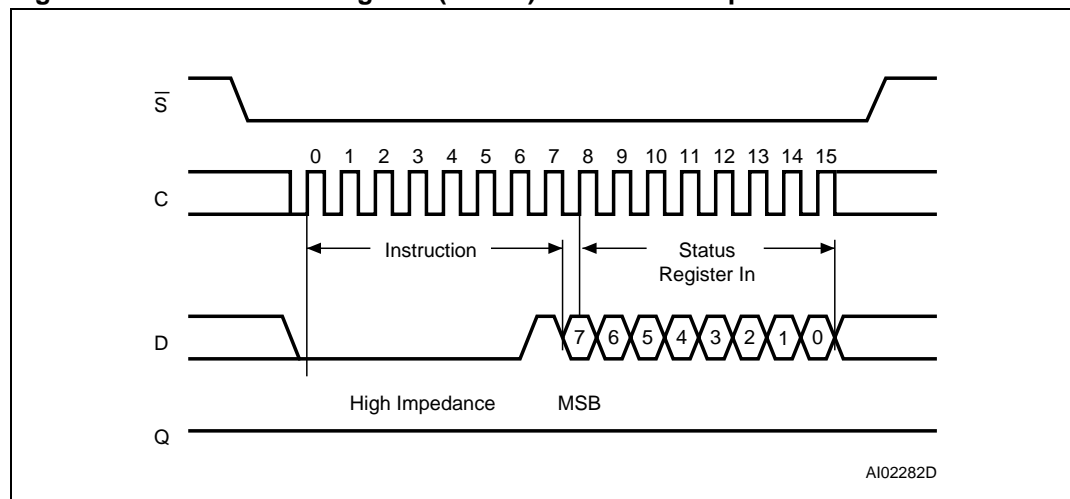
The instruction sequence is shown in [Figure 12](#).

The Write Status Register (WRSR) instruction has no effect on b6, b5, b1 and b0 of the Status Register. b6 and b5 are always read as 0.

Chip Select ( $\overline{S}$ ) must be driven High after the eighth bit of the data byte has been latched in. If not, the Write Status Register (WRSR) instruction is not executed. As soon as Chip Select ( $\overline{S}$ ) is driven High, the self-timed Write Status Register cycle (whose duration is  $t_W$ ) is initiated. While the Write Status Register cycle is in progress, the Status Register may still be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Write Status Register cycle, and is 0 when it is completed. When the cycle is completed, the Write Enable Latch (WEL) is reset.

The Write Status Register (WRSR) instruction allows the user to change the values of the Block Protect (BP2, BP1, BP0) bits, to define the size of the area that is to be treated as read-only, as defined in [Table 2](#). The Write Status Register (WRSR) instruction also allows the user to set or reset the Status Register Write Disable (SRWD) bit in accordance with the Write Protect ( $\overline{W}$ ) signal. The Status Register Write Disable (SRWD) bit and Write Protect ( $\overline{W}$ ) signal allow the device to be put in the Hardware Protected mode (HPM). The Write Status Register (WRSR) instruction is not executed once the Hardware Protected mode (HPM) is entered.

**Figure 12. Write Status Register (WRSR) instruction sequence**



**Table 7. Protection modes**

| $\overline{W}$ signal | SRWD bit | Mode                          | Write Protection of the Status Register                                   | Memory content                                              |                                                            |
|-----------------------|----------|-------------------------------|---------------------------------------------------------------------------|-------------------------------------------------------------|------------------------------------------------------------|
|                       |          |                               |                                                                           | Protected area <sup>(1)</sup>                               | Unprotected area <sup>(1)</sup>                            |
| 1                     | 0        | Software Protected mode (SPM) | Status Register is writable (if the WREN instruction has set the WEL bit) | Protected against Page Program, Sector Erase and Bulk Erase | Ready to accept Page Program and Sector Erase instructions |
| 0                     | 0        |                               | The values in the SRWD, BP2, BP1 and BP0 bits can be changed              |                                                             |                                                            |
| 1                     | 1        | Hardware Protected mode (HPM) | Status Register is Hardware write protected                               | Protected against Page Program, Sector Erase and Bulk Erase | Ready to accept Page Program and Sector Erase instructions |
| 0                     | 1        |                               | The values in the SRWD, BP2, BP1 and BP0 bits cannot be changed           |                                                             |                                                            |

1. As defined by the values in the Block Protect (BP2, BP1, BP0) bits of the Status Register, as shown in [Table 6](#).

The protection features of the device are summarized in [Table 7](#).

When the Status Register Write Disable (SRWD) bit of the Status Register is 0 (its initial delivery state), it is possible to write to the Status Register provided that the Write Enable Latch (WEL) bit has previously been set by a Write Enable (WREN) instruction, regardless of the whether Write Protect ( $\overline{W}$ ) is driven High or Low.

When the Status Register Write Disable (SRWD) bit of the Status Register is set to '1', two cases need to be considered, depending on the state of Write Protect ( $\overline{W}$ ):

- 1 If Write Protect ( $\overline{W}$ ) is driven High, it is possible to write to the Status Register provided that the Write Enable Latch (WEL) bit has previously been set by a Write Enable (WREN) instruction
- 1 If Write Protect ( $\overline{W}$ ) is driven Low, it is not possible to write to the Status Register even if the Write Enable Latch (WEL) bit has previously been set by a Write Enable (WREN) instruction (attempts to write to the Status Register are rejected, and are not accepted for execution). As a consequence, all the data bytes in the memory area that are software protected (SPM) by the Block Protect (BP2, BP1, BP0) bits of the Status Register, are also hardware protected against data modification.

Regardless of the order of the two events, the Hardware Protected mode (HPM) can be entered:

- 1 by setting the Status Register Write Disable (SRWD) bit after driving Write Protect ( $\overline{W}$ ) Low
- 1 or by driving Write Protect ( $\overline{W}$ ) Low after setting the Status Register Write Disable (SRWD) bit.

The only way to exit the Hardware Protected mode (HPM) once entered is to pull Write Protect ( $\overline{W}$ ) High.

If Write Protect ( $\overline{W}$ ) is permanently tied High, the Hardware Protected mode (HPM) can never be activated, and only the Software Protected mode (SPM), using the Block Protect (BP2, BP1, BP0) bits of the Status Register, can be used.

## 6.6 Read Data Bytes (READ)

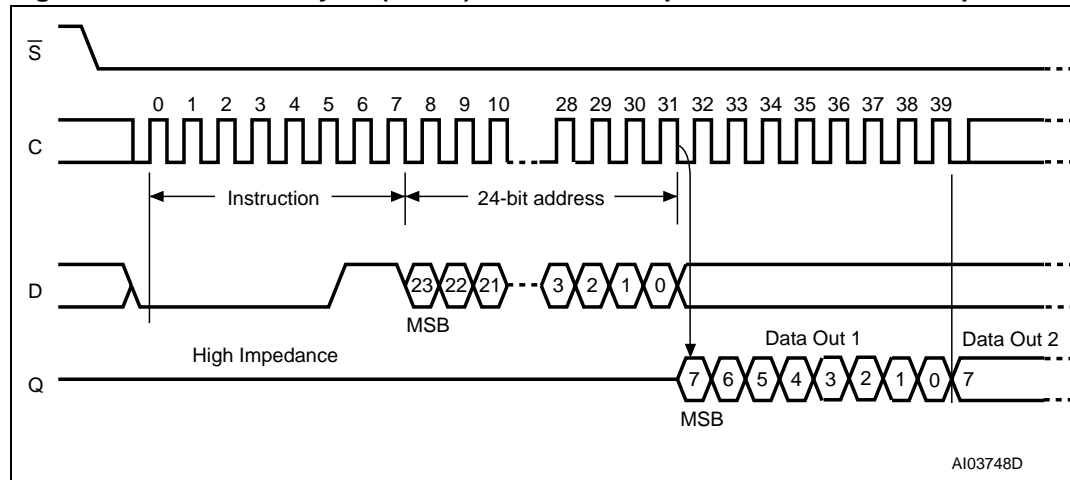
The device is first selected by driving Chip Select ( $\bar{S}$ ) Low. The instruction code for the Read Data Bytes (READ) instruction is followed by a 3-byte address (A23-A0), each bit being latched-in during the rising edge of Serial Clock (C). Then the memory contents, at that address, is shifted out on Serial Data output (Q), each bit being shifted out, at a maximum frequency  $f_R$ , during the falling edge of Serial Clock (C).

The instruction sequence is shown in [Figure 13](#).

The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. The whole memory can, therefore, be read with a single Read Data Bytes (READ) instruction. When the highest address is reached, the address counter rolls over to 000000h, allowing the read sequence to be continued indefinitely.

The Read Data Bytes (READ) instruction is terminated by driving Chip Select ( $\bar{S}$ ) High. Chip Select ( $\bar{S}$ ) can be driven High at any time during data output. Any Read Data Bytes (READ) instruction, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

**Figure 13. Read Data Bytes (READ) instruction sequence and data-out sequence**



1. Address bits A23 to A21 are Don't care.

## 6.7 Read Data Bytes at Higher Speed (FAST\_READ)

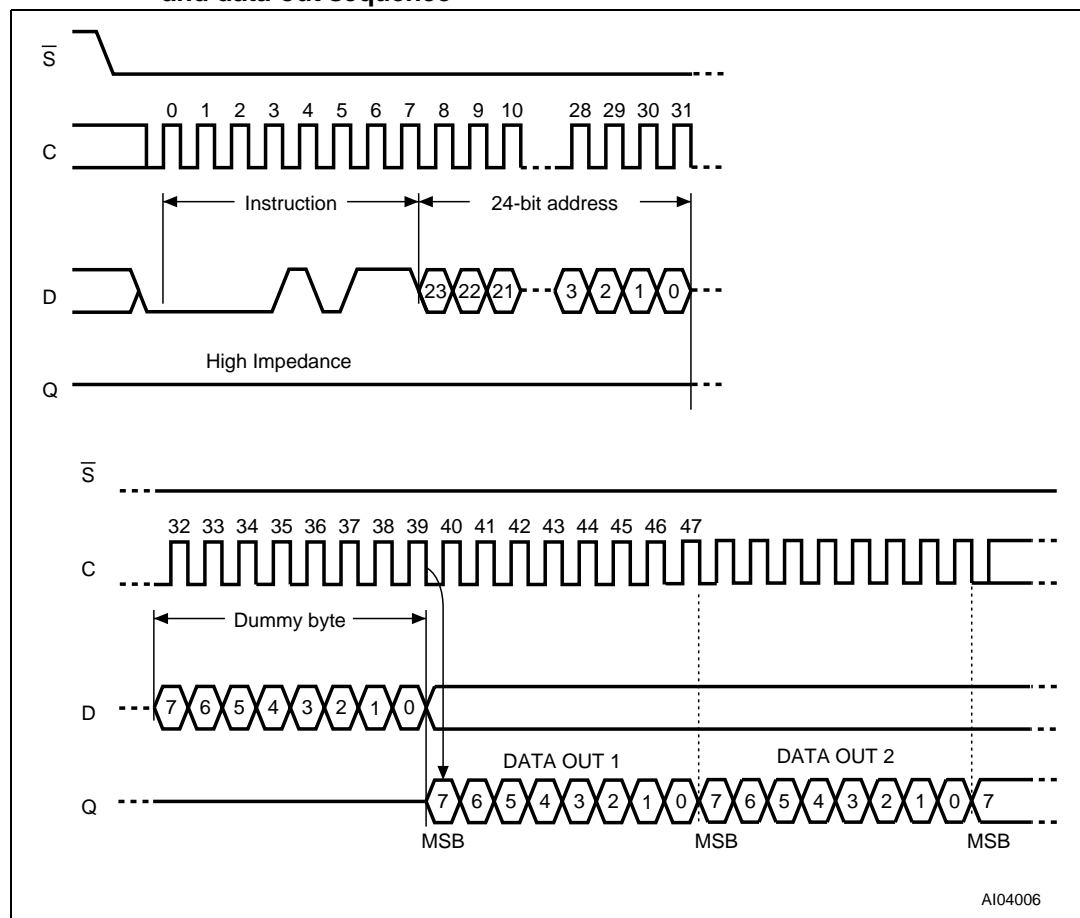
The device is first selected by driving Chip Select ( $\overline{S}$ ) Low. The instruction code for the Read Data Bytes at Higher Speed (FAST\_READ) instruction is followed by a 3-byte address (A23-A0) and a dummy byte, each bit being latched-in during the rising edge of Serial Clock (C). Then the memory contents, at that address, is shifted out on Serial Data output (Q), each bit being shifted out, at a maximum frequency  $f_C$ , during the falling edge of Serial Clock (C).

The instruction sequence is shown in [Figure 14](#).

The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. The whole memory can, therefore, be read with a single Read Data Bytes at Higher Speed (FAST\_READ) instruction. When the highest address is reached, the address counter rolls over to 000000h, allowing the read sequence to be continued indefinitely.

The Read Data Bytes at Higher Speed (FAST\_READ) instruction is terminated by driving Chip Select ( $\overline{S}$ ) High. Chip Select ( $\overline{S}$ ) can be driven High at any time during data output. Any Read Data Bytes at Higher Speed (FAST\_READ) instruction, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

**Figure 14. Read Data Bytes at Higher Speed (FAST\_READ) instruction sequence and data-out sequence**



1. Address bits A23 to A21 are Don't care.

## 6.8 Page Program (PP)

The Page Program (PP) instruction allows bytes to be programmed in the memory (changing bits from 1 to 0). Before it can be accepted, a Write Enable (WREN) instruction must previously have been executed. After the Write Enable (WREN) instruction has been decoded, the device sets the Write Enable Latch (WEL).

The Page Program (PP) instruction is entered by driving Chip Select ( $\overline{S}$ ) Low, followed by the instruction code, three address bytes and at least one data byte on Serial Data input (D). If the 8 least significant address bits (A7-A0) are not all zero, all transmitted data that goes beyond the end of the current page are programmed from the start address of the same page (from the address whose 8 least significant bits (A7-A0) are all zero). Chip Select ( $\overline{S}$ ) must be driven Low for the entire duration of the sequence.

The instruction sequence is shown in [Figure 15](#).

If more than 256 bytes are sent to the device, previously latched data are discarded and the last 256 data bytes are guaranteed to be programmed correctly within the same page. If less than 256 data bytes are sent to device, they are correctly programmed at the requested addresses without having any effects on the other bytes of the same page.

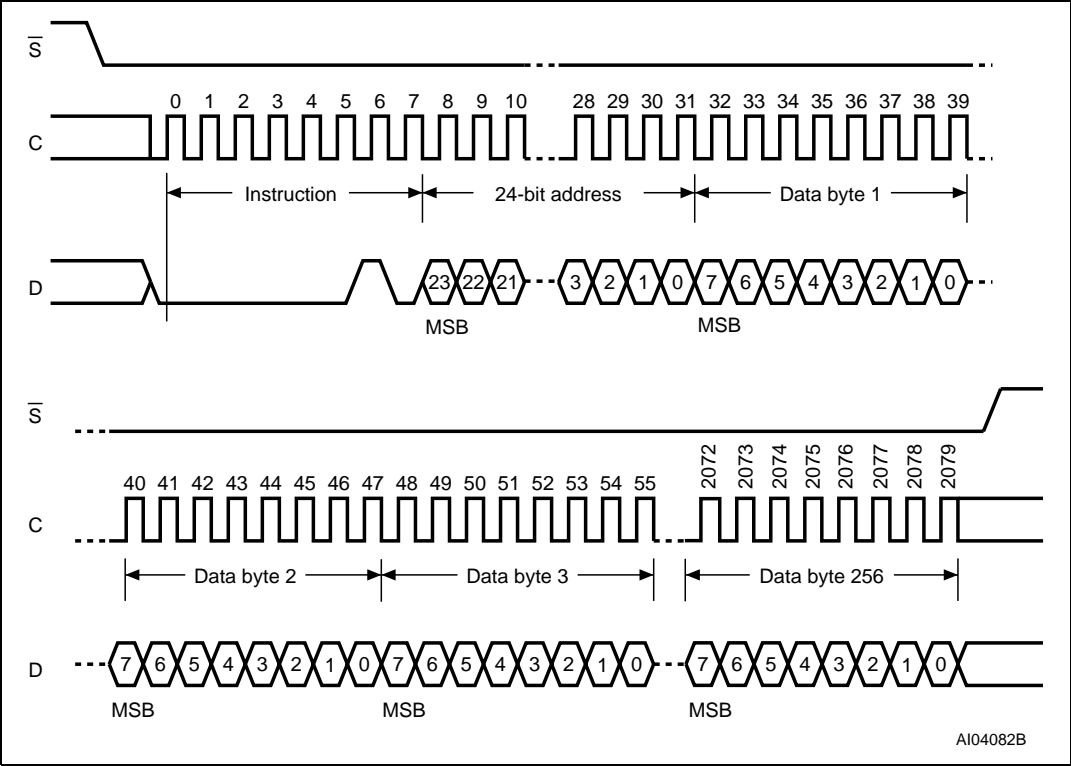
For optimized timings, it is recommended to use the Page Program (PP) instruction to program all consecutive targeted bytes in a single sequence versus using several Page Program (PP) sequences with each containing only a few bytes.

Chip Select ( $\overline{S}$ ) must be driven High after the eighth bit of the last data byte has been latched in, otherwise the Page Program (PP) instruction is not executed.

As soon as Chip Select ( $\overline{S}$ ) is driven High, the self-timed Page Program cycle (whose duration is  $t_{pp}$ ) is initiated. While the Page Program cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Page Program cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

A Page Program (PP) instruction applied to a page which is protected by the Block Protect (BP2, BP1, BP0) bits (see [Table 2](#) and [Table 3](#)) is not executed.

Figure 15. Page Program (PP) instruction sequence



1. Address bits A23 to A21 are Don't care.

## 6.9 Sector Erase (SE)

The Sector Erase (SE) instruction sets to '1' (FFh) all bits inside the chosen sector. Before it can be accepted, a Write Enable (WREN) instruction must previously have been executed. After the Write Enable (WREN) instruction has been decoded, the device sets the Write Enable Latch (WEL).

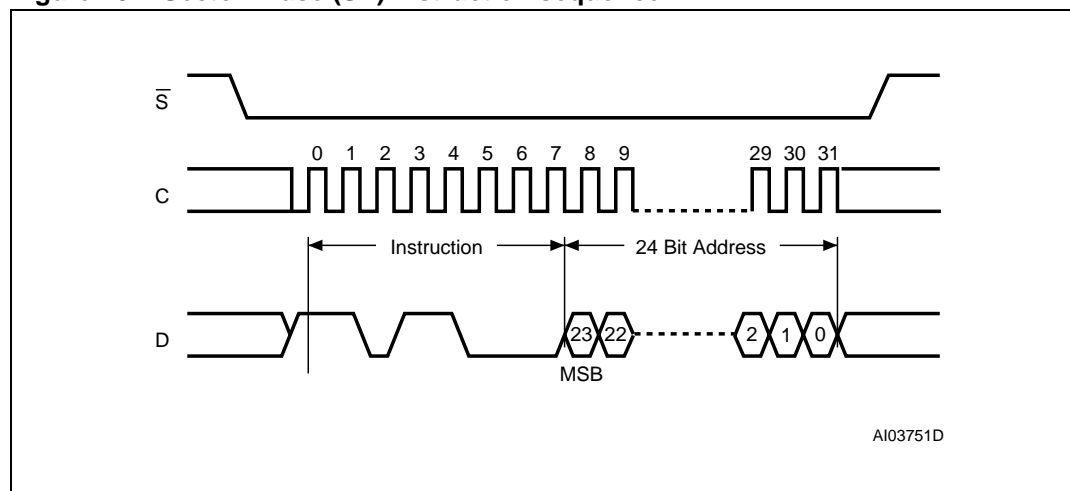
The Sector Erase (SE) instruction is entered by driving Chip Select ( $\overline{S}$ ) Low, followed by the instruction code, and three address bytes on Serial Data input (D). Any address inside the sector (see [Table 3](#)) is a valid address for the Sector Erase (SE) instruction. Chip Select ( $\overline{S}$ ) must be driven Low for the entire duration of the sequence.

The instruction sequence is shown in [Figure 16](#).

Chip Select ( $\overline{S}$ ) must be driven High after the eighth bit of the last address byte has been latched in, otherwise the Sector Erase (SE) instruction is not executed. As soon as Chip Select ( $\overline{S}$ ) is driven High, the self-timed Sector Erase cycle (whose duration is  $t_{SE}$ ) is initiated. While the Sector Erase cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Sector Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

A Sector Erase (SE) instruction applied to a page which is protected by the Block Protect (BP2, BP1, BP0) bits (see [Table 2](#) and [Table 3](#)) is not executed.

**Figure 16. Sector Erase (SE) instruction sequence**



1. Address bits A23 to A21 are Don't care.

## 6.10 Bulk Erase (BE)

The Bulk Erase (BE) instruction sets all bits to '1' (FFh). Before it can be accepted, a Write Enable (WREN) instruction must previously have been executed. After the Write Enable (WREN) instruction has been decoded, the device sets the Write Enable Latch (WEL).

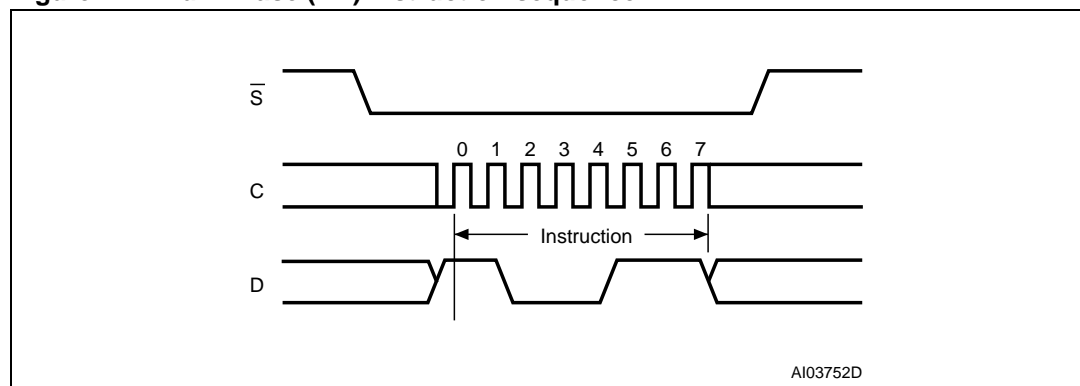
The Bulk Erase (BE) instruction is entered by driving  $\overline{\text{CS}}$  Low, followed by the instruction code on Serial Data input (D). Chip Select ( $\overline{\text{S}}$ ) must be driven Low for the entire duration of the sequence.

The instruction sequence is shown in [Figure 17](#).

Chip Select ( $\overline{\text{S}}$ ) must be driven High after the eighth bit of the instruction code has been latched in, otherwise the Bulk Erase instruction is not executed. As soon as Chip Select ( $\overline{\text{S}}$ ) is driven High, the self-timed Bulk Erase cycle (whose duration is  $t_{\text{BE}}$ ) is initiated. While the Bulk Erase cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Bulk Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

The Bulk Erase (BE) instruction is executed only if all Block Protect (BP2, BP1, BP0) bits are 0. The Bulk Erase (BE) instruction is ignored if one, or more, sectors are protected.

**Figure 17. Bulk Erase (BE) instruction sequence**





## 6.11 Deep Power-down (DP)

Executing the Deep Power-down (DP) instruction is the only way to put the device in the lowest consumption mode (the Deep Power-down mode). It can also be used as a software protection mechanism, while the device is not in active use, as in this mode, the device ignores all Write, Program and Erase instructions.

Driving Chip Select ( $\overline{S}$ ) High deselects the device, and puts the device in the Standby mode (if there is no internal cycle currently in progress). But this mode is not the Deep Power-down mode. The Deep Power-down mode can only be entered by executing the Deep Power-down (DP) instruction, subsequently reducing the standby current (from  $I_{CC1}$  to  $I_{CC2}$ , as specified in [Table 14](#)).

To take the device out of Deep Power-down mode, the Release from Deep Power-down and Read Electronic Signature (RES) instruction must be issued. No other instruction must be issued while the device is in Deep Power-down mode.

The Release from Deep Power-down and Read Electronic Signature (RES) instruction also allows the electronic signature of the device to be output on Serial Data output (Q).

The Deep Power-down mode automatically stops at power-down, and the device always powers up in the Standby mode.

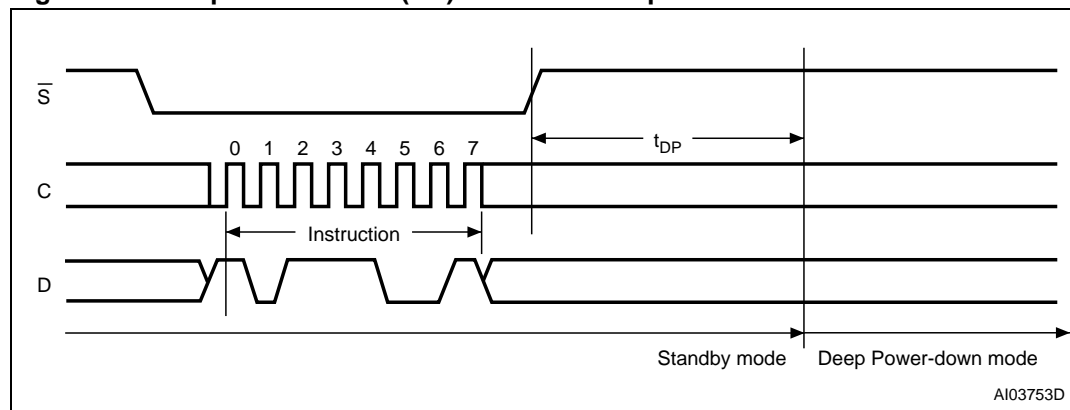
The Deep Power-down (DP) instruction is entered by driving Chip Select ( $\overline{S}$ ) Low, followed by the instruction code on Serial Data input (D). Chip Select ( $\overline{S}$ ) must be driven Low for the entire duration of the sequence.

The instruction sequence is shown in [Figure 18](#).

Chip Select ( $\overline{S}$ ) must be driven High after the eighth bit of the instruction code has been latched in, otherwise the Deep Power-down (DP) instruction is not executed. As soon as Chip Select ( $\overline{S}$ ) is driven High, it requires a delay of  $t_{DP}$  before the supply current is reduced to  $I_{CC2}$  and the Deep Power-down mode is entered.

Any Deep Power-down (DP) instruction, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

**Figure 18. Deep Power-down (DP) instruction sequence**



## 6.12 Release from Deep Power-down and Read Electronic Signature (RES)

To take the device out of Deep Power-down mode, the Release from Deep Power-down and Read Electronic Signature (RES) instruction must be issued. No other instruction must be issued while the device is in Deep Power-down mode.

The instruction can also be used to read, on Serial Data output (Q), the old-style 8-bit electronic signature, whose value for the M25P16 is 14h.

Please note that this is not the same as, or even a subset of, the JEDEC 16-bit electronic signature that is read by the Read Identifier (RDID) instruction. The old-style electronic signature is supported for reasons of backward compatibility, only, and should not be used for new designs. New designs should, instead, make use of the JEDEC 16-bit electronic signature, and the Read Identifier (RDID) instruction.

Except while an Erase, Program or Write Status Register cycle is in progress, the Release from Deep Power-down and Read Electronic Signature (RES) instruction always provides access to the old-style 8-bit electronic signature of the device, and can be applied even if the Deep Power-down mode has not been entered.

Any Release from Deep Power-down and Read Electronic Signature (RES) instruction while an Erase, Program or Write Status Register cycle is in progress, is not decoded, and has no effect on the cycle that is in progress.

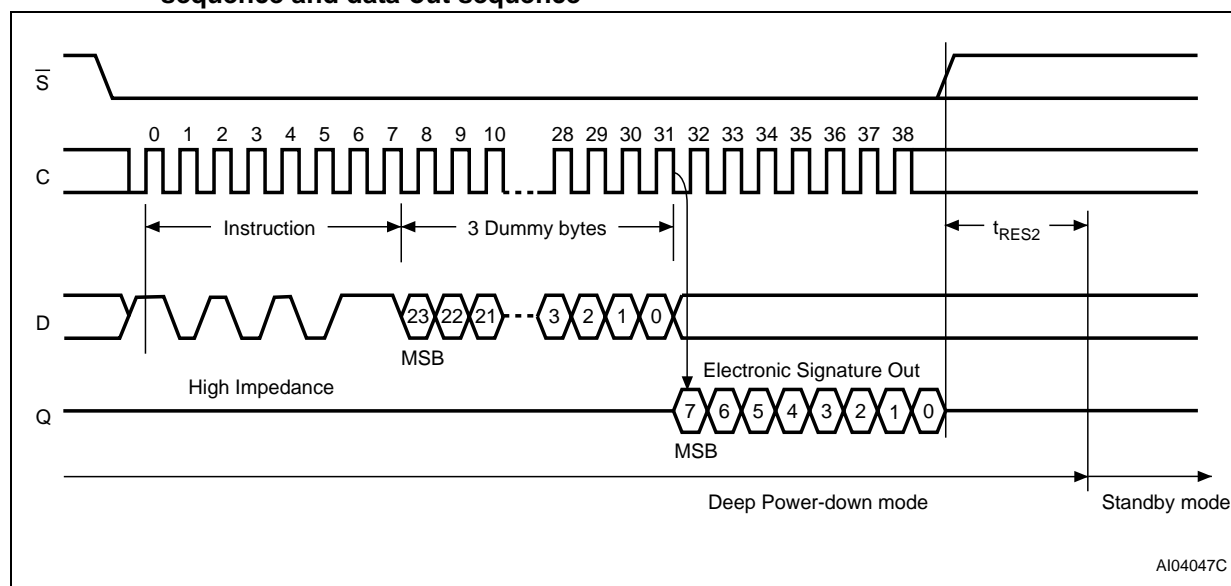
The device is first selected by driving Chip Select ( $\overline{S}$ ) Low. The instruction code is followed by 3 dummy bytes, each bit being latched-in on Serial Data input (D) during the rising edge of Serial Clock (C). Then, the old-style 8-bit electronic signature, stored in the memory, is shifted out on Serial Data output (Q), each bit being shifted out during the falling edge of Serial Clock (C).

The instruction sequence is shown in [Figure 19](#).

The Release from Deep Power-down and Read Electronic Signature (RES) instruction is terminated by driving Chip Select ( $\overline{S}$ ) High after the electronic signature has been read at least once. Sending additional clock cycles on Serial Clock (C), while Chip Select ( $\overline{S}$ ) is driven Low, cause the electronic signature to be output repeatedly.

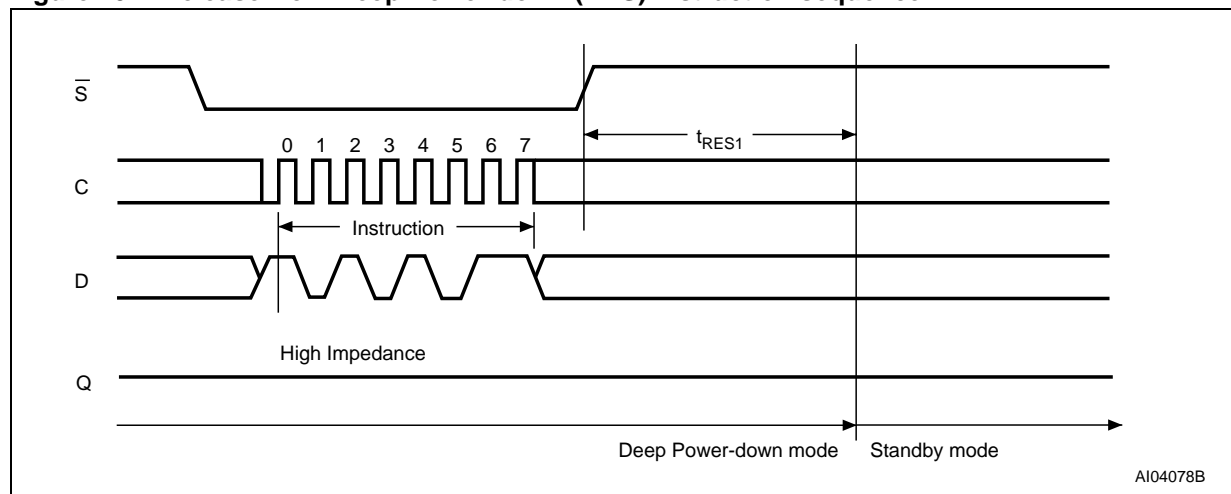
When Chip Select ( $\overline{S}$ ) is driven High, the device is put in the Standby Power mode. If the device was not previously in the Deep Power-down mode, the transition to the Standby Power mode is immediate. If the device was previously in the Deep Power-down mode, though, the transition to the Standby Power mode is delayed by  $t_{RES2}$ , and Chip Select ( $\overline{S}$ ) must remain High for at least  $t_{RES2}(\text{max})$ . Once in the Standby Power mode, the device waits to be selected, so that it can receive, decode and execute instructions.

**Figure 19. Release from Deep Power-down and Read Electronic Signature (RES) instruction sequence and data-out sequence**



1. The value of the 8-bit electronic signature, for the M25P16, is 14h.

**Figure 20. Release from Deep Power-down (RES) instruction sequence**



Driving Chip Select ( $\overline{S}$ ) High after the 8-bit instruction byte has been received by the device, but before the whole of the 8-bit electronic signature has been transmitted for the first time (as shown in [Figure 20](#)), still ensures that the device is put into Standby Power mode. If the device was not previously in the Deep Power-down mode, the transition to the Standby Power mode is immediate. If the device was previously in the Deep Power-down mode, though, the transition to the Standby Power mode is delayed by  $t_{RES1}$ , and Chip Select ( $\overline{S}$ ) must remain High for at least  $t_{RES1}(\text{max})$ . Once in the Standby Power mode, the device waits to be selected, so that it can receive, decode and execute instructions.

## 7 Power-up and power-down

At power-up and power-down, the device must not be selected (that is Chip Select ( $\overline{S}$ ) must follow the voltage applied on  $V_{CC}$ ) until  $V_{CC}$  reaches the correct value:

- 1  $V_{CC}(\text{min})$  at power-up, and then for a further delay of  $t_{VSL}$
- 1  $V_{SS}$  at power-down

A safe configuration is provided in [Section 3: SPI modes](#).

To avoid data corruption and inadvertent write operations during power-up, a Power On Reset (POR) circuit is included. The logic inside the device is held reset while  $V_{CC}$  is less than the Power On Reset (POR) threshold voltage,  $V_{WI}$  – all operations are disabled, and the device does not respond to any instruction.

Moreover, the device ignores all Write Enable (WREN), Page Program (PP), Sector Erase (SE), Bulk Erase (BE) and Write Status Register (WRSR) instructions until a time delay of  $t_{PUW}$  has elapsed after the moment that  $V_{CC}$  rises above the  $V_{WI}$  threshold. However, the correct operation of the device is not guaranteed if, by this time,  $V_{CC}$  is still below  $V_{CC}(\text{min})$ . No Write Status Register, Program or Erase instructions should be sent until the later of:

- 1  $t_{PUW}$  after  $V_{CC}$  passed the  $V_{WI}$  threshold
- 1  $t_{VSL}$  after  $V_{CC}$  passed the  $V_{CC}(\text{min})$  level.

These values are specified in [Table 8](#).

If the delay,  $t_{VSL}$ , has elapsed, after  $V_{CC}$  has risen above  $V_{CC}(\text{min})$ , the device can be selected for READ instructions even if the  $t_{PUW}$  delay is not yet fully elapsed.

At power-up, the device is in the following state:

- 1 The device is in the Standby mode (not the Deep Power-down mode)
- 1 The Write Enable Latch (WEL) bit is reset
- 1 The Write In Progress (WIP) bit is reset.

Normal precautions must be taken for supply rail decoupling, to stabilize the  $V_{CC}$  supply. Each device in a system should have the  $V_{CC}$  rail decoupled by a suitable capacitor close to the package pins (generally, this capacitor is of the order of 100 nF).

At power-down, when  $V_{CC}$  drops from the operating voltage, to below the Power On Reset (POR) threshold voltage,  $V_{WI}$ , all operations are disabled and the device does not respond to any instruction (the designer needs to be aware that if a power-down occurs while a Write, Program or Erase cycle is in progress, some data corruption can result).

Figure 21. Power-up timing

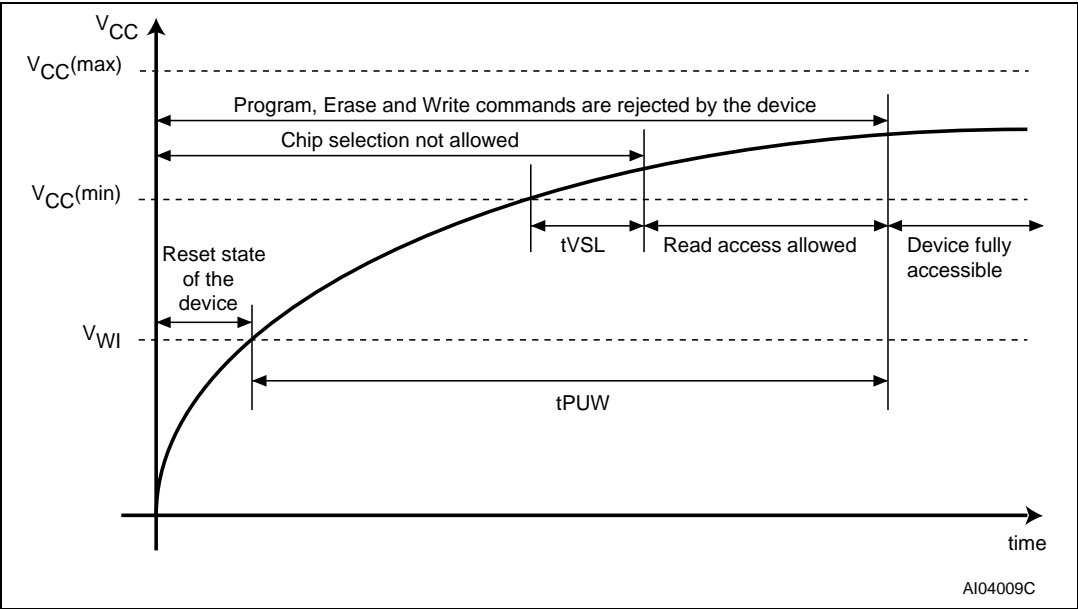


Table 8. Power-up timing and  $V_{WI}$  threshold

| Symbol          | Parameter                           | Min | Max | Unit    |
|-----------------|-------------------------------------|-----|-----|---------|
| $t_{VSL}^{(1)}$ | $V_{CC(min)}$ to $\overline{S}$ Low | 30  |     | $\mu s$ |
| $t_{PUW}^{(1)}$ | Time delay to Write instruction     | 1   | 10  | ms      |
| $V_{WI}^{(1)}$  | Write Inhibit voltage               | 1.5 | 2.5 | V       |

1. These parameters are characterized only.

## 8 Initial delivery state

The device is delivered with the memory array erased: all bits are set to '1' (each byte contains FFh). The Status Register contains 00h (all Status Register bits are 0).

## 9 Maximum rating

Stressing the device above the rating listed in [Table 9: Absolute maximum ratings](#) may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Refer also to the Numonyx SURE Program and other relevant quality documents.

**Table 9. Absolute maximum ratings**

| Symbol     | Parameter                                                         | Min                 | Max                           | Unit |
|------------|-------------------------------------------------------------------|---------------------|-------------------------------|------|
| $T_{STG}$  | Storage temperature                                               | -65                 | 150                           | °C   |
| $T_{LEAD}$ | Lead temperature during soldering                                 |                     | see <sup>(1)</sup>            | °C   |
| $V_{IO}$   | Input and output voltage (with respect to ground)                 | -0.6 <sup>(2)</sup> | $V_{CC} + 0.6$ <sup>(3)</sup> | V    |
| $V_{CC}$   | Supply voltage                                                    | -0.6                | 4.0                           | V    |
| $V_{ESD}$  | Electrostatic discharge voltage (Human Body model) <sup>(4)</sup> | -2000               | 2000                          | V    |

1. Compliant with JEDEC Std J-STD-020C (for small body, Sn-Pb or Pb assembly), the Numonyx RoHS compliant 7191395 specification, and the European directive on Restrictions on Hazardous Substances (RoHS) 2002/95/EU.
2. The minimum voltage may reach the value of -2 V for no more than 20 ns during transitions.
3. The maximum voltage may reach the value of  $V_{CC}+2$  V for no more than 20 ns during transitions.
4. JEDEC Std JESD22-A114A (C1 = 100 pF, R1 = 1500  $\Omega$ , R2 = 500  $\Omega$ ).

## 10 DC and AC parameters

This section summarizes the operating and measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC characteristic tables that follow are derived from tests performed under the measurement conditions summarized in the relevant tables. Designers should check that the operating conditions in their circuit match the measurement conditions when relying on the quoted parameters.

**Table 10. Operating conditions**

| Symbol   | Parameter                     |         | Min | Max | Unit |
|----------|-------------------------------|---------|-----|-----|------|
| $V_{CC}$ | Supply voltage                |         | 2.7 | 3.6 | V    |
| $T_A$    | Ambient operating temperature | grade 3 | −40 | 125 | °C   |
|          |                               | grade 6 | −40 | 85  | °C   |

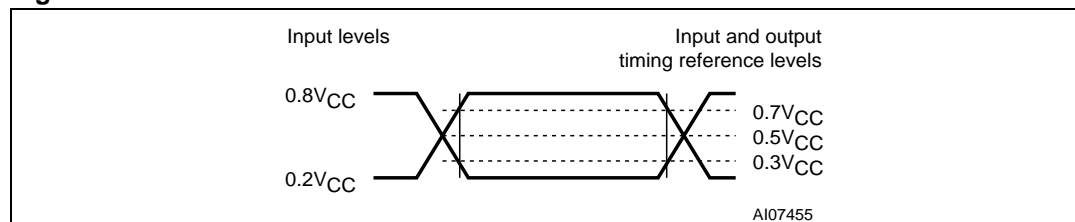
**Table 11. Data retention and endurance**

| Parameter            | Condition      | Min     | Max | Unit              |
|----------------------|----------------|---------|-----|-------------------|
| Erase/Program cycles | Device grade 6 | 100 000 |     | Cycles per sector |
|                      | Device grade 3 | 10 000  |     |                   |
| Data retention       | at 55 °C       | 20      |     | years             |

**Table 12. AC measurement conditions**

| Symbol | Parameter                        | Min                                      | Max | Unit |
|--------|----------------------------------|------------------------------------------|-----|------|
| $C_L$  | Load capacitance                 | 30                                       |     | pF   |
|        | Input rise and fall times        |                                          | 5   | ns   |
|        | Input pulse voltages             | 0.2V <sub>CC</sub> to 0.8V <sub>CC</sub> |     | V    |
|        | Input timing reference voltages  | 0.3V <sub>CC</sub> to 0.7V <sub>CC</sub> |     | V    |
|        | Output timing reference voltages | V <sub>CC</sub> / 2                      |     | V    |

**Figure 22. AC measurement I/O waveform**



**Table 13. Capacitance<sup>(1)</sup>**

| Symbol    | Parameter                      | Test Condition         | Min | Max | Unit |
|-----------|--------------------------------|------------------------|-----|-----|------|
| $C_{OUT}$ | Output capacitance (Q)         | V <sub>OUT</sub> = 0 V |     | 8   | pF   |
| $C_{IN}$  | Input capacitance (other pins) | V <sub>IN</sub> = 0 V  |     | 6   | pF   |

1. Sampled only, not 100% tested, at  $T_A$  = 25 °C and a frequency of 20 MHz.

Table 14. DC characteristics

| Symbol    | Parameter                |         | Test condition (in addition to those in Table 10)      | Min          | Max          | Unit    |
|-----------|--------------------------|---------|--------------------------------------------------------|--------------|--------------|---------|
| $I_{LI}$  | Input leakage current    |         |                                                        |              | $\pm 2$      | $\mu A$ |
| $I_{LO}$  | Output leakage current   |         |                                                        |              | $\pm 2$      | $\mu A$ |
| $I_{CC1}$ | Standby current          | Grade 6 | $\bar{S} = V_{CC}, V_{IN} = V_{SS} \text{ or } V_{CC}$ |              | 50           | $\mu A$ |
|           |                          | Grade 3 |                                                        |              | 100          | $\mu A$ |
| $I_{CC2}$ | Deep Power-down current  | Grade 6 | $\bar{S} = V_{CC}, V_{IN} = V_{SS} \text{ or } V_{CC}$ |              | 10           | $\mu A$ |
|           |                          | Grade 3 |                                                        |              | 100          | $\mu A$ |
| $I_{CC3}$ | Operating current (READ) |         | $C = 0.1V_{CC} / 0.9.V_{CC}$ at 75 MHz, Q = open       |              | 12           | mA      |
|           |                          |         | $C = 0.1V_{CC} / 0.9.V_{CC}$ at 33 MHz, Q = open       |              | 4            | mA      |
| $I_{CC4}$ | Operating current (PP)   |         | $\bar{S} = V_{CC}$                                     |              | 15           | mA      |
| $I_{CC5}$ | Operating current (WRSR) |         | $\bar{S} = V_{CC}$                                     |              | 15           | mA      |
| $I_{CC6}$ | Operating current (SE)   |         | $\bar{S} = V_{CC}$                                     |              | 15           | mA      |
| $I_{CC7}$ | Operating current (BE)   |         | $\bar{S} = V_{CC}$                                     |              | 15           | mA      |
| $V_{IL}$  | Input low voltage        |         |                                                        | -0.5         | $0.3V_{CC}$  | V       |
| $V_{IH}$  | Input high voltage       |         |                                                        | $0.7V_{CC}$  | $V_{CC}+0.4$ | V       |
| $V_{OL}$  | Output low voltage       |         | $I_{OL} = 1.6 \text{ mA}$                              |              | 0.4          | V       |
| $V_{OH}$  | Output high voltage      |         | $I_{OH} = -100 \mu A$                                  | $V_{CC}-0.2$ |              | V       |



**Table 15. AC characteristics (T9HX technology)**

| Applies only to products made with T9HX technology, identified with process digit '4' <sup>(1)</sup><br>Test conditions specified in <a href="#">Table 10</a> and <a href="#">Table 12</a> |           |                                                                                                                    |      |                    |     |         |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------|--------------------------------------------------------------------------------------------------------------------|------|--------------------|-----|---------|
| Symbol                                                                                                                                                                                     | Alt.      | Parameter                                                                                                          | Min  | Typ <sup>(2)</sup> | Max | Unit    |
| $f_C$                                                                                                                                                                                      | $f_C$     | Clock frequency for the following instructions:<br>FAST_READ, PP, SE, BE, DP, RES, WREN,<br>WRDI, RDID, RDSR, WRSR | D.C. |                    | 75  | MHz     |
| $f_R$                                                                                                                                                                                      |           | Clock frequency for READ instructions                                                                              | D.C. |                    | 33  | MHz     |
| $t_{CH}^{(3)}$                                                                                                                                                                             | $t_{CLH}$ | Clock High time                                                                                                    | 6    |                    |     | ns      |
| $t_{CL}^{(2)}$                                                                                                                                                                             | $t_{CLL}$ | Clock Low time                                                                                                     | 6    |                    |     | ns      |
| $t_{CLCH}^{(4)}$                                                                                                                                                                           |           | Clock Rise time <sup>(5)</sup> (peak to peak)                                                                      | 0.1  |                    |     | V/ns    |
| $t_{CHCL}^{(4)}$                                                                                                                                                                           |           | Clock Fall time <sup>(5)</sup> (peak to peak)                                                                      | 0.1  |                    |     | V/ns    |
| $t_{SLCH}$                                                                                                                                                                                 | $t_{CSS}$ | $\overline{S}$ Active Setup time (relative to C)                                                                   | 5    |                    |     | ns      |
| $t_{CHSL}$                                                                                                                                                                                 |           | $\overline{S}$ Not Active Hold time (relative to C)                                                                | 5    |                    |     | ns      |
| $t_{DVCH}$                                                                                                                                                                                 | $t_{DSU}$ | Data In Setup time                                                                                                 | 2    |                    |     | ns      |
| $t_{CHDX}$                                                                                                                                                                                 | $t_{DH}$  | Data In Hold time                                                                                                  | 5    |                    |     | ns      |
| $t_{CHSH}$                                                                                                                                                                                 |           | $\overline{S}$ Active Hold time (relative to C)                                                                    | 5    |                    |     | ns      |
| $t_{SHCH}$                                                                                                                                                                                 |           | $\overline{S}$ Not Active Setup time (relative to C)                                                               | 5    |                    |     | ns      |
| $t_{SHSL}$                                                                                                                                                                                 | $t_{CSH}$ | $\overline{S}$ Deselect time                                                                                       | 100  |                    |     | ns      |
| $t_{SHQZ}^{(4)}$                                                                                                                                                                           | $t_{DIS}$ | Output Disable time                                                                                                |      |                    | 8   | ns      |
| $t_{CLQV}$                                                                                                                                                                                 | $t_V$     | Clock Low to Output Valid under 30 pF/10 pF                                                                        |      |                    | 8/6 | ns      |
| $t_{CLQX}$                                                                                                                                                                                 | $t_{HO}$  | Output Hold time                                                                                                   | 0    |                    |     | ns      |
| $t_{HLCH}$                                                                                                                                                                                 |           | $\overline{HOLD}$ Setup time (relative to C)                                                                       | 5    |                    |     | ns      |
| $t_{CHHH}$                                                                                                                                                                                 |           | $\overline{HOLD}$ Hold time (relative to C)                                                                        | 5    |                    |     | ns      |
| $t_{HHCH}$                                                                                                                                                                                 |           | $\overline{HOLD}$ Setup time (relative to C)                                                                       | 5    |                    |     | ns      |
| $t_{CHHL}$                                                                                                                                                                                 |           | $\overline{HOLD}$ Hold time (relative to C)                                                                        | 5    |                    |     | ns      |
| $t_{HHQX}^{(4)}$                                                                                                                                                                           | $t_{LZ}$  | $\overline{HOLD}$ to Output Low-Z                                                                                  |      |                    | 8   | ns      |
| $t_{HLQZ}^{(4)}$                                                                                                                                                                           | $t_{HZ}$  | $\overline{HOLD}$ to Output High-Z                                                                                 |      |                    | 8   | ns      |
| $t_{WHSL}^{(6)}$                                                                                                                                                                           |           | Write Protect Setup time                                                                                           | 20   |                    |     | ns      |
| $t_{SHWL}^{(6)}$                                                                                                                                                                           |           | Write Protect Hold time                                                                                            | 100  |                    |     | ns      |
| $t_{DP}^{(4)}$                                                                                                                                                                             |           | $\overline{S}$ High to Deep Power-down mode                                                                        |      |                    | 3   | $\mu s$ |
| $t_{RES1}^{(4)}$                                                                                                                                                                           |           | $\overline{S}$ High to Standby mode without Read Electronic Signature                                              |      |                    | 30  | $\mu s$ |
| $t_{RES2}^{(4)}$                                                                                                                                                                           |           | $\overline{S}$ High to Standby mode with Read Electronic Signature                                                 |      |                    | 30  | $\mu s$ |
| $t_W$                                                                                                                                                                                      |           | Write Status Register cycle time                                                                                   |      | 1.3                | 15  | ms      |

**Table 15. AC characteristics (T9HX technology) (continued)**

| Applies only to products made with T9HX technology, identified with process digit '4' <sup>(1)</sup><br>Test conditions specified in <a href="#">Table 10</a> and <a href="#">Table 12</a> |      |                                                       |     |                                     |     |      |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|-------------------------------------------------------|-----|-------------------------------------|-----|------|
| Symbol                                                                                                                                                                                     | Alt. | Parameter                                             | Min | Typ <sup>(2)</sup>                  | Max | Unit |
| $t_{PP}^{(7)}$                                                                                                                                                                             |      | Page Program cycle time (256 bytes)                   |     | 0.64                                | 5   | ms   |
|                                                                                                                                                                                            |      | Page Program cycle time (n bytes, where n = 1 to 4)   |     | 0.01                                |     |      |
|                                                                                                                                                                                            |      | Page Program cycle time (n bytes, where n = 5 to 256) |     | $\text{int}(n/8) \times 0.02^{(8)}$ |     |      |
| $t_{SE}$                                                                                                                                                                                   |      | Sector Erase cycle time                               |     | 0.6                                 | 3   | s    |
| $t_{BE}$                                                                                                                                                                                   |      | Bulk Erase cycle time                                 |     | 13                                  | 40  | s    |

1. Details of how to find the technology process in the marking are given in AN1995, see also [Section 12: Part numbering](#).
2. Typical values given for  $T_A = 25^\circ\text{C}$ .
3.  $t_{CH} + t_{CL}$  must be greater than or equal to  $1/f_C$ .
4. Value guaranteed by characterization, not 100% tested in production.
5. Expressed as a slew-rate.
6. Only applicable as a constraint for a WRSR instruction when SRWD is set at '1'.
7. When using the Page Program (PP) instruction to program consecutive bytes, optimized timings are obtained with one sequence including all the bytes versus several sequences of only a few bytes ( $1 \leq n \leq 256$ ).
8.  $\text{int}(A)$  corresponds to the upper integer part of A. For instance,  $\text{int}(12/8) = 2$ ,  $\text{int}(32/8) = 4$ ,  $\text{int}(15.3) = 15$ .

Table 16. AC characteristics (25 MHz operation)

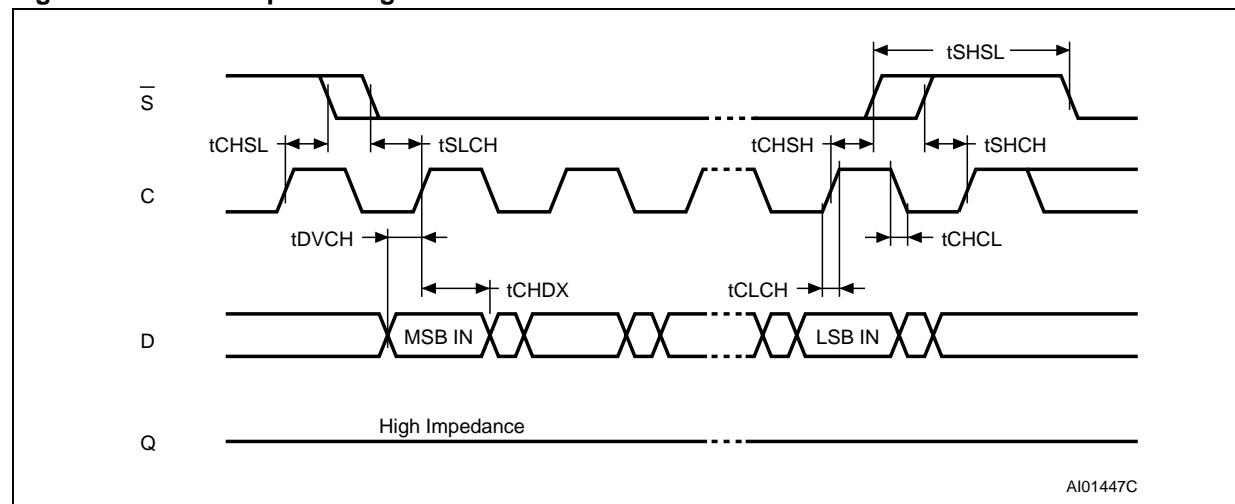
| Test conditions specified in <a href="#">Table 10</a> and <a href="#">Table 12</a> |           |                                                                                                        |      |                                      |     |         |
|------------------------------------------------------------------------------------|-----------|--------------------------------------------------------------------------------------------------------|------|--------------------------------------|-----|---------|
| Symbol                                                                             | Alt.      | Parameter                                                                                              | Min  | Typ                                  | Max | Unit    |
| $f_C$                                                                              | $f_C$     | Clock frequency for the following instructions: FAST_READ, PP, SE, BE, DP, RES, WREN, WRDI, RDSR, WRSR | D.C. |                                      | 25  | MHz     |
| $f_R$                                                                              |           | Clock frequency for READ instructions                                                                  | D.C. |                                      | 20  | MHz     |
| $t_{CH}^{(1)}$                                                                     | $t_{CLH}$ | Clock High time                                                                                        | 18   |                                      |     | ns      |
| $t_{CL}^{(1)}$                                                                     | $t_{CLL}$ | Clock Low time                                                                                         | 18   |                                      |     | ns      |
| $t_{CLCH}^{(2)}$                                                                   |           | Clock Rise time <sup>(3)</sup> (peak to peak)                                                          | 0.1  |                                      |     | V/ns    |
| $t_{CHCL}^{(2)}$                                                                   |           | Clock Fall time <sup>(3)</sup> (peak to peak)                                                          | 0.1  |                                      |     | V/ns    |
| $t_{SLCH}$                                                                         | $t_{CSS}$ | $\overline{S}$ Active Setup time (relative to C)                                                       | 10   |                                      |     | ns      |
| $t_{CHSL}$                                                                         |           | $\overline{S}$ Not Active Hold time (relative to C)                                                    | 10   |                                      |     | ns      |
| $t_{DVCH}$                                                                         | $t_{DSU}$ | Data In Setup time                                                                                     | 5    |                                      |     | ns      |
| $t_{CHDX}$                                                                         | $t_{DH}$  | Data In Hold time                                                                                      | 5    |                                      |     | ns      |
| $t_{CHSH}$                                                                         |           | $\overline{S}$ Active Hold time (relative to C)                                                        | 10   |                                      |     | ns      |
| $t_{SHCH}$                                                                         |           | $\overline{S}$ Not Active Setup time (relative to C)                                                   | 10   |                                      |     | ns      |
| $t_{SHSL}$                                                                         | $t_{CSH}$ | $\overline{S}$ Deselect time                                                                           | 100  |                                      |     | ns      |
| $t_{SHQZ}^{(2)}$                                                                   | $t_{DIS}$ | Output Disable time                                                                                    |      |                                      | 15  | ns      |
| $t_{CLQV}$                                                                         | $t_V$     | Clock Low to Output Valid                                                                              |      |                                      | 15  | ns      |
| $t_{CLQX}$                                                                         | $t_{HO}$  | Output Hold time                                                                                       | 0    |                                      |     | ns      |
| $t_{HLCH}$                                                                         |           | $\overline{HOLD}$ Setup time (relative to C)                                                           | 10   |                                      |     | ns      |
| $t_{CHHH}$                                                                         |           | $\overline{HOLD}$ Hold time (relative to C)                                                            | 10   |                                      |     | ns      |
| $t_{HHCH}$                                                                         |           | $\overline{HOLD}$ Setup time (relative to C)                                                           | 10   |                                      |     | ns      |
| $t_{CHHL}$                                                                         |           | $\overline{HOLD}$ Hold time (relative to C)                                                            | 10   |                                      |     | ns      |
| $t_{HHQX}^{(2)}$                                                                   | $t_{LZ}$  | $\overline{HOLD}$ to Output Low-Z                                                                      |      |                                      | 15  | ns      |
| $t_{HLQZ}^{(2)}$                                                                   | $t_{HZ}$  | $\overline{HOLD}$ to Output High-Z                                                                     |      |                                      | 20  | ns      |
| $t_{WHSL}^{(4)}$                                                                   |           | Write Protect Setup time                                                                               | 20   |                                      |     | ns      |
| $t_{SHWL}^{(4)}$                                                                   |           | Write Protect Hold time                                                                                | 100  |                                      |     | ns      |
| $t_{DP}^{(2)}$                                                                     |           | $\overline{S}$ High to Deep Power-down mode                                                            |      |                                      | 3   | $\mu$ s |
| $t_{RES1}^{(2)}$                                                                   |           | $\overline{S}$ High to Standby mode without Electronic Signature Read                                  |      |                                      | 3   | $\mu$ s |
| $t_{RES2}^{(2)}$                                                                   |           | $\overline{S}$ High to Standby mode with Electronic Signature Read                                     |      |                                      | 1.8 | $\mu$ s |
| $t_W^{(5)}$                                                                        |           | Write Status Register cycle time                                                                       |      | 1.5                                  | 15  | ms      |
| $t_{PP}^{(5)}$                                                                     |           | Page Program cycle time (256 bytes)                                                                    |      | 0.8                                  | 5   | ms      |
|                                                                                    |           | Page Program cycle time (n bytes)                                                                      |      | $\text{int}(n/8) \times 0.025^{(6)}$ |     |         |

**Table 16. AC characteristics (25 MHz operation) (continued)**

| Test conditions specified in <a href="#">Table 10</a> and <a href="#">Table 12</a> |      |                         |     |     |     |      |
|------------------------------------------------------------------------------------|------|-------------------------|-----|-----|-----|------|
| Symbol                                                                             | Alt. | Parameter               | Min | Typ | Max | Unit |
| t <sub>SE</sub> <sup>(5)</sup>                                                     |      | Sector Erase cycle time |     | 0.8 | 3   | s    |
| t <sub>BE</sub> <sup>(5)</sup>                                                     |      | Bulk Erase cycle time   |     | 17  | 40  | s    |

1.  $t_{CH} + t_{CL}$  must be greater than or equal to  $1/f_C$ .
2. Value guaranteed by characterization, not 100% tested in production.
3. Expressed as a slew-rate.
4. Only applicable as a constraint for a WRSR instruction when SRWD is set at '1'.
5. Typical values given for  $T_A = 85^\circ\text{C}$ .
6.  $\text{int}(A)$  corresponds to the upper integer part of  $A$ . For instance,  $\text{int}(12/8) = 2$ ,  $\text{int}(32/8) = 4$   $\text{int}(15.3) = 15$ .

### Figure 23. Serial input timing



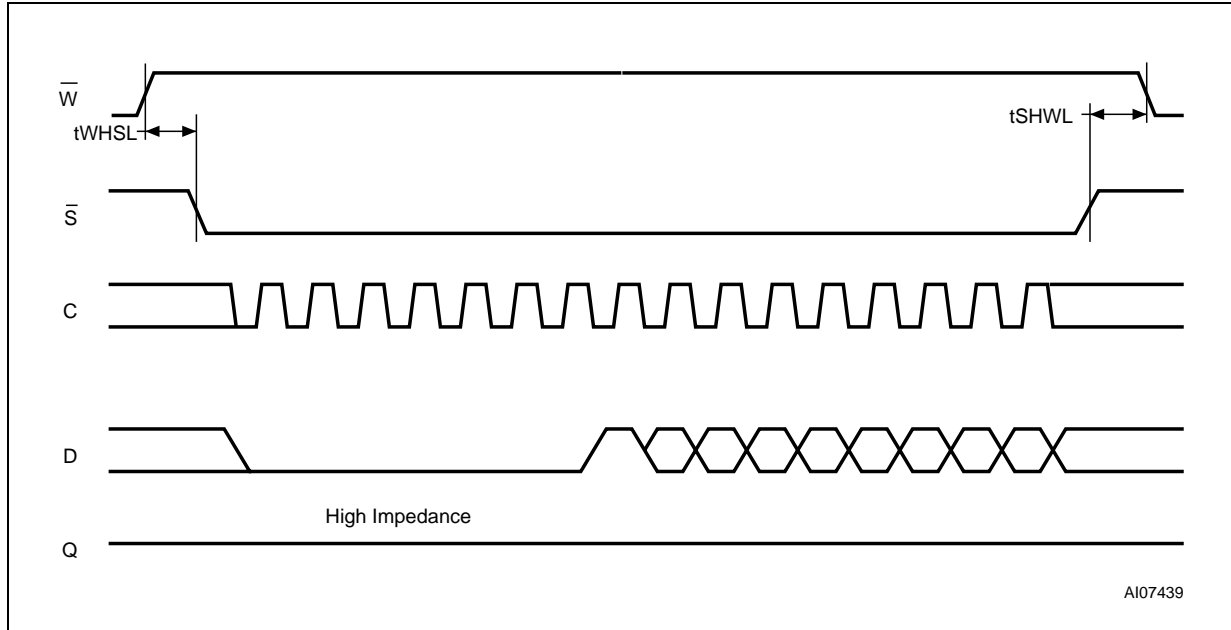
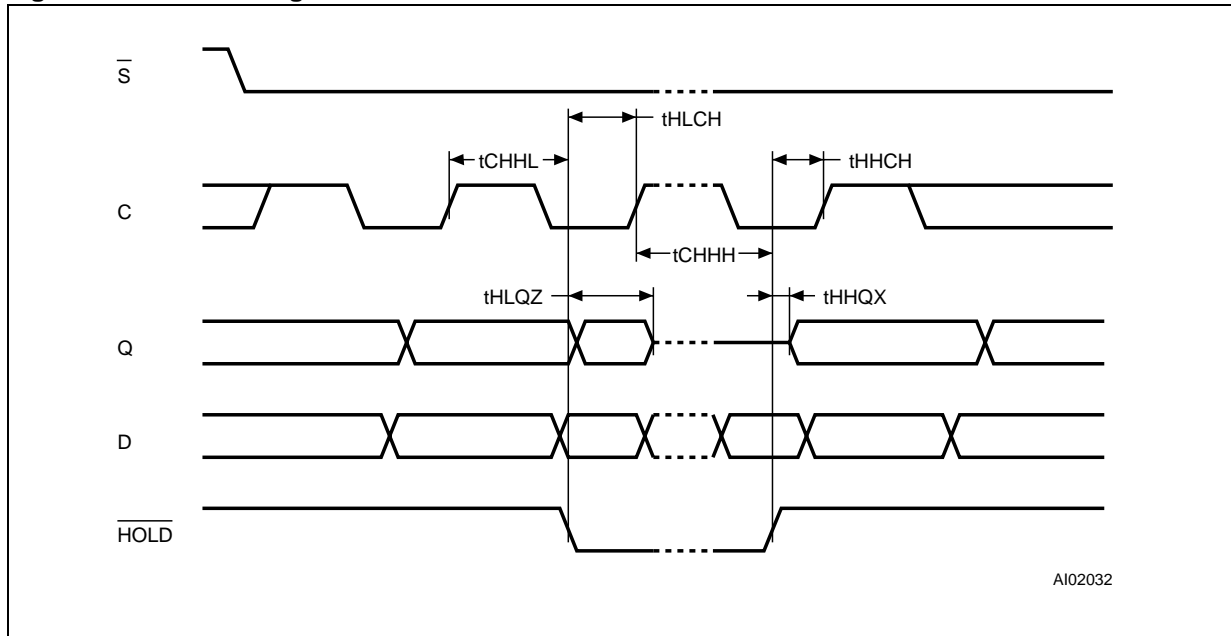
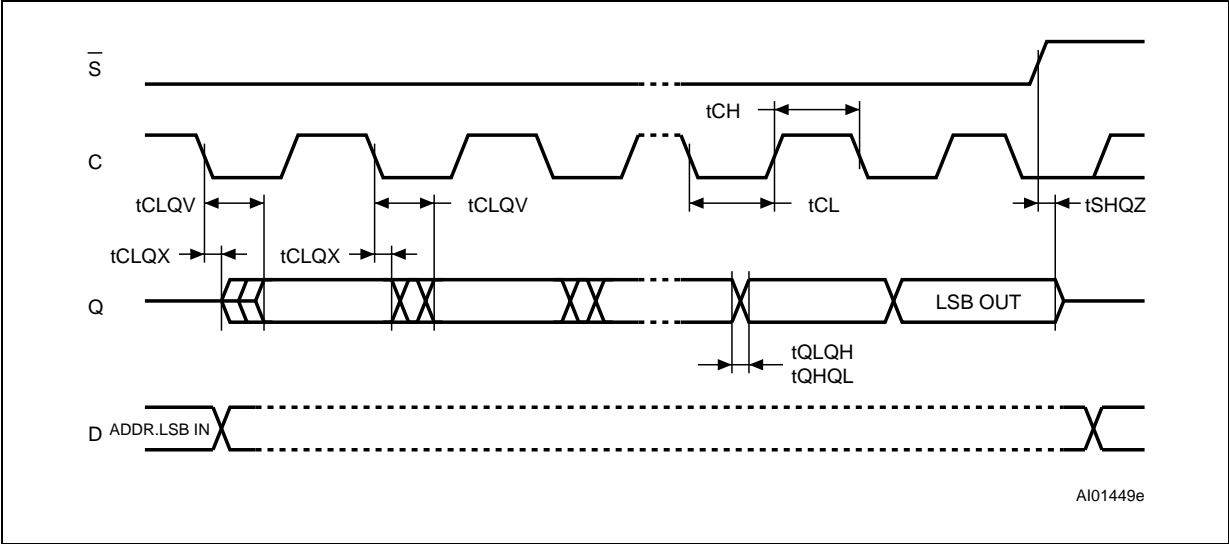
**Figure 24. Write Protect setup and hold timing during WRSR when SRWD = 1****Figure 25. Hold timing**

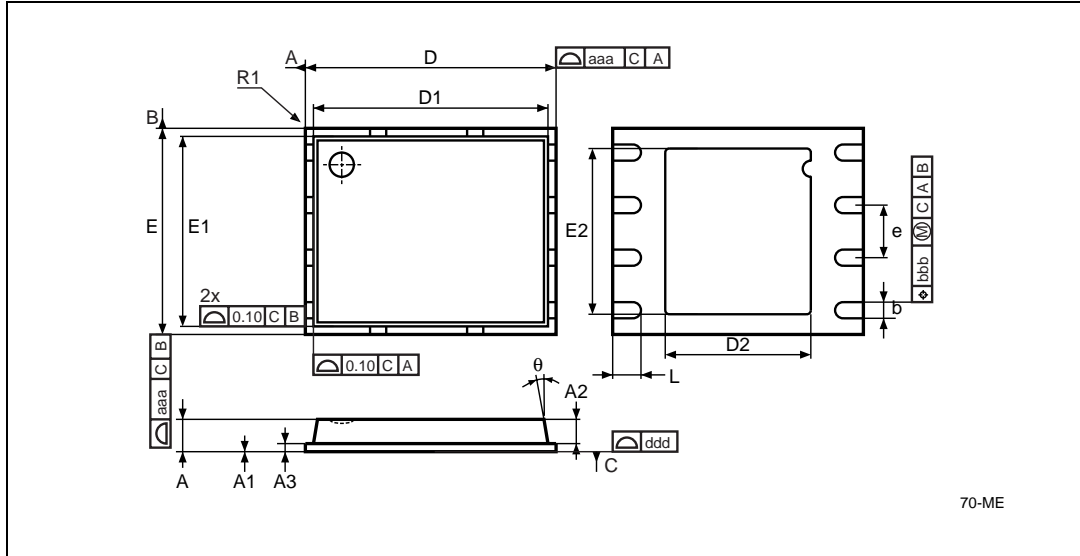
Figure 26. Output timing



# 11 Package mechanical

In order to meet environmental requirements, Numonyx offers these devices in RoHS compliant packages, which have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label.

**Figure 27. VFQFPN8 (MLP8) 8-lead very thin fine pitch quad flat package no lead, 6 × 5 mm, package outline**



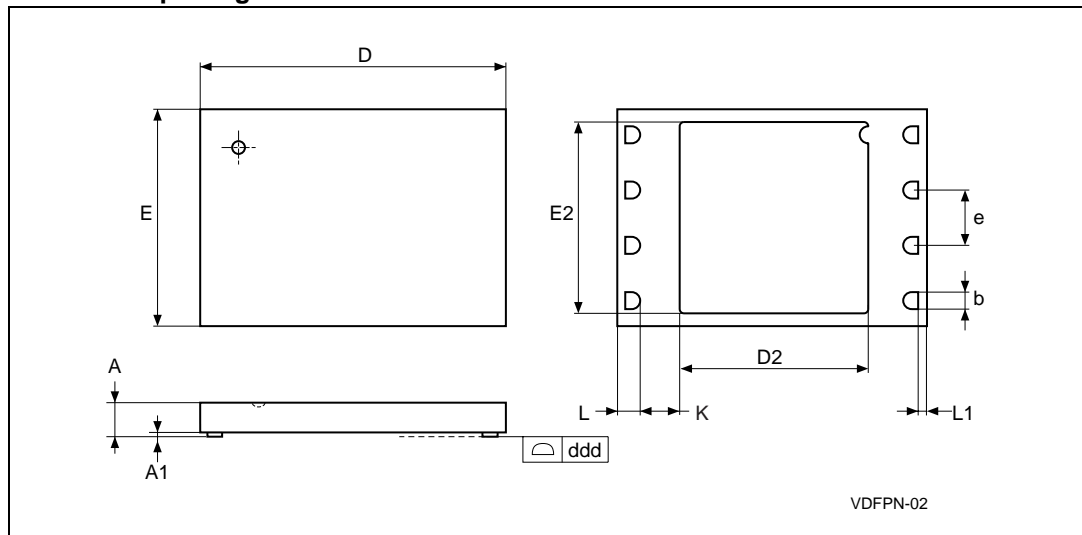
1. Drawing is not to scale.
2. The circle in the top view of the package indicates the position of pin 1.

**Table 17. VFQFPN8 (MLP8) 8-lead very thin fine pitch quad flat package no lead, 6 × 5 mm, package mechanical data**

| Symbol | millimeters |      |      | inches |       |       |
|--------|-------------|------|------|--------|-------|-------|
|        | Typ         | Min  | Max  | Typ    | Min   | Max   |
| A      | 0.85        | 0.80 | 1.00 | 0.033  | 0.031 | 0.039 |
| A1     |             | 0.00 | 0.05 |        | 0.000 | 0.002 |
| A2     | 0.65        |      |      | 0.026  |       |       |
| A3     | 0.20        |      |      | 0.008  |       |       |
| b      | 0.40        | 0.35 | 0.48 | 0.016  | 0.014 | 0.019 |
| D      | 6.00        |      |      | 0.236  |       |       |
| D1     | 5.75        |      |      | 0.226  |       |       |
| D2     | 3.40        | 3.20 | 3.60 | 0.134  | 0.126 | 0.142 |
| E      | 5.00        |      |      | 0.197  |       |       |
| E1     | 4.75        |      |      | 0.187  |       |       |
| E2     | 4.00        | 3.80 | 4.30 | 0.157  | 0.150 | 0.169 |
| e      | 1.27        | –    | –    | 0.050  | –     | –     |
| R1     | 0.10        | 0.00 |      | 0.004  | 0.000 |       |
| L      | 0.60        | 0.50 | 0.75 | 0.024  | 0.020 | 0.029 |
| Θ      |             |      | 12°  |        |       | 12°   |
| aaa    |             |      | 0.15 |        |       | 0.006 |
| bbb    |             |      | 0.10 |        |       | 0.004 |
| ddd    |             |      | 0.05 |        |       | 0.002 |



**Figure 28. VDFPN8 (MLP8) 8-lead very thin dual flat package no lead, 8 × 6 mm, package outline**



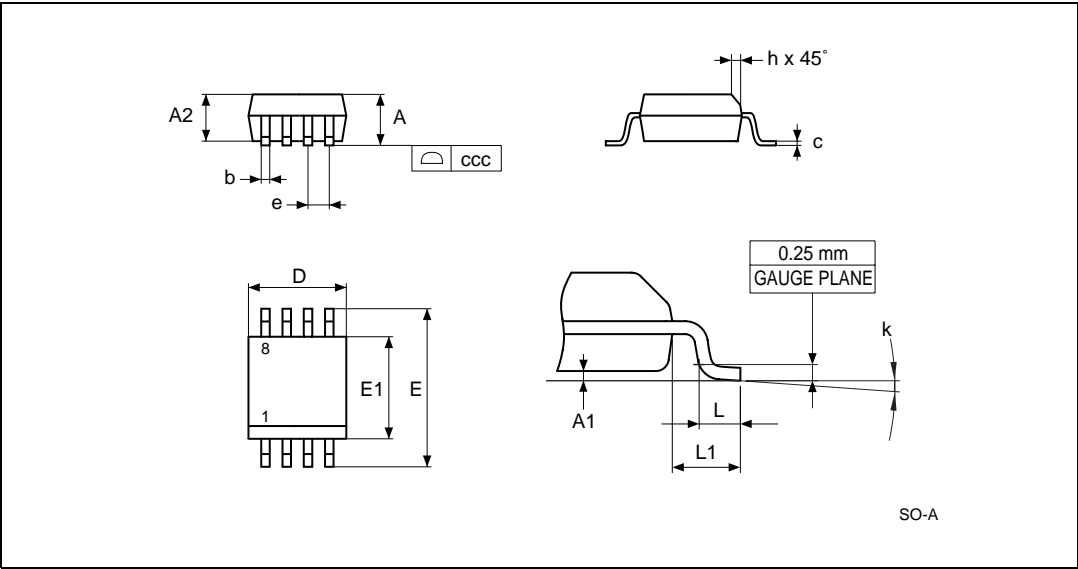
1. Drawing is not to scale.
2. The circle in the top view of the package indicates the position of pin 1.

**Table 18. VDFPN8 (MLP8) 8-lead very thin dual flat package no lead, 8 × 6 mm, package mechanical data**

| Symbol | millimeters |      |      | inches |       |       |
|--------|-------------|------|------|--------|-------|-------|
|        | Typ         | Min  | Max  | Typ    | Min   | Max   |
| A      | 0.85        |      | 1.00 | 0.033  |       | 0.039 |
| A1     |             | 0.00 | 0.05 |        | 0.000 | 0.002 |
| b      | 0.40        | 0.35 | 0.48 | 0.016  | 0.014 | 0.019 |
| D      | 8.00        |      |      | 0.315  |       |       |
| D2     | 5.16        |      | (1)  | 0.203  |       |       |
| ddd    |             |      | 0.05 |        |       | 0.002 |
| E      | 6.00        |      |      | 0.236  |       |       |
| E2     | 4.80        |      |      | 0.189  |       |       |
| e      | 1.27        | —    | —    | 0.050  | —     | —     |
| K      |             | 0.82 |      |        | 0.032 |       |
| L      | 0.50        | 0.45 | 0.60 | 0.020  | 0.018 | 0.024 |
| L1     |             |      | 0.15 |        |       | 0.006 |
| N      | 8           |      |      | 8      |       |       |

1. D2 Max should not exceed  $(D - K - 2 \times L)$ .

Figure 29. SO8N – 8 lead plastic small outline, 150 mils body width, package outline

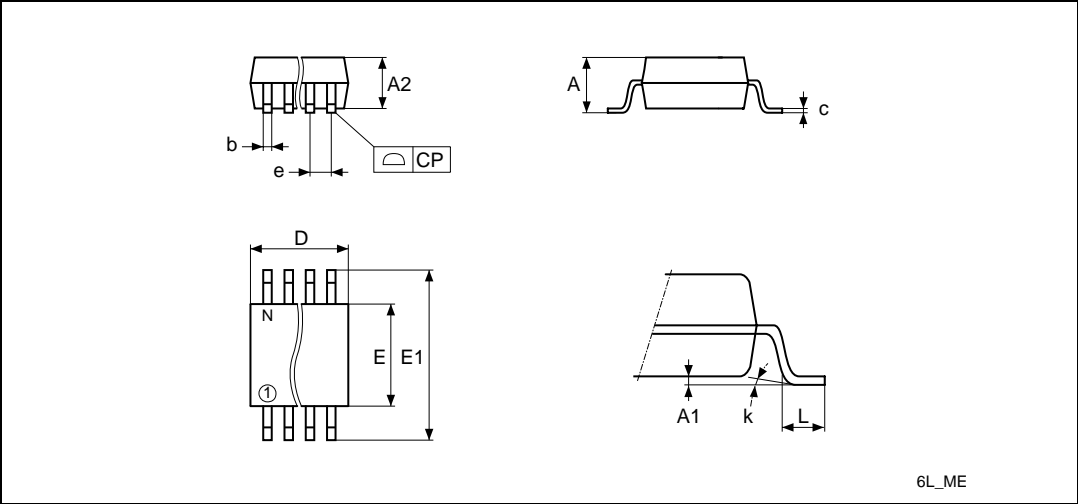


1. Drawing is not to scale.

Table 19. SO8N – 8 lead plastic small outline, 150 mils body width, package mechanical data

| Symbol | millimeters |      |      | inches |       |       |
|--------|-------------|------|------|--------|-------|-------|
|        | Typ         | Min  | Max  | Typ    | Min   | Max   |
| A      |             |      | 1.75 |        |       | 0.069 |
| A1     |             | 0.10 | 0.25 |        | 0.004 | 0.010 |
| A2     |             | 1.25 |      |        | 0.049 |       |
| b      |             | 0.28 | 0.48 |        | 0.011 | 0.019 |
| c      |             | 0.17 | 0.23 |        | 0.007 | 0.009 |
| ccc    |             |      | 0.10 |        |       | 0.004 |
| D      | 4.90        | 4.80 | 5.00 | 0.193  | 0.189 | 0.197 |
| E      | 6.00        | 5.80 | 6.20 | 0.236  | 0.228 | 0.244 |
| E1     | 3.90        | 3.80 | 4.00 | 0.154  | 0.150 | 0.157 |
| e      | 1.27        | –    | –    | 0.050  | –     | –     |
| h      |             | 0.25 | 0.50 |        | 0.010 | 0.020 |
| k      |             | 0°   | 8°   |        | 0°    | 8°    |
| L      |             | 0.40 | 1.27 |        | 0.016 | 0.050 |
| L1     | 1.04        |      |      | 0.041  |       |       |

Figure 30. SO8W – 8 lead plastic small outline, 208 mils body width, package outline

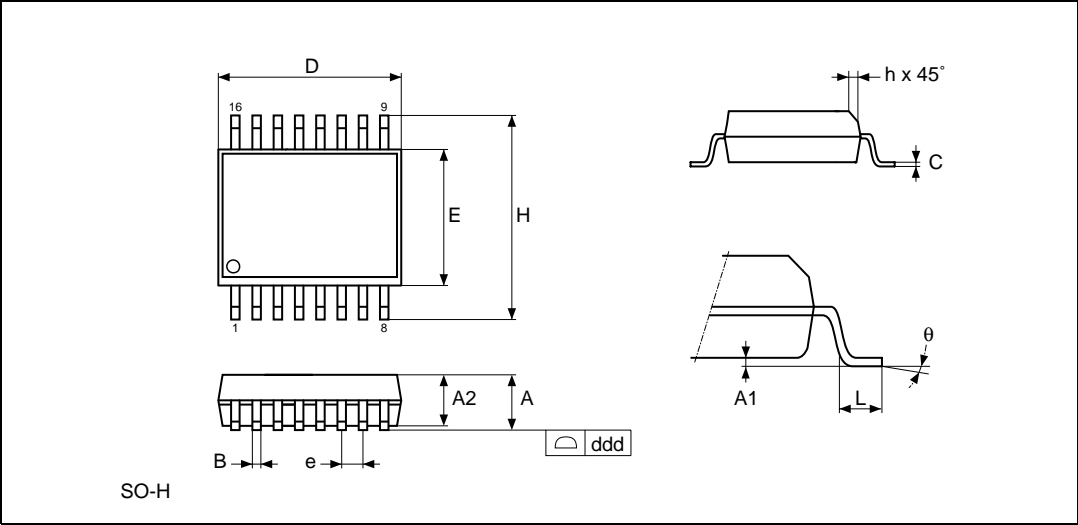


1. Drawing is not to scale.

Table 20. SO8 wide – 8 lead plastic small outline, 208 mils body width, package mechanical data

| Symbol | millimeters |      |      | inches |       |       |
|--------|-------------|------|------|--------|-------|-------|
|        | Typ         | Min  | Max  | Typ    | Min   | Max   |
| A      |             |      | 2.50 |        |       | 0.098 |
| A1     |             | 0.00 | 0.25 |        | 0.000 | 0.010 |
| A2     |             | 1.51 | 2.00 |        | 0.059 | 0.079 |
| b      | 0.40        | 0.35 | 0.51 | 0.016  | 0.014 | 0.020 |
| c      | 0.20        | 0.10 | 0.35 | 0.008  | 0.004 | 0.014 |
| CP     |             |      | 0.10 |        |       | 0.004 |
| D      |             |      | 6.05 |        |       | 0.238 |
| E      |             | 5.02 | 6.22 |        | 0.198 | 0.245 |
| E1     |             | 7.62 | 8.89 |        | 0.300 | 0.350 |
| e      | 1.27        | –    | –    | 0.050  | –     | –     |
| k      |             | 0°   | 10°  |        | 0°    | 10°   |
| L      |             | 0.50 | 0.80 |        | 0.020 | 0.031 |
| N      | 8           |      |      | 8      |       |       |

Figure 31. SO16 wide – 16-lead plastic small outline, 300 mils body width, package outline

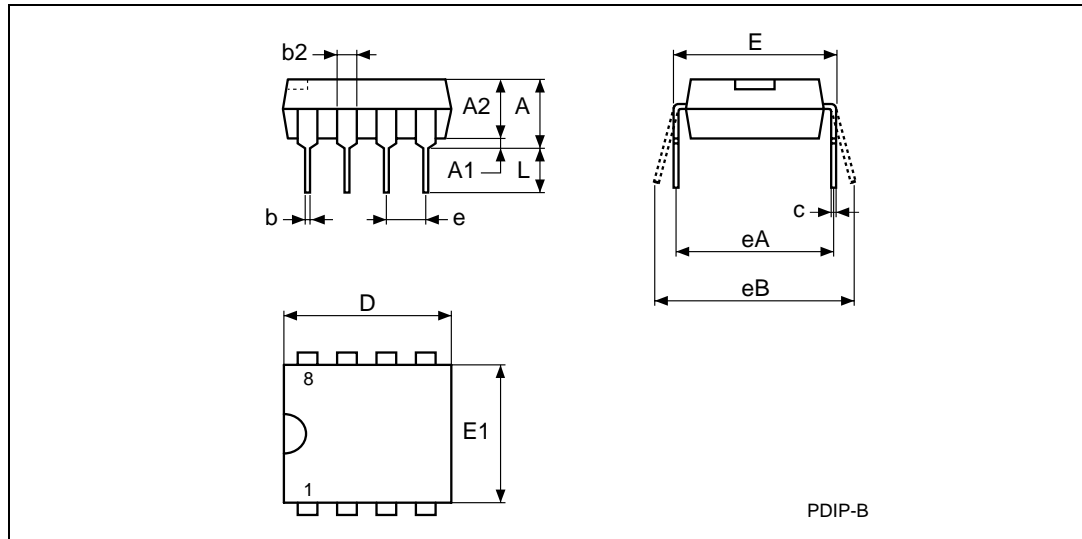


1. Drawing is not to scale.

Table 21. SO16 wide – 16-lead plastic small outline, 300 mils body width, mechanical data

| Symbol | millimeters |       |       | inches |       |       |
|--------|-------------|-------|-------|--------|-------|-------|
|        | Typ         | Min   | Max   | Typ    | Min   | Max   |
| A      |             | 2.35  | 2.65  |        | 0.093 | 0.104 |
| A1     |             | 0.10  | 0.30  |        | 0.004 | 0.012 |
| B      |             | 0.33  | 0.51  |        | 0.013 | 0.020 |
| C      |             | 0.23  | 0.32  |        | 0.009 | 0.013 |
| D      |             | 10.10 | 10.50 |        | 0.398 | 0.413 |
| E      |             | 7.40  | 7.60  |        | 0.291 | 0.299 |
| e      | 1.27        | –     | –     | 0.050  | –     | –     |
| H      |             | 10.00 | 10.65 |        | 0.394 | 0.419 |
| h      |             | 0.25  | 0.75  |        | 0.010 | 0.030 |
| L      |             | 0.40  | 1.27  |        | 0.016 | 0.050 |
| θ      |             | 0°    | 8°    |        | 0°    | 8°    |
| ddd    |             |       | 0.10  |        |       | 0.004 |

**Figure 32. PDIP8 – 8 lead Plastic Small Outline, 300 mils body width, package outline**



1. Package is not to scale.

**Table 22. PDIP8 – 8 lead Plastic Small Outline, 300 mils body width, package mechanical data**

| Symbol | millimeters |      |       | inches |       |       |
|--------|-------------|------|-------|--------|-------|-------|
|        | Typ         | Min  | Max   | Typ    | Min   | Max   |
| A      |             |      | 4.80  |        |       | 0.188 |
| A1     | 0.50        |      |       | 0.019  |       |       |
| A2     | 3.10        | 3.30 | 3.50  | 0.122  | 0.129 | 0.137 |
| b      | 0.38        |      | 0.55  | 0.014  |       | 0.021 |
| b2     | 1.47        | 1.52 | 1.57  | 0.057  | 0.059 | 0.061 |
| c      | 0.21        |      | 0.35  | 0.008  |       | 0.013 |
| D      | 9.10        | 9.20 | 9.30  | 0.358  | 0.362 | 0.366 |
| E      | 7.62        | 7.87 | 8.25  | 0.300  | 0.309 | 0.324 |
| E1     | 6.25        | 6.35 | 6.45  | 0.246  | 0.250 | 0.253 |
| e      |             | 2.54 |       |        | 0.100 |       |
| eA     |             | 7.62 |       |        | 0.300 |       |
| eB     | 7.62        | 8.80 | 10.90 | 0.300  | 0.346 | 0.429 |
| L      | 2.92        | 3.30 | 3.81  | 0.114  | 0.122 | 0.150 |

## 12 Part numbering

**Table 23. Ordering information scheme**

|                                                                 |        |   |   |    |   |   |   |
|-----------------------------------------------------------------|--------|---|---|----|---|---|---|
| Example:                                                        | M25P16 | – | V | ME | 6 | T | P |
| <b>Device type</b>                                              |        |   |   |    |   |   |   |
| M25P = Serial Flash memory for code storage                     |        |   |   |    |   |   |   |
| <b>Device function</b>                                          |        |   |   |    |   |   |   |
| 16 = 16 Mbit (2 Mbit × 8)                                       |        |   |   |    |   |   |   |
| <b>Security features<sup>(1)</sup></b>                          |        |   |   |    |   |   |   |
| – = no extra security                                           |        |   |   |    |   |   |   |
| S = CFD programmed with UID                                     |        |   |   |    |   |   |   |
| <b>Operating voltage</b>                                        |        |   |   |    |   |   |   |
| V = V <sub>CC</sub> = 2.7 V to 3.6 V                            |        |   |   |    |   |   |   |
| <b>Package</b>                                                  |        |   |   |    |   |   |   |
| MP = VFQFPN8 6 × 5 mm (MLP8)                                    |        |   |   |    |   |   |   |
| ME = VDFPN8 8 × 6 mm (MLP8) <sup>(2)</sup>                      |        |   |   |    |   |   |   |
| MN = SO8N (150 mils width)                                      |        |   |   |    |   |   |   |
| MW = SO8W (208 mils width)                                      |        |   |   |    |   |   |   |
| MF = SO16 (300 mils width)                                      |        |   |   |    |   |   |   |
| BA = PDIP8 (300 mils width)                                     |        |   |   |    |   |   |   |
| <b>Device grade</b>                                             |        |   |   |    |   |   |   |
| 6 = Industrial temperature range, –40 to 85 °C.                 |        |   |   |    |   |   |   |
| Device tested with standard test flow                           |        |   |   |    |   |   |   |
| 3 <sup>(3)</sup> = Automotive temperature range, –40 to 125 °C. |        |   |   |    |   |   |   |
| Device tested with high reliability certified flow.             |        |   |   |    |   |   |   |
| <b>Option</b>                                                   |        |   |   |    |   |   |   |
| blank = Standard packing                                        |        |   |   |    |   |   |   |
| T = Tape and reel packing                                       |        |   |   |    |   |   |   |
| <b>Plating Technology</b>                                       |        |   |   |    |   |   |   |
| P or G = RoHS compliant                                         |        |   |   |    |   |   |   |

1. Secure options are available upon customer request.

2. Not for new design, please use VFQFPN8 6 × 5 mm.

3. Grade 3 is available only in devices delivered in SO8N packages.

**Note:** For a list of available options (speed, package, etc.), for further information on any aspect of this device or when ordering parts operating at 75 MHz (0.11 μm, process digit '4'), please contact your nearest Numonyx Sales Office.

## 13 Revision history

**Table 24. Document revision history**

| Date        | Revision | Changes                                                                                                                                                                                                                                                                                                                                                                                              |
|-------------|----------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 16-Jan-2002 | 0.1      | Target Specification Document written                                                                                                                                                                                                                                                                                                                                                                |
| 23-Apr-2002 | 0.4      | Clarification of descriptions of entering Standby Power mode from Deep Power-down mode, and of terminating an instruction sequence or data-out sequence.<br>ICC2(max) value changed to 10 $\mu$ A                                                                                                                                                                                                    |
| 13-Dec-2002 | 0.5      | Typical Page Program time improved. Write Protect setup and hold times specified, for applications that switch Write Protect to exit the Hardware Protection mode immediately before a WRSR, and to enter the Hardware Protection mode again immediately after                                                                                                                                       |
| 15-May-2003 | 0.6      | MLP8 package added                                                                                                                                                                                                                                                                                                                                                                                   |
|             | 0.7      | 50MHz operation, and RDID instruction added. Published internally, only                                                                                                                                                                                                                                                                                                                              |
| 20-Jun-2003 | 0.8      | 8x6 MLP8 and SO16(300 mil) packages added                                                                                                                                                                                                                                                                                                                                                            |
| 24-Sep-2003 | 1.0      | $t_{PP}$ , $t_{SE}$ and $t_{BE}$ revised. SO16 package code changed. Output Timing Reference Voltage changed. Document promoted to Preliminary Data.                                                                                                                                                                                                                                                 |
| 24-Nov-2003 | 2.0      | Table of contents, warning about exposed paddle on MLP8, and Pb-free options added.<br>Value of $t_{VSL}$ (min) and $t_{BE}$ (typ) changed. Change of naming for VDFPN8 packages. Document promoted to full Datasheet.                                                                                                                                                                               |
| 17-May-2004 | 3.0      | MLP8(5x6) package removed. Soldering temperature information clarified for RoHS compliant devices. Device Grade clarified                                                                                                                                                                                                                                                                            |
| 01-Apr-2005 | 4.0      | Notes 1 and 2 removed from <a href="#">Table 23: Ordering information scheme</a> . Small text changes.<br><a href="#">Read Identification (RDID)</a> , <a href="#">Deep Power-down (DP)</a> and <a href="#">Release from Deep Power-down and Read Electronic Signature (RES)</a> instructions, and <a href="#">Active Power, Standby Power and Deep Power-down modes</a> paragraph clarified.        |
| 01-Aug-2005 | 5.0      | Updated Page Program (PP) instructions in <a href="#">Page programming, Page Program (PP)</a> and Table 15: AC characteristics (Grade 6).                                                                                                                                                                                                                                                            |
| 20-Oct-2005 | 6.0      | VFQFPN8 package added (see <a href="#">Figure 27: VFQFPN8 (MLP8) 8-lead very thin fine pitch quad flat package no lead, 6 × 5 mm, package outline</a> and <a href="#">Table 17: VFQFPN8 (MLP8) 8-lead very thin fine pitch quad flat package no lead, 6 × 5 mm, package mechanical data</a> ).<br>All packages are RoHS compliant. "Blank" option removed under <a href="#">Plating Technology</a> . |
| 27-Feb-2006 | 7        | SO8 Narrow and SO8 Wide packages added (see <a href="#">Section 11: Package mechanical</a> ). VDFPN8 package updated (see <a href="#">Table 18: VDFPN8 (MLP8) 8-lead very thin dual flat package no lead, 8 × 6 mm, package mechanical data</a> ). <a href="#">Note 2</a> added to <a href="#">Table 23: Ordering information scheme</a> .                                                           |
| 04-Jul-2006 | 8        | <a href="#">Figure 4: Bus master and memory devices on the SPI bus</a> updated and <a href="#">Note 2</a> added. SO8N package specifications updated (see <a href="#">Figure 29</a> and <a href="#">Table 19</a> ). Small text changes.                                                                                                                                                              |

**Table 24. Document revision history (continued)**

| Date        | Revision | Changes                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|-------------|----------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10-Oct-2006 | 9        | Page Program, Sector Erase and Bulk Erase updated in <a href="#">Features</a> .<br>V <sub>IO</sub> max modified in <a href="#">Table 9: Absolute maximum ratings</a> .<br><a href="#">Table 15: AC characteristics (T9HX technology)</a> added.<br>VFQFPN8 package specifications updated (see <a href="#">Table 17</a> ). <a href="#">Note 1</a> added to <a href="#">Table 18</a> . <a href="#">Note: on page 54</a> modified.                                                                                                                                                                                                                                                                                                                                                                                           |
| 09-Jan-2007 | 10       | Small text changes. Hardware Write protection added to <a href="#">Features</a> .<br><a href="#">VCC supply voltage</a> and <a href="#">VSS ground</a> signal descriptions added. <a href="#">Figure 4: Bus master and memory devices on the SPI bus</a> modified, note 2 removed and replaced by an explanatory paragraph. Write In Progress bit behavior specified at Power-up (see <a href="#">Section 7: Power-up and power-down</a> ). T <sub>LEAD</sub> added to <a href="#">Table 9: Absolute maximum ratings</a> . Grade 3 temperature range added.<br><a href="#">Table 11: Data retention and endurance</a> and <a href="#">Table 16: AC characteristics (25 MHz operation)</a> added.<br>SO8W and VFQFPN8 package specifications updated (see <a href="#">Section 11: Package mechanical</a> ).                 |
| 15-Jun-2007 | 11       | Eliminated the reference to the Deep Power-down mode and updated the Read Identification instruction in <a href="#">Section 6.3: Read Identification (RDID)</a> .<br>Inserted UID and CFI content columns in <a href="#">Table 5: Read Identification (RDID) data-out sequence</a> .<br>Modified Data bytes for RDID instruction in <a href="#">Table 4: Instruction set</a> .<br>Modified Q signal in <a href="#">Figure 10: Read Identification (RDID) instruction sequence and data-out sequence</a> .<br>Modified Test condition and maximum values for I <sub>CC3</sub> in <a href="#">Table 14: DC characteristics</a> .<br>Eliminated <a href="#">Table 15: AC characteristics (Grade 6)</a> .<br>Modified the maximum value for f <sub>C</sub> in <a href="#">Table 15: AC characteristics (T9HX technology)</a> . |
| 31-Oct-2007 | 12       | Removed 'low voltage' from the title. Changed the typical time for Bulk Erase on page 1.<br><a href="#">Section 6.3: Read Identification (RDID)</a> updated.<br>Added note 2 and 3 to <a href="#">Table 9: Absolute maximum ratings</a> .<br>Modified maximum value for t <sub>CLQV</sub> in <a href="#">Table 15: AC characteristics (T9HX technology)</a> .                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| 10-Dec-2007 | 13       | Applied Numonyx branding.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 20-Jun-2008 | 14       | Added a reference to customer's ability to request dedicated part number in <a href="#">Section 6.3: Read Identification (RDID) on page 22</a> .<br>Moved specifications in "max" column to "min" column and changed the "min" for grade 3 to 10,000 in <a href="#">Table 11: Data retention and endurance on page 39</a> .<br>Deleted "grade 6" reference in <a href="#">Table 15: AC characteristics (T9HX technology) on page 41</a> .<br>Deleted "grade 3" reference and "preliminary note" in <a href="#">Table 16: AC characteristics (25 MHz operation) on page 43</a> .<br>Revised <a href="#">Section 12: Part numbering on page 54</a> .                                                                                                                                                                         |
| 5-Dec-2008  | 15       | Added the PDIP8 (BA), 300 mils width package information.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |



**Please Read Carefully:**

INFORMATION IN THIS DOCUMENT IS PROVIDED IN CONNECTION WITH NUMONYX™ PRODUCTS. NO LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE, TO ANY INTELLECTUAL PROPERTY RIGHTS IS GRANTED BY THIS DOCUMENT. EXCEPT AS PROVIDED IN NUMONYX'S TERMS AND CONDITIONS OF SALE FOR SUCH PRODUCTS, NUMONYX ASSUMES NO LIABILITY WHATSOEVER, AND NUMONYX DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY, RELATING TO SALE AND/OR USE OF NUMONYX PRODUCTS INCLUDING LIABILITY OR WARRANTIES RELATING TO FITNESS FOR A PARTICULAR PURPOSE, MERCHANTABILITY, OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

Numonyx products are not intended for use in medical, life saving, life sustaining, critical control or safety systems, or in nuclear facility applications.

Numonyx may make changes to specifications and product descriptions at any time, without notice.

Numonyx, B.V. may have patents or pending patent applications, trademarks, copyrights, or other intellectual property rights that relate to the presented subject matter. The furnishing of documents and other materials and information does not provide any license, express or implied, by estoppel or otherwise, to any such patents, trademarks, copyrights, or other intellectual property rights.

Designers must not rely on the absence or characteristics of any features or instructions marked "reserved" or "undefined." Numonyx reserves these for future definition and shall have no responsibility whatsoever for conflicts or incompatibilities arising from future changes to them.

Contact your local Numonyx sales office or your distributor to obtain the latest specifications and before placing your product order.

Copies of documents which have an order number and are referenced in this document, or other Numonyx literature may be obtained by visiting Numonyx's website at <http://www.numonyx.com>.

Numonyx StrataFlash is a trademark or registered trademark of Numonyx or its subsidiaries in the United States and other countries.

\*Other names and brands may be claimed as the property of others.

Copyright © 2008, Numonyx, B.V., All Rights Reserved.