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Product Anomaly Notification (PAN)

Device affected (product name):	**Active device version(s)**:
nRF51822-QFAA and nRF51422-QFAA	Build code CA
Date (YYYY-MM-DD):	**PAN no.:**
2012-09-26	PAN-028
Nordic Semiconductor reference:	**Document version**:
Thomas Embla Bonnerud	1.1

Anomalies in active device version(s)

Summary:

Anomalies in active device versions:

1. ADC: ADC module analog front end do not power down when END event occurs
2. ADC: STOP task clears the RESULT register
3. ANT: Erroneous packet transmission
4. ANT: Bursting on a non-tracking channel
5. CLOCK: Clock is paused when switching clock source for HFCLK clock
6. DIF: Missing pull down on SWDCLK
7. GPIO: SENSE mechanism fires under some circumstances when it should not.
8. GPIOTE: OUTINIT field in CONFIGn register is not functional
9. GPIOTE: The module cannot receive tasks or detect transitions on the pad during the first 3 clock periods after being enabled
10. GPIOTE: The output value of the pin cannot be controlled by GPIOTE when the pin is configured as event generator
11. HFCLK: Base current with HFCLK running is too high
12. LFCLK: Calibration does not request HFCLK
13. POWER: It is not possible to distinguish between Power on reset and reset from off by RESETREAS
14. RADIO: END to START connection using PPI or short is not functional
15. RADIO: RSSI module analog front end do not power down when RSSIEND event occurs
16. RADIO: RSSISTOP task clears the RSSISAMPLE register
17. RADIO: State Register is not functional
18. RNG: Generated random value is reset when VALRDY event is cleared
19. RNG: STOP task clears the VALUE register
20. RNG: The STOP task cannot be assigned to a PPI channel
21. RTC and WDT: Reset on 32KiHz domains delayed when peripherals turned off and 32KiHz clock is running
22. System: Issues with disable system OFF mechanism
23. System: Manual setup is required to enable use of peripherals
24. TEMP: Negative measured values are not represented correctly.
25. TEMP: STOP task clears the TEMP register.
26. TEMP: TEMP module analog front end do not power down when DATARDY event occurs.
27. TEMP: Temperature offset value has to be manually loaded to the TEMP module
28. TIMER: BITMODE is not functional
29. TIMER: The CC registers does not generate an event when the previous value generated an event in the same CC register
30. TIMER: Timer cannot handle quick START-STOP-START tasks correctly
31. TWI: Shortcuts described in nRF51 Reference Manual are not functional
32. UART: After a STOPRX task the UART will not be able to finish transaction
33. WDT: The watchdog config option "RUN while paused by the debugger" does not work

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Marking / tracing:

nRF51822-QFAA and nRF51422-QFAA

Build: CA

Build: CA

Where the letters on the last line of the chip marking means:

- Y = Year assembly marking, e.g. YY=11
- W = Week assembly marking, e.g. WW=35
- L = Wafer lot, step letters for each lot, e.g. LL={AA, AB,…,AZ, BA,…,ZZ, AA, AB,…}

Authorization for Nordic Semiconductor

Product Manager	Date:	Sign:
Thomas Embla Bonnerud	25/09/2012	

Changelog

Version	Change
1.1	Changed sorting of PANS to alphabetical sorting
	Added anomaly: GPIO: SENSE mechanism fires under some circumstances when it should not
	Added code example to anomaly: GPIOTE: OUTINIT field in CONFIGn register is not functional
	Added anomaly: HFCLK: XTALFREQ register is not functional
	Added anomaly: System: Issues with disable system OFF mechanism
	Added anomaly: TEMP: Negative measured values are not represented correctly
	Added anomaly: TEMP: STOP task clears the TEMP register
	Added anomaly: TEMP: TEMP module analog front end do not power down when DATARDY event occurs
	Removed anomaly: TEMP: The module is not functional
	Added anomaly: TEMP: Temperature offset value has to be manually loaded to the TEMP module
	Added information on which anomalies that are planned fixed for the next version of the IC

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1. ADC: ADC module analog front end does not power down when END event occurs	**Device version(s) affected**: nRF51422/nRF51822 Build code CA
Symptoms: Higher current consumption.	
Conditions: Always.	
Consequences: Higher current consumption.	
Workaround: Trigger STOP task to power down analog front end and reduce power consumption. This anomaly will be fixed in the next version of the IC.	

2. ADC: STOP task clears the RESULT register	**Device version(s) affected**: nRF51422/nRF51822 Build code CA
Symptoms: When STOP task is triggered, VALUE register is cleared.	
Conditions: Always.	
Consequences: If STOP task is triggered before reading the converted value in RESULT, the value will be lost and read as 0x00.	
Workaround: Read RESULT before triggering STOP task. This anomaly will be fixed in the next version of the IC.	

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3. ANT: Erroneous packet transmission	**Device version(s) affected**: nRF51422 Build code CA

Symptoms:

Packets can be erroneous and sporadically transmitted in the reverse-channel direction when running a receive channel.

Conditions:

This can happen if the Channel ID (Device number, Device type and Transmission type) of the receive channel is also set on another channel on the device and the last transmission to be sent from the device was done from the other channel.

Consequences:

The receive channel could sporadically transmit packets in the reverse-channel direction even though no packet transmission was initiated by the host.

Workaround:

Avoid setting the same Channel ID (Device number, Device type and Transmission type) on multiple channels.

4. ANT: Bursting on a non-tracking channel	**Device version(s) affected**: nRF51422 Build code CA

Symptoms:

The burst handler can become “stuck” and will not allow any further transfers.

Conditions:

This will happen if the application initiates sending a burst transfer on a channel when it is not in the tracking state (that is, when the channel is either searching or not opened).

Consequences:

The burst handler will not complete the current transfer and will not allow sending any new transfers.

Workaround:

Avoid sending a burst transfer when the channel is not in a tracking state. In the event that the transfer handler does become stuck issuing a stack reset will clear the condition.

5. CLOCK: Clock is paused when switching clock source for HFCLK clock	**Device version(s) affected**: nRF51422/nRF51822 Build code CA

Symptoms:

When switching from 16 MHz RC oscillator to 16 MHz crystal oscillator the system clock will be stopped for 8 clock cycles (0.5µs).
When switching from 16 MHz crystal oscillator to 16 MHz RC oscillator the system clock will be stopped for tSTART,RC16M.

Conditions:

When 16 MHz crystal oscillator is requested by triggering HFCLKSTART the system will run on 16 MHz RC oscillator until the 16 MHz crystal oscillator is started. At that point the system will automatically switch to 16 MHz crystal oscillator, but the anomaly will delay this switch.
When 16 MHz crystal oscillator is no longer requested by triggering HFCLKSTOP the system will automatically switch back to 16 MHz RC oscillator, but the anomaly will delay this switch.

Consequences:

Timing for Serial interfaces and other modules and code that uses GPIO's will be affected during switching of HFCLK clock source.

Workaround:

Care has to be taken to avoid switching clock source when using serial interfaces to avoid timing problems.

This anomaly will be fixed in the next version of the IC.

6. DIF: Missing pull down on SWDCLK	**Device version(s) affected**: nRF51422/nRF51822 Build code CA

Symptoms:

- Pin reset function may not work
- High current consumption
- Device is hanging

Conditions:

Always.

Consequences:

- Pin reset function may not work
- High current consumption
- Device is hanging

Workaround:

Add external pull down on SWDCLK pin.

This anomaly will be fixed in the next version of the IC.

7. GPIO: SENSE mechanism fires under some circumstances when it should not.	**Device version(s) affected**: nRF51422/nRF51822 Build code CA

Symptoms:

Sometimes a PORT event is generated when it should not have been generated.

Conditions:

Input buffer is disconnected and then wakeup functionality and buffer connect are enabled on a pad in the same write operation to PIN_CNF.

Consequences:

False interrupt and/or PORT event might be triggered at write to PIN_CNF register.

Workaround:

Connect input buffer before enabling the wakeup functionality.

This anomaly will be fixed in the next version of the IC.

8. GPIOTE: OUTINIT field in CONFIGn register is not functional	**Device version(s) affected**: nRF51422/nRF51822 Build code CA

Symptoms:

Initial value for GPIOTE output after configuration is undefined.

Conditions:

Configuring a GPIOTE channel as a task.

Consequences:

Application specific.

Workaround:

1. Configure the GPIOTE channel as follows:
   - MODE: TASK
   - PSEL: Set to unused output pin.
   - POLARITY: LOTOHI if initial high desired, or HITOLO if initial low desired.
2. Trigger the OUT task
3. Reconfigure the GPIOTE channel as follows:
   - MODE: TASK
   - PSEL: <GPIO used for function>
   - POLARITY: <Desired polarity (Toggle, LoToHi or HiToLo>
   - OUTINIT: <Desired initial value>

The following inline function can be used to perform this action:

```
static __INLINE void nrf_gpiote_task_config(uint32_t channel_number, uint32_t pin_number,
nrf_gpiote_polarity_t polarity, nrf_gpiote_outinit_t initial_value)
{
    /* Check if the output desired is high or low */
    if (initial_value == GPIOTE_CONFIG_OUTINIT_Low)
    {
        /* Configure channel to Pin31, not connected to the pin, and configure as a tasks that will
set it to proper level */
        NRF_GPIOTE->CONFIG[channel_number] = (GPIOTE_CONFIG_MODE_Task       <<
```

```
GPIOTE_CONFIG_MODE_Pos)     |
                                        (31UL                           <<
GPIOTE_CONFIG_PSEL_Pos)     |
                                        (GPIOTE_CONFIG_POLARITY_HiToLo <<
GPIOTE_CONFIG_POLARITY_Pos);
    }
    else
    {
        /* Configure channel to Pin31, not connected to the pin, and configure as a tasks that will
set it to proper level */
        NRF_GPIOTE->CONFIG[channel_number] = (GPIOTE_CONFIG_MODE_Task       <<
GPIOTE_CONFIG_MODE_Pos)     |
                                        (31UL                           <<
GPIOTE_CONFIG_PSEL_Pos)     |
                                        (GPIOTE_CONFIG_POLARITY_LoToHi <<
GPIOTE_CONFIG_POLARITY_Pos);
    }

    /* Three NOPs are required to make sure configuration is written before setting tasks or
getting events */
    __NOP();
    __NOP();
    __NOP();

    /* Launch the task to take the GPIOTE channel output to the desired level */
    NRF_GPIOTE->TASKS_OUT[channel_number] = 1;

    /* Finally configure the channel as the caller expects. If OUTINIT works, the channel is
configured properly.
       If it does not, the channel output inheritance sets the proper level. */
    NRF_GPIOTE->CONFIG[channel_number] = (GPIOTE_CONFIG_MODE_Task << GPIOTE_CONFIG_MODE_Pos)     |
                                         ((uint32_t)pin_number    << GPIOTE_CONFIG_PSEL_Pos)     |
                                         ((uint32_t)polarity      << GPIOTE_CONFIG_POLARITY_Pos) |
                                         ((uint32_t)initial_value << GPIOTE_CONFIG_OUTINIT_Pos);

    /* Three NOPs are required to make sure configuration is written before setting tasks or
getting events */
    __NOP();
    __NOP();
    __NOP();
}
```

This anomaly will be fixed in the next version of the IC.

9. GPIOTE: The module cannot receive tasks or detect transitions on the pad during the first 3 clock periods after being enabled

Device version(s) affected:
nRF51422/nRF51822
Build code CA

Symptoms:

A task is not always detected by the module.

Conditions:

Right after enabling the module.

Consequences:

None other than the effect it will have on the application.

Workaround:

Ensure that no task is sent to the module the first 3 clock cycles after enabling.
Adding NOP statements between enable and setting tasks is recommended.

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10. GPIOTE: The output value of the pin cannot be controlled by GPIOTE when the pin is configured as event generator	**Device version(s) affected**: nRF51422/nRF51822 Build code CA

Symptoms:

The output value of the pin is not controlled by GPIO when the pin is configured as a GPIOTE event generator.

Conditions:

Always.

Consequences:

The output value of a pin is not controlled by GPIO when the pin is configured as a GPIOTE event generator. GPIOTE cannot be used to generate events from output pins.

Workaround:

None.

11. HFCLK: Base current with HFCLK running is too high	**Device version(s) affected**: nRF51422/nRF51822 Build code CA

Symptoms:

Base current is up to 700 µA higher than stated in the product specification.

Conditions:

When HFCLK clock is running.

Consequences:

1. If Timer is the only module running, too much power is drawn from the power supply. Therefore, the operation cannot be guaranteed in all situations.
2. Average current consumption for the system will be higher than specified.

Workaround:

To avoid potential problems while HFCLK is running use constant latency mode, see POWER.CONSTLAT task. To minimize idle current, use the POWER.LOWPWR task when HFCLK is not running.

This anomaly will be fixed in the next version of the IC.

12. LFCLK: Calibration does not request HFCLK	**Device version(s) affected**: nRF51422/nRF51822 Build code CA

Symptoms:

Calibration of the RC32.768 kHz clock does not finish.

Conditions:

If RcOsc calibration module is the only module requiring HFCLK clock.

Consequences:

DONE event does not occur until some module has requested HFCLK long enough for the calibration to finish. Calibration result is wrong.

Workaround:

Trigger the CONSTLAT task before starting the calibration.
Trigger the LOWPWR task when the calibration is finished.

This anomaly will be fixed in the next version of the IC.

13. POWER: It is not possible to distinguish between Power on reset and reset from off by RESETREAS	**Device version(s) affected**: nRF51422/nRF51822 Build code CA

Symptoms:

Both PowerOnReset and WakingFromOff status bits are set in RESETREAS register when entering system-off.

Conditions:

When entering system-off.

Consequences:

Impossible to distinguish between the two reset sources in question.

Workaround:

Check state of the General Purpose Retention register GPREGRET, it will keep its contents in System-off but not in Power-on reset.

This anomaly will be fixed in the next version of the IC.

14. RADIO: END to START connection using PPI or short is not functional	**Device version(s) affected**: nRF51422/nRF51822 Build code CA

Symptoms:

1. Radio SHORTS (END->START) is not functional.
2. Connecting the END event to the START event in the Radio using a PPI channel does not work.

Conditions:

Always applies.

Consequences:

Radio will not catch the START task and remain in READY state.

Workaround:

Do not use SHORTS (END->START).
Add a spacing of one or more system clock cycles between END and START triggers. This can be done by using the CPU to trigger the START task based on the END event.

This anomaly will be fixed in the next version of the IC.

15. RADIO: RSSI module analog front end do not power down when RSSIEND event occurs	**Device version(s) affected**: nRF51422/nRF51822 Build code CA

Symptoms:

Higher current consumption.

Conditions:

Always after RSSI measurement.

Consequences:

Higher current consumption.

Workaround:

Trigger RSSISTOP task to power down RSSI.

This anomaly will be fixed in the next version of the IC.

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16. RADIO: RSSISTOP task clears the RSSISAMPLE register	**Device version(s) affected**: nRF51422/nRF51822 Build code CA

Symptoms:

When RSSISTOP task is triggered, RSSISAMPLE register is cleared.

Conditions:

Always.

Consequences:

If RSSISTOP task is triggered before reading the value in RSSISAMPLE, the RSSI value will be lost and read as 0x00.

Workaround:

Read RSSISAMPLE before triggering STOP task.

This anomaly will be fixed in the next version of the IC.

17. RADIO: State Register is not functional	**Device version(s) affected**: nRF51422/nRF51822 Build code CA

Symptoms:

Reading the STATE register in the RADIO always returns 0.

Conditions:

Always.

Consequences:

It is not possible to check the current state of the radio.

Workaround:

None.

This anomaly will be fixed in the next version of the IC.

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18. RNG: Generated random value is reset when VALRDY event is cleared	**Device version(s) affected**: nRF51422/nRF51822 Build code CA

Symptoms:

A random value of 0 is read from the Random Number Generator.

Conditions:

The VALRDY (Value Ready) event, and consequently the IRQ from the module, is cleared before the generated value is read.

Consequences:

Algorithms based on random numbers will be broken.

Workaround:

Read the generated random number before the VALRDY event is cleared.

This anomaly will be fixed in the next version of the IC.

19. RNG: STOP task clears the VALUE register	**Device version(s) affected**: nRF51422/nRF51822 Build code CA

Symptoms:

When STOP task is triggered, VALUE register is cleared.

Conditions:

Always.

Consequences:

If STOP task is triggered before reading the random value in VALUE, the random value will be lost and read as 0x00.

Workaround:

Read VALUE before triggering STOP task.

This anomaly will be fixed in the next version of the IC.

20. RNG: The STOP task cannot be assigned to a PPI channel	**Device version(s) affected**: nRF51422/nRF51822 Build code CA

Symptoms:

When a PPI channel is configured to stop the Random Number Generator the task never reaches the module.

Conditions:

Always.

Consequences:

The module will continue generating the number it is working on.

Workaround:

The random number generator has to be stopped by writing to the STOP task register.

This anomaly will be fixed in the next version of the IC.

21. RTC and WDT: Reset on 32.768 kHz domains delayed when peripherals turned off and 32.768 kHz clock running	**Device version(s) affected**: nRF51422/nRF51822 Build code CA

Symptoms:

Reset of registers in the 32.768 domain will be delayed for 1 to 2 clock periods of the 32.768 kHz clock before it is asserted when the 32.768 kHz clock is running.

Conditions:

32.768 kHz clock is running.

Consequences:

This may affect timing for programs using the timers.

Workaround:

If Reset of these registers is necessary, make sure that sufficient margin is added to ensure that the registers are reset.

22. System: Issues with disable system OFF mechanism	**Device version(s) affected**: nRF51422/nRF51822 Build code CA

Symptoms:

- Recover sequence is not functional
- Unable to program device when entering system_off

Conditions:

When the program is entering system_off within 500µs after startup.

Consequences:

Unable to program device when entering system_off.

Workaround:

Unable to program device when entering system_off.

This anomaly will be fixed in the next version of the IC.

23. System: Manual setup is required to enable use of peripherals	**Device version(s) affected**: nRF51422/nRF51822Build code CA

Symptoms:

It is not possible to configure or use peripherals.

Conditions:

Always.

Consequences:

Peripherals are unusable.

Workaround:

The following instruction must be executed before any peripheral can be used:

```
*(uint32_t *)0x40000504 = 0xC007FF9F;
```

Execute it as early as possible, for example, in the SystemInit function in system_nrf51.c. This operation will allow configuration and use of all peripherals except GPIOTE.

Before GPIOTE usage, one of the following instructions must be executed before configuration or use, depending on the state of the Softdevice.
Softdevice disabled or no Softdevice in project:

```
*(uint32_t *)0x40000504 = 0xC007FFDF;
```

Softdevice enabled:

```
(void) nrf_power_perpower_set(0x00000040);
```

After GPIOTE usage, one of the following instructions must be executed depending on the state of the Softdevice.
Softdevice disabled or no Softdevice in project:

```
*(uint32_t *)0x40000504 = 0xC007FF9F;
```

Softdevice enabled:

```
(void) nrf_power_perpower_clr(0x00000040);
```

Failure to execute the last instruction after GPIOTE usage is finished will increase current consumption.

This anomaly will be fixed in the next version of the IC.

24. TEMP: Negative measured values are not represented correctly	**Device version(s) affected**: nRF51422/nRF51822 Build code CA

Symptoms:

Negative numbers are not represented correctly. Bit extension does not work properly.

Conditions:

Always.

Consequences:

When a temperature below 0 degrees is measured, bit extension only happens up to bit 9.

Workaround:

To correctly read the measured temperature perform the following operation using an inline function:

```
return ((NRF_TEMP->TEMP & MASK_SIGN) != 0) ? (NRF_TEMP->TEMP |
MASK_SIGN_EXTENSION) : (NRF_TEMP->TEMP);
```

where:

```
MASK_SIGN = (0x00000200)
MASK_SIGN_EXTENSION = (0xFFFFFC00)
```

This anomaly will be fixed in the next version of the IC.

25. TEMP: STOP task clears the TEMP register	**Device version(s) affected**: nRF51422/nRF51822 Build code CA

Symptoms:

When STOP task is triggered, TEMP register is cleared.

Conditions:

Always.

Consequences:

If STOP task is triggered before reading the measured temperature in TEMP register, the measurement will be lost. If TEMP is read afterwards, 0x00 will be read.

Workaround:

Read TEMP before triggering STOP task.

This anomaly will be fixed in the next version of the IC.

26. TEMP: TEMP module analog front end do not power down when DATARDY event occurs

Device version(s) affected:
nRF51422/nRF51822
Build code CA

Symptoms:

Higher power consumption.

Conditions:

Always.

Consequences:

Higher current consumption.

Workaround:

Trigger STOP task to power down analog front end and reduce power consumption.

This anomaly will be fixed in the next version of the IC.

27. TEMP: Temperature offset value has to be manually loaded to the TEMP module

Device version(s) affected:
nRF51422/nRF51822
Build code CA

Symptoms:

The temperature sensor gives wrong values.

Conditions:

Always.

Consequences:

Wrong temperature VALUE is read.

Workaround:

Register 0x4000C504 needs to be written to 0x00000000 before triggering the START task. If it is done, the temperature is measured correctly:

```
*(uint32_t *)0x4000C504 = 0x00000000;
```

This anomaly will be fixed in the next version of the IC.

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28. TIMER: BITMODE is not functional	**Device version(s) affected**: nRF51422/nRF51822 Build code CA
Symptoms: The counter only supports the default bit width stated in the data sheet.	
Conditions: Always.	
Consequences: Depends on application.	
Workaround: Code that uses the timers has to be written accordingly. This anomaly will be fixed in the next version of the IC.	

29. TIMER: The CC registers does not generate an event when the previous value generated an event in the same CC register	**Device version(s) affected**: nRF51422/nRF51822 Build code CA
Symptoms: A timer event is not generated when the timer reaches the value stored in the CC register.	
Conditions: When the same CC register was used to generate an event at the desired value minus one.	
Consequences: No event is generated.	
Workaround: Use another CC register to generate the event. This anomaly will be fixed in the next version of the IC.	

30. TIMER: Timer cannot handle quick START-STOP-START tasks correctly	**Device version(s) affected**: nRF51422/nRF51822Build code CA

Symptoms:

STOP task may be ignored by the system in some corner cases.

Conditions:

A STOP task is ignored if it occurs in the same timer period (set by PRESCALER) as a START task.
For example, within the same PRESCALER period START has priority, not the latest arriving task.

Consequences:

The timer may continue to run and requests resources, thereby increasing current consumption.

Workaround:

None.

This anomaly will be fixed in the next version of the IC.

31. TWI: Shortcuts described in the nRF51 Reference Manual are not functional	**Device version(s) affected**: nRF51422/nRF51822 Build code CA

Symptoms:

The following shortcuts are not implemented:

- Short-cut between BB event and SUSPEND task.
- Short-cut between BB event and STOP task.

Conditions:

Always.

Consequences:

Shortcuts have to be set up using a PPI channel.

Workaround:

See Consequences.

This anomaly will be fixed in the next version of the IC.

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32. UART: After a STOPRX task the UART will not be able to finish a transaction	**Device version(s) affected**: nRF51422/nRF51822 Build code CA

Symptoms:

When handshake is used the "QOS" cannot be guaranteed with respect to RTS going inactive as result of triggering the STOPRX task.
When the STOPRX task is triggered, the UART will set the RTS line inactive, followed by switching off the clocks to the UART's receiver. The UART specification states that the counterpart UART transmitter can send one byte after the RTS line has been deactivated. However, this last byte will be lost if the UART's receiver is stopped (STOPRX) before or during reception of the last byte.

Conditions:

This may occur when the STOPRX task is used to end a transmission while flow-control is used.

Consequences:

If conditions are met the last byte received will be lost.

Workaround:

Instead of stopping the UART using STOPRX only, firmware can first disconnect the RTS line from the GPIO using PSELRTS=0xFFFFFFFF, then use a timer to time the period to listen for the last byte, before triggering the STOPRX task. The time required to listen for the last byte depends on the link-speed and the protocol used.

This anomaly will be fixed in the next version of the IC.

33. WDT: The watchdog config option "RUN while paused by the debugger" does not work	**Device version(s) affected**: nRF51422/nRF51822 Build code CA

Symptoms:

The debugger and microcontroller do not communicate. The microcontroller does not run any code.

Conditions:

The watchdog is configured to "run while halted by the debugger", and the watchdog timer expires with the debugger connected.

Consequences:

The debugger and microcontroller do not communicate. The microcontroller does not run any code.

Workaround:

Do not configure the watchdog timer to run while paused by the debugger.

This anomaly will be fixed in the next version of the IC.