Section 4. Program Memory

HIGHLIGHTS

This section of the manual contains the following topics:

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4.1 PROGRAM MEMORY ADDRESS MAP

The PIC24F devices can have up to 4M x 24-bit program memory address space, as shown in Figure 4-2. There are three methods for accessing program space.

1. Via the 23-bit PC.
2. Via table read (TBLRD) and table write (TBLWT) instructions.
3. By mapping any 32-Kbyte segment of program memory into the data memory address space.
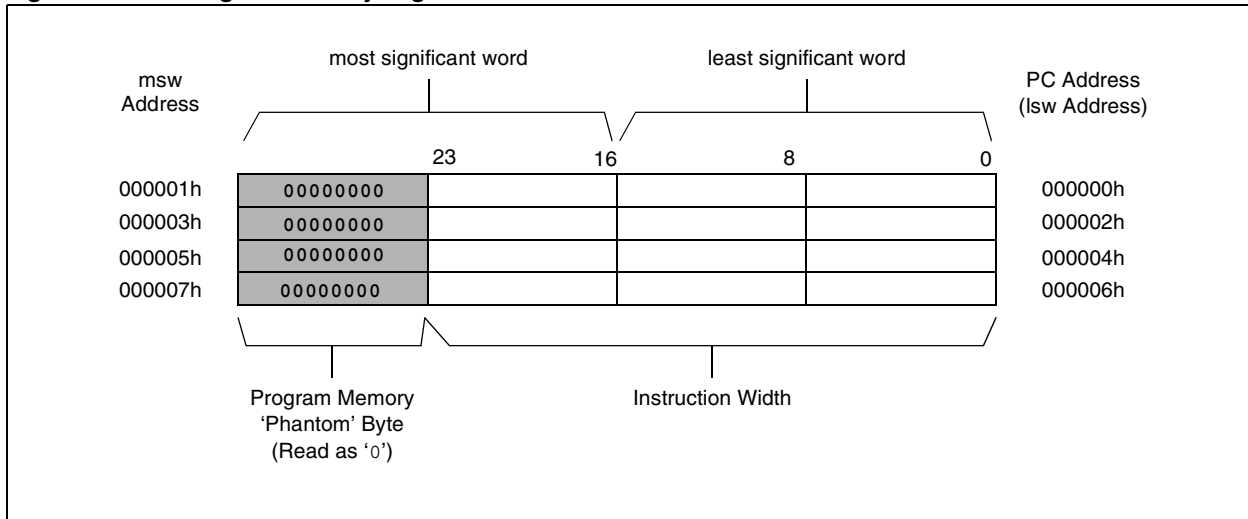
The program memory map is divided into the user program space and the configuration space. The user program space (000000h to 7FFFFFh) contains the Reset vector, interrupt vector tables and program memory. Device Configuration registers and Device ID sections are mapped in configuration space. Configuration bits and Device IDs can be read from these locations; however, the Configuration bits can be set or cleared by programming the desired values in the Flash Configuration Words. The top two words of the on-chip program memory are reserved for configuration information. On device Reset, the configuration information is copied into the appropriate Configuration registers. For more information on Configuration bits, see **Section 32. "Device Configuration"**.

4.1.1 Program Memory Organization

The program memory space is organized as word addressable blocks. Although it is treated as 24 bits wide, it is more appropriate to think of each address of the program memory as a lower and upper word, with the upper byte of the upper word being unimplemented. The lower word always has an even address, while the upper word has an odd address (Figure 4-1).

Program memory addresses are always word-aligned on the lower word, and addresses are incremented or decremented by two during code execution.

Figure 4-1: Program Memory Organization

Figure 4-2: Example Program Space Memory Map[(1)]

	Reset – GOTO Instruction	000000
	Reset – GOTO Address	000002
	Reserved	000004
	Oscillator Fail Trap Vector	
	Address Error Trap Vector	
	Stack Error Trap Vector	
	Math Error Trap Vector	
	Reserved	
	Reserved	
	Reserved	
	Interrupt Vector 0	000014
	Interrupt Vector 1	
	~	
	~	
	Interrupt Vector 52	
	Interrupt Vector 53	00007E
	Interrupt Vector 54	000080
	~	
	~	
	Interrupt Vector 116	0000FC
	Interrupt Vector 117	0000FE
	Reserved	000100
	Reserved	
	Reserved	
	Oscillator Fail Trap Vector	
	Address Error Trap Vector	
	Stack Error Trap Vector	
	Math Error Trap Vector	
	Reserved	
	Reserved	
	Reserved	
	Interrupt Vector 0	000114
	Interrupt Vector 1	
	~	
	~	
	Interrupt Vector 52	00017C
	Interrupt Vector 53	00017E
	Interrupt Vector 54	000180
	~	
	~	
	Interrupt Vector 116	0001FE
	Interrupt Vector 117	000200
	User Flash Program Memory (48K Instructions)[(2)]	017FFE[(2)]
	Unimplemented (Read as '0's)	018000 / 7FFFFE
	Reserved	800000 / F7FFFE
	Data Configuration Registers	F80000 / F8000E
	Reserved	F80010 / FEFFFE
	DEVID (2)	FF0000 / FFFFFE

Interrupt Vector Table (000004 – 0000FC)

Alternate Interrupt Vector Table (000100 – 000180)

User Memory Space (000000 – 7FFFFE)

Configuration Memory Space (800000 – FFFFFE)

Note 1: Memory areas are not shown to scale.
2: The address boundaries for user Flash program memory and Flash Configuration Words will depend on the PIC24F device variant that is selected. Refer to the appropriate device data sheet for further details.

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4.2 PROGRAM COUNTER

The PC increments by 2 with the LSb set to '0' to provide compatibility with data space addressing. Sequential instruction words are addressed in the 4M program memory space by PC<22:1>. Each instruction word is 24 bits wide.

The LSb of the program memory address (PC<0>) is reserved as a byte select bit for program memory accesses from data space that use Program Space Visibility (PSV) or table instructions. For instruction fetches via the PC, the byte select bit is not required. Therefore, PC<0> is always set to '0'.

An instruction fetch example is shown in Figure 4-3. Note that incrementing PC<22:1> by one is equivalent to adding 2 to PC<22:0>.

Figure 4-3: Instruction Fetch Example

Note 1: Increment of PC<22:1> is equivalent to PC<22:0> + 2.
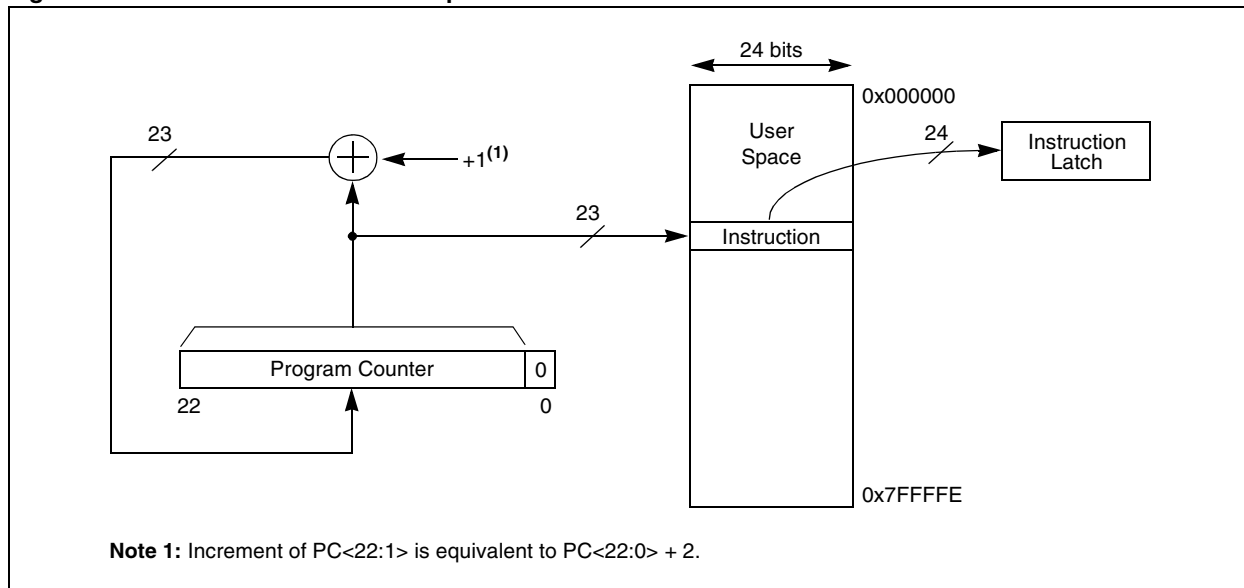
4.3 DATA ACCESS FROM PROGRAM MEMORY

There are two methods by which data can be transferred between the program memory and data memory spaces: via special table instructions or through remapping of a 32-Kbyte program space page into the upper half of data space. The TBLRDL and TBLWTL instructions offer a direct method of reading or writing the least significant word (lsw) of any address within program space without going through the data space, which is preferable for some applications. The TBLRDH and TBLWTH instructions are the only method whereby the upper 8 bits of a program word can be accessed as data.

4.3.1 Table Instruction Summary

A set of table instructions is provided to move byte or word-sized data between program space and data space. The table read instructions are used to read from the program memory space into data memory space. The table write instructions allow data memory to be written into the program memory space.

> **Note:** Detailed code examples using table instructions can be found in **Section 5. "Flash Memory Operation"**.

The four available table instructions are listed below:

- TBLRDL: Table Read Low
- TBLWTL: Table Write Low
- TBLRDH: Table Read High
- TBLWTH: Table Write High

For table instructions, program memory can be regarded as two, 16-bit word-wide address spaces, residing side by side, each with the same address range as shown in Figure 4-4.

TBLRDL and TBLWTL access the lsw of the program memory, and TBLRDH and TBLWTH access the upper word. As program memory is only 24 bits wide, the upper byte from this latter space does not exist, though it is addressable. It is, therefore, termed the 'phantom' byte.

Figure 4-4:   High and Low Address Regions for Table Operations
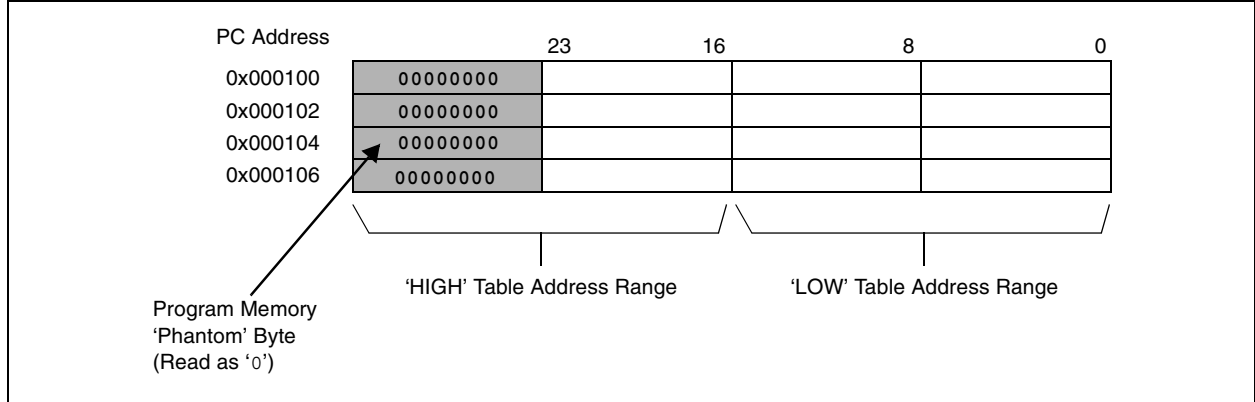
4.3.2   Table Address Generation

For all table instructions, a W register address value is concatenated with the 8-bit Table Page Address Pointer, TBLPAG, to form a 23-bit effective program space address, plus a byte select bit, as shown in Figure 4-5. As there are 15 bits of program space address, provided from the W register, the data table page in program memory is, therefore, 32K words.

Figure 4-5:   Address Generation for Table Operations

4
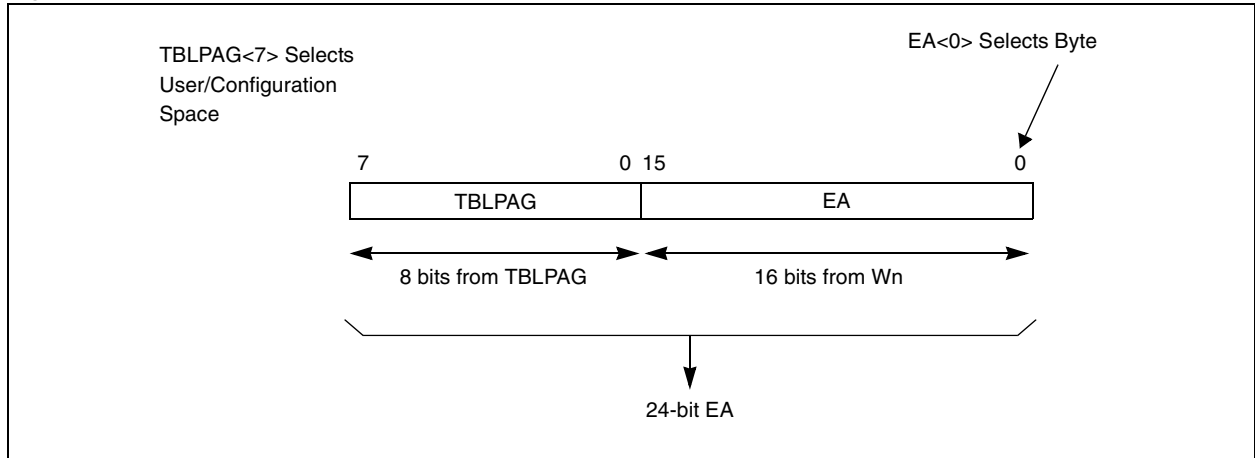
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4.3.3   Program Memory Low Word Access

The TBLRDL and TBLWTL instructions are used to access the lower 16 bits of program memory data. The LSb of the W register address is ignored for word-wide table accesses. For byte-wide accesses, the LSb of the W register address determines which byte is read. Figure 4-6 demonstrates the program memory data regions accessed by the TBLRDL and TBLWTL instructions.

Figure 4-6:   Program Data Table Access (lsw)
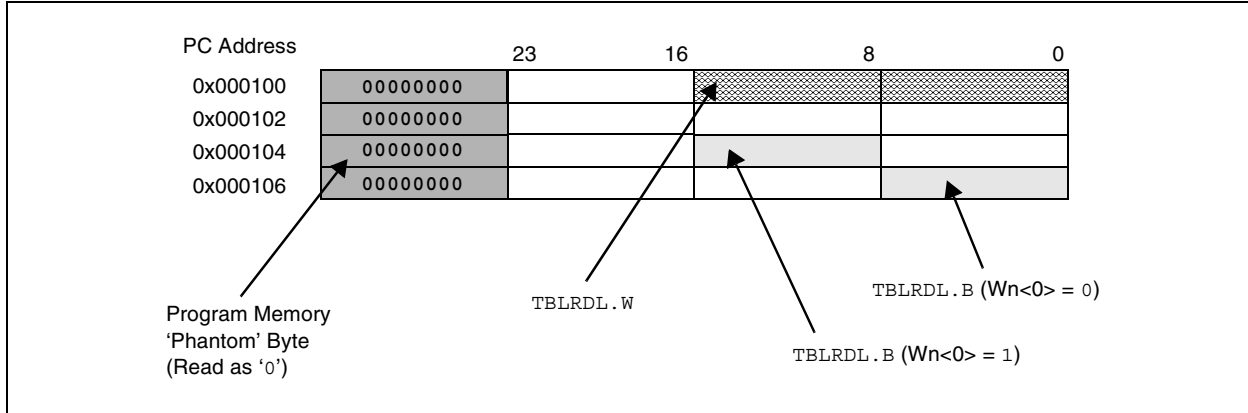
4.3.4   Program Memory High Word Access

The TBLRDH and TBLWTH instructions are used to access the upper 8 bits of the program memory data. These instructions also support Word or Byte Access modes for orthogonality, but the high byte of the program memory data will always return '0', as shown in Figure 4-7.

Figure 4-7:   Program Data Table Access (MSB)
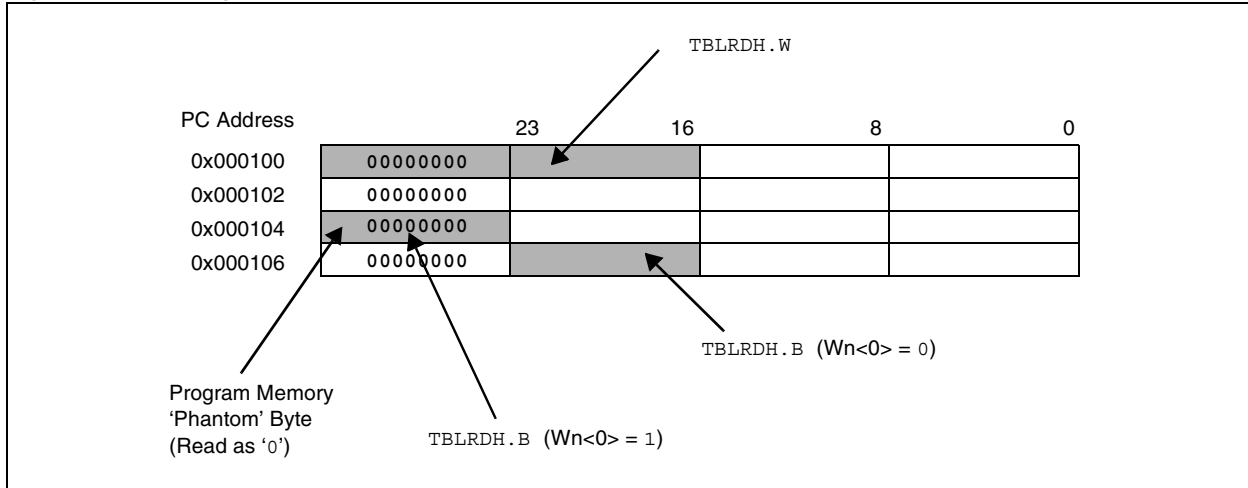
4.3.5   Data Storage in Program Memory

It is assumed that for most applications, the high byte (P<23:16>) will not be used for data, making the program memory appear 16 bits wide for data storage. It is recommended that the upper byte of program data be programmed either as a NOP (0x00 or 0xFF), or as an illegal opcode (0x3F) value, to protect the device from accidental execution of stored data. The TBLRDH and TBLWTH instructions are primarily provided for array program/verification purposes and for those applications that require compressed data storage.

4.4   PROGRAM SPACE VISIBILITY FROM DATA SPACE

The upper 32 Kbytes of the PIC24F data memory address space may optionally be mapped into any 16K word program space page. This mode of operation is called Program Space Visibility (PSV) and provides transparent access of stored constant data from data space without the need to use special instructions (i.e., TBLRD, TBLWT).

4.4.1   PSV Configuration

Program Space Visibility is enabled by setting the PSV bit (CORCON<2>). A description of the CORCON register can be found in **Section 2. "CPU"**.

When PSV is enabled, each data space address in the upper half of the data memory map (data memory with higher addresses) will map directly into a program address (see Figure 4-8). The PSV window allows access to the lower 16 bits of the 24-bit program word. The upper 8 bits of the program memory data should be programmed to force an illegal instruction, or a NOP, to maintain machine robustness. Note that table instructions provide the only method of reading the upper 8 bits of each program memory word.

Figure 4-9 shows how the PSV address is generated. The 15 LSbs of the PSV address are provided by the W register that contains the effective address. The MSb of the W register is not used to form the address. Instead, the MSb specifies whether to perform a PSV access from program space or a normal access from data memory space. If a W register effective address of 0x8000 or greater is used, the data access will occur from program memory space when PSV is enabled. All accesses will occur from data memory when the W register effective address is less than 0x8000.

The remaining address bits are provided by the PSVPAG register (PSVPAG<7:0>), as shown in Figure 4-9. The PSVPAG bits are concatenated with the 15 LSbs of the W register, holding the effective address to form a 23-bit program memory address. PSV can only be used to access values in program memory space. Table instructions must be used to access values in the user configuration space.

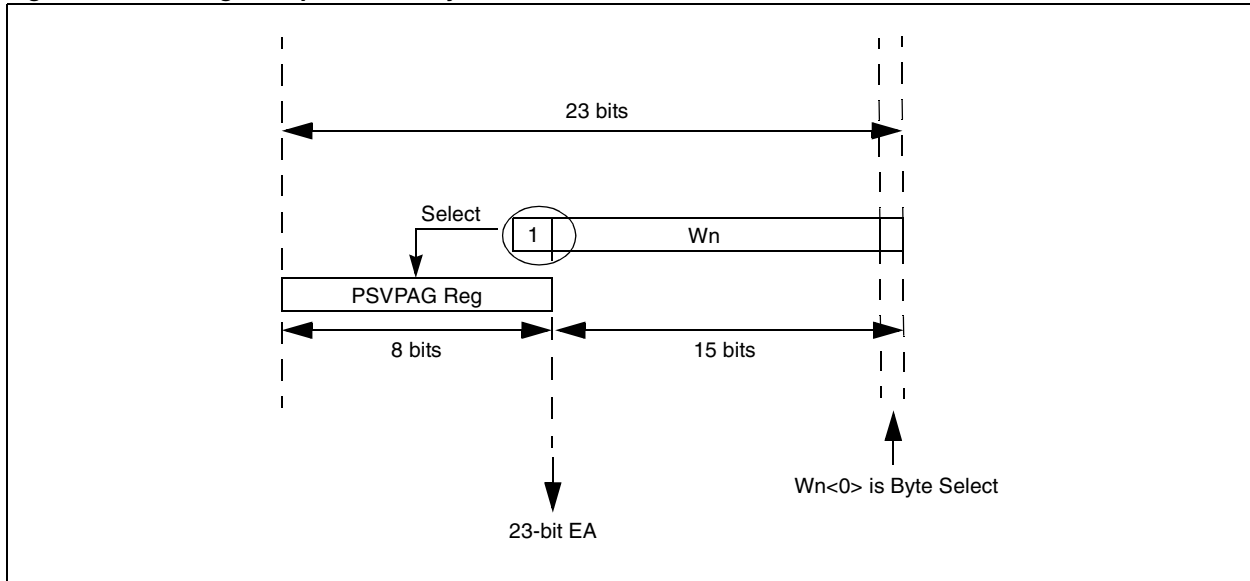The LSb of the W register value is used as a byte select bit, which allows instructions using PSV to operate in Byte or Word mode.

Figure 4-8: **Program Space Visibility Operation**
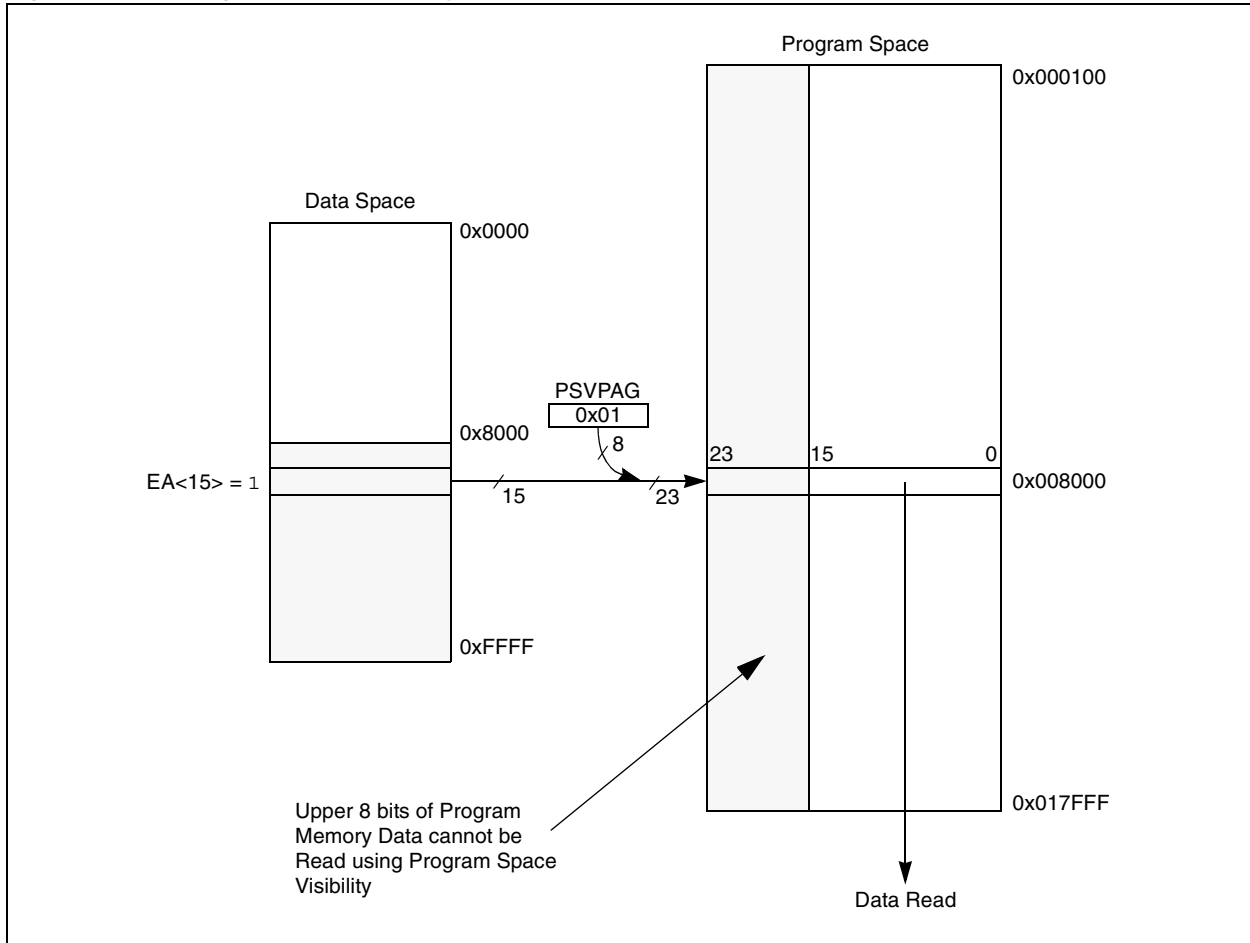
Figure 4-9: **Program Space Visibility Address Generation**

4.4.2   PSV Timing

Instructions that use PSV will require two extra instruction cycles to complete execution, except all MOV instructions (including the MOV.D instruction) that require only one extra cycle to complete execution.

The additional instruction cycles are used to fetch the PSV data on the program memory bus.

4.4.2.1   USING PSV IN A REPEAT LOOP

Instructions that use PSV within a REPEAT loop eliminate the extra instruction cycle(s) required for the data access from program memory, hence incurring no overhead in execution time. However, the following iterations of the REPEAT loop will incur an overhead of two instruction cycles to complete execution:

- The first iteration.
- The last iteration.
- Instruction execution prior to exiting the loop due to an interrupt.
- Instruction execution upon re-entering the loop after an interrupt is serviced.

4.4.2.2   PSV AND INSTRUCTION STALLS

Refer to **Section 2. "CPU"** for more information about instruction stalls using PSV.

4.5   PROGRAM MEMORY WRITES

This section describes the programming technique for Flash program memory. The PIC24F devices have an internal programmable Flash memory for execution of user code. There are two methods to program this memory:

- Run-Time Self-Programming (RTSP)
- In-Circuit Serial Programming™ (ICSP™)
- Enhanced In-Circuit Serial Programming (EICSP)
- JTAG Programming

RTSP is performed by the user's software. ICSP and EICSP are performed using a serial data connection to the device and allow much faster programming time than RTSP. RTSP techniques are described in this section.

The ICSP and EICSP protocols are defined in the *"PIC24FJXXXGA0XX Flash Programming Specification"* (DS39768), which can to be downloaded from the Microchip web site (www.microchip.com). The JTAG programming is defined in the programming section of the IEEE 1149.1-2001, *"IEEE Standard Test Access Port and Boundary Scan Architecture"*.

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4.6   TABLE INSTRUCTION OPERATION

The table instructions provide one method of transferring data between the program memory space and the data memory space of the PIC24F devices. A summary of the table instructions used during programming of the Flash program memory is provided in this section. There are four basic table instructions:

- TBLRDL: Table Read Low
- TBLRDH: Table Read High
- TBLWTL: Table Write Low
- TBLWTH: Table Write High

The TBLRDL and the TBLWTL instructions are used to read and write to bits<15:0> of program memory space. TBLRDL and TBLWTL can access program memory in Word or Byte mode.

The TBLRDH and TBLWTH instructions are used to read or write to bits<23:16> of program memory space. TBLRDH and TBLWTH can access program memory in Word or Byte mode. Since the program memory is only 24 bits wide, the TBLRDH and TBLWTH instructions have the ability to address an upper byte of program memory that does not exist. This byte is called the 'phantom byte'. Any read of the phantom byte will return 0x00 and a write to the phantom byte has no effect.

The 24-bit program memory can be regarded as two, side-by-side 16-bit spaces, with each space sharing the same address range. Therefore, the TBLRDL and TBLWTL instructions access the 'low' program memory space (PM<15:0>). The TBLRDH and TBLWTH instructions access the 'high' program memory space (PM<31:16>). Any reads or writes to PM<31:24> will access the phantom (unimplemented) byte. When any of the table instructions are used in Byte mode, the LSb of the table address will be used as the byte select bit. The LSb determines which byte in the high or low program memory space is accessed.

Figure 4-10 shows how the program memory is addressed using the table instructions. A 24-bit program memory address is formed using the TBLPAG<7:0> bits and the Effective Address (EA) from a W register, specified in the table instruction. The 24-bit program counter is shown in Figure 4-10 for reference. The upper 23 bits of the EA are used to select the program memory location. For the Byte mode table instructions, the LSb of the W register EA is used to pick which byte of the 16-bit program memory word is addressed. A '1' selects bits<15:8>, a '0' selects bits<7:0>. The LSb of the W register EA is ignored for a table instruction in Word mode.

In addition to the program memory address, the table instructions also specify a W register (or a W Pointer to a memory location) that is the source of the program memory data to be written, or the destination for a program memory read. For a table write operation in Byte mode, bits<15:8> of the working source register are ignored.

Figure 4-10:   Addressing for Table Registers
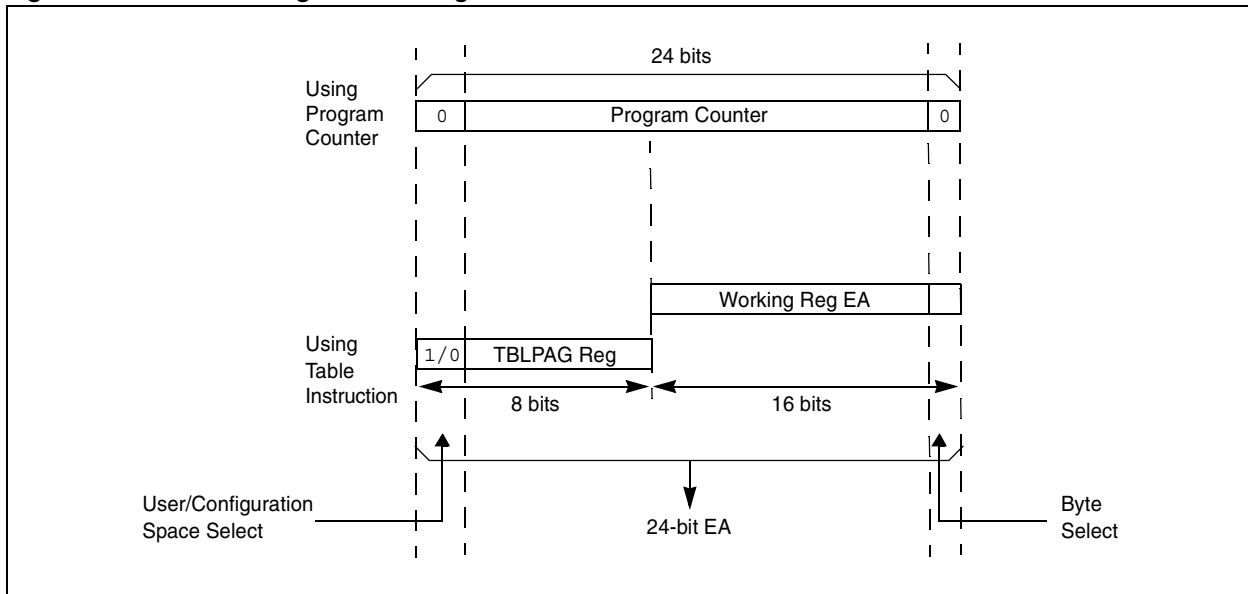
4.6.1 Using Table Read Instructions

Table reads require two steps. First, an Address Pointer is set up using the TBLPAG register and one of the W registers. Then, the program memory contents at the address location may be read.

4.6.1.1 READING PROGRAM MEMORY USING TABLE INSTRUCTIONS

The following code examples show how to read a word of program memory using the table instructions in Word/Byte mode:

Example 4-1: Read Word Mode

```
; Setup the address pointer to program space
    MOV         #tblpage(PROG_ADDR),W0   ; get table page value
    MOV         W0,TBLPAG                 ; load TBLPAG register
    MOV         #tbloffset(PROG_ADDR),W0  ; load address LS word
; Read the program memory location
    TBLRDH      [W0],W3                   ; Read high byte to W3
    TBLRDL      [W0],W4                   ; Read low word to W4

Equivalent C Code
int addrOffset;
int VarWord;
int VarWord1;

{
:
:
    TBLPAG = ((PROG_ADDR & 0x7F0000)>>16);
    addrOffset = (PROG_ADDR & 0x00FFFF);
    asm("tblrdh.w [%1], %0" : "=r"(VarWord1)    : "r"(addrOffset));
    asm("tblrdl.w [%1], %0" : "=r"(VarWord)     : "r"(addrOffset));

:
:
:
}
```

   Note: Save all the working registers prior to using them.

Example 4-2: Read Byte Mode

```
; Setup the address pointer to program space
    MOV         #tblpage(PROG_ADDR),W0   ; get table page value
    MOV         W0,TBLPAG                 ; load TBLPAG register
    MOV         #tbloffset(PROG_ADDR),W0  ; load address LS word
; Read the program memory location
    TBLRDH.B    [W0],W3                   ; Read high byte to W3
    TBLRDL.B    [W0++],W4                 ; Read low byte to W4
    TBLRDL.B    [W0++],W5                 ; Read middle byte to W5

Equivalent C Code
int  addrOffset;
char VarByte1;
char VarByte2;
char VarByte3;

{
:
:
TBLPAG = ((PROG_ADDR & 0x7F0000)>>16);
addr = (PROG_ADDR & 0x00FFFF);

asm("tblrdl.b [%1], %0" : "=r"(LocalVarByte1) : "r"(addrOffset))    ; // Read low byte
asm("tblrdl.b [%1], %0" : "=r"(LocalVarByte2) : "r"(addrOffset +1)) ;//Read middle byte
asm("tblrdh.b [%1], %0" : "=r"(LocalVarByte3) : "r"(addrOffset))    ; // Read high byte
:
:
}
```

   Note: Save all the working registers prior to using them.

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In Example 4-1 and Example 4-2, the post-increment operator on the read of the low byte causes the address in the working register to increment by one. This sets EA<0> to '1' for access to the middle byte in the third write instruction. The last post-increment sets W0 back to an even address, pointing to the next program memory location.

> **Note:** The `tblpage()` and `tbloffset()` directives are provided by the Microchip assembler for the PIC24F. These directives select the appropriate TBLPAG and W register values for the table instruction from a program memory address value. Refer to *"MPLAB® ASM 30, MPLAB® LINK30 and Utilities User's Guide"* (DS51317) for further details.

4.6.2   Using Table Write Instructions

4.6.2.1   TABLE WRITE HOLDING LATCHES

Table write instructions do not write directly to the nonvolatile program. Instead, the table write instructions load holding latches that store the write data. The holding latches are not memory mapped and can only be accessed using table write instructions. When all of the holding latches have been loaded, the actual memory programming operation is started by executing a special sequence of instructions.

Please refer to the specific device data sheet for further details.

4.6.2.2   WRITING A SINGLE PROGRAM MEMORY LATCH IN WORD/BYTE MODE

The following sequence can be used to write a single program memory latch location in Word mode:

Example 4-3:   Write Word Mode

```
; Setup the address pointer to program space
    MOV     #tblpage(PROG_ADDR),W0    ; get table page value
    MOV     W0,TBLPAG                 ; load TBLPAG register
    MOV     #tbloffset(PROG_ADDR),W0  ; load address LS word
; Load write data into W registers
    MOV     #PROG_LOW_WORD,W2
    MOV     #PROG_HI_BYTE,W3
; Perform the table writes to load the latch
    TBLWTL  W2,[W0]
    TBLWTH  W3,[W0++]
```

Equivalent C Code
```
int VarWord1 = 0xXXXX;
int VarWord2 = 0xXXXX;
int addrOffset;
{
:
:

TBLPAG =  ((PROG_ADDR & 0x7F0000)>>16);
addrOffset = (PROG_ADDR & 0x00FFFF);
asm("tblwtl %1, [%0]" : "=r"(addrOffset) : "d"(VarWord))    ;
asm("tblwth %1, [%0]" : "=r"(addrOffset) : "d"(VarWord1))   ;
:
:
}
```

> **Note:**   Save all the working registers prior to using them.

In this example, the contents of the upper byte of W3 does not matter because this data will be written to the phantom byte location. W0 is post-incremented by 2, after the second TBLWTH instruction, to prepare for the write to the next program memory location.

To write a single program memory latch location in Byte mode, the following code sequence can be used:

Example 4-4:   Write Byte Mode

```
; Setup the address pointer to program space
    MOV         #tblpage(PROG_ADDR),W0    ; get table page value
    MOV         W0,TBLPAG                 ; load TBLPAG register
    MOV         #tbloffset(PROG_ADDR),W0  ; load address LS word
; Load data into working registers
    MOV         #LOW_BYTE,W2
    MOV         #MID_BYTE,W3
    MOV         #HIGH_BYTE,W4
; Write data to the latch
    TBLWTH.B    W4,[W0]                   ; write high byte
    TBLWTL.B    W2,[W0++]                 ; write low byte
    TBLWTL.B    W3,[W0++]                 ; write middle byte
```

Equivalent C Code
```
char VarByte1 = 0xXX;
char VarByte2 = 0xXX;
char VarByte3 = 0xXX;

{
:
:

TBLPAG =  ((PROG_ADDR & 0x7F0000)>>16);
addr = (PROG_ADDR & 0x00FFFF);
asm("tblwtl.b %1, [%0]" : "=r"(addr) : "d"(VarByte1)) ;//Low Byte
asm("tblwth.b %1, [%0]" : "=r"(addr) : "d"(VarByte3)) ;//Upper Byte
addr++;
asm("tblwtl.b %1, [%0]" : "=r"(addr) : "d"(VarByte2)) ;//Middle Byte
:
}
```

   Note: Save all the working registers prior to using them.

In the code example above, the post-increment operator on the write to the low byte causes the address in W0 to increment by one. This sets EA<0> = 1 for access to the middle byte in the third write instruction. The last post-increment sets W0 back to an even address, pointing to the next program memory location.

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4.6.3 Run-Time Self-Programming (RTSP)

RTSP allows the user code to modify Flash program memory contents. RTSP is accomplished using `TBLRD` (table read) and `TBLWT` (table write) instructions, and the NVM Control registers. With RTSP, the user can erase program memory, 8 rows (64x8 = 512 instructions) at a time, and can write program memory data, single rows (64 instructions) at a time

4.6.3.1 RTSP OPERATION

The PIC24F Flash program memory array is organized into rows of 64 instructions or 192 bytes. RTSP allows the user to erase blocks of eight rows (512 instructions) at a time, and to program 64 instructions at a time. The 8-row erase blocks and single row write blocks are edge-aligned, from the beginning of program memory, on boundaries of 1536 bytes and 192 bytes, respectively.

The program memory implements holding buffers that can contain 64 instructions of programming data. Prior to the actual programming operation, the write data must be loaded into the buffers in sequential order. The instruction words loaded must always be from a group of 64 boundaries.

The basic sequence for RTSP programming is to set up a Table Pointer, then do a series of `TBLWT` instructions to load the buffers. Programming is performed by setting the control bits in the NVMCON register. A total of 64 `TBLWTL` and `TBLWTH` instructions are required to load the instructions.

All of the table write operations are single-word writes (2 instruction cycles), because only the buffers are written. A programming cycle is required for programming each row.

> **Note:** The number of rows, blocks and holding latches may vary from device to device; please refer to the specific device data sheet for actual numbers.

4.6.4 Control Registers

There are two SFRs used to read and write the program Flash memory: NVMCON and NVMKEY. The NVMCON register (Register 4-1) controls which blocks are to be erased, which memory type is to be programmed and the start of the programming cycle.

NVMKEY is a write-only register that is used for write protection. To start a program or erase sequence, the user must consecutively write 55h and AAh to the NVMKEY register.

4.6.4.1 NVMCON REGISTER

The NVMCON register is the primary control register for Flash and EEPROM program/erase operations. This register selects whether an erase or program operation will be performed, and is used to start the program or erase cycle.

The NVMCON register is shown in Register 4-1. The lower byte of NVMCOM configures the type of NVM operation that will be performed.

Register 4-1:   **NVMCOM: Nonvolatile Flash Memory Control Register**

R/SO-0[(1)]	R/W-0[(1)]	R/W-0[(1)]	U-0	U-0	U-0	U-0	U-0
WR	WREN	WRERR	—	—	—	—	—
bit 15							bit 8

U-0	R/W-0[(1)]	U-0	U-0	R/W-0[(1)]	R/W-0[(1)]	R/W-0[(1)]	R/W-0[(1)]
—	ERASE	—	—	NVMOP3[(2)]	NVMOP2[(2)]	NVMOP1[(2)]	NVMOP0[(2)]
bit 7							bit 0

Legend:		SO = Settable-Only bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at Reset	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15   **WR:** Write Control bit[(1)]

         1 = Initiates a Flash memory program or erase operation. The operation is self-timed and the bit is cleared by hardware once the operation is complete.
         0 = Program or erase operation is complete and inactive

bit 14   **WREN:** Write Enable bit[(1)]

         1 = Enable Flash program/erase operations
         0 = Inhibit Flash program/erase operations

bit 13   **WRERR:** Write Sequence Error Flag bit[(1)]

         1 = An improper program or erase sequence attempt or termination has occurred (bit is set automatically on any set attempt of the WR bit)
         0 = The program or erase operation completed normally

bit 12-7   **Unimplemented:** Read as '0'

bit 6   **ERASE:** Erase/Program Enable bit[(1)]

         1 = Perform the erase operation specified by NVMOP3:NVMOP0 on the next WR command
         0 = Perform the program operation specified by NVMOP3:NVMOP0 on the next WR command

bit 5-4   **Unimplemented:** Read as '0'

bit 3-0   **NVMOP3:NVMOP0:** NVM Operation Select bits[(2)]

         1111 = Memory bulk erase operation (ERASE = 1) or no operation (ERASE = 0)[(3)]
         0011 = Memory word program operation (ERASE = 0) or no operation (ERASE = 1)
         0010 = Memory page erase operation (ERASE = 1) or no operation (ERASE = 0)
         0001 = Memory row program operation (ERASE = 0) or no operation (ERASE = 1)

Note 1:   These bits can only be reset on POR.
       2:   All other combinations of NVMOP3:NVMOP0 are unimplemented.
       3:   This operation is available in ICSP™ mode only.

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4.6.4.2   NVMKEY REGISTER

NVMKEY is a write-only register that is used to prevent accidental writes/erasures of Flash memory. To start a program or erase sequence, the following steps must be taken in the exact order shown:

1. Write 0x55 to NVMKEY.
2. Write 0xAA to NVMKEY.
3. Execute two NOP instructions.

After this sequence, a write will be allowed to the NVMCON register for one instruction cycle. In most cases, the user will simply need to set the WR bit in the NVMCON register to start the program or erase cycle. Interrupts should be disabled during the unlock sequence. The code example below shows how the unlock sequence is performed:

Example 4-5:   Performing the Unlock Sequence

```
;   PUSH    SR              ; Disable interrupts, if enabled
    MOV     #0x00E0,W0
    IOR     SR

    MOV     #0x55,W0
    MOV     #0xAA,W0
    MOV     W0,NVMKEY
    MOV     W0,NVMKEY       ; NOP not required
    BSET    NVMCON,#WR      ; Start the program/erase cycle
    NOP
    NOP
    POP     SR              ; Re-enable interrupts
```

Equivalent C Code
```
    NVMKEY = 0x55;
    NVMKEY = 0xAA;
    NVMCONbits.WR=1;
    Nop();
    Nop();
```

   Note: Save all the working registers prior to using them.

Refer to **Section 4.7 "Flash Programming Operations"** for further programming examples.

4.7 FLASH PROGRAMMING OPERATIONS

A complete programming sequence is necessary for programming or erasing the internal Flash in RTSP mode. A programming operation is nominally 4 ms[1] in duration and the processor stalls (waits) until the operation is finished. Setting the WR bit (NVMCON<15>) starts the operation and the WR bit is automatically cleared when the operation is finished.

> **Note 1:** Programming time may vary from device to device; please refer to the specific device data sheet for the exact value.

Flash programming operations are controlled using the following Nonvolatile Memory (NVM) control register:

- NVMCON
- NVMKEY

4.7.1 Flash Program Memory Programming Algorithm

The user can program one row of program Flash memory at a time. To do this, it is necessary to erase the 8-row erase block containing the desired row. The general process is:

1. Read eight rows of program memory (512 instructions) and store in data RAM.
2. Update the program data in RAM with the desired new data.
3. Erase the block:
   a) Set the NVMOP bits (NVMCOM<3:0>) to '0010' to configure for block erase. Set the ERASE (NVMCOM<6>) and WREN (NVMCOM<14>) bits.
   b) Write the starting address of the block to be erased into the TBLPAG and W registers.
   c) Write 55h to NVMKEY.
   d) Write AAh to NVMKEY.
   e) Set the WR bit (NVMCOM<15>). The erase cycle begins and the CPU stalls for the duration of the erase cycle. When the erase is done, the WR bit is cleared automatically.
4. Write the first 64 instructions from data RAM into the program memory buffers (see **Section 4.5 "Program Memory Writes"**).
5. Write the program block to Flash memory:
   a) Set the NVMOP bits to '0001' to configure for row programming. Clear the ERASE bit and set the WREN bit.
   b) Write 55h to NVMKEY.
   c) Write AAh to NVMKEY.
   d) Set the WR bit. The programming cycle begins and the CPU stalls for the duration of the write cycle. When the write to Flash memory is done, the WR bit is cleared automatically.
6. Repeat steps 4 and 5, using the next available 64 instructions from the block in data RAM by incrementing the value in TBLPAG, until all 512 instructions are written back to Flash memory.

For protection against accidental operations, the write initiate sequence for NVMKEY must be used to allow any erase or program operation to proceed. After the programming command has been executed, the user must wait for the programming time until programming is complete. The two instructions following the start of the programming sequence should be NOPs, as shown in **Section 4.6.4.2 "NVMKEY Register"**.

> **Note 1:** Please refer to the specific device data sheet for the complete reference code of Flash memory programming.
>
> **2:** The number of rows, blocks and holding latches may vary from device to device; please refer to the specific device data sheet for actual numbers.

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Program Memory

4.8   REGISTER MAPS

A summary of the Special Function Registers associated with the PIC24F program memory is provided in Table 4-1.

Table 4-1:   Special Function Registers Associated with the Program Memory[1]

File Name	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets[2]
TBLPAG	—	—	—	—	—	—	—	—			Table Page Address Pointer				—	—	0000
NVMCON	WR	WREN	WRERR	—	—	—	—	—	—	ERASE	—	—	NVMOP3	NVMOP2	NVMOP1	NVMOP0	0000
NVMKEY	—	—	—	—	—	—	—	—				NVMKEY<7:0>					0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1:   Please Refer to the device data sheet for specific memory map details.

    2:   Reset value shown is for POR only. Value on other Reset states is dependent on the state of memory write or erase operations at the time of Reset.

Advance Information

4.9   RELATED APPLICATION NOTES

This section lists application notes that are related to this section of the manual. These application notes may not be written specifically for the PIC24F device family, but the concepts are pertinent and could be used with modification and possible limitations. The current application notes related to the program memory are:

Title   **Application Note #**

No related application notes at this time.

> **Note:**   Please visit the Microchip web site (www.microchip.com) for additional application notes and code examples for the PIC24F family of devices.

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Program Memory

4.10   REVISION HISTORY

Revision A (January 2007)

This is the initial released revision of this document.

Advance Information