nRF51422

ANT™ System on Chip

Preliminary Product Specification 0.7.1

Key Features

- Preprogrammed S210 SoftDevice featuring ANT™ Protocol
- 2.4 GHz transceiver
    - -90 dBm sensitivity ANT mode
    - TX Power -20 to +4 dBm in 4 dB steps
    - TX Power -30 dBm Whisper mode
    - 13 mA peak RX, 10.5 mA peak TX (0 dBm)
    - RSSI (1 dBm resolution)
- ARM® Cortex™-M0 32 bit processor
    - 275 µA/MHz running from flash memory
    - 150 µA/MHz running from RAM
    - Serial Wire Debug (SWD)
- Memory
    - 256 KB embedded flash program memory
    - 16 KB RAM
- Support for non-concurrent multi-protocol operation
    - On-air compatibility with nRF24L series
- Flexible Power Management
    - Supply voltage range 1.8 V to 3.6 V
    - 2.5 µs fast wake-up using 16 MHz RCOSC
    - 420 nA @ 3 V OFF mode
    - 530 nA @ 3 V in OFF mode + 1 region RAM retention
    - 2.3 µA @ 3 V ON mode, all blocks IDLE
- 8/9/10 bit ADC - 8 configurable channels
- 24/32 General Purpose I/O Pins
- Two 16 bit and one 24 bit timers with counter mode
- SPI Master
- Two-wire Master (I2C compatible)
- UART (CTS/RTS)
- CPU independent Programmable Peripheral Interconnect (PPI)
- Quadrature Decoder (QDEC)
- AES HW encryption
- Real Timer Counter (RTC)
- 6x6 mm QFN package

Applications

- Personal Area Networks
    - Health and Fitness sensor and monitor devices
    - Medical devices
    - Key-fobs + wrist watch
- Home/industrial automation
- Environmental sensor networks
- Active RFID
- Logistics/goods tracking
- Audience-response systems

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Datasheet Status

Status	Description
Objective Product Specification (OPS)	This product specification contains target specifications for product development.
Preliminary Product Specification (PPS)	This product specification contains preliminary data; supplementary data may be published from Nordic Semiconductor ASA later.
Product Specification (PS)	This product specification contains final product specifications. Nordic Semiconductor ASA reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

Revision History

Date	Version	Description
September 2012	0.7.1	Updated reference design in ***chapter 11 on page 48***
September 2012	0.7	First release of Preliminary Product Specification (PPS)

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1 Introduction

nRF51422 is an ultra-low power 2.4 GHz wireless System-on-Chip (SoC) integrating the nRF51 series 2.4 GHz transceiver, a 32 bit ARM® Cortex™-M0 CPU, flash memory, and analog and digital peripherals.

nRF51422 comes with a preprogrammed 8 channel ANT core stack. The ANT software stack is completed by ANT+ device profiles and examples in the nRF514 SDK.

For further information, we encourage customers to read the S210 SoftDevice Specification that can be downloaded from www.nordicsemi.com.

1.1 Required reading

The nRF51 Reference Manual is required reading.

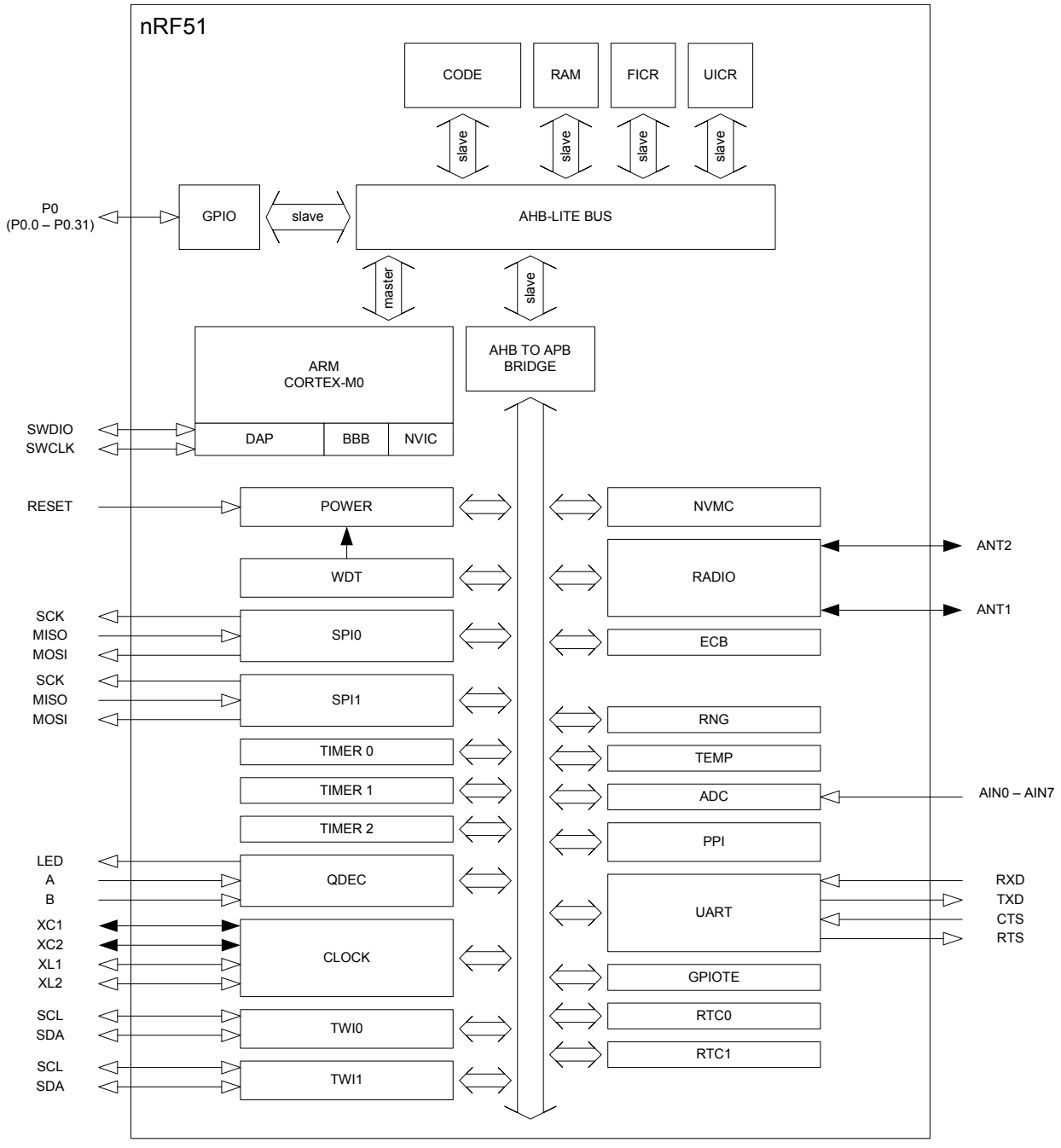
1.2 Writing conventions

This product specification follows a set of typographic rules to ensure that the document is consistent and easy to read. The following writing conventions are used:

- Command, event names, and bit state conditions, are written in `Lucida Console`.
- Pin names and pin signal conditions are written in **`Consolas.`**
- File names and User Interface components are written in **bold**.
- Internal cross references are italicized and written in ***semi-bold.***
- Placeholders for parameters are written in italic regular text font. For example, a syntax description of Connect will be written as:
  SetChannelPeriod*(ChannelNumber, MessagingPeriod)*.
- Fixed parameters are written in regular text font. For example, a syntax description of SetChannelPeriod will be written as:
  SetChannelPeriod (0, Period).

2 Product overview

2.1 Block diagram



Note: RESET is disabled by default.

Figure 1 *nRF51422 block diagram*

2.1.1 Pin assignments and functions

2.1.1.1 Pin assignment nRF51422-QFAA

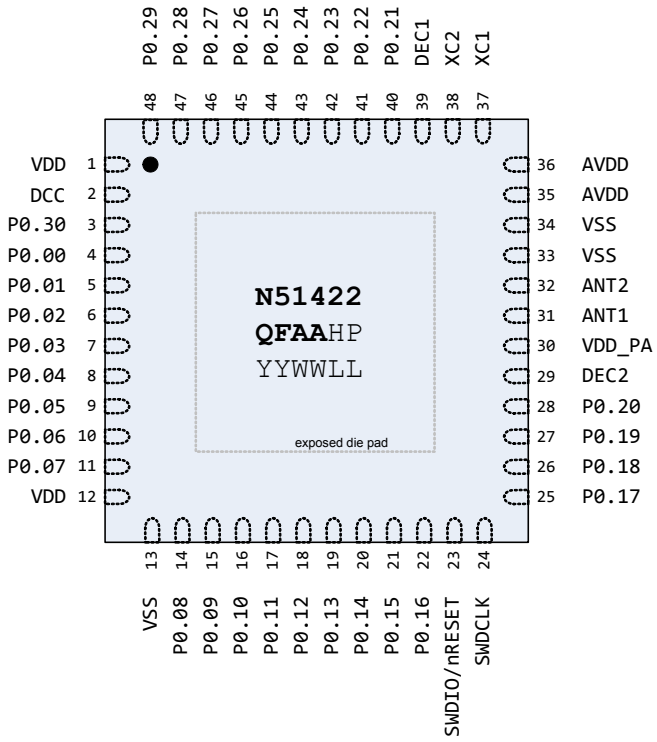


Figure 2 *Pin assignment - nRF51422-QFAA*

Note: HP = Build code, YYWWLL = Tracking code

2.1.1.2 Pin functions nRF51422-QFAA

Pin	Pin name	Pin function	Description
1	VDD	Power	Power supply
2	DCC	Power	DC/DC output voltage to external LC filter
3	P0.30	Digital I/O	General purpose I/O pin
4	P0.00 AREF0	Digital I/O Analog input	General purpose I/O pin ADC Reference voltage
5	P0.01 AIN2	Digital I/O Analog input	General purpose I/O pin ADC input 2
6	P0.02 AIN3	Digital I/O Analog input	General purpose I/O pin ADC input 3
7	P0.03 AIN4	Digital I/O Analog input	General purpose I/O pin ADC input 4
8	P0.04 AIN5	Digital I/O Analog input	General purpose I/O pin ADC input 5
9	P0.05 AIN6	Digital I/O Analog input	General purpose I/O pin ADC input 6
10	P0.06 AIN7 AREF1	Digital I/O Analog input Analog input	General purpose I/O pin ADC input 7 ADC Reference voltage
11	P0.07	Digital I/O	General purpose I/O pin
12	VDD	Power	Power supply
13	VSS	Power	Ground (0 V)[1]
14 to 22	P0.08 to P0.16	Digital I/O	General purpose I/O pin
23	SWDIO/nRESET	Digital I/O	System reset (active low). Also HW debug and flash programming I/O
24	SWDCLK	Digital input	HW debug and flash programming I/O
25 to 28	P0.17 to P0.20	Digital I/O	General purpose I/O pin
29	DEC2	Power	Power supply decoupling
30	VDD_PA	Power output	Power supply output (+1.6 V) for on-chip RF power amp
31	ANT1	RF	Differential antenna connection (TX and RX)
32	ANT2	RF	Differential antenna connection (TX and RX)
33, 34	VSS	Power	Ground (0 V)
35, 36	AVDD	Power	Analog Power supply
37	XC1	Analog input	Crystal connection for 16 MHz crystal oscillator or external 16 MHz crystal reference
38	XC2	Analog output	Crystal connection for 16 MHz crystal
39	DEC1	Power	Power supply decoupling

Pin	Pin name	Pin function	Description
40 to 44	P0.21 to P0.25	Digital I/O	General purpose I/O pin
45	P.026 AIN0 XL2	Digital I/O Analog input Analog output	General purpose I/O pin ADC input 0 Crystal connection for 32.768 kHz crystal oscillator
46	P.027 AIN1 XL1	Digital I/O Analog input Analog input	General purpose I/O pin ADC input 1 Crystal connection for 32.768 kHz crystal oscillator or external 32.768 kHz crystal reference
47, 48	P0.28 and P0.29	Digital I/O	General purpose I/O pin

1. The exposed center pad of the QFN48 package must be connected to supply ground for proper device operation.

Table 1 *Pin functions nRF51422-QFAA*

3 System blocks

The nRF51422 contains system-level features common to all nRF51 series devices including clock control, power and reset, interrupt system, Programmable Peripheral Interconnect (PPI), watchdog, and GPIO.

System blocks which have a register interface and/or interrupt vector assigned are instantiated in the device address space. The instances of system blocks, their associated ID (for those with interrupt vectors) and base address are found in ***Table 10 on page 24***. Detailed functional descriptions, configuration options, and register interfaces can be found in the nRF51 Reference Manual.

3.1 CPU

The ARM® Cortex™-M0 CPU has a 16 bit instruction set with 32 bit extensions (Thumb-2® technology) that delivers high-density code with a small-memory-footprint. By using a single-cycle 32 bit multiplier, a 3-stage pipeline and a Nested Vector Interrupt Controller (NVIC), the ARM Cortex-M0 CPU makes program execution simple and highly efficient.

The ARM Cortex Microcontroller Software Interface Standard (CMSIS) hardware abstraction layer for the ARM Cortex-M processor series is implemented and available for M0 CPU. Code is forward compatible with ARM Cortex M3 based devices.

3.2 Memory

All memory and registers are found in the same address space as shown in the Device Memory Map, see ***Figure 3***. Devices in the nRF51 series have flash program memory and internal SRAM.

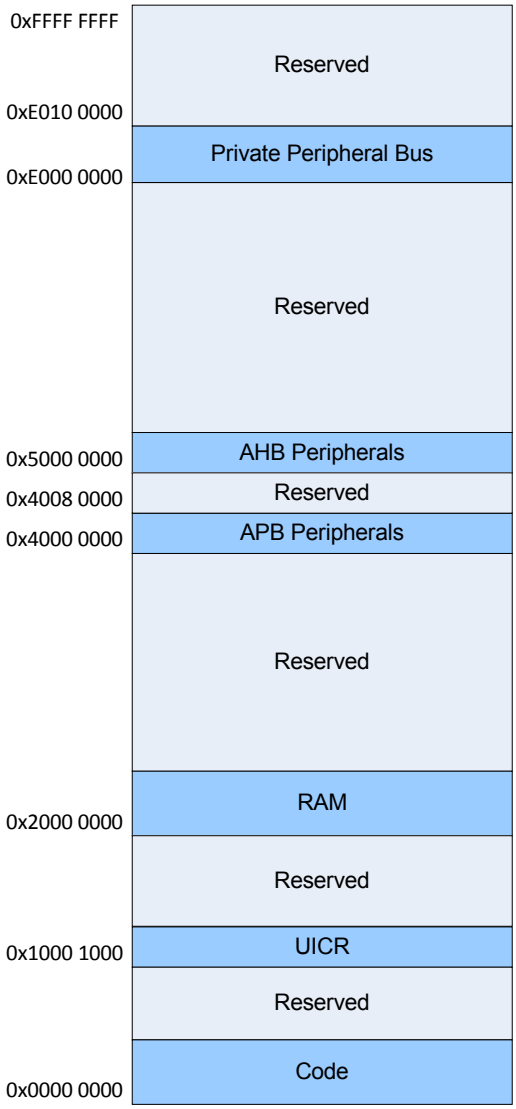


Figure 3 *Device Memory Map*

The embedded flash memory for program and static data can be programmed using In Application Programming (IAP) routines from RAM trough the SWD interface, or in-system from a program executing from flash. The Non-Volatile Memory Controller (NVMC) is used for program/erase operations. A User Information Configuration Register (UICR) contains the lock byte for read-back protect enable to secure IP.

3.2.1 RAM organization

RAM is divided into blocks for separate power management as described in the nRF51 Reference Manual. The RAM power management is controlled by the POWER System Block.

Block	Size	Start address
Block0	8 kB	0x2000 0000
Block1	8 kB	0x2000 2000

Table 2 *RAM organization*

3.3 Power management (POWER)

The power management system is highly flexible with functional blocks such as the CPU, Radio Transceiver, and peripherals having separate power state control in addition to the global System ON and OFF modes. In System OFF mode, RAM can be retained and the device state can be changed to System ON through reset or GPIO signal. When in System ON mode, all functional blocks will independently be in IDLE or RUN mode depending on needed functionality.

Power management features:

- System ON/OFF modes
- Brown-out reset
- Power fail comparator
- Pin wake-up from System OFF
- Functional block RUN/IDLE modes
- 2-region RAM retention in System OFF mode

Power supply features:

- Supervisor HW to manage power on reset, brown out, and power fail
- 1.8 to 3.6 V supply voltage range using internal LDO regulator
- 1.75 to 1.95 V Low voltage mode (external voltage regulator is required)
- 2.1 to 3.6 V supply voltage range using internal buck DC/DC converter

3.3.1 Low voltage mode

Devices can be used in Low voltage mode where a steady 1.8 V supply is available externally. To use the device in the Low voltage mode, the circuit must be modified as per the reference circuitry provided in section ***11.3 on page 54***.

3.3.2 DC/DC converter

The nRF51 DC/DC buck converter transforms battery voltage to lower internal voltage with minimal power loss. The converted voltage is then available to the linear regulator input. The DC/DC converter can be disabled when the supply voltage drops to the lower limit of the voltage range so the LDO can be used for low supply voltages. When enabled, the DC/DC converter operation is automatically suspended when only the low current regulator is needed internally.

This feature is particularly useful for applications using battery technologies with higher nominal cell voltages. The reduction in supply voltage level from a high voltage to a low voltage reduces the peak power drain from the battery. Used with a 3 V coin-cell battery, the peak current drawn from the battery is reduced by approximately 30%.

Note: Three external discrete components are required in order to use the DC/DC converter. See section ***11.1 on page 48*** for details on the schematic, layout, and BOM differences.

3.4 Programmable Peripheral Interconnect (PPI)

The Programmable Peripheral Interconnect (PPI) enables peripherals to interact autonomously with each other using tasks and events independent of the CPU. This feature allows precise synchronization between peripherals when application real-time constraints exist and eliminates the need for CPU activity to implement behavior which can be predefined using PPI.

Instance	Number of channels	Number of groups
PPI	16	4

Table 3 *PPI properties*

3.5 Clock management (CLOCK)

The advanced clock management system can source the system clocks from a range of internal or external high and low frequency oscillators and distribute them to modules based upon a module's individual requirements. This prevents large clock trees being active and drawing power when no system modules needing this clock reference are active.

If an application enables a module that needs a clock reference without the corresponding oscillator running, the clock management system will automatically enable the RC oscillator option and provide the clock. When the module goes back to idle, the clock management will automatically set the oscillator to idle as well. To avoid delays involved in starting a given oscillator, or if a specific oscillator is required, the application can override the automatic oscillator management so it keeps oscillators active when no system modules require the clock reference.

Clocks are only available in System ON mode and can be sourced from the following oscillators:

Clock	Source	Frequency options
High Frequency Clock (HFCLK)	External Crystal Oscillator (XOSC)[1]	16 MHz
	Internal RC Oscillator (RCOSC)	16 MHz
Low Frequency Clock (LFCLK)	External Crystal Oscillator (XOSC)	32.768 kHz
	Internal RC Oscillator (RCOSC)	32.768 kHz ± 2%

1. External Crystal Oscillator must be used for Radio operation

Table 4 *Clock properties*

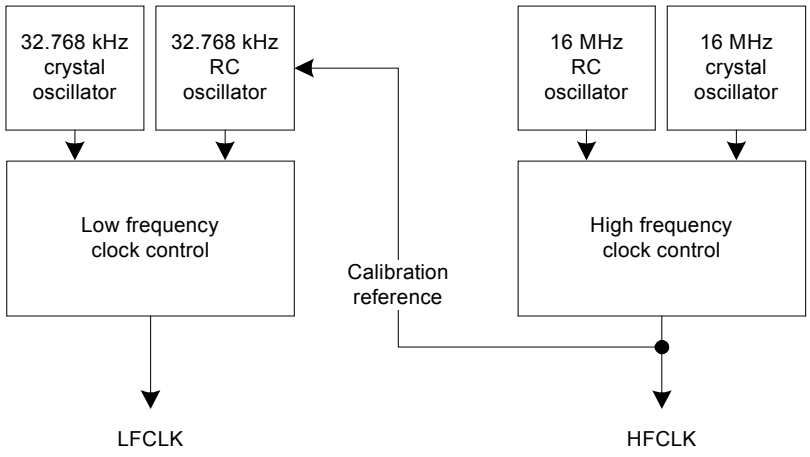


Figure 4 *Clock management*

3.5.1 16 MHz crystal oscillator

The 16 MHz crystal oscillator is designed for use with an AT-cut quartz crystal in parallel resonant mode. To achieve correct oscillation frequency, the load capacitance must match the specification in the crystal data sheet. ***Figure 5*** shows how the crystal is connected to the 16 MHz crystal oscillator.

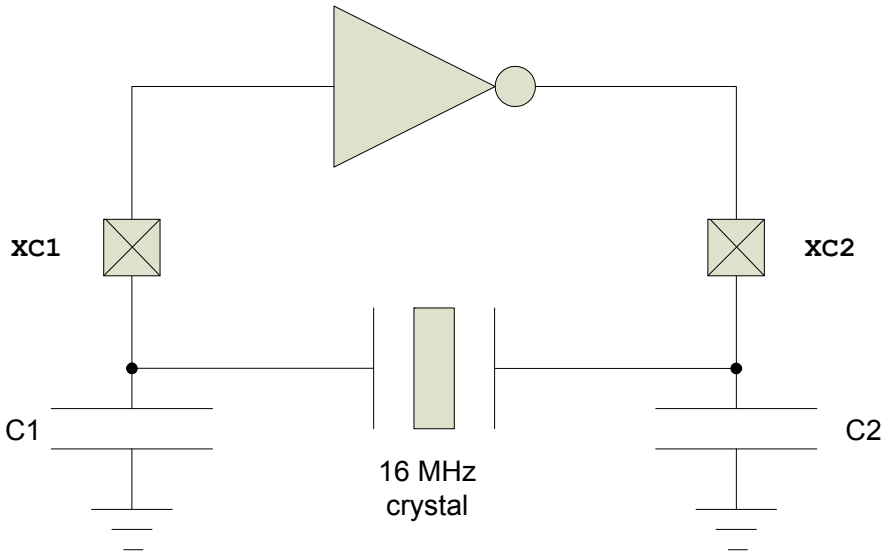


Figure 5 *Circuit diagram of the 16 MHz crystal oscillator*

The load capacitance (CL) is the total capacitance seen by the crystal across its terminals and is given by:

$$CL = \frac{(C1' \cdot C2')}{(C1' + C2')}$$

$$C1' = C1 + C\_pcb1 + C\_pin$$

$$C2' = C2 + C\_pcb2 + C\_pin$$

C1 and C2 are ceramic SMD capacitors connected between each crystal terminal and ground. C_pcb1 and C_pcb2[1] are stray capacitances on the PCB. C_pin is the pin input capacitance on the XC1 and XC2 pins, see ***Table 14 on page 27***. The load capacitance C1 and C2 should be of the same value.

1. See ***chapter 11 on page 48*** for the capacitance value used for C_pcb1 and C_pcb2 in reference circuitry.

3.5.2 32.768 kHz crystal oscillator

The 32.768 kHz crystal oscillator is designed for use with a quartz crystal in parallel resonant mode. To achieve correct oscillation frequency, the load capacitance must match the specification in the crystal data sheet. ***Figure 6*** shows how the crystal is connected to the 32.768 kHz crystal oscillator.

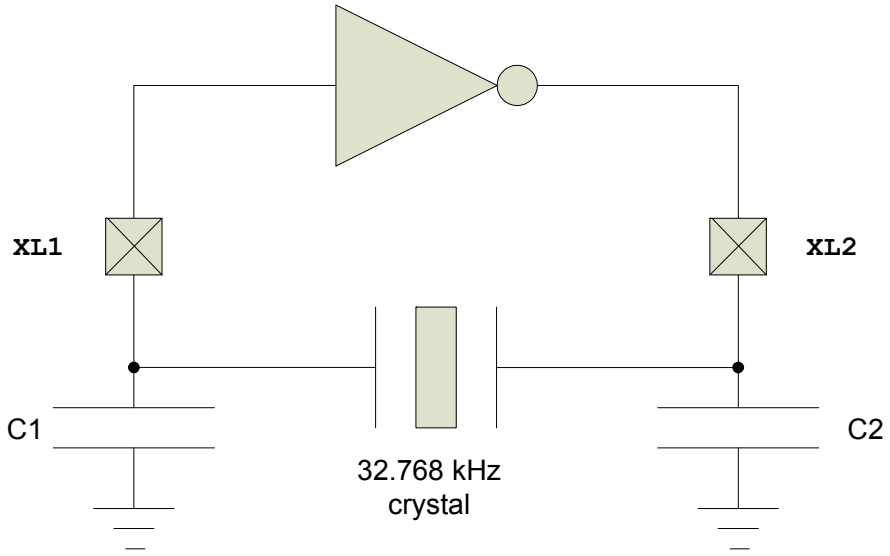


Figure 6 *Circuit diagram of the 32.768 kHz crystal oscillator*

The load capacitance (CL) is the total capacitance seen by the crystal across its terminals and is given by:

$$CL = \frac{(C1' \cdot C2')}{(C1' + C2')}$$

$$C1' = C1 + C\_pcb1 + C\_pin$$

$$C2' = C2 + C\_pcb2 + C\_pin$$

C1 and C2 are ceramic SMD capacitors connected between each crystal terminal and ground. C_pcb1 and C_pcb2[2] are stray capacitances on the PCB. C_pin is the pin input capacitance on the XC1 and XC2 pins, see ***Table 16 on page 28***. The load capacitance C1 and C2 should be of the same value.

3.5.3 32.768 kHz RC oscillator

The 32.768 kHz RC low frequency oscillator may be used as an alternative to the 32.768 kHz crystal oscillator. It has a frequency accuracy of ± 250 ppm in a stable temperature environment or when calibration is periodically performed in changing temperature environments. The 32.768 kHz RC oscillator does not require external components.

2. See ***chapter 11 on page 48*** for the capacitance value used for C_pcb1 and C_pcb2 in reference circuitry.

3.6 GPIO

The Flexible general purpose I/O is organized as one port with up to 32 I/Os (dependant on package) enabling access and control of up to 32 pins through one port. Each GPIO can also be accessed individually and each has the following user configured features.

- Input/output direction
- Output drive strength
- Internal pull up and pull down resistors
- Wake-up from high or low level triggers on all pins
- Trigger interrupt on all pins
- All pins can be used by the PPI task/event system; the maximum number of pins that can be interfaced through the PPI at the same time is limited by the number of GPIOTE modules
- All pins can be individually configured to carry serial interface or quadrature demodulator signals

3.7 Debugger support

The 2-pin Serial Wire Debug (SWD) interface provided as a part of the Debug Access Port (DAP) in conjunction with the Basic Branch Buffer (BBB) offers a flexible and powerful mechanism for non-intrusive debugging of program code. Breakpoints, single stepping, and instruction trace capture of code execution flow are part of this support.

4 Peripheral blocks

Peripheral blocks which have a register interface and/or interrupt vector assigned are instantiated, one or more times, in the device address space. The instances, associated ID (for those with interrupt vectors), and base address of features are found in ***Table 10 on page 24.***[3] Detailed functional descriptions, configuration options, and register interfaces can be found in the nRF51 Reference Manual.

4.1 2.4 GHz radio (RADIO)

The nRF51 series ultra-low power 2.4 GHz GFSK RF transceiver is designed and optimized to operate in the worldwide ISM frequency band at 2.400 to 2.4835 GHz. Radio modulation modes and configurable packet structure make the transceiver interoperable with *Bluetooth*® low energy (BLE), ANT™, Enhanced ShockBurst™, and other 2.4 GHz protocol implementations[4].

The transceiver receives and transmits data directly to and from system memory for flexible and efficient packet data management.

- General modulation features
  - GFSK modulation
  - Data Whitening
    - 7 bit linear feedback shift register (programmable IV)
  - On-air data rates
    - 250 kbps
    - 1 Mbps
    - 2 Mbps
- Transmitter with programmable output power of +4 dBm to -20 dBm, in 4 dB steps
- Transmitter whisper mode: -30 dBm
- RSSI function (1 dB resolution, ± 6 dB accuracy)
- Receiver with integrated channel filters achieving maximum sensitivity
  - -96 dBm @ 250 kbps
  - -90 dBm @ 1 Mbps
  - -85 dBm @ 2 Mbps
- RF Synthesizer
  - 1 MHz frequency programming resolution
  - 1 MHz non-overlapping channel spacing at 1 Mbps and 250 kbps
  - 2 MHz non-overlapping channel spacing at 2 Mbps
  - Works with low-cost ±60 ppm 16 MHz crystal oscillators
- Baseband controller
  - EasyDMA[5] RX and TX packet transfer directly to and from RAM
  - Dynamic payload length
  - On-the-fly packet assembly/disassembly and AES CCM payload encryption
  - 8 bit, 16 bit, and 24 bit CRC check (programmable polynomial and initial value)

3. Information of which peripherals that are restricted, blocked or open by the SoftDevice may be found in S210 SoftDevice specification.
4. nRF51422 S210 SoftDevice must be disabled, in order to run other protocol stacks.
5. EasyDMA - is an integrated DMA implementation requiring no configuration to take advantage of flexible data management and avoid copy operations to and from RAM.

4.2 Timer/counters (TIMER)

The TIMER timer/counter runs on the high-frequency clock source (HFCLK) and includes a 4 bit ($1/2^X$) prescaler that can divide the HFCLK.

The extensive TIMER task/event and interrupt features makes it possible to use the PPI system to do timing/count tasks to/from any system peripheral including any GPIO of the device. The PPI system also enables it to output periodic signals and PWM to any GPIO. Number of input/outputs used at the same time is limited by the number of GPIOTE modules.

Instance	Bit-width	Capture/Compare registers
TIMER0	24	4
TIMER1	16	4
TIMER2	16	4

Table 5 *Timer / Counter properties*

4.3 Real Time Counter (RTC)

The Real Time Counter (RTC) module provides a generic, low power timer on the low-frequency clock source (LFCLK). The RTC features a 24 bit COUNTER, 12 bit (1/X) prescaler, capture/compare registers, and a tick event generator for low-power, tickless RTOS implementation.

Instance	Capture/Compare registers
RTC0	4
RTC1	3

Table 6 *RTC properties*

4.4 AES-ECB encryption (ECB)

The ECB encryption block supports 128 bit AES encryption. It can be used for a range of cryptographic functions like hash generation, digital signatures, and keystream generation for data encryption/decryption. It operates with EasyDMA access to system RAM for in-place operations on cleartext and ciphertext during encryption.

4.5 Random Number Generator (RNG)

The Random Number Generator (RNG) generates true non-deterministic random numbers based on internal thermal noise. These random numbers are suitable for cryptographic purposes. The RNG does not require a seed value.

4.6 Watchdog Timer (WDT)

A countdown watchdog timer using the low-frequency clock source (LFCLK) offers configurable and robust protection against application lock-up. The watchdog can be paused during long CPU sleep periods for low-power applications and when the debugger has halted the CPU.

4.7 Temperature sensor

The temperature sensor measures die temperature over the rated temperature range of the device with 0.25° C resolution.

4.8 SPI (SPI)

The SPI interface enables full duplex synchronous communication between devices. It supports a 3-wire (SCK, MISO, MOSI) bidirectional bus with fast data transfers to multiple slaves. Individual chip select signals will be necessary for each of the slave devices attached to a bus, but control of these is left to the application through use of GPIO signals. I/O data is double buffered.

The GPIOs used for each SPI interface line can be chosen from any GPIO on the device and are independently configurable. This enables great flexibility in device pin-out and enables efficient use of printed circuit board space and signal routing.

The SPI peripheral supports SPI mode 0, 1, 2, and 3.

Instance	Master/Slave
SPI0	Master
SPI1	Master

Table 7 *SPI properties*

4.9 Two-wire interface (TWI)

The Two-wire interface can interface a bi-directional wired-AND bus with two lines (SCL, SDA). The protocol makes it possible to interconnect up to 128 individually addressable devices. The interface is capable of clock stretching and data rates of 100 kbps and 400 kbps are supported.

The GPIOs used for each Two-wire interface line can be chosen from any GPIO on the device and are independently configurable. This enables great flexibility in device pin-out and enables efficient use of board space and signal routing.

Instance	Master/Slave
TWI0	Master
TWI1	Master

Table 8 *Two-wire properties*

4.10 UART (UART)

The Universal Asynchronous Receiver/Transmitter offers fast, full-duplex, asynchronous serial communication with built-in flow control (CTS, RTS) support in HW up to 1 Mbps baud. Parity checking and generation for the 9th data bit are supported.

The GPIOs used for each UART interface line can be chosen from any GPIO on the device and are independently configurable. This enables great flexibility in device pin-out and enables efficient use of board space and signal routing.

4.11 Quadrature Decoder (QDEC)

The quadrature decoder provides buffered decoding of quadrature-encoded sensor signals. It is suitable for mechanical and optical sensors with an optional LED output signal and input debounce filters. The sample period and accumulation are configurable to match application requirements.

4.12 Analog to Digital Converter (ADC)

The 10 bit incremental Analog to Digital Converter (ADC) enables sampling of up to 8 external signals through a front end MUX. The ADC has configurable input and reference prescaling, and sample resolution (8, 9, and 10 bit).

4.13 GPIO Task Event blocks (GPIOTE)

A GPIO TE block enables GPIOs on Port 0 to generate events on pin state change which can be used to carry out tasks through the PPI system. A GPIO can also be driven to change state on system events using the PPI system.

Instance	Number of GPIO's
GPIOTE	4

Table 9 *GPIOTE properties*

5 Instance table

The peripheral instantiation of the nRF51422 is shown in the table below.

ID	Base address	Peripheral	Instance	Description
0	0x40000000	POWER	POWER	Power Control
0	0x40000000	CLOCK	CLOCK	Clock Control
1	0x40001000	RADIO	RADIO	2.4 GHz Radio
2	0x40002000	UART	UART0	Universal Asynchronous Receiver/ Transmitter
3	0x40003000	SPI	SPIM0	SPI0
3	0x40003000	TWI	TWI0	I2C compatible Two-Wire Interface
4	0x40004000	SPI	SPI1	SPI1
4	0x40004000	TWI	TWI1	I2C compatible Two-Wire Interface 1
5				Unused
6	0x40006000	GPIOTE	Port 0 Task and events	GPIO Tasks and events
7	0x40007000	ADC	ADC	Analog-to-Digital Converter
8	0x40008000	TIMER	TIMER0	Timer Counter 0
9	0x40009000	TIMER	TIMER1	Timer Counter 1
10	0x4000A000	TIMER	TIMER2	Timer Counter 2
11	0x4000B000	RTC	RTC0	Real Time Counter 0
12	0x4000C000	TEMP	TEMP	Temperature Sensor
13	0x4000D000	RNG	RNG	Random Number Generator
14	0x4000E000	ECB	ECB	Crypto AES ECB
15	0x4000F000	CCM	CCM	AES Crypto CCM
15	0x4000F000	AAR	AAR	Accelerated Address Resolver
16	0x40010000	WDT	WDT	Watchdog Timer
17	0x40011000	RTC	RTC1	Real Time Counter 1
18	0x40012000	QDEC	QDEC	Quadrature Decoder
19				Unused
20				Reserved as software input
21				Reserved as software input
22				Reserved as software input
23				Reserved as software input
24				Reserved as software input
25				Reserved as software input
26				Unused
27				Unused
28				Unused
29				Unused
30	0x4001E000	NVMC	NVMC	Non-Volatile Memory Controller
31	0x4001F000	PPI	PPI	Programmable Peripheral Interconnect
NA	0x50000000			General Purpose Input and Output

Table 10 *Peripheral instance reference*

Note: Some peripherals will not be available when a SoftDevice is programmed. See the applicable SoftDevice specification for resource usage.

6 Absolute maximum ratings

Maximum ratings are the extreme limits to which nRF51422 can be exposed without permanently damaging it. Exposure to absolute maximum ratings for prolonged periods of time may affect the reliability of nRF51422. ***Table 11*** specifies the absolute maximum ratings for nRF51422.

Symbol	Min.	Max.	Unit
Supply voltages			
VDD	-0.3	+3.6	V
DEC2[1]		2	V
VSS		0	V
I/O pin voltage			
VIO	-0.3	VDD + 0.3	V
Temperature			
Storage temperature	-40	+125	°C

1. Forced in Low voltage mode

Table 11 *Absolute maximum ratings*

7 Operating conditions

The operating conditions are the physical parameters that nRF51422 can operate within as defined in ***Table 12***.

Symbol	Parameter	Notes	Min.	Nom.	Max.	Units
VDD	Supply voltage, normal mode		1.8	3.0	3.6	V
VDD	Supply voltage, normal mode, DC/DC output voltage 1.9 V		2.1	3.0	3.6	V
VDD	Supply voltage, Low voltage mode		1.75	1.8	1.95	V
t_{R_VDD}	Supply rise time (0 V to 1.8 V)	1			60	ms
T_A	Operating temperature		-25	25	75	°C
ESD HBM	Human Body Model Class 2				4	kV
ESD CDM_{QF}	Charged Device Model (QFN48, 6x6 mm package)				750	V
MSL	Moisture Sensitivity Level				2	

1. The on-chip power-on reset circuitry may not function properly for rise times outside the specified interval.

Table 12 *Operating conditions*

Nominal operating conditions (NOC) under which nRF51422 is operated and tested are the nominal (Nom.) values in ***Table 12***.

Extreme operating conditions (EOC) under which nRF51422 is operated and tested are the minimum (Min.) and maximum (Max.) values in ***Table 12***.

8 Electrical specifications

This chapter contains electrical specifications for device interfaces and peripherals including radio parameters and current consumption.

The test levels referenced are defined in ***Table 13***.

Test level	Description
1	Simulated, calculated, by design (specification limit) or prototype samples tested at NOC
2	Parameters have been verified at Test level 1 and in addition: Prototype samples tested at EOC
3	Parameters have been verified at Test level 2 and in addition: Production samples tested at EOC in accordance with JEDEC47
4	Parameters have been verified at Test level 3 and in addition: Production devices are limit tested at NOC

Table 13 *Test level definitions*

8.1 Clock sources

8.1.1 16 MHz crystal oscillator (16M XOSC)

Symbol	Description	Note	Min.	Nom.	Max.	Units	Test level
$f_{NOM,X16M}$	Crystal frequency			16		MHz	N/A
$f_{TOL,X16M}$	Frequency tolerance				±60	ppm	N/A
$C_{L,X16M}$	Load capacitance				16		N/A
$C_{0,X16M}$	Shunt capacitance				7		N/A
$R_{S,X16M}$	Equivalent series resistance	C0 = 7 pF C0 = 5 pF C0 = 3 pF		30 30 30	100 150 200	Ω Ω Ω	N/A N/A N/A
$P_{D,X16M}$	Drive level				100	µW	N/A
C_{pin}	Input capacitance on XC1 and XC2 pads			4		pF	
I_{X16M}	Run current for 16 MHz crystal oscillator	With TSX4025 16MHz crystal		55		µA	1
$I_{STBY,X16M}$	Standby current for 16 MHz crystal oscillator	With TSX4025 16MHz crystal		20		µA	1
$I_{START,X16M}$	Startup current for 16 MHz crystal oscillator	With TSX4025 16MHz crystal		1		mA	1
$t_{START,X16M}$	Startup time for 16 MHz crystal oscillator	With TSX4025 16MHz crystal		0.4	0.5[1]	ms	2

1. Crystals with other specifications than TSX4025 may have up to 1.5 ms startup time.

Table 14 *16 MHz crystal oscillator*

8.1.2 16 MHz RC oscillator (16M RCOSC)

Symbol	Description	Min.	Nom.	Max.	Units	Test level
$f_{NOM,RC16M}$	Nominal frequency		16		MHz	2
$f_{TOL,RC16M}$	Frequency tolerance		±1	±5	%	1
I_{RC16M}	Run current for 16 MHz RC oscillator		400		µA	1
$t_{START,RC16M}$	Startup time for 16 MHz RC oscillator		2.5	3.5	µs	1

Table 15 *16 MHz RC oscillator*

8.1.3 32.768 kHz crystal oscillator (32k XOSC)

Symbol	Description	Min.	Nom.	Max.	Units	Test level
$f_{NOM,X32k}$	Crystal frequency		32,768		kHz	N/A
$f_{TOL,X32k}$	Frequency tolerance			250	ppm	N/A
$C_{L,X32k}$	Load capacitance			12.5	pF	N/A
$C_{0,X32k}$	Shunt capacitance			2	pF	N/A
$R_{S,X32k}$	Equivalent series resistance		50	80	Ω	N/A
$P_{D,X32k}$	Drive level			1	µW	N/A
C_{pin}	Input capacitance on XL1 and XL2 pads		4		pF	1
I_{X32k}	Run current for 32.768 kHz crystal oscillator		0.4	1	µA	1
$I_{START,X32k}$	Startup current for 32.768 kHz crystal oscillator		1.3	1.8	µA	1
$t_{START,X32k}$	Startup time for 32.768 kHz crystal oscillator		0.3	1	ms	2

Table 16 *32.768 kHz crystal oscillator*

8.1.4 32.768 kHz RC oscillator (32k RCOSC)

Symbol	Description	Note	Min.	Nom.	Max.	Units	Test level
$f_{NOM,RC32k}$	Nominal frequency			32.768		kHz	2
$f_{TOL,RC32k}$	Frequency tolerance			±2		%	1
$f_{TOL,CAL,RC32k}$	Frequency tolerance for 32.768 kHz RC oscillator after calibration	Calibration interval TBD			250	ppm	1
I_{RC32k}	Run current for 32.768 kHz RC oscillator		0.5	0.8	1.1	µA	1
$t_{START,RC32k}$	Startup time for 32.768 kHz RC oscillator			100		µs	1

Table 17 *32.768 kHz RC oscillator*

8.2 Power management

Symbol	Description	Note	Min.	Nom.	Max.	Units	Test level
VPOF	Nominal power level warning thresholds (falling supply voltage)			2.1 2.3 2.5 2.7		V	1
$t_{POR, 1µs}$	Time Reset is active from VDD reaches 1.7 V with 1 µs rise time		0.2	2.7		ms	1
$t_{POR, 50 ms}$	Time Reset is active from VDD reaches 1.7 V with 50 ms rise time		6.5	29		ms	1
V_{TOL}	Threshold voltage tolerance				±5	%	1
V_{HYST}	Threshold voltage hysteresis			100		mV	1
I_{OFF}	Current in SYSTEM-OFF, no RAM retention			410		nA	1
$I_{OFF, 16 k}$	Current in SYSTEM-OFF mode 16 kB SRAM retention			740		nA	1
$I_{OFF, 8 k}$	Current in SYSTEM-OFF mode 8 kB SRAM retention			530		nA	1
I_{OFF2ON}	OFF to ON mode transition current			400		µA	1
t_{OFF2ON}	OFF to CPU execute			6.5	7.5	µs	1
I_{ON}	SYSTEM-ON base current			2.3		µA	2
I_{1V2}	Current drawn by 1V2 regulator			290		µA	2
I_{1V7}	Current drawn by 1V7 regulator			90		µA	2
t_{1V2}	Startup time for 1V2 regulator			2.3		µs	1
t_{1V7}	Startup time for 1V7 regulator			2	3.6	µs	1
$I_{1V2RC16}$	Current drawn by 1V2 regulator and 16 MHz RCOSC when both are on at the same time	See ***Table 19***		480		µA	1
$I_{1V2XO16}$	Current drawn by 1V2 regulator and 16 MHz XOSC when both are on at the same time	See ***Table 19***		350		µA	1

Table 18 *Power management*

8.3 Block resource requirements

Block	ID	Required resources				Comment
		1V2	1V7	16M	32k	
Radio	1	x		x		Requires 16M XOSC
UART	2	x		x		
SPI	3, 4	x		x		
2W	3, 4	x		x		
GPIOTE	6	x		x		
ADC	7	x		x		Requires 16M XOSC
TIMER	8, 9, 10			x		
RTC	11, 17				x	
TEMP	12	x		x		Requires 16M XOSC
RNG	13	x				
ECB	14	x		x		
WDT	16				x	
QDEC	18	x		x		
CPU		x	x	x		

Table 19 *Clock and power requirements for different blocks*

8.4 CPU

Symbol	Description	Min.	Nom.	Max.	Units	Test level
$I_{CPU, Flash}$	Run current @ 16 MHz, Executing code from flash memory		4.4[1]		mA	2
$I_{CPU, RAM}$	Run current @ 16 MHz, Executing code from RAM		2.4[2]		mA	1
$I_{START, CPU}$	CPU startup current		0.6		mA	1
$t_{START, CPU}$	IDLE to CPU execute	0	[3]		µs	1

1. Includes CPU, flash, 1V2, 1V7, RC16M
2. Includes CPU, RAM, 1V2, RC16M
3. t_{1V2} if 1V2 regulator is not running already

Table 20 *CPU specifications*

8.5 Radio transceiver

8.5.1 General radio characteristics

Symbol	Description	Note	Min.	Nom.	Max.	Units	Test level
f_{OP}	Operating frequencies	1 MHz channel spacing	2400		2483	MHz	N/A
PLL_{res}	PLL programming resolution			1		MHz	N/A
$\Delta f250$	Frequency deviation @ 250 kbps			±170		kHz	2
Δf_{1M}	Frequency deviation @ 1 Mbps			±170		kHz	2
Δf_{2M}	Frequency deviation @ 2 Mbps			±320		kHz	2
Δf_{BLE}	Frequency deviation @ BLE		±225	±250	±275	kHz	2
bps_{FSK}	On-air data rate		250		2000	kbps	N/A

Table 21 *General radio characteristics*

8.5.2 Radio current consumption

Symbol	Description	Min.	Nom.	Max.	Units	Test level
$I_{TX,+4dBm}$	TX only run current @ P_{OUT} = +4 dBm		16		mA	2
$I_{TX,0dBm}$	TX only run current @ P_{OUT} = 0 dBm		10.5		mA	2
$I_{TX,-4dBm}$	TX only run current @ P_{OUT} = -4 dBm		8		mA	2
$I_{TX,-8dBm}$	TX only run current @ P_{OUT} = -8 dBm		7		mA	2
$I_{TX,-12dBm}$	TX only run current @ P_{OUT} = -12 dBm		6.5		mA	2
$I_{TX,-16dBm}$	TX only run current @ P_{OUT} = -16 dBm		6		mA	2
$I_{TX,-20dBm}$	TX only run current @ P_{OUT} = -20 dBm		5.5		mA	2
$I_{TX,-30dBm}$	TX only run current @ P_{OUT} = -30 dBm		5.5		mA	2
$I_{START,TX}$	TX startup current[1]		7		mA	1
I_{RX}	RX only run current @ 1 Mbps		13		mA	2
$I_{START,RX}$	RX startup current[2]		8.7		mA	1

1. Average current consumption (at 0 dBm TX output power) for TX startup (130 µs), and when changing mode from RX to TX (130 µs).
2. Average current consumption for RX startup (130 µs), and when changing mode from TX to RX (130 µs).

Table 22 *Radio current consumption*

8.5.3 Transmitter specification

Symbol	Description	Min.	Nom.	Max.	Units	Test level
P_{RF}	Maximum output power		4		dBm	2
P_{RFC}	RF power control range	20	24		dB	2
PRFCR	RF power accuracy			±4	dB	1
P_{WHISP}	RF power whisper mode		-30		dBm	2
P_{BW2}	20 dB bandwidth for modulated carrier (2 Mbps)		1800	2000	kHz	2
P_{BW1}	20 dB bandwidth for modulated carrier (1 Mbps)		950	1100	kHz	2
P_{BW250}	20 dB bandwidth for modulated carrier (250 kbps)		700	800	kHz	2
$P_{RF1.2}$	1^{st} Adjacent Channel Transmit Power 2 MHz (2 Mbps)			-20	dBc	2
$P_{RF2.2}$	2^{nd} Adjacent Channel Transmit Power 4 MHz (2 Mbps)			-45	dBc	2
$P_{RF1.1}$	1^{st} Adjacent Channel Transmit Power 1 MHz (1 Mbps)			-20	dBc	2
$P_{RF2.1}$	2^{nd} Adjacent Channel Transmit Power 2 MHz (1 Mbps)			-40	dBc	2
$P_{RF1.250}$	1^{st} Adjacent Channel Transmit Power 1 MHz (250 kbps)			-25	dBc	2
$P_{RF2.250}$	2^{nd} Adjacent Channel Transmit Power 2 MHz (250 kbps)			-40	dBc	2

Table 23 *Transmitter specification*

8.5.4 Receiver specification

Symbol	Description	Min.	Nom.	Max.	Units	Test level
Receiver operation						
PRX_{MAX}	Maximum received signal strength at < 0.1% PER		0		dBm	1
$PRX_{SENS,2M}$	Sensitivity (0.1% BER) @ 2 Mbps		-85		dBm	2
$PRX_{SENS,1M}$	Sensitivity (0.1% BER) @ 1 Mbps		-90		dBm	2
$PRX_{SENS,250k}$	Sensitivity (0.1% BER) @ 250 kbps		-96		dBm	2
P_{SENS} IT 1 Mbps BLE	Receiver sensitivity: Ideal transmitter		-93		dBm	2
P_{SENS} DT 1 Mbps BLE	Receiver sensitivity: Dirty transmitter		-91		dBm	2
RX selectivity - modulated interfering signal[1]						
	2 Mbps					
C/I_{CO}	C/I co-channel		12		dB	2
C/I_{1ST}	1^{st} ACS, C/I 2 MHz		-4		dB	2
C/I_{2ND}	2^{nd} ACS, C/I 4 MHz		-24		dB	2
C/I_{3RD}	3^{rd} ACS, C/I 6 MHz		-28		dB	2
C/I_{6th}	6^{th} ACS, C/I 12 MHz		-44		dB	2
C/I_{Nth}	N^{th} ACS, C/I f_i > 25 MHz		-50		dB	2
	1 Mbps					
C/I_{CO}	C/I co-channel (1 Mbps)		12		dB	2
C/I_{1ST}	1^{st} ACS, C/I 1 MHz		4		dB	2
C/I_{2ND}	2^{nd} ACS, C/I 2 MHz		-24		dB	2
C/I_{3RD}	3^{rd} ACS, C/I 3 MHz		-30		dB	2
C/I_{6th}	6^{th} ACS, C/I 6 MHz		-40		dB	2
C/I_{12th}	12^{th} ACS, C/I 12 MHz		-50		dB	2
C/I_{Nth}	N^{th} ACS, C/I f_i > 25 MHz		-53		dB	2

Symbol	Description	Min.	Nom.	Max.	Units	Test level
	250 kbps					
C/I_{CO}	C/I co-channel		4		dB	2
C/I_{1ST}	1st ACS, C/I 1 MHz		-10		dB	2
C/I_{2ND}	2nd ACS, C/I 2 MHz		-34		dB	2
C/I_{3RD}	3rd ACS, C/I 3 MHz		-39		dB	2
C/I_{6th}	6th ACS, C/I f_i > 6 MHz		-50		dB	2
C/I_{12th}	12th ACS, C/I 12 MHz		-55		dB	2
C/I_{Nth}	Nth ACS, C/I f_i > 25 MHz		-60		dB	2
	***Bluetooth* Low Energy RX selectivity**					
C/I_{CO}	C/I co-channel		10		dB	2
C/I_{1ST}	1st ACS, C/I 1 MHz		1		dB	2
C/I_{2ND}	2nd ACS, C/I 2 MHz		-25		dB	2
C/I_{3+N}	ACS, C/I (3+n) MHz offset [n = 0, 1, 2, . . .]		-51		dB	2
C/I_{Image}	Image blocking level		-30		dB	
$C/I_{Image±1MHz}$	Adjacent channel to image blocking level (±1 MHz)		-31		dB	
RX intermodulation[2]						
P_IMD_{2Mbps}	IMD performance, 2 Mbps, 3rd, 4th and 5th offset channel		-41		dBm	2
P_IMD_{1Mbps}	IMD performance, 1 Mbps, 3rd, 4th and 5th offset channel		-40		dBm	2
$P\_IMD_{250kbps}$	IMD performance, 250 kbps, 3rd, 4th and 5th offset channel		-36		dBm	2
P_IMD_{BLE}	IMD performance, 1 Mbps BLE, 3rd, 4th and 5th offset channel		-39		dBm	2

1. Wanted signal level at P_{IN} = -67 dBm. One interferer is used, having equal modulation as the wanted signal. The input power of the interferer where the sensitivity equals BER = 0.1% is presented.
2. Wanted signal level at P_{IN} = -64 dBm. Two interferers with equal input power are used. The interferer closest in frequency is unmodulated, the other interferer is modulated equal with the wanted signal. The input power of interferers where the sensitivity equals BER = 0.1% is presented.

Table 24 *Receiver specification*

8.5.5 Radio timing parameters

Symbol	Description	250 k	1 M	2 M	BLE	Jitter	Units
t_{TXEN}	Time between TXEN task and READY event	132	132	132	140	0	µs
$t_{TXDISABLE}$	Time between DISABLE task and DISABLED event when the radio was in TX	10	4	3	4	1	µs
t_{RXEN}	Time between the RXEN task and READY event	130	130	130	138	0	µs
$t_{RXDISABLE}$	Time between DISABLE task and DISABLED event when the radio was in RX	0	0	0	0	1	µs
$t_{TXCHAIN}$	TX chain delay	5	1	0.5	1	0	µs
$t_{RXCHAIN}$	RX chain delay	12	2	2.5	3	0	µs

Table 25 *Radio timing*

8.6 RSSI specifications

Symbol	Description	Note	Min.	Nom.	Max.	Units	Test level
$RSSI_{ACC}$	RSSI accuracy	Valid between: -50 dBm and -80 dBm			±6	dB	2
$RSSI_{RESOLUTION}$	RSSI resolution			1		dB	1
$RSSI_{PERIOD}$	Sample period		8.8			µs	1
$RSSI_{CURRENT}$	Current consumption in addition to I_{RX}			250		µA	1

Table 26 *RSSI specifications*

8.7 UART specifications

Symbol	Description	Note	Min.	Nom.	Max.	Units	Test level
I_{UART1M}	Run current @ max baud rate			0.23		mA	1
$I_{UART115k}$	Run current @ 115200 bps			TBD		mA	
$I_{UART1k2}$	Run current @ 1200 bps			TBD		mA	
f_{UART}	Baud rate for UART	1 Mbps line drivers	1.2		921.6	kbps	N/A

Table 27 *UART specifications*

8.8 SPI specifications

Symbol	Description	Min.	Nom.	Max.	Units	Test level
$I_{SPI125K}$	Run current for SPI master @ 125 kbps		5		µA	
I_{SPI8M}	Run current for SPI master @ 8 Mbps		0.2		mA	1
f_{SPI}	Bit rates for SPI	0.125		8	Mbps	N/A

***Table 28** SPI specifications*

8.9 TWI specifications

Symbol	Description	Min.	Nom.	Max.	Units	Test level
I_{2W100K}	Run current for TWI @ 100 kbps		0.38		mA	1
I_{2W400K}	Run current for TWI @ 400 kbps		TBD		mA	1
f_{2W}	Bit rates for TWI	100		400	kbps	N/A

***Table 29** TWI specifications*

8.10 GPIOTE specifications

Symbol	Description	Min.	Nom.	Max.	Units	Test level
$I_{GPIOTE,IN}$	Run current with GPIOTE active in Input mode		0.1		mA	1
$I_{GPIOTE,OUT}$	Run current with GPIOTE active in Output mode		0.1		µA	1

***Table 30** GPIOTE specifications*

8.11 Analog-to-Digital Converter (ADC) specifications

Symbol	Description	Note	Min.	Nom.	Max.	Units	Test level
DNL_{10b}	Differential non-linearity (10 bit mode)			< 1		LSB	1
INL_{10b}	Integral non-linearity (10 bit mode)			2		LSB	1
V_{OS}	Offset error		-2		2	%	2
e_G	Gain error		-2		2	%	2
V_{REF_INT}	Internal reference voltage		-1.5	1.20 V	+1.5	%	2
TC_{REF_INT}	Internal reference voltage drift		-200		200	ppm/°C	2
V_{REF_EXT}	External reference voltage		0.83	1.2	1.3	V	
t_{ADC10b}	Time required to convert a single sample in 10 bit mode			68		µs	1
t_{ADC9b}	Time required to convert a single sample in 9 bit mode			36		µs	1
t_{ADC8b}	Time required to convert a single sample in 8 bit mode			20		µs	1
I_{ADC}	Current drawn by ADC during conversion			0.25		mA	1
ADC_ERR_1V8	Absolute error when used for battery measurement at 1.8 V, 2.2 V, 2.6 V, 3.0 V and 3.4 V	Internal reference, input from VDD/3 10 bit setting		TBD		LSB	
ADC_ERR_2V2				TBD		LSB	
ADC_ERR_2V6				TBD		LSB	
ADC_ERR_3V0				TBD		LSB	
ADC_ERR_3V4				TBD		LSB	

Table 31 *Analog-to-Digital Converter (ADC) specifications*

8.12 Timer specifications

Symbol	Description	Note	Min.	Nom.	Max.	Units	Test level
$I_{TIMER0/1/2,1M}$	Timer @1 MHz run current	32 bit				µA	
		24 bit		25		µA	1
		16 bit		20		µA	1
		8 bit				µA	
$I_{TIMER0/1/2,16M}$	Timer @16 MHz run current	32 bit				µA	
		24 bit		258		µA	1
		16 bit		178		µA	1
		8 bit				µA	

Table 32 *Timer specifications*

8.13 RTC

Symbol	Description	Min.	Nom.	Max.	Units	Test level
I_{RTC}	Timer (LFCLK source)		0.2		µA	1

Table 33 *RTC*

8.14 Temperature sensor

Symbol	Description	Min.	Nom.	Max.	Units	Test level
I_{TEMP}	Run current for Temperature sensor		185		µA	
t_{TEMP}	Time required for temperature measurement		35		µs	
T_{RANGE}	Temperature sensor range	-25		75	°C	N/A
T_{ACC}	Temperature sensor accuracy	-4		4	°C	N/A

Table 34 *Temperature sensor*

8.15 Random Number Generator (RNG) specifications

Symbol	Description	Note	Min.	Nom.	Max.	Units	Test level
I_{RNG}	Run current @ 16 MHz			60		µA	1
$t_{RNG,RAW}$	Run time per byte in RAW mode	Uniform distribution of 0 and 1 is not guaranteed		167		µs	1
$t_{RNG,UNI}$	Run time per byte in Uniform mode	Uniform distribution of 0 and 1 is guaranteed. Time to generate a byte cannot be guaranteed		677		µs	1

Table 35 *Random Number Generator (RNG) specifications*

8.16 ECB/CCM/AAR specifications

Symbol	Description	Min.	Nom.	Max.	Units	Test level
I_{CRYPTO}	Run current for Crypto in all modes		0.4		mA	1
t_{CRYPTO}	Run time per 16 byte block in all modes		8.5		µs	1

Table 36 *ECB/CCM/AAR specifications*

8.17 Watch Dog Timer specifications

Symbol	Description	Min.	Nom.	Max.	Units	Test level
I_{WDT}	Run current for watch dog timer		1		µA	1
t_{WDT}	Time out interval, watch dog timer	30 µs		36 hrs		1

Table 37 *Watch Dog Timer specifications*

8.18 Quadrature Decoder specifications

Symbol	Description	Note	Min.	Nom.	Max.	Units	Test level
I_{QDEC}				250		µA	
t_{SAMPLE}	Time between sampling signals from quadrature decoder		128		16384	µs	N/A
t_{LED}	Time from LED is turned on to signals are sampled	Only valid for optical sensors	0		511	µs	N/A

Table 38 *Quadrature Decoder specifications*

8.19 NVMC specifications

Symbol	Description	Simulated			Units	Test ID	Test level
		Min.	Nom.	Max.			
$t_{EREASEALL}$	Erase flash memory		21		ms		
$t_{PAGEERASE}$	Erase page in flash memory		21		ms		
t_{WRITE}[1]	Write one word to flash memory		22	43	µs		

1. Nominal value applies when writing 32 words or more. Maximum value applies when writing a single word.

Note: The CPU will be halted for the duration of NVMC operations.

Table 39 *NVMC specifications*

8.20 General purpose I/O (GPIO) specification

Symbol	Parameter (condition)	Note	Min.	Nom.	Max.	Units
V_{IH}	Input high voltage		0.7 VDD		VDD	V
V_{IL}	Input low voltage		VSS		0.3 VDD	V
V_{OH}	Output high voltage (std. drive, 0.5 mA)		VDD-0.3		VDD	V
V_{OH}	Output high voltage (high-drive, 5 mA)	1	VDD-0.3		VDD	V
V_{OL}	Output low voltage (std. drive, 0.5 mA)		VSS		0.3	V
V_{OL}	Output low voltage (high-drive, 5 mA)		VSS		0.3	V
R_{PU}	Pull-up resistance		11	13	16	kΩ
R_{PD}	Pull-down resistance		11	13	16	kΩ

1. Maximum number of pins with 5 mA high drive is 3.

Table 40 *General purpose I/O (GPIO) specification*

8.21 Calculating current when the DC/DC converter is enabled

The current drawn when DC/DC converter is enabled can be calculated using ***Equation 1*** together with the conversion efficiency chart in ***Figure 7***.

Parameter	Description	Value
I_{SPEC}	Specified current draw under Normal Test Conditions (NTC)	Sum of values from Electrical Specification tables
$V_{DC/DC}$	Output voltage of the DC/DC converter	1.9 V
η	DC/DC conversion efficiency	Interpolated from ***Figure 7***.
V_{DD}	Battery voltage, voltage at VDD	Interpolated from ***Figure 7***.

Table 41 *DC/DC current calculation parameters*

$$I_{DC/DC} = \frac{V_{DC/DC} \cdot I_{spec}}{\eta \cdot V_{DD}}$$

Equation 1 *DC/DC current calculation*

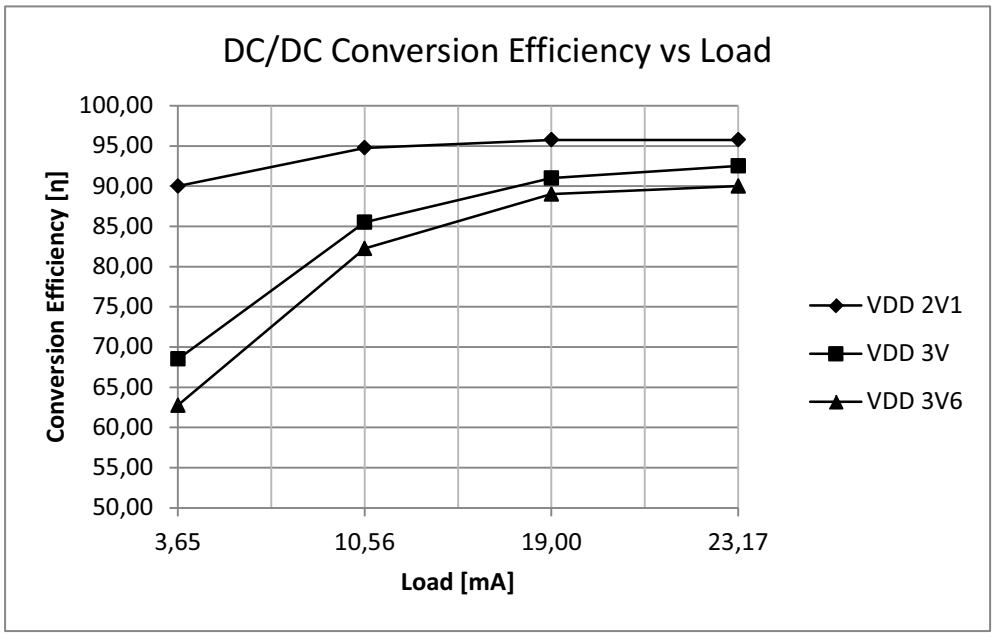


Figure 7 *DC/DC conversion efficiency*

Table 42 shows examples of the current and power consumption of some selected blocks in the device when the DC/DC converter is disabled (I_{spec}, P_{spec}) or enabled ($I_{DC/DC}$, $P_{DC/DC}$).

I_{spec} values can be found in the Electrical specification, see ***chapter 8 on page 27***.

DC/DC efficiency (η) is read from the chart in ***Figure 7*** based on V_{DD} and I_{spec}.
$I_{DC/DC}$ is then calculated using ***Equation 1***.

The P_{spec} and $P_{DC/DC}$ are included to show that for higher efficiencies, the block power consumption will decrease.

Symbol	Description	V_{DD} (V)	DC/DC disabled		η	DC/DC enabled	
			I_{spec} (mA)	P_{spec} (mW)	(I_{spec}, V_{DD})	$I_{DC/DC}$ (mA)	$P_{DC/DC}$ (mW)
I_{TX}	Radio in TX	2.1	10.5	22	95%	10	21
		3	10.5	31.5	86%	7.7	23.1
		3.6	10.5	37.8	84%	6.6	23.8
I_{RX}	Radio in RX	2.1	13	27.3	95%	12.4	26
		3	13	39	87%	9.5	28.5
		3.6	13	46.8	85%	8.1	29.2
$I_{CPUACTIVE}$	CPU executing from flash	2.1	4.4	9.2	92%	4.3	9
		3	4.4	13.2	72%	3.9	11.7
		3.6	4.4	15.84	64%	3.6	13

Table 42 *Current calculation with DC/DC present*

9 Mechanical specifications

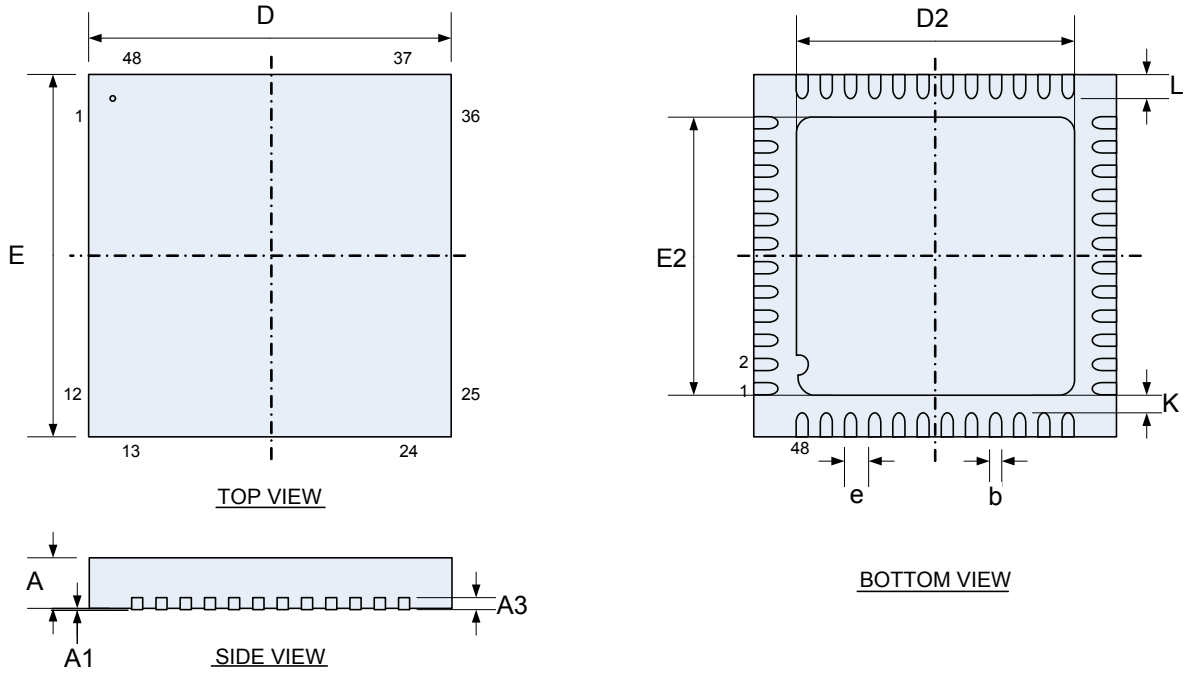


Figure 8 *QFN48 6x6 mm package*

Package	A	A1	A3	b	D, E	D2, E2	e	K	L	
	0.80	0.00		0.15		4.50		0.20	0.35	**Min.**
QFN48 (6 x 6)	0.85	0.02	0.2	0.20	6.0	4.60	0.4		0.40	**Nom.**
	0.90	0.05		0.25		4.70			0.45	**Max.**

Table 43 *QFN48 dimensions in millimeters*

10 Ordering information

10.1 Package marking

N	5	1	4	2	2
<P	P>	<V	V>	<H>	<P>
<Y	Y>	<W	W>	<L	L>

Table 44 *Package marking*

10.2 Order code

n	R	F	5	1	4	2	2	-	<P	P>	<V	V>	-	<C	C>

Table 45 *Order code*

10.3 Abbreviations

Abbreviation	Definition and Implemented Codes
N51 / nRF51	nRF51 series product
422	Part code
<PP>	Package code
<VV>	Variant code
<H><P>	Build code H - Hardware version code P - Production version code (production site, etc.)
<YY><WW><LL>	Tracking code YY - Year code WW - Assembly week number LL - Wafer lot code
<CC>	Container code

Table 46 *Abbreviations*

10.4 Code ranges and values

<PP>	Packet	Size (mm)	Pin Count	Pitch (mm)
QF	QFN	6 x 6	48	0.4

Table 47 Package codes

<VV>	Flash (kB)	RAM (kB)	DC/DC Bond-out
AA	256	16	YES

Table 48 Variant codes

<H>	Description
[A. .Z]	Hardware version/revision identifier (incremental)

Table 49 Hardware version codes

<P>	Description
[0. .9]	Production device identifier (incremental)
[A. .T]	Engineering device identifier (incremental)

Table 50 Production version codes

<YY>	Description
[12. .99]	Production year: 2012 to 2099

Table 51 Year codes

<WW>	Description
[1. .52]	Week of production

Table 52 Week codes

<LL>	Description
[AA. .ZZ]	Wafer production lot identifier

Table 53 Lot codes

<CC>	Description
R7	7” Reel
R	13” Reel
T	Tray

Table 54 Container codes

10.5 Product options

10.5.1 nRF ICs

Order code	MOQ[1]
nRF51422-QFAA-R7	TBD

1. Minimum Order Quantity

Table 55 *Order code*

10.5.2 Development tools

Order code	Description
nRF51422-DK	nRF51422 Development Kit[1]
nRF51422-EK	nRF51422 Evaluation Kit
nRF6700	nRFgo Starter Kit

1. Requires nRF6700 nRFgo Starter Kit

Table 56 *Development tools*

11 Reference circuitry

Note: For the following reference layouts, C_pcb, between X1 and XC1/XC2, are estimated to 0.5 pF each.

Note: The exposed center pad of the QFN48 package must be connected to supply ground for proper device operation.

11.1 nRF51422 QFAA with internal DC/DC converter

11.1.1 Schematic

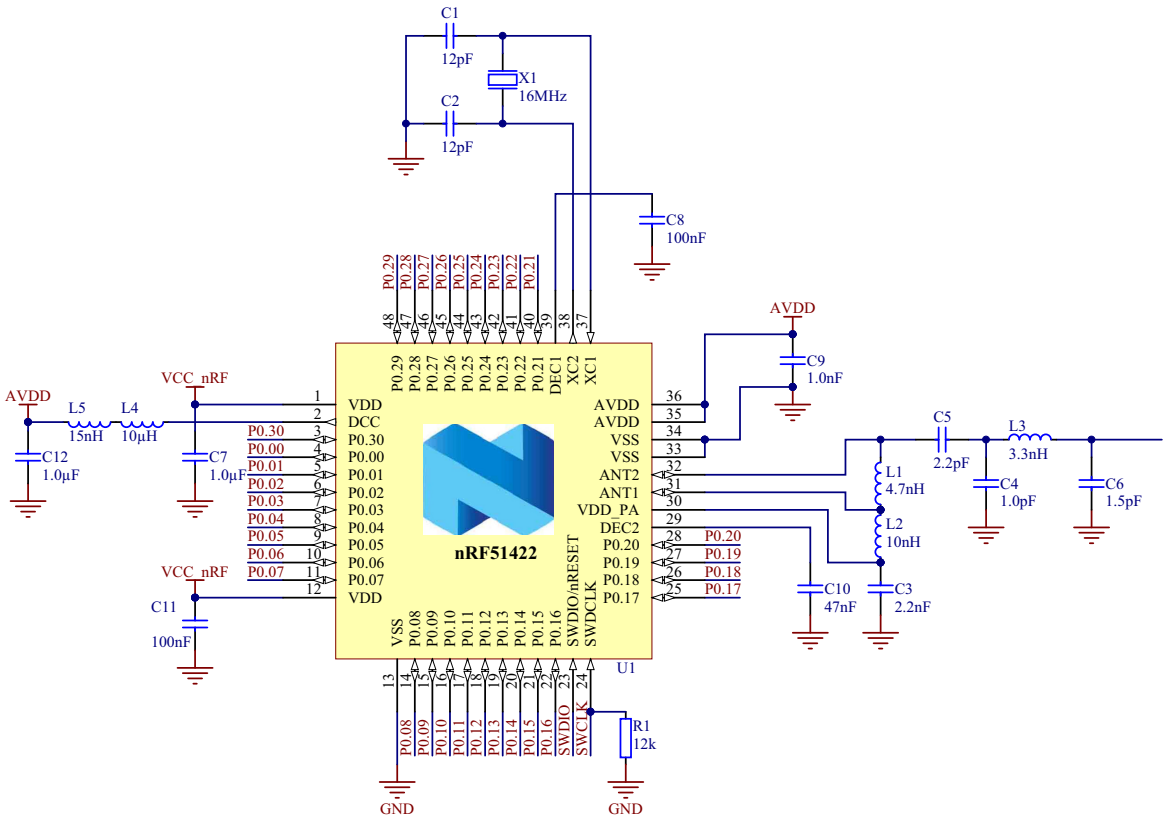
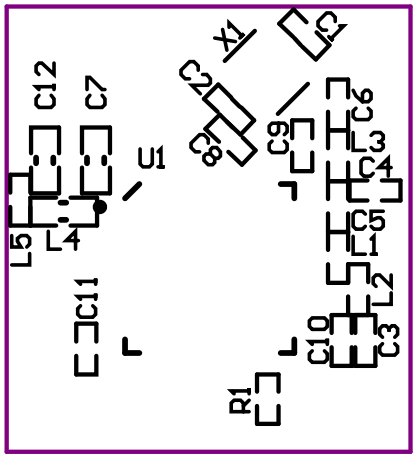


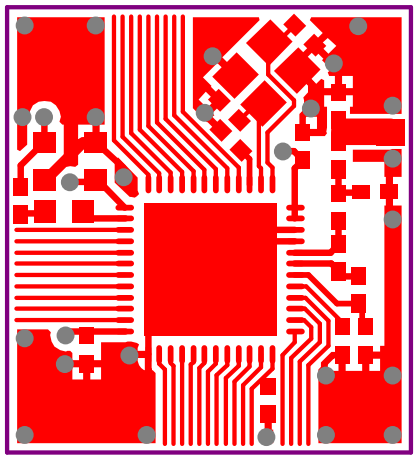
Figure 9 *nRF51422-QFAA with DC/DC converter - Schematic*

11.1.2 Layout

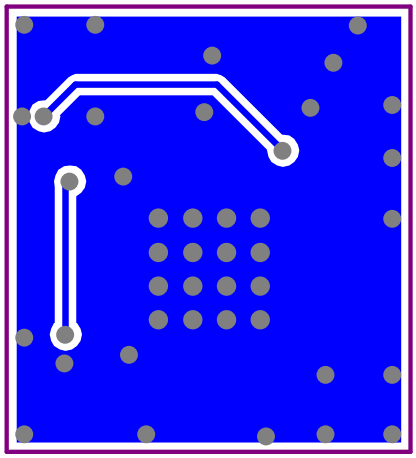


Top silk screen

No components
in bottom layer



Top view



Bottom view

Figure 10 *nRF51422-QFAA with DC/DC regulator - Layout*

11.1.3 Bill of Materials

Designator	Value	Description	Footprint
C1, C2	12 pF	Capacitor, NP0, ±2%	0402
C3	2.2 nF	Capacitor, X7R ±10%	0402
C4	1.0 pF	Capacitor, NP0, ±0.1 pF	0402
C5	2.2 pF	Capacitor, NP0, ±0.1 pF	0402
C6	1.5 pF	Capacitor, NP0, ±0.1 pF	0402
C7, C12	1.0 µF	Capacitor, X7R, ±10%	0603
C8, C11	100 nF	Capacitor, X7R, ±10%	0402
C9	1.0 nF	Capacitor, X7R, ±10%	0402
C10	47 nF	Capacitor, X7R, ±10%	0402
L1	4.7 nH	High frequency chip inductor ±5%	0402
L2	10 nH	High frequency chip inductor ±5%	0402
L3	3.3 nH	High frequency chip inductor ±5%	0402
L4	10 µH	Chip inductor, $I_{DC,min}$ = 50 mA, ±20%	0603
L5	15 nH	High frequency chip inductor ±10%	0402
R1	12 kΩ	Resistor, ±5%, 0.063 W	0402
U1	nRF51422	RF SoC	QFN40P600X600X90-48N
X1	16 MHz	Crystal SMD 2520, 16 MHz, 8 pF, ±40 ppm	2.5 x 2.0 mm

Table 57 *nRF51422-QFAA with DC/DC regulator - Bill of materials*

11.2 nRF51422-QFAA with internal LDO regulator only

11.2.1 Schematic

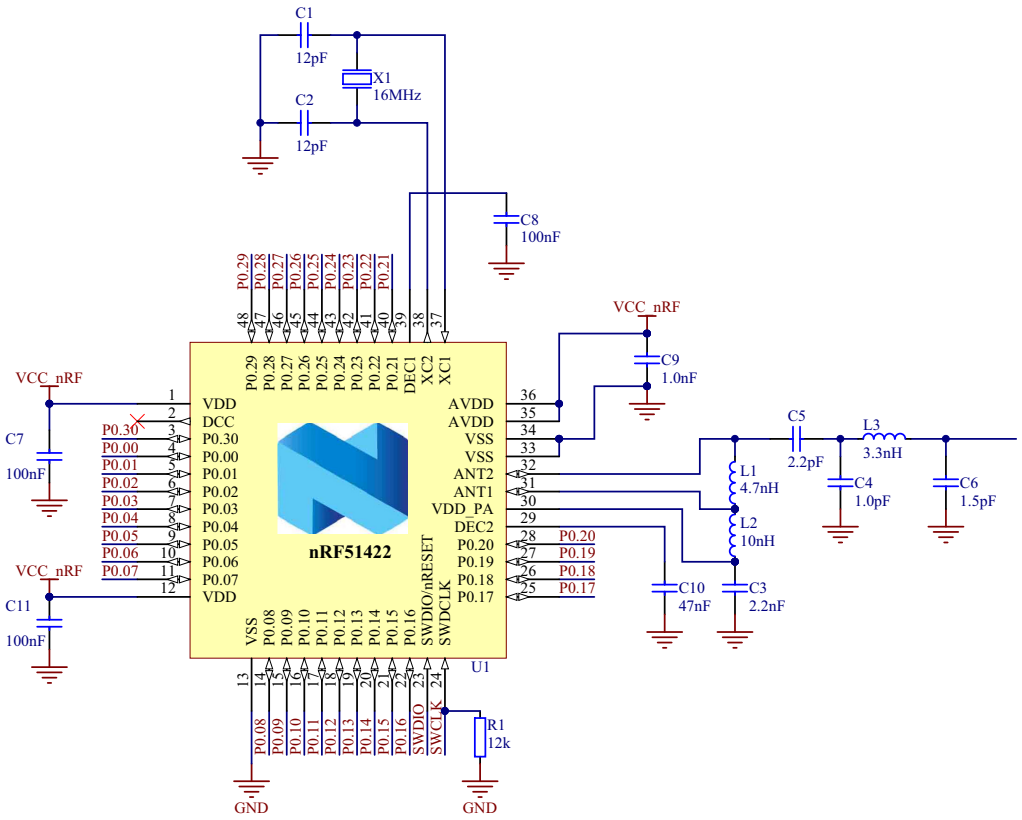
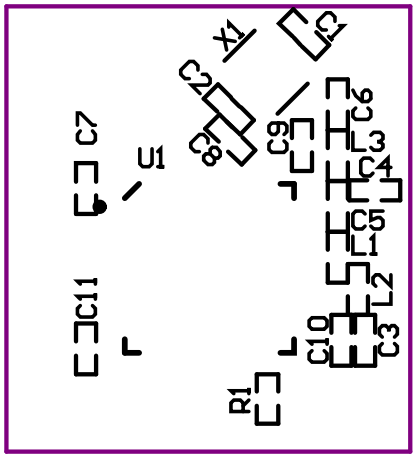


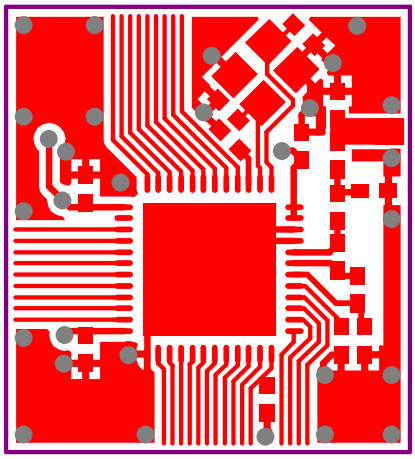
Figure 11 *nRF51422-QFAA with internal LDO regulator only - Schematic*

11.2.2 Layout

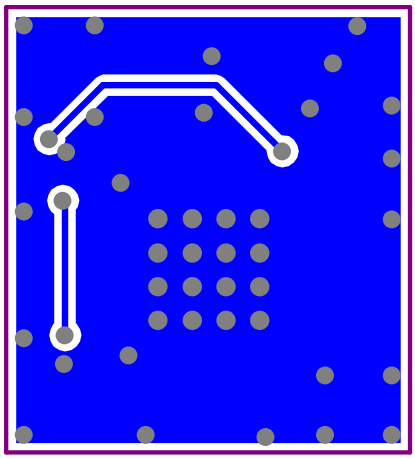


Top silk screen

No components
in bottom layer



Top view



Bottom view

Figure 12 *nRF51422-QFAA with internal LDO regulator only - Layout*

11.2.3 Bill of Materials

Designator	Value	Description	Footprint
C1, C2	12 pF	Capacitor, NP0, ±2%	0402
C3	2.2 nF	Capacitor, X7R, ±10%	0402
C4	1.0 pF	Capacitor, NP0, ±0.1 pF	0402
C5	2.2 pF	Capacitor, NP0, ±0.1 pF	0402
C6	1.5 pF	Capacitor, NP0, ±0.1 pF	0402
C7, C8, C11	100 nF	Capacitor, X7R, ±10%	0402
C9	1.0 nF	Capacitor, X7R, ±10%	0402
C10	47 nF	Capacitor, X7R, ±10%	0402
L1	4.7 nH	High frequency chip inductor ±5%	0402
L2	10 nH	High frequency chip inductor ±5%	0402
L3	3.3 nH	High frequency chip inductor ±5%	0402
R1	12 kΩ	Resistor, ±5%, 0.063 W	0402
U1	nRF51422	RF SoC	QFN40P600X600X90-48N
X1	16 MHz	Crystal SMD 2520, 16 MHz, 8 pF, ±40 ppm	2.5 x 2.0 mm

Table 58 *nRF51422-QFAA with internal LDO regulator only - Bill of materials*

11.3 nRF51422-QFAA with 1.8 V Low voltage mode

11.3.1 Schematic

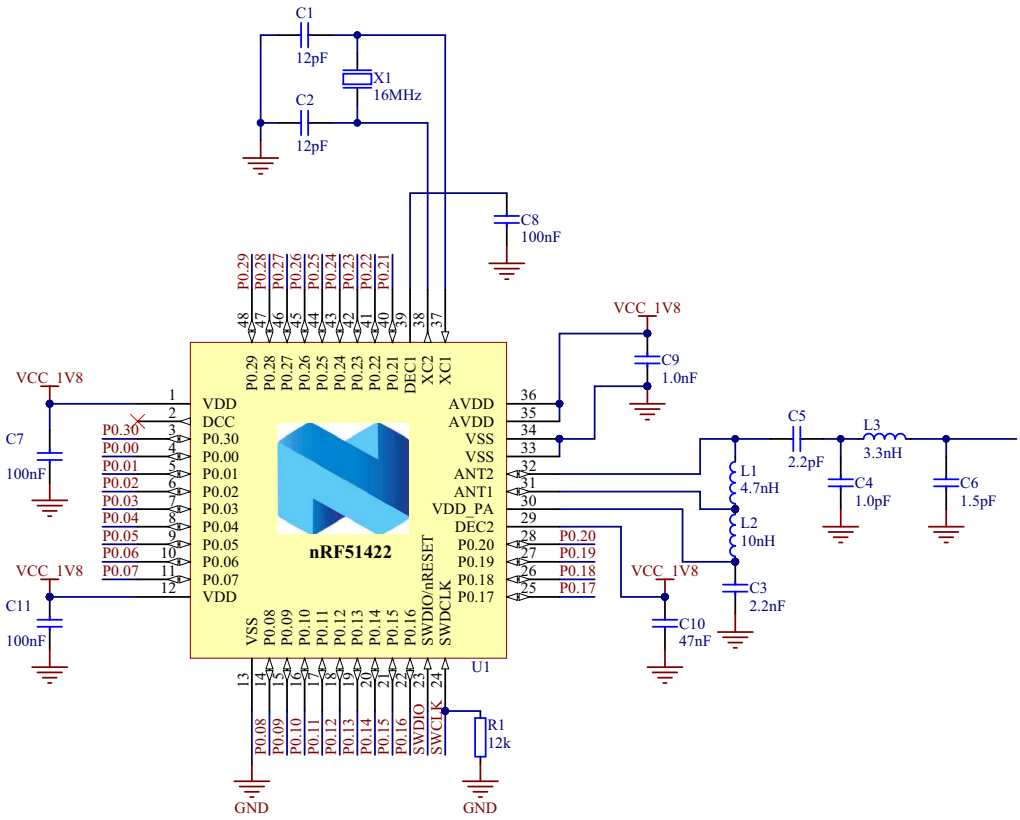
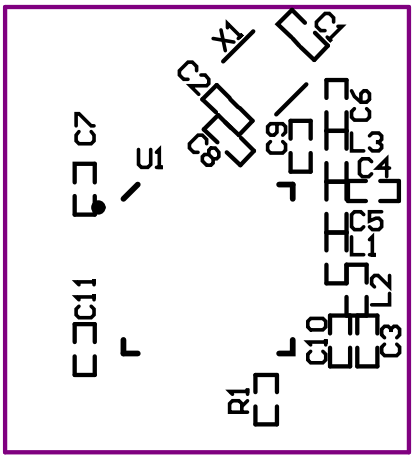


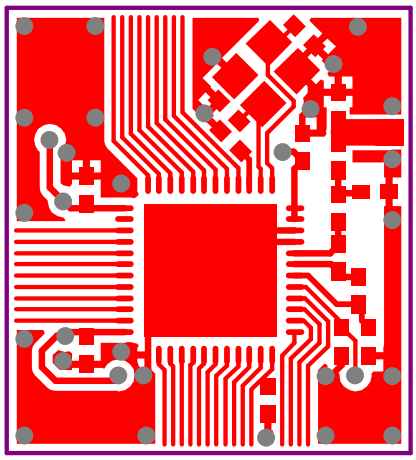
Figure 13 *nRF51422-QFAA with 1.8 V Low voltage mode - Schematic*

11.3.2 Layout

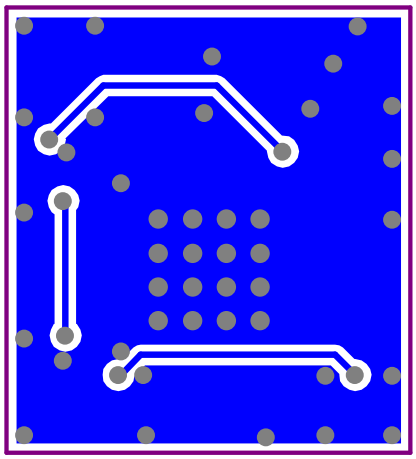


Top silk screen

No components
in bottom layer



Top view



Bottom view

Figure 14 *nRF51422-QFAA with 1.8 V Low voltage mode - Layout*

11.3.3 Bill of Materials

Designator	Value	Description	Footprint
C1, C2	12 pF	Capacitor, NP0, ±2%	0402
C3	2.2 nF	Capacitor, X7R, ±10%	0402
C4	1.0 pF	Capacitor, NP0, ±0.1 pF	0402
C5	2.2 pF	Capacitor, NP0, ±0.1 pF	0402
C6	1.5 pF	Capacitor, NP0, ±0.1 pF	0402
C7, C8, C11	100 nF	Capacitor, X7R, ±10%	0402
C9	1.0 nF	Capacitor, X7R, ±10%	0402
C10	47 nF	Capacitor, X7R, ±10%	0402
L1	4.7 nH	High frequency chip inductor ±5%	0402
L2	10 nH	High frequency chip inductor ±5%	0402
L3	3.3 nH	High frequency chip inductor ±5%	0402
R1	12 kΩ	Resistor, ±5%, 0.063 W	0402
U1	nRF51422	RF SoC	QFN40P600X600X90-48N
X1	16 MHz	Crystal SMD 2520, 16 MHz, 8 pF, ±40 ppm	2.5 x 2.0 mm

Table 59 *nRF51422-QFAA with 1.8 V Low voltage mode - Bill of materials*

12 Glossary

Term	Description
EOC	Extreme Operating Conditions
GFSK	Gaussian Frequency-Shift Keying
GPIO	General Purpose Input Output
ISM	Industrial Scientific Medical
MOQ	Minimum Order Quantity
NOC	Nominal Operating Conditions
NVMC	Non-Volatile Memory Controller
QDEC	Quadrature Decoder
RF	Radio Frequency
RoHS	Restriction of Hazardous Substances
RSSI	Radio Signal Strength Indicator
SPI	Serial Peripheral Interface
TWI	Two-Wire Interface
UART	Universal Asynchronous Receiver Transmitter

Table 60 *Glossary*