CYN DWITH

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EDUCATION

University of Maryland College Park **May 2015**
Master of Science - Electrical and Computer Engineering **GPA: 3.7/4**

National Institute of Technology, Warangal **May 2013**
Bachelor of Technology - Electronics and Communication Engineering **GPA: 3.7/4**

SKILLS

- **Programming:** C/C++, Python, Verilog, System Verilog(UVM), Assembly (x86), VHDL, Perl, Tcl, OpenCV, OpenCL
- **Operating Systems:** Linux, Mac OSX, Windows.
- **Software tools:** Matlab, ModelSim, AVR Studio, Eagle, Cadence Virtuoso (Specter/HSpice), Cadence CIS, Xilinx ISE, NI LabView

WORK EXPERIENCE

Texas Instruments, Bangalore, India **July 2014- July 2015**
Analog Application and Validation Engineer: Developing Hardware and Software for Post Silicon Validation of Mixed Signal Products

- Developed hardware and software for characterization and testing of High Voltage Multiplexer and Precision References
- ATE board Schematic Design with Cadence (Virtuoso) and Mentor Graphics Schematic Editor tools
- Developed Test Automation modules for NI PXI System using NI Lab view and Test Bench
- Improved leakage(~5pA)and Charge Injection(~0.5pC) measurement time by half through innovative circuit design techniques
- Presented the work in Texas Instruments India Technical Conference (TIITC - 2014)
- Designed an Isolated DC-DC (24V-12V) power converter for customer application
- Implemented electronic smart motor drive to replace existing solid state relay in automobiles
- Presented the work as a poster in Texas Instruments India Technical Conference (TIITC - 2013)

Indian Institute of Sciences, Bangalore, India **May-July 2012**
UGC Research Intern: Developed Parallel Algorithms for Face recognition and Texture classification on GPGPU using OpenCL

- Implemented and Evaluated parallel algorithms for face recognition and texture classification
- Improved the execution time of algorithms by 30 folds through heterogeneous programming (OpenCL)
- Published in 13th International Conference of Parallel and Distributed Computing (2013) and International Journal of Computer Application (IJCA)

Young Engineers, Hyderabad, India **May-July 2011**
Interim Engineering Intern: Designed and developed of Autonomous Vacuum cleaner using ATmega16 microcontroller

PROJECTS

Pipelined RiSC16 Processor Design using Verilog **May - 2014**

- Developed Assembler in C for converting Assembly code to machine language for RiSC16 Instruction Set
- Designed pipelined stage with data forwarding, branch prediction, cache interface and precision interrupt.

Low Power CMOS (MOSIS 0.35um) Front End Design **April - 2014**

- Studied and Analyzed topologies and most low power topology was selected and implemented in Cadence Virtuoso (Specter)
- Designed low power inductive degenerated LNA tuned for 900MHz (sub GHz) with conversion gain > 20dB
- Implemented sub harmonic passive mixer to have low power and minimize local oscillator leakage/coupling
- Simulated key parameters like Noise Figure, Voltage Conversion Gain, Linearity (1dB Compression Point/IIP3),

Virtual Memory Simulator (VMS) for Intel i7 **Dec. – 2013**

- Designed VMS to highlight key steps of address translation operation in iTLB, dTLB and TLB.
- Implemented associative search, tag matching and cache replacement scheme (LRU) in L1/L2/L3 Cache
- Framework was developed in C++ with Qt GUI to display different metric like CPI, TLB Misses, Cache Misses and Miss rates

Efficient VLSI Architecture for Motion Estimation in H.264/SVC **May - 2013**

- Built a Real Time Hand Gesture Recognition system in order to facilitate the communication of disabled people.
- Involves elimination of face region and detection of hand region.
- Classification of hand gesture done using trained Haar cascade classifiers.
- Implemented the hand gesture recognition algorithm on OpenCV

Parallel Algorithm for Face recognition and Texture classification on GPGPU using OPENCL **Dec. - 2012**

- Accelerated Red Eye Removal Algorithm using OPENCL framework on GPU. Achieved Red Eye Removal using normalized cross correlation of red eye image with a template image.
- Implemented the algorithm using global memory and local memory to compare the efficiency between the two methods
- Working on adaptive prefetching on GPUs for energy efficiency

Device to Assist Communication of Disabled based on Hand Gesture **March - 2013**

- Built a Real Time Hand Gesture Recognition system in order to facilitate the communication of disabled people.
- Involves elimination of face region and detection of hand region.
- Classification of hand gesture done using trained Haar cascade classifiers.
- Implemented the hand gesture recognition algorithm on OpenCV

Rank Order Filter on FPGA **March - 2012**

- Implemented erosion, dilation and averaging algorithms using rank order filter on FPGA
- Implemented rank order filter on Virtex 2.0 FPGA board.