2015

Low Power sub GHz Direct Conversion Front End Design

RF VLSI 614 Project Report

The main goal of the project is to design two major blocks (LNA and Mixer) of the direct conversion receiver. We discuss Low Noise Amplifier (LNA) and Mixer topologies and most power optimal solution was selected and implemented.

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Content

ENEE 614: RF VLSI Design Project

I. Introduction

a. Motivation

In the past few years the advent of "Internet of things (IoT)", wearable technology has laid a lot of emphasis in low power compact wireless transceiver architectures. Especially applications of IEEE 802.11a /Zigbee standards demand for low power, low cost and short range requirements that dominate transceiver development.

The report discusses the direct conversion architecture that has advantages of compact design with fewer blocks compared to conventional heterodyne architecture, thereby inherently reducing the power and improving the efficiency of integrated solution.

b. System Specification

In order to design a low power receiver we implement a low power, low noise LNA along with passive mixer. The requirement for development of Internet of things are quite distinct from traditional RF technology, these wireless nodes are connected through various networks topologies and reliable short range communication with low/medium data rates are sufficient to transmit data from each device. This is a crucial detail in terms of frequency selection typically lower frequencies have the ability to overcome obstacles better than higher frequencies. For instance, 2.4GHz installation will have roughly 8.5dB of additional path loss when compared to 900MHz [3]. For this project we have chosen 900MHz frequency design to take advantages of existing standards of Zigbee and other sub GHz technologies.

Parameter	Requirement
Frequency Range	(890-910) MHz
Technology	CMOS 0.35um
Supply Voltage	3.3 V
Distance/Range	Short Range

Table1. System Specification of sub GHz Transceiver

II. Direct Conversion Architecture

Direct Conversion Receiver (DCR) unlike the traditional super heterodyne architecture uses only a single stage conversion with zero-IF frequency. Since, the RF signal frequency is reduced to zero-IF frequency; base band signal is its own image. The absence of image frequency reduces the requirement on having Image rejection filter and later stages associated with IF frequency in heterodyne architecture, which can be replaced with simple base band amplifier followed by low pass filter. However, DCR suffers from inherent drawbacks DC offset, LO Leakage and 1/f Noise. Fig1. shows all blocks of direct conversion architecture and highlights blocks (in blue) that are covered in details for design.

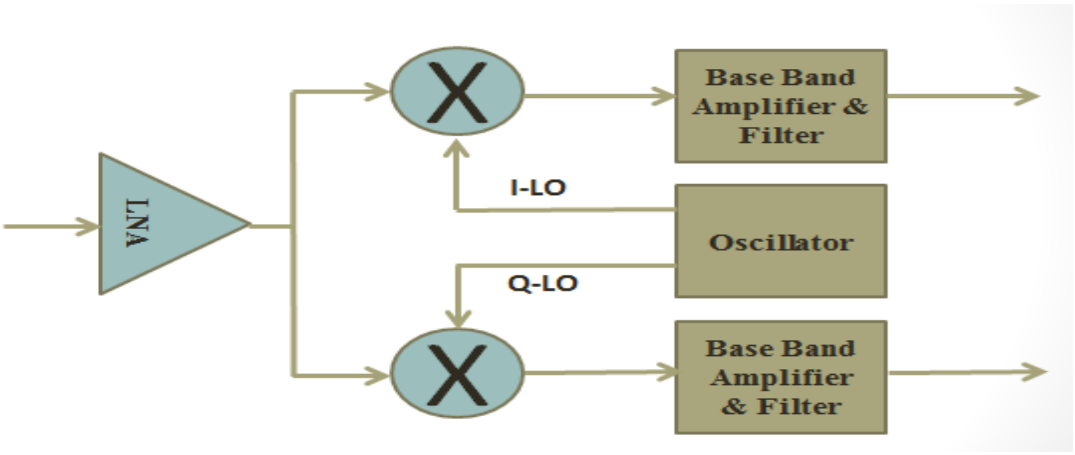


Fig1. Direct Conversion Architecture

III. Low Noise Amplifier

a. LNA Topology

The design of Low Noise Amplifier is to have minimum noise contribution with high gain to minimize noise contribution from later stages to noise factor of the system. An effective LNA stage must have low noise, impedance matching, low power and good isolation.

Traditionally differential LNA structure is used to achieve good isolation at the cost of increased power. The differential LNA provide the same noise figure as a single ended LNA but at twice the power consumption. In order to have low power consumption we will use single ended LNA with cascode stage to improve isolation. The isolation of LNA to minimize LO leakage is achieved by using sub harmonic mixer discussed in section IV. In this section we will discuss the practical aspects of LNA design.

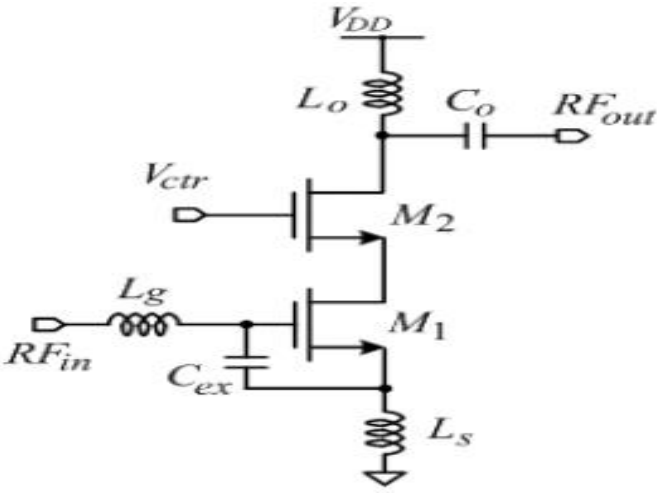


Fig2. Low Noise Amplifier [1]

We use inductive source degeneration (Ls) to generate resistive load at resonance without adding any extra noise. The input impedance is generally matched to 50 Ohms impedance of the antenna in RF systems. The input impedance of the LNA at resonance is given by Rin = (gm/(Cgs+Cex))Ls, once we have reasonable value of source degeneration inductance (Ls) we get required Cgs which can be generated by scaling the MOSFET (M1). This leads to MOSFET sizes that would need large biasing current resulting in higher power. Using external capacitance (Cex) as an alternative for scaling [4], we can reduce the power consumption. However, it leads to reduction in unity current gain bandwidth with is found to be acceptable for sub GHz application.

IV. Mixer

Traditional RF CMOS mixers are active mixers that use current switching for mixing operations. The most widely known topology of doubly balanced gilbert cell uses voltage to current conversion and current switching to achieve the desired mixing. However an alternative topology called passive mixer, uses voltage switching. The choice of mixer is based on low power design. Passive mixers provide power efficient solution but have a drawback of not having a gain through mixer stage.

a. Mixer Topology

Passive mixers use MOSFET as a switch, they do not need to be biased unlike conventional mixer, which leads to considerable reduction in power. The absence of DC current through switches makes it possible to eliminate 1/f noise, which otherwise is a problem especially for direct conversion receiver.

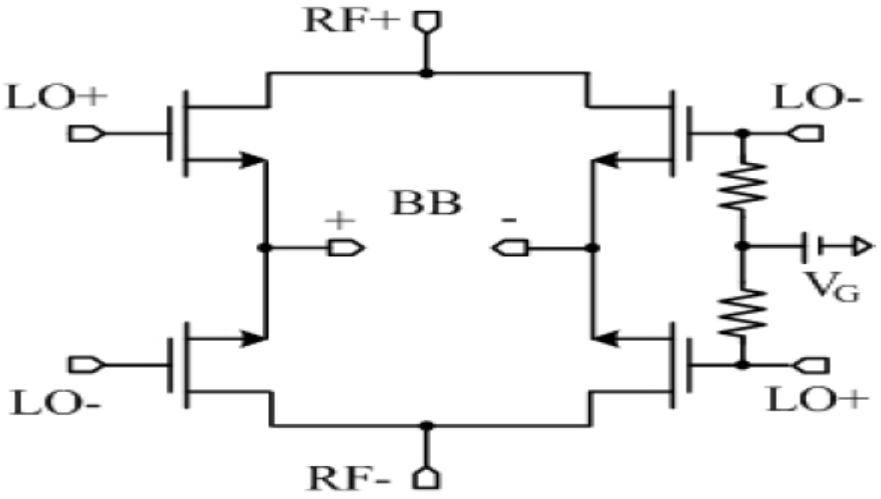
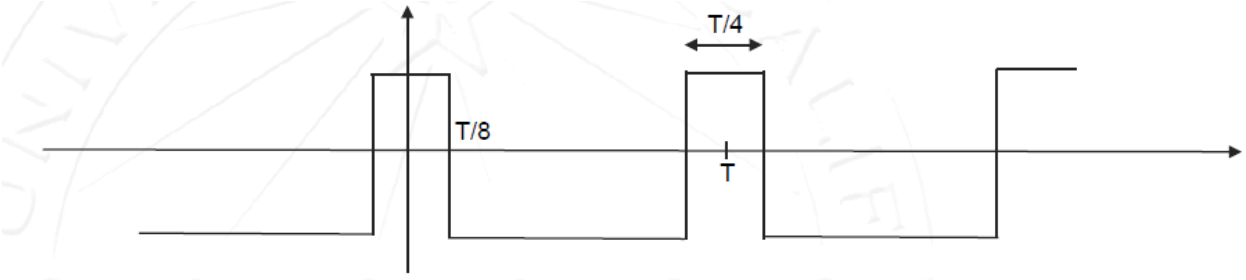


Fig3. Passive Mixer [1]

b. Harmonic Mixer

The subharmonic mixer use a fraction of desired LO frequency as input LO Signal. The mixer is designed to generate the required harmonics or use the harmonics in the LO signal to generated required IF frequency signal. The sub Harmonic mixer offer many advantages in terms of reduced self-mixing as local generator does not give RF frequency but a harmonics and any coupling due to harmonic leakage will be out of band from base band signal.

In case of passive mixer LO signal with 50% duty cycles degenerates only odd harmonics. However, 25% duty cycle LO has required second harmonics as shown [5] in Fig4.



The Fourier series expansion of the above square wave is:

$$V_{\Phi 1} = \frac{1}{\pi}\left[\sqrt{2}\cos(\omega_0 t) + \cos(2\omega_0 t) + \frac{\sqrt{2}}{3}\cos(3\omega_0 t) - \frac{\sqrt{2}}{5}\cos(5\omega_0 t) + \ldots\right]$$

Fig4. LO signal for sub Harmonic Mixing in Passive Mixer

The sub harmonic mixer topology uses two identical mixers excited by two phases of 25% duty cycles. The RF signal is multiplied by these two delayed 25% LO signals by T/2 relative to each other. The resulting IF output is the product of the RF signal and an effective LO that has twice the sub harmonic LO frequency, which is in fact the desired LO frequency. We can similarly extend the analysis to Quadrature component of the LO signal.

V. Test and Analysis

In this section we summarize the simulation results and test procedures for LNA and Mixer.

a. LNA Results

i. LNA Circuit Design

The design of LNA circuit involves selection of reasonable value of degeneration inductance (Ls). We can either choose scaling of MOSFET or use external capacitance (Cex) that saves power. We use an active biasing circuit with high value resistance to avoid any

coupling effects at the input. Input of the LNA is matched to 50 Ohms source impedance using Lg and source degeneration resistance Ls. Proper scaling of current mirror enables us to further reduce any coupling effects of biasing circuits gate-source capacitance.

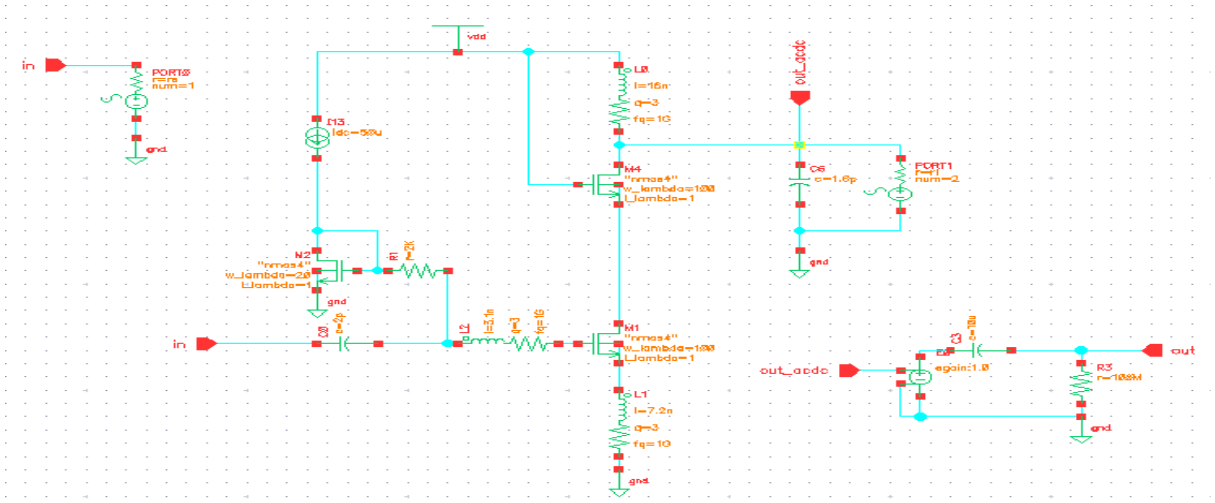


Fig5. LNA Schematic Design

ii. Test Plan and Simulation Results

The S-parameters are generally used to characterize the RF system. They define input-output relation based on incident and reflected wave. In case of LNA, we would want the input reflection (S11), which is a measure of input matching, which we need to be as low as possible (S11<-12dB) over a frequency range of (890-910) MHz. One of the most important parameter of LNA is its gain that needs to be high to suppress noise contributions from later states. S21 describes the forward gain of the LNA circuit, we observed a gain S21>20dB within desired frequency-range.

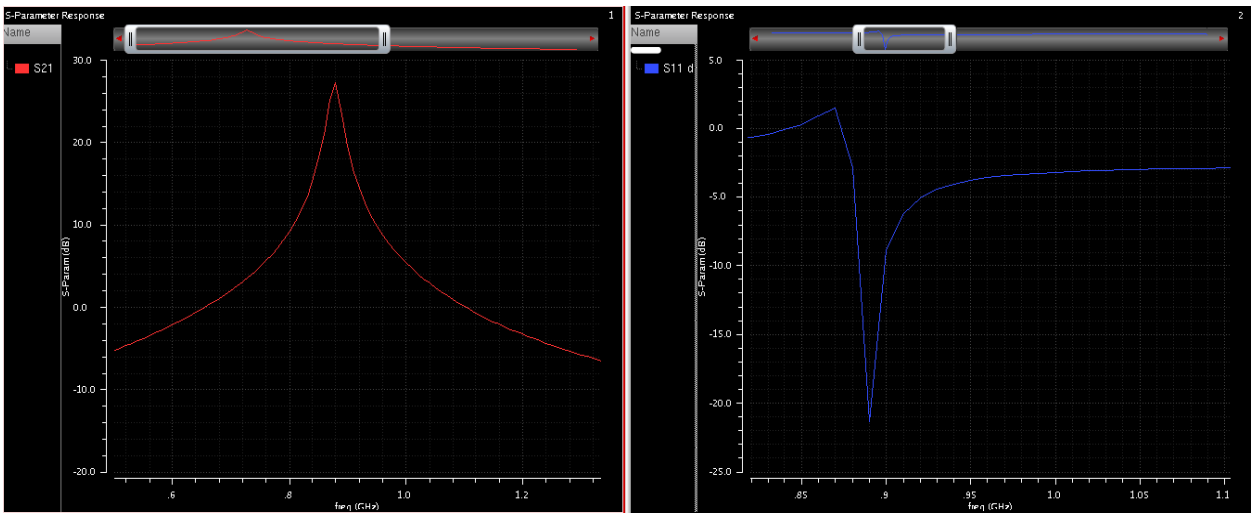


Fig6. S21 (>20dB) and S11 (<-15d) Parameter for LNA

Noise figure (NF) of LNA is crucial parameter as the first stage of transceiver signal chain. NF is defined as the ratio of output noise power divided by noise power of input. We observe that the minimum possible NF is 1.5dB however it does not match with the input matching for power transfer. For maximum input power matching we get a noise figure of 2.35dB as shown in the figure below.

LNA must be able to handle wide range of signal strengths, when the receiver is close to the station with signal strengths upto -20dB and must be sensitive enough to detect signals with strength of -80dB. Hence, we need a highly linear LNA within this range of signal strengths. The 1dB compression is used as measure of linearity, it the input amplitude where the output amplitude is 1dB less than amplitude for earlier increasing input signal strength. Similarly IIP3 (-9.8dB) is used as a measure of LNA linearity [2].

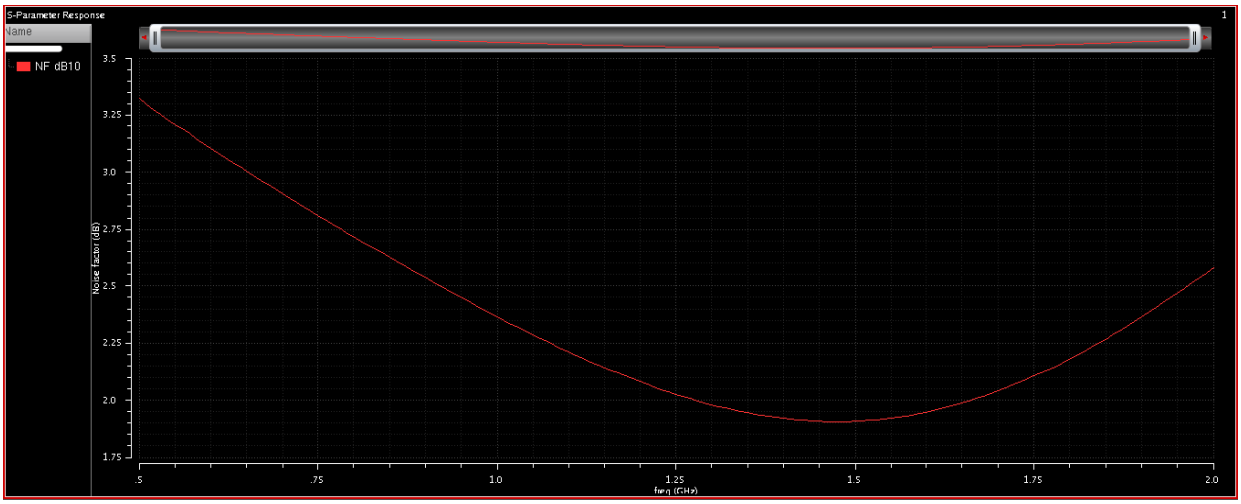


Fig7. Noise Figure (NF-dB) of LNA

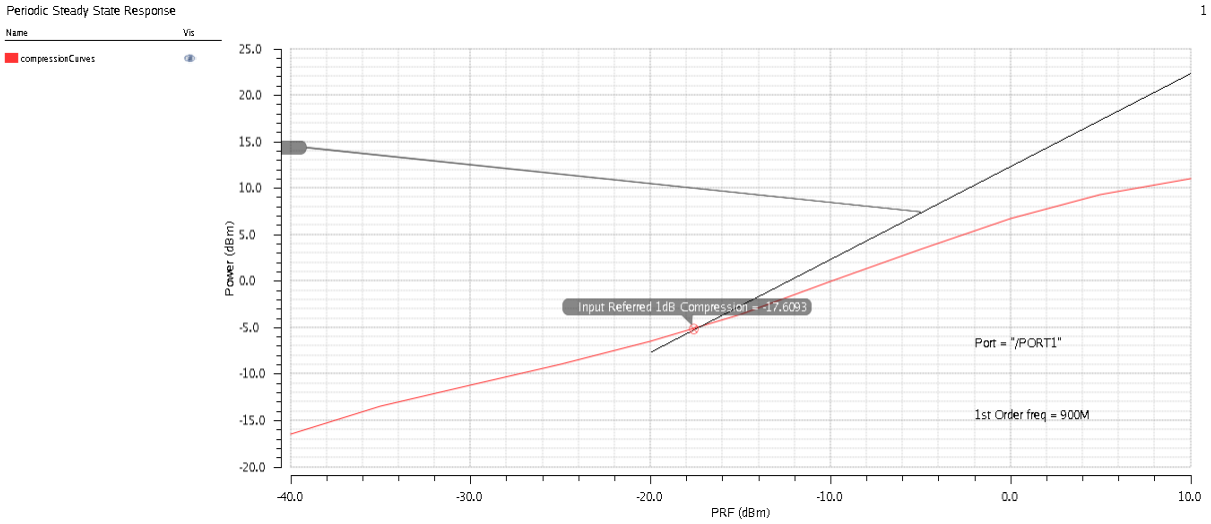


Fig8. Linearity of LNA (1dB Compression Point)

iii. LNA Performance Summary

LNA Parameter	Value
Noise Figure	2.5dB
Conversion Gain (S21)	>20dB
Input Matching (S11)	<-15dB
1dB Compression	-17.6dB
I-bias Current	2mA
Power	6.6mW
IIP3/IIP2	-9.8dB/+25.2dB

Table1. LNA Performance Summary

b. Mixer Results

i. Mixer Circuit Design

Passive mixers in CMOS do not need any DC current, which minimizes the 1/f Noise, which is critical for low frequency applications. We choose NMOS switches for their superior performance in switching speed, when compared to PMOS devices, due to the mobility of charge carriers. In order to optimize the design we need to have proper transistor sizing and correct biasing such that the DC current through these NMOS switches is zero.

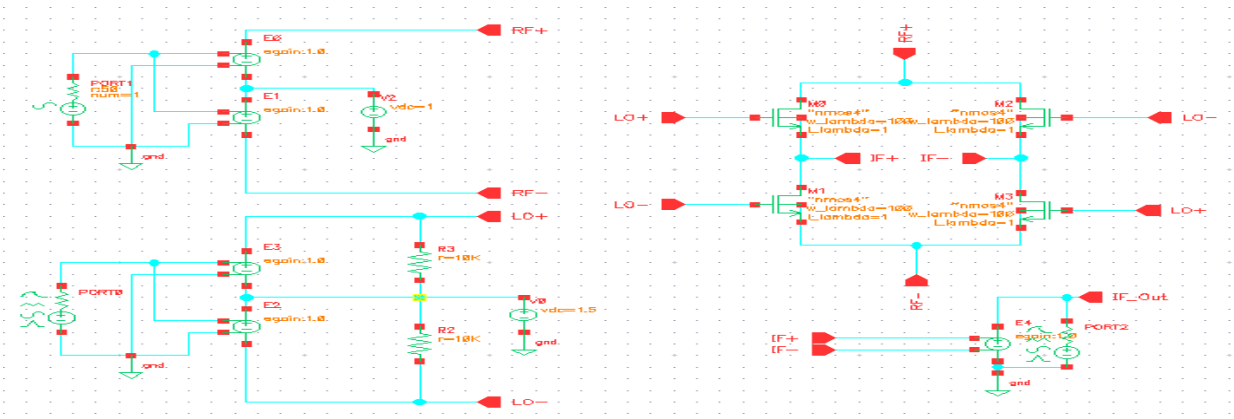


Fig9. Passive CMOS Mixer Schematic

ii. Test Plan & Simulation Results

In order to maintain the report within a specified time frame the simulation results and analysis of the mixer was carried out as a conventional mixer with RF(=900MHz) and LO frequency (1GHz) . In fig.4, you see the transient response of the mixer with LO signal at 1GHz and RF Signal at 900MHz. we see a resulting signal IF of frequency 100MHz. Similar to LNA we define noise figure (NF) and linearity of mixer. Fig11. Shows the 1dB compression point of the Mixer (-4.1dB) and Fig12. Shows the IIP3 (-10.5dB) and IIP2 (+15dB) respectively.

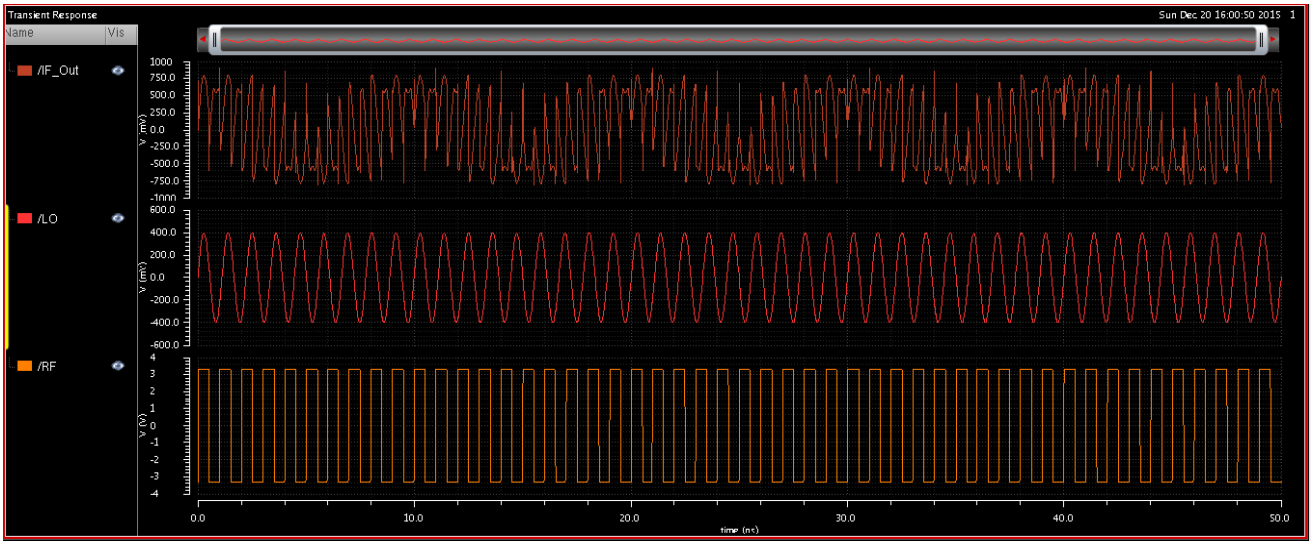


Fig10. Transient response of Mixer (RF, LO and IF Signals)

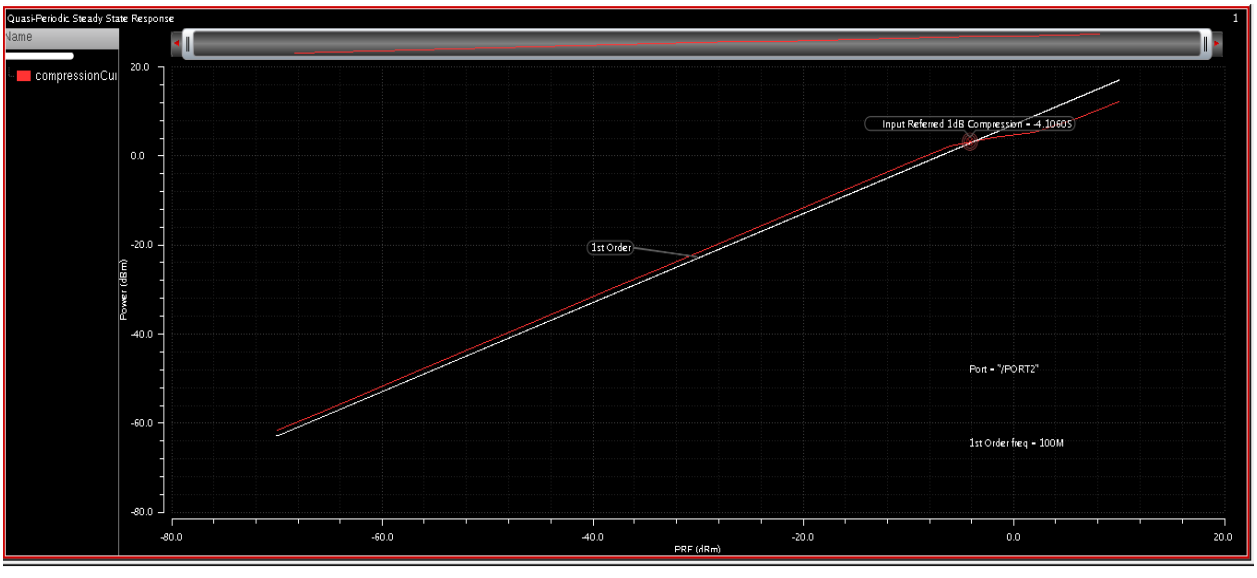


Fig11. Linearity of Mixer - 1dB Compression Point (-4.8dBm)

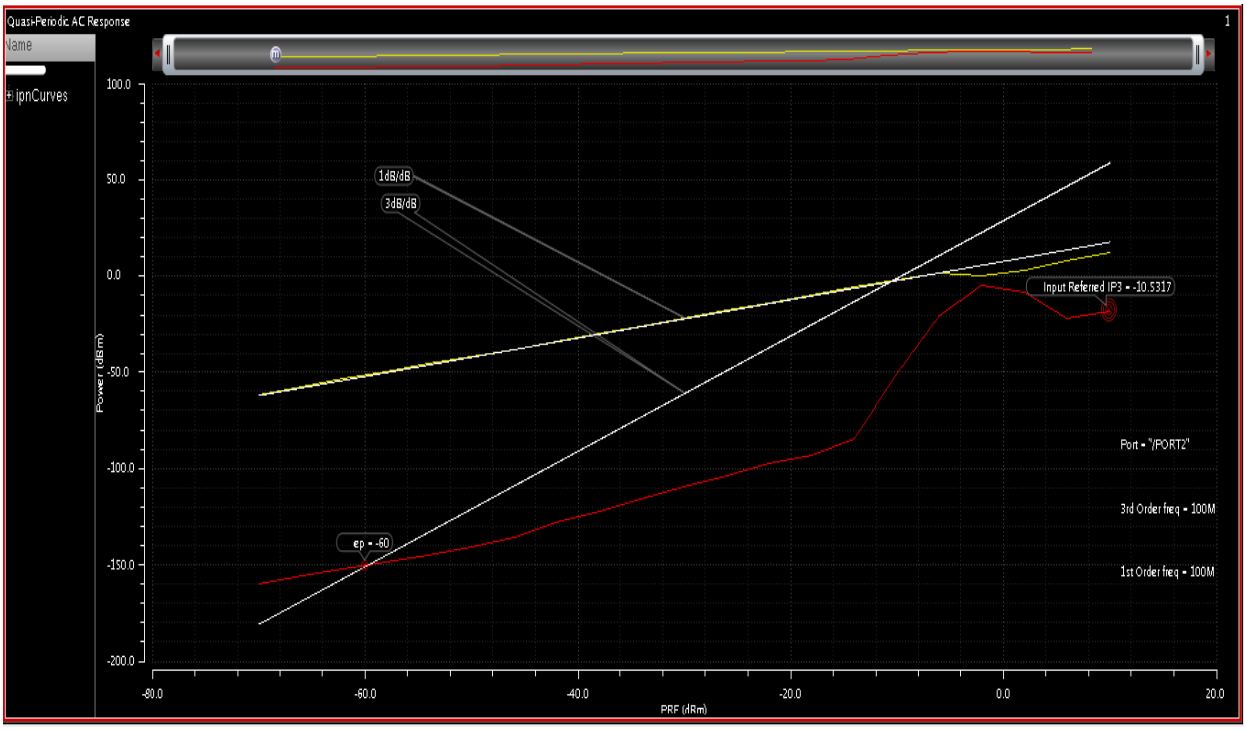


Fig12. Linearity of Mixer – IIP3 (-10.5dB)

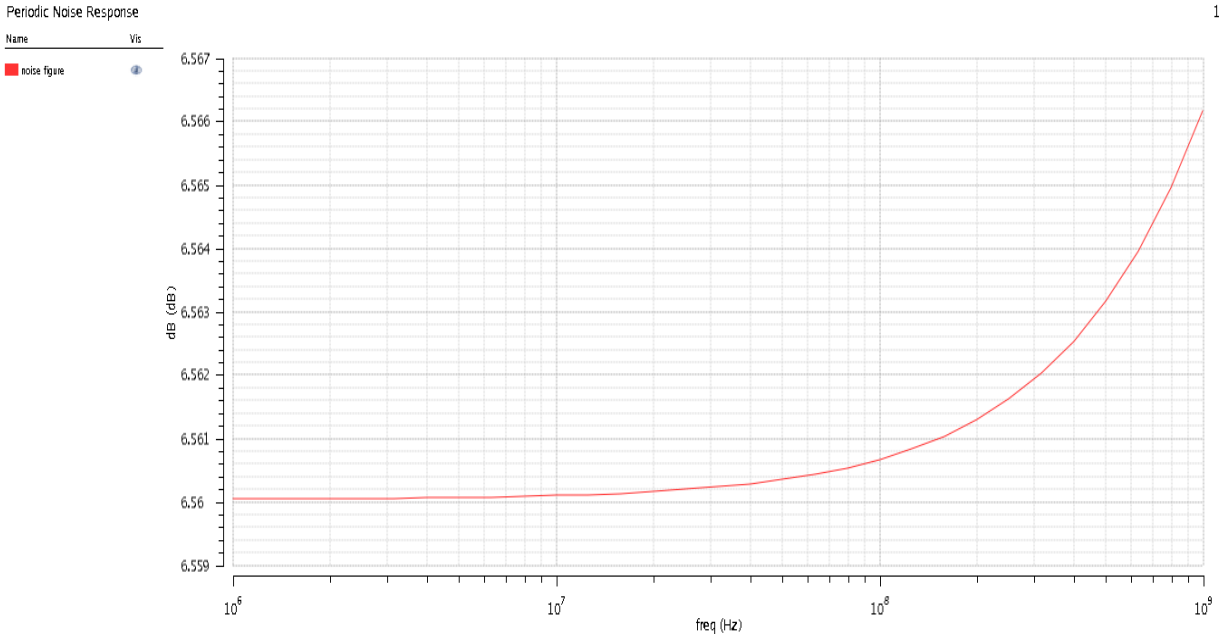


Fig11. Noise Figure of Mixer

iii. Mixer Performance Summary

This section summarizes all the parameters of the Mixer discussed in this section in Table 2.

Mixer Parameter	Value
Noise Figure	**6.5dB**
Linearity (1dB Compression)	**-4.1dBm**
IIP3/IIP2	**-10.5dBm/+15.4dBm**
Technology	**CMOS 0.35u**

Table2. Mixer Performance Summary

Summary

The main goal of the project was to design two major blocks (LNA and Mixer) of the direct conversion receiver. We discussed LNA and Mixer topologies and most power optimal solution was selected and implemented. The summary of results and analysis is presented in Table3.

System Level Specification	Value
Frequency Range	**(890-910) MHz**
Technology	**CMOS 0.35um**
Distance/Range	**Short Range**
Power	**~6.6mW**
Noise Figure (LNA/Mixer)	**2.5dB/6.5dB**
Conversion Gain (LNA)	**>20dB**
Linearity (LNA/Mixer)	**-17.6dBm/-4.1dBm**

Table3. Summary of Specification for the Design

Future Work

The report does not emphasize on bias circuit stability across temperature and process variations. We can use advanced biasing circuits to improve the performance across temperature and process variation. We discussed the components as individual blocks due to limited time the combined analysis of system with LO signal will give a better insight into overall system performance.

References

[1] A 900 MHz CMOS RF direct conversion receiver front-end with 3-dB NF and 30-KHz 1/f noise corner

[2] Design of a Direct-conversion Radio Receiver Front-end in CMOS Technology

[3] The Ten Commandments of Wireless Communications

[4] T.-K. Nguyen, et al., "CMOS Low-Noise Amplifier Design Optimization Techniques," IEEE Transactions on Microwave Theory and Techniques, vol. 52, pp. 1433-1442, May 2004.

[5] Professor Ali M. Niknejad, Advanced Communication Integrated Cricuits,EECS 242: Mixer Noise and Design