```
set link_library ./db/saed90nm_typ_ht.db
set target_library [list ./db/saed90nm_typ_ht.db]
set symbol_library [list ./db/saed90nm_typ_ht.sdb]
set synthetic_library
/opt/CAD/Synopsys/Current/Synthesis/libraries/syn/dw_foundation.sldb
set link_library [concat $link_library $synthetic_library
$target_library]
set synthetic_library
/opt/CAD/Synopsys/Current/Synthesis/libraries/syn/dw_foundation.sldb
set link_library [concat $link_library $synthetic_library
$target_library]
set synthetic_library
/opt/CAD/Synopsys/Current/Synthesis/libraries/syn/dft_jtag.sldb
set link_library [concat $link_library $synthetic_library
$target_library]



read_verilog ./src/gcd_bsd.v
read_verilog ./src/TOP.v
set current_design TOP
link

set_dft_signal -view existing_dft -type ScanClock -port CLK -timing
[list 45 55]

read_pin_map ./src/pin.txt   #assigns the location of the pin(pin
#structure)

set_dft_signal -view spec -type TCK -port TCK
set_dft_signal -view spec -type TDI -port TDI
set_dft_signal -view spec -type TDO -port TDO
set_dft_signal -view spec -type TMS -port TMS
set_dft_signal -view spec -type TRST -port TRST
#the hook up pin connects the TDI chain to the test_si
set_dft_signal -view spec -type tdi -hookup_pin core/test_si
# the hook up pin connects the test_so to tdo type pins
set_dft_signal -view spec -type tdo -hookup_pin core/test_so
set_dft_signal -view spec -type bsd_shift_en -hookup_pin core/test_se
set_dft_signal -view spec -type capture_clk -hookup_pin core/clk
set_scan_path STT_REG -class bsd -view spec -hookup {BSR_SI BSR_SO
core/test_si core/test_so core/test_se core/clk} -exact_length 34
#assigns the scan chain length
create_clock CLK -period 100 -waveform {0 50}

set_bsd_configuration -ir_width 4 #sets instruction register length
#these commands set the instruction value for each operation
set_bsd_instruction -view spec [list EXTEST] -code [list 0000] -reg
BOUNDARY
set_bsd_instruction -view spec [list SAMPLE] -code [list 0100] -reg
BOUNDARY
set_bsd_instruction -view spec [list PRELOAD] -code [list 0100] -reg
BOUNDARY
set_bsd_instruction -view spec [list BYPASS] -code [list 1111] -reg
BYPASS

set_bsd_instruction -view spec [list CLAMP] -code [list 0010] -reg
BYPASS
set_bsd_instruction SCANCH -register STT_REG -code 1101
```

```
set_bsd_compliance -name P1 -pattern {TEST_SE 1 RST 0}

#sets unique identification code for the chip
set_bsd_instruction IDCODE -register DEVICE_ID -code 0111 -
capture_value {32'b00000000000000000000000000000111}

set_dft_configuration -bsd enable -scan disable
preview_dft

#insert jtag..includes compile
insert_dft
#Compliance checking
check_bsd -verbose

#Generate bsdl file
write_bsdl -out ./src/TOP_bsd.bsdl
#Generate bsd patterns
create_bsd_patterns -type all
write_test -format stil_testbench -output ./src/bsd_patterns
# generate verilog TAP testbench
write_test -format verilog -output ./src/BSD_tb.v
#write out jtag-inserted netlist
write -format ddc -hierarchy -output ./src/TOP_bsd.ddc
change_names -rules verilog -hier
write -format verilog -hierarchy -output ./src/TOP_bsd.v
```

Schematic after combining Boundary Scan with internal Scan Chain: