Test mode readback select between
buffer data or adder output

Sprite line # for rendering

Y match

Inverted internally
FLIP
INVERTER
HIRO
Adds 2 or -2 to Y pos
depending on screen flip
HECTOR
JASON
JASON
BUF_D0
BUF_D1
BUF_D2
BUF_D3
TESTMODE
PIN_D0_OUT
PIN_D1_OUT
PIN_D2_OUT
PIN_D3_OUT
4MUX2
VCC
ADD4
FOX
GRACIE
JOSHUA
BUF_D4
BUF_D5
BUF_D6
BUF_D7
PIN_D4_OUT
PIN_D5_OUT
PIN_D6_OUT
PIN_D7_OUT
Nuts.
HABIB
PIN_57
AND_4
Inverted internally
FLIP
INVERTER
JERRY
Invert raster line #
depending on screen flip
HELEN
HANS
HENRY
HARRY
FLORA
FRANK
FELIX
DOUG
PIN_V1
PIN_V2
PIN_V3
PIN_V4
PIN_V5
PIN_V6
PIN_V7
PIN_V8
XOR_2
Inverted internally
FLIP
INVERTER
HELIO
Adds 1 or -1 to Y pos
depending on screen flip
FRIDA
FABIO2
CLK
D0 D1 D2 D3
Q0 Q1 Q2 Q3
4DFF
GARY
GERALD
FREYA
Catch sprite Y position byte
from active list currently read
FRITZ
FABIO3
ACTIVE_D0
ACTIVE_D1
ACTIVE_D2
ACTIVE_D3
ELISE
HAROLD
ACTIVE_D4
ACTIVE_D5
ACTIVE_D6
ACTIVE_D7
GORDON
For 32 and 64 pixels high sprites ?
AIDEN
BLAKE
PIN_54
PIN_55
BUFFER
Inverted internally
PIN_VFLP
BEN
BUCK
BILLY
BRUCE
AGNES
ABEL
ALICE
ALLEN
PIN_VLB0
PIN_VLB1
PIN_VLB2
PIN_VLB3

TITLE: Capcom 86S105 Y POSITION	DATE: 21/11/2023
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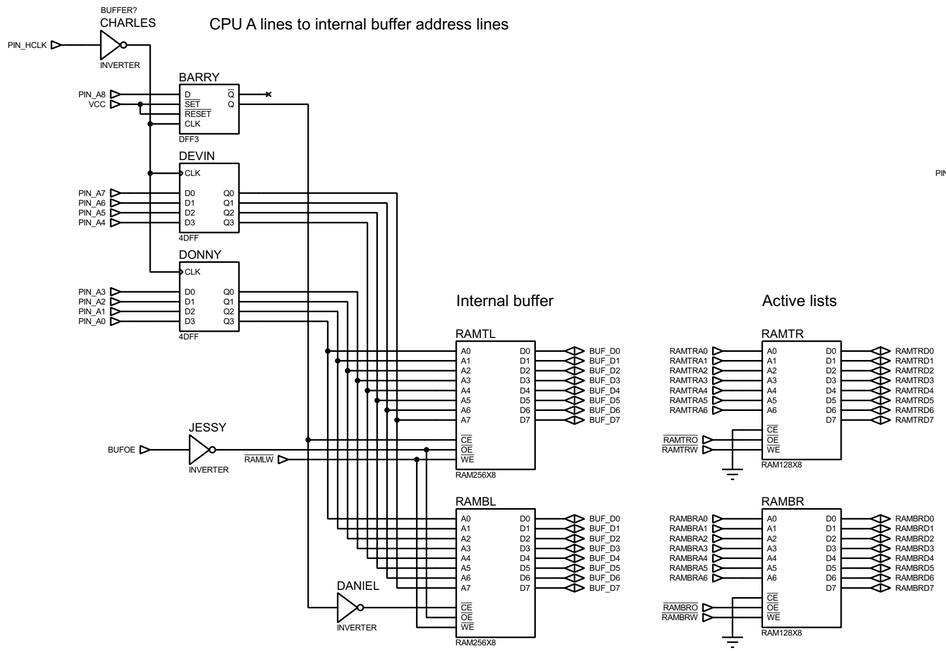
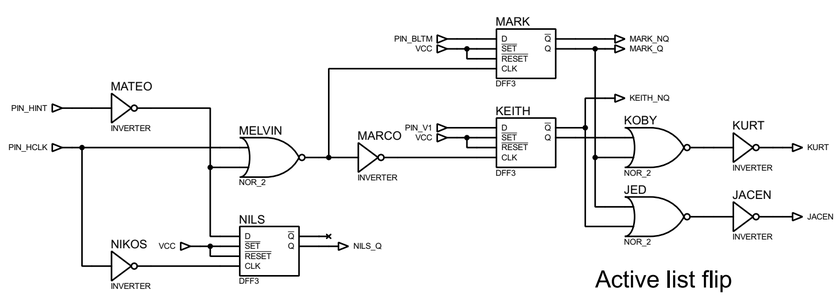
The internal buffer can hold 128 4-byte entries = 512 bytes
[0] is tile #
[1] is attributes (flags, palette...)
[2] is Y pos
[3] is X pos

The two smaller RAM blocks are the active sprite lists
When one is used for rendering, the other is filled

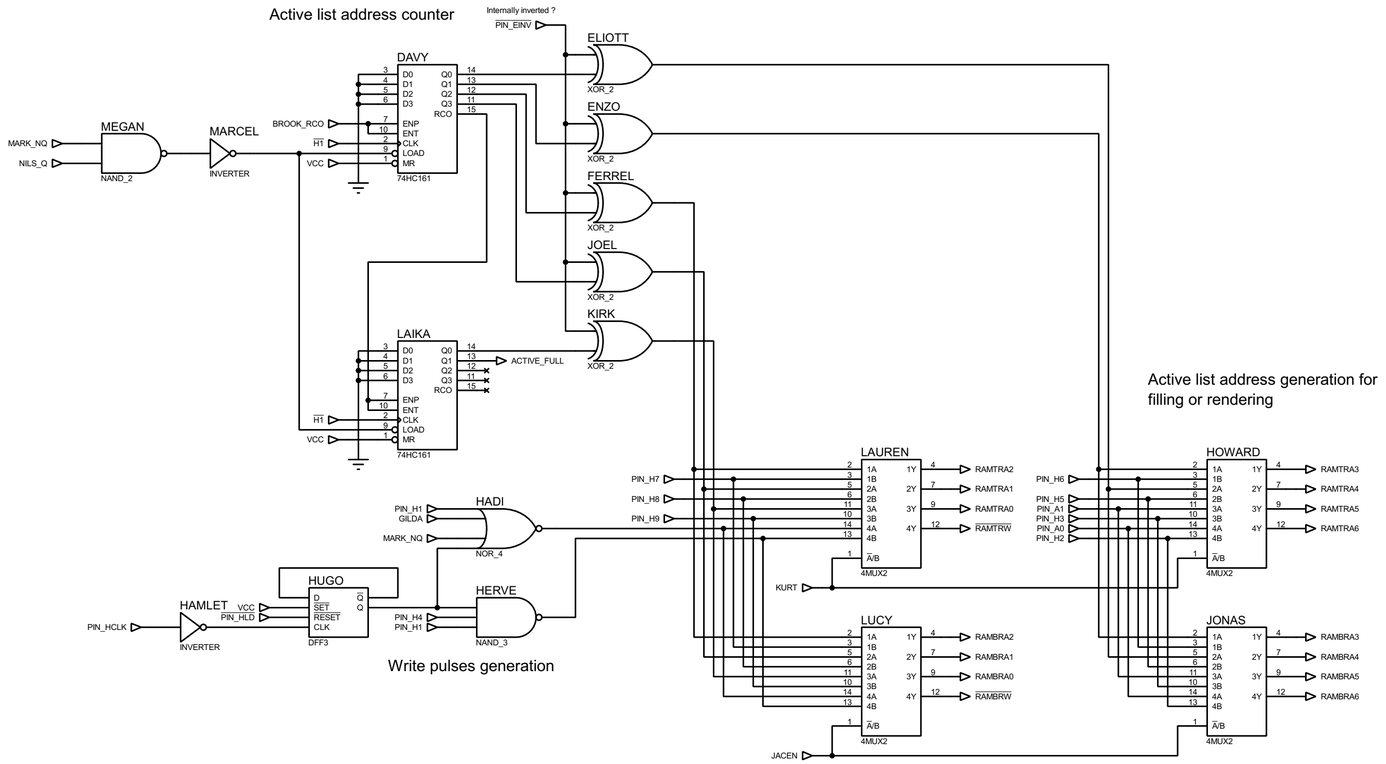
This chip DMAs the main work RAM to its internal buffer once per frame, and does Y matching to build active sprite lists each scanline.

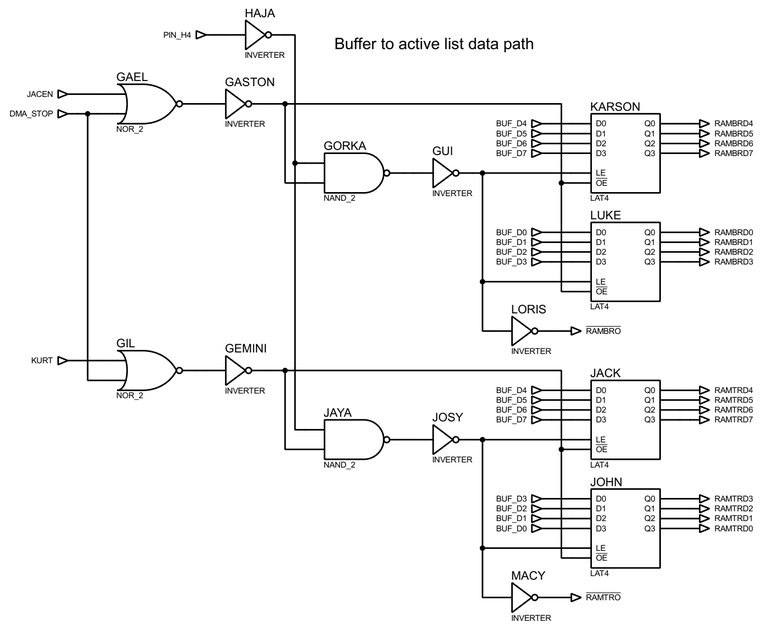
During rendering, the tile #, attributes and X pos bytes are output all at the same time (pipelines are used) for the external circuitry to fill the line buffers with the right pixels.





Active list flip

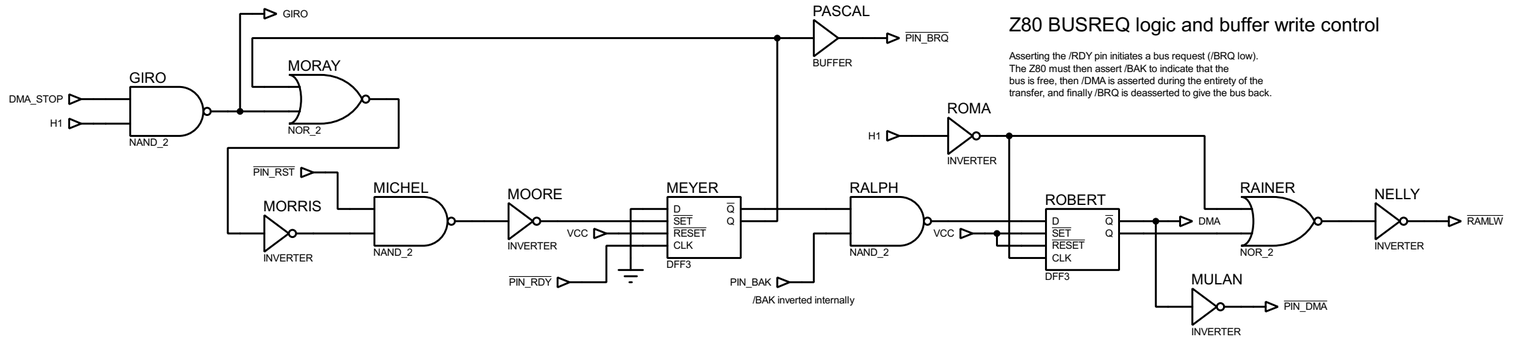


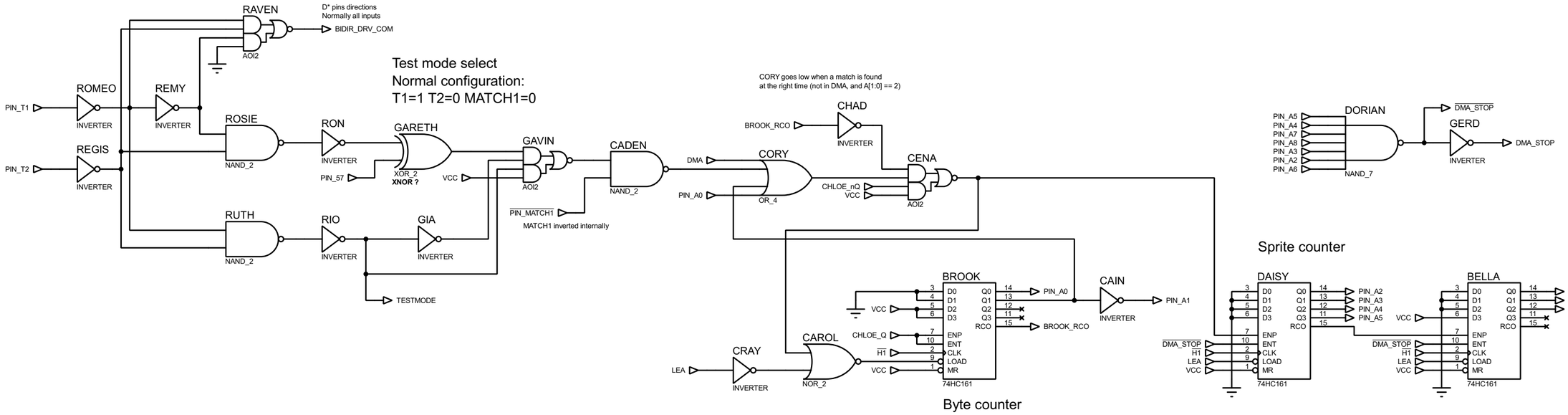


TITLE: Capcom 86S105 INTERNAL MEMORY	DATE: 21/11/2023
BY: Sean Gonsalves REV: @REV	PAGE: 2/4

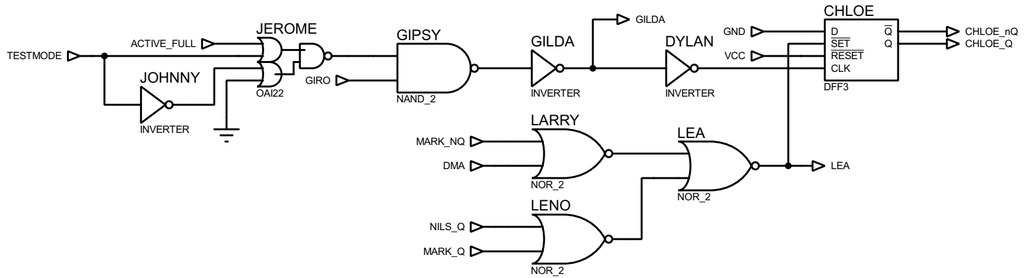
Z80 BUSREQ logic and buffer write control

Asserting the /RDY pin initiates a bus request (/BRQ low).
The Z80 must then assert /BAK to indicate that the
bus is free, then /DMA is asserted during the entirety of the
transfer, and finally /BRQ is deasserted to give the bus back.

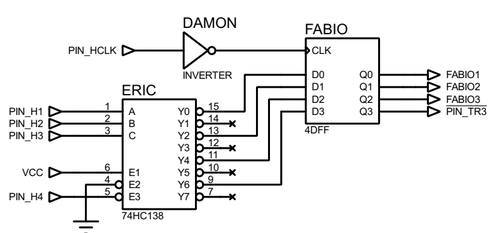




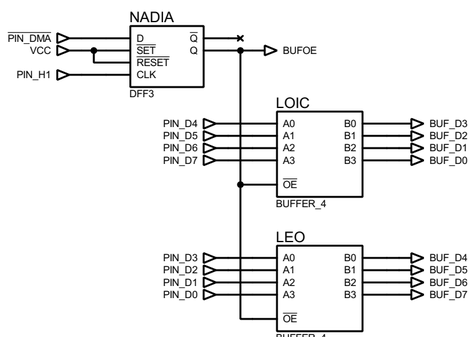
Buffer to active list copy sequencing



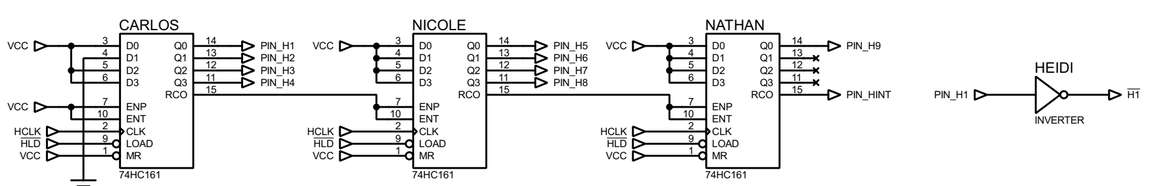
Final output sequencer



DMA Z80 data bus to internal buffer RAM

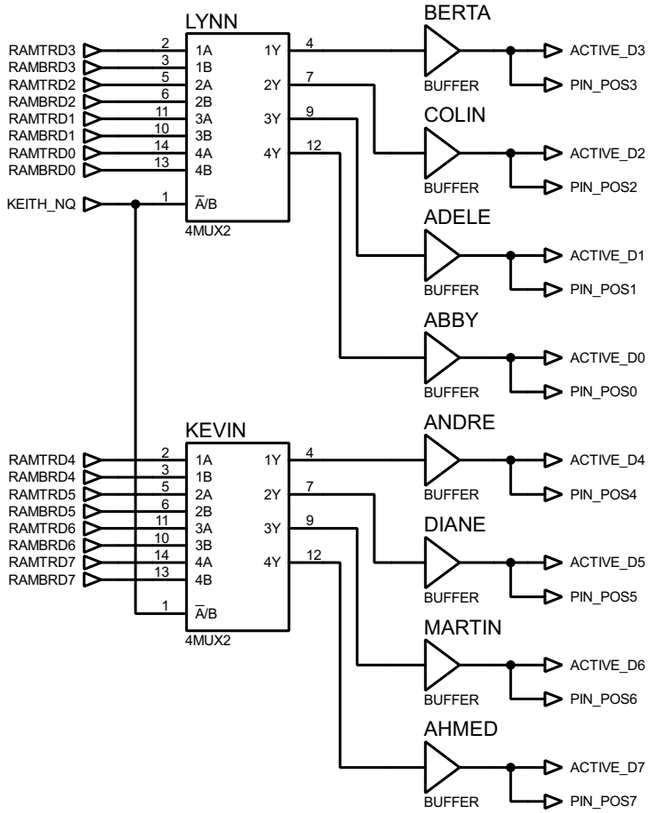


Internal horizontal counter

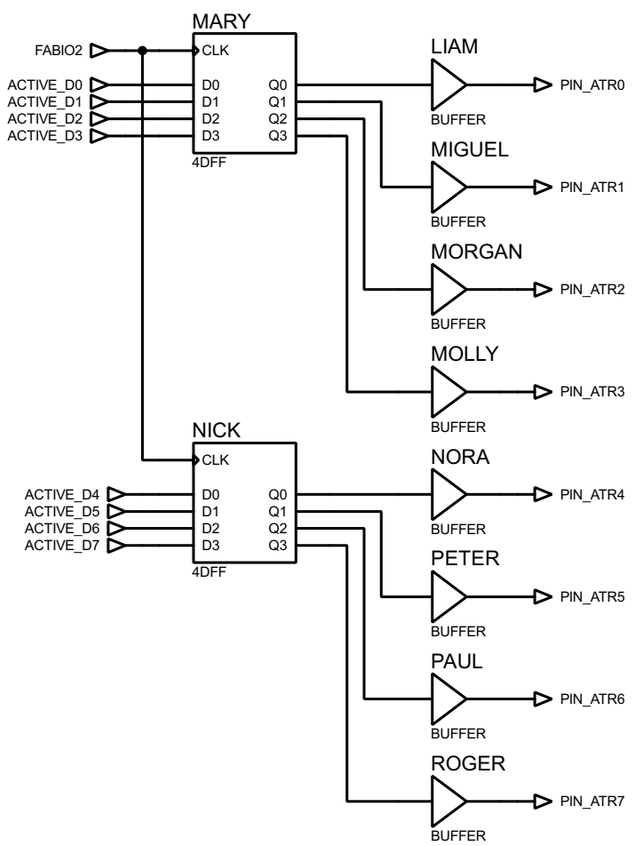


TITLE: Capcom 86S105 SEQUENCING	DATE: 21/11/2023
BY: Sean Gonsalves REV: @REV	PAGE: 3/4

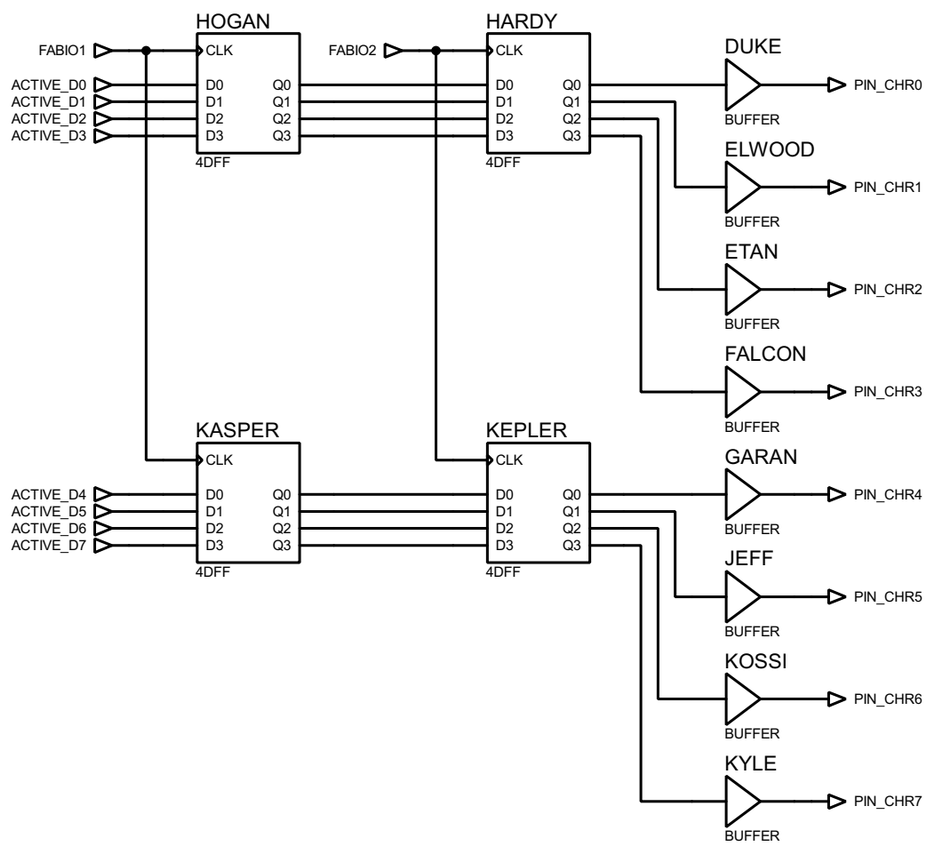
Active list selection for rendering
and x position byte output to POS pins



Active list attribute byte to ATR pins delay x1



Active list tile # byte to CHR pins delay x2



TITLE: Capcom 86S105 FINAL OUTPUTS	DATE: 21/11/2023
BY: Sean Gonsalves REV: @REV	PAGE: 4/4