Modeling and Optimization of a Solar Energy Harvester System for Self-Powered Wireless Sensor Networks

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***Abstract*—In this paper, we propose a methodology for optimizing a solar harvester with maximum power point tracking for self-powered wireless sensor network (WSN) nodes. We focus on maximizing the harvester's efficiency in transferring energy from the solar panel to the energy storing device. A photovoltaic panel analytical model, based on a simplified parameter extraction procedure, is adopted. This model predicts the instantaneous power collected by the panel helping the harvester design and optimization procedure. Moreover, a detailed modeling of the harvester is proposed to understand basic harvester behavior and optimize the circuit. Experimental results based on the presented design guidelines demonstrate the effectiveness of the adopted methodology. This design procedure helps in boosting efficiency, allowing to reach a maximum efficiency of 85% with discrete components. The application field of this circuit is not limited to self-powered WSN nodes; it can easily be extended in embedded portable applications to extend the battery life.**

***Index Terms*—Maximum power point tracking (MPPT), modeling and optimization, PSpice simulations, solar harvester.**

I. Introduction

THE DEVELOPMENT of perpetually powered systems avoiding periodical battery replacement and/or recharge is one of the ultimate goals in sensor network design. Indeed, even if advances in low-power design can help extend the battery lifetime, the amount of energy provided by storage devices still constrains the autonomy of distributed embedded systems, such as wireless sensor networks (WSNs).

Maximum power point tracking (MPPT) techniques are very common in the world of large-scale solar cells. The extra energy that is consumed by the maximum power point (MPP) tracker is easily offset by the much higher amount of energy that can be harvested from the environment. Sensor nodes are often required to be small, and therefore, they are powered by small solar cells that generate limited energy. For those cells, the gain in input energy is not always higher than the additional losses that are caused by the MPP tracking operation. The energy consumption and efficiency of the MPP tracker are, therefore, very important design criteria in energy scavengers for sensor nodes. The optimization of the energy harvesting process under varying light irradiance conditions is certainly one of the major design challenges. In particular, maximizing harvester circuit efficiency becomes fundamental at low light irradiance.

The photovoltaic (PV) harvesting circuits proposed for WSN applications adopt different solutions [1]–[5]. In [1] and [2], the direct connection between the PV panel and the energy storage element, i.e., a supercapacitor (SC), does not implement MPPT strategies, forcing the PV operating point to the SC voltage V_{SC}. On the contrary, the *Everlast* harvester system exploits a microcontroller to track MPP under varying light conditions [5]. Unfortunately, they do not use circuit simulations to optimize system design and to improve harvester circuit efficiency.

The definition of a clear design flow is fundamental to develop circuit solutions with optimized efficiency and better performances. This requires circuit simulations of the complete solar harvester system, which have been proposed for large-scale PV systems [6]–[8], [16]–[18], but are also highly desirable for low-power harvester circuits for WSNs.

To obtain representative simulations, accurate models should be developed. Therefore, the validation of an accurate compact model of the nonlinear I–V characteristics of PV modules is essential to design efficient photovoltaic harvester systems. In this scenario, this paper presents a compact model for the PV module, allowing to reproduce its I–V characteristics without numerical approaches typically adopted [9]–[11]. This permits to improve the design process of the dc–dc converter at the solar harvester input stage, typically required to match the PV module input impedance and according to SC voltage limits. Simplified models of the dc–dc converter and MPPT analog circuits are fundamental to improve system performances and to reduce the system design time. Using the models and the methodology described in this paper, we optimize a solar harvester operating under different light irradiance conditions.

This paper is organized as follows. Section II provides a brief overview on the circuit architecture and MPPT technique

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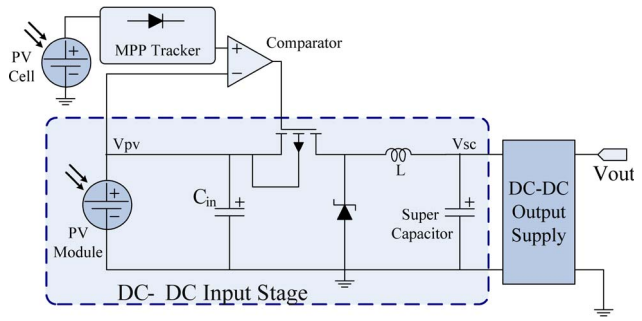

Fig. 1. Schematic diagram of the solar harvester.

adopted. Sections III and IV describe models of the PV module and the harvester circuit, respectively. Section V describes the circuit optimization methodology and provides some useful guidelines for solar harvester design. Section VI presents experimental results and a comparison between two different solar harvester circuit implementations designed following the proposed guidelines. Finally, Section VII concludes this paper.

II. Solar Harvesting Circuit

A. Circuit Architecture

The circuit architecture of the developed solar harvester is presented in [12] and depicted in Fig. 1. It consists of three main building blocks.

1) DC–DC Input Stage: Most of the MPPT systems proposed in the literature employ standard switch-mode power supply technologies, with switching transistors, diodes, and capacitors. They are driven by a pulsewidth-modulated (PWM) signal generated by a control algorithm. The three basic topologies are buck (step down), boost (step up), and buck–boost (step up–down). In this implementation, a buck topology is used to interface the voltage from the PV module to the SC. The operation of the input dc–dc stage differs from the one of a standard buck converter because input and output voltages do vary during the SC charge process, as well as duty cycle, period, and switching frequency of the MOSFET switch.

2) MPP Tracker: The MPP tracking is implemented by the analog circuit highlighted in Fig. 1. It autonomously estimates the MPP using an open-loop configuration without any interference to the PV module. This way, the control unit is simply implemented with a single low-power comparator that compares the current PV module voltage to the estimated MPP to generate the PWM control signal. No costly DSP or digital controllers are necessary. The details of the generation of the estimated MPP have been left out of the figure for the sake of simplicity. The PWM control signal forces the pseudo-buck dc–dc input stage to work within a narrow voltage window centered on the MPP voltage V_{mpp}.

3) Output DC–DC Converter: The output dc–dc converter delivering power supply to the wireless sensor node is required to match the input voltage of the WSN node. This component is not taken into account in this paper, because it needs custom design related to the operating voltage of the WSN node adopted. Moreover, commercial integrated dc–dc converters usually provide an efficiency on the order of 90%.

TABLE I
MPP Voltages Measured and Calculated Through (1) Considering $K_{\mathrm{FOC}} = 0.74$ on a Wide Range of Light Conditions

S [W/m^2]	$V_{mpp,cal}$ [V]	$V_{mpp,\,meas}$ [V]	Err [%]
20	2.38	2.29	+4.0
40	2.67	2.69	–0.7
60	2.82	2.92	–3.4
80	2.94	3.08	–4.5
100	3.00	3.12	–3.9
200	3.01	3.17	–4.6
400	3.14	3.19	–1.6
600	3.15	3.24	–2.9
800	3.16	3.27	–3.2
1000 (STC)	3.18	3.29	–3.3

The power supply for the harvester circuit is provided by both the PV module and the output dc–dc power supply. This design choice allows to improve the efficiency during the initial phase of SC charging and enables the harvester circuit to start operating when the SC voltage is low. For efficient harvester operation, the MPP should continuously be tracked; hence, the input stage and the comparator should also be powered when the output dc–dc converter is off because the SC voltage is below the start-up threshold. For this reason, the power supply to the input MPPT stage is provided by the PV panel even when the dc–dc converter is not operating.

B. MPPT Technique

There are several methods and algorithms to track the MPP voltage [13]–[15]. The most popular ones are Perturb and Observe (P&O) [13], [19] and Fractional Open-Circuit Voltage (FOCV) [14], which is the one we adopted.

The P&O method is an approach that is widely used with medium–high power PV modules, since it allows very accurate MPP calculation. However, it requires complex control actions that are often implemented using microcontrollers or DSPs. Although analog versions are implemented, the main shortcoming of this method is the high cost and complexity of the system.

On the other hand, FOCV is largely used in small-scale PV systems. This method exploits the nearly linear relationship between the operating voltage at MPP V_{mpp} of a PV module and its open-circuit voltage V_{OC}, i.e.,

$$V_{\mathrm{mpp}} \cong K_{\mathrm{FOC}} \cdot V_{\mathrm{OC}}. \tag{1}$$

K_{FOC} is a constant that ranges from 0.71 to 0.78, which slightly depends on irradiance conditions [1]. Considering K_{FOC} as a constant under different irradiance conditions leads to small errors in the V_{mpp} evaluation but strongly simplifies circuit solutions adopted to implement MPPT, also reducing its power consumption. Table I reports that the maximum difference between MPP voltages measured during PV panel characterization $(V_{\mathrm{mpp,meas}})$ and calculated through (1) assuming $K_{\mathrm{FOC}} = 0.74(V_{\mathrm{mpp,cal}})$ [12] is smaller than 5% on a wide range of light irradiance conditions.

V_{OC} of small-size solar cells can be estimated by exploiting sensing devices that autonomously monitor the environmental light, such as light intensity sensors, voltage output sensors

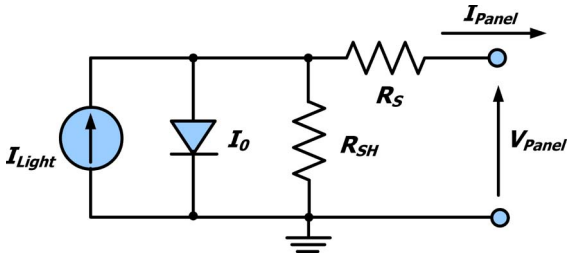

Fig. 2. Equivalent circuit of the PV cell representing the model parameters and the cell output.

[20], or additional single PV modules [12], manufactured using the same technology of the main PV module array. The last one is the solution we adopted in our system.

III. Photovoltaic Cell Modeling

Compact models capable of accurately reproducing the electrical behavior of solar cells are essential to develop and optimize harvester systems through circuit simulations. PV modules are manufactured using different technologies (monocrystalline silicon, polycrystalline, and amorphous silicon) and exhibit different current–voltage characteristics. Furthermore, manufacturers do not provide SPICE-like models of their PV modules, but only a few electrical parameters such as the open-circuit voltage ($V_{\rm OC}$), the short-circuit current ($I_{\rm SC}$), the MPP voltage ($V_{\rm mpp}$) and current ($I_{\rm mpp}$), and the temperature drift coefficients at open-circuit voltage and short-circuit current ($\beta_{V_{\rm OC}}$ and $\alpha_{I_{\rm SC}}$, respectively). These values are usually provided in Standard Test Conditions (STC), i.e., when the irradiance is 1000 W/m^2 and the panel temperature (T_C) is 25 °C. These conditions provide the highest output power, and they are rarely experienced in real environments. Further, the output power delivered by a PV module strongly depends on irradiance, cell temperature, solar incidence angle, and load resistance.

Targeting the harvester for specific environmental conditions requires predicting the available power in a more accurate way, granting a reliable circuit design. For these reasons, an accurate, reliable, and easy way to use model that describes the electrical behavior of PV modules is very attractive for solar harvester designers.

Generally, the PV panel can be modeled using the equivalent circuit shown in Fig. 2 [9]–[11]. This lumped circuit includes a current generator providing the short-circuit current ($I_{\rm Light}$), which is a function of the solar irradiation, a diode to account for the typical knee of the current–voltage curve through the reverse saturation current (I_0), a series resistor (R_S), and a shunt resistor ($R_{\rm SH}$), emulating intrinsic losses depending on PV cell series and parallel connections. The PV module current at a given cell temperature and solar irradiance is given by

$$I_{\rm panel} = I_{\rm Light} - I_0\left(e^{\frac{V_{\rm panel}+I_{\rm panel}R_S}{a}} - 1\right) - \frac{V_{\rm panel}+I_{\rm panel}R_S}{R_{\rm SH}}. \quad (2)$$

a is the modified panel ideal factor defined by

$$a \equiv \frac{N_S \gamma k T_C}{q}. \quad (3)$$

q is the electron charge, k is Boltzmann's constant, γ is the usual PV single-cell ideal factor (typically ranging between 1 and 2), N_S is the number of cells in series, and T_C is the PV panel temperature [9]. The model parameters are extracted over a wide range of irradiance conditions by adopting the simplified procedure briefly described in the following [12].

The technology-dependent parameters, i.e., R_S and $R_{\rm SH}$, do not depend on irradiance, and they are determined from experimental current–voltage curves. Other parameters depending on irradiance and temperature are derived from PV module intrinsic relations [12].

Assuming that the short-circuit current is equal to $I_{\rm Light}$ [6], it depends on the open-circuit voltage in a simple way, i.e.,

$$I_{\rm SC} = I_0\left(e^{\frac{q\cdot V_{\rm OC}}{k\cdot T_C}} - 1\right) + \frac{V_{\rm OC}}{R_{\rm SH}}. \quad (4)$$

Since the ratio between $V_{\rm OC}$ and $R_{\rm SH}$ is typically negligible, $V_{\rm OC}$ can be derived from the diode saturation current as

$$V_{\rm OC} = \left(\frac{k\cdot T_C}{q}\right)\ln\left(\frac{I_{\rm SC}}{I_0}+1\right). \quad (5)$$

I_0 and $I_{\rm Light}$ depend on irradiance and temperature as [2], [9]

$$I_0 = I_{0,\rm STC}\left(\frac{T_C}{T_{\rm ref}}\right)^3 e^{\left(\frac{q\cdot E_G}{k\cdot T_C}\right)\left(\frac{1}{T_{\rm ref}}-\frac{1}{T_C}\right)} \quad (6)$$

$$I_{\rm Light} = I_{\rm Light,STC}S + \alpha_{I_{\rm SC}}\left(\frac{1}{T_{\rm ref}} - \frac{1}{T_C}\right). \quad (7)$$

S is the solar irradiance expressed in W/m^2 [K]. $I_{0,\rm STC}$, which is the diode saturation current in STC, is extracted from (4), imposing STC. $I_{\rm Light,STC}$ is determined by considering that, at zero output voltage, $I_{\rm Light}$ is equal to the short-circuit current.

Once the parameters have been extracted, the model is verified by comparing simulations to measurements under varying irradiance conditions, performed by a characterization setup based on a halogen light source. The overheating and thermal drift phenomena induced by the halogen light source on the PV module have been taken into account by exploiting the thermal drift coefficients ($\beta_{V_{\rm OC}}$ and $\alpha_{I_{\rm SC}}$) to scale all curves to the equivalent temperature of 25 °C. Fig. 3 shows I–V measurements and simulations of real panel under low irradiance conditions. As shown, the agreement between measurements and simulations demonstrates the accuracy of the model under different irradiance conditions.

Fig. 4 shows the output power delivered by the PV panel in the same conditions, and the MPPT hysteresis window centered on the estimated $V_{\rm mpp}$ for maximum light irradiance, allowing to keep the PV module voltage locked to the MPP voltage. The MPP tracker voltage hysteresis, which has a constant amplitude, instantaneously follows (i.e., is centered on) the optimum MPP voltage under varying light irradiance conditions.

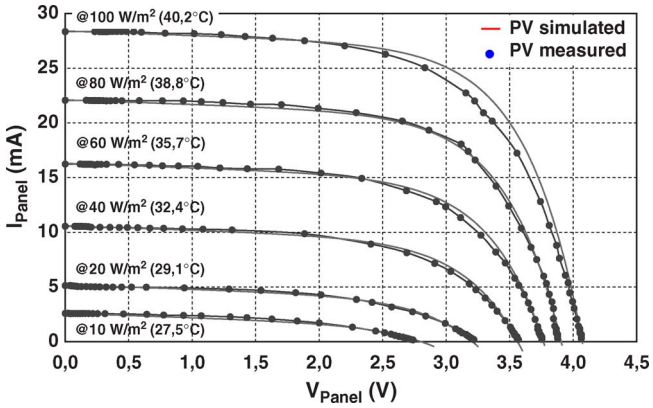

Fig. 3. Comparison of PV panel PSpice model output current with measured output current under low irradiance conditions (from 10 to 100 W/m^2).

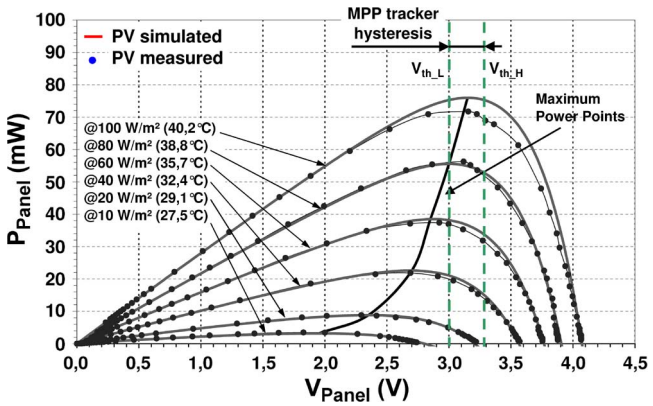

Fig. 4. Measurements and simulations of PV module output power under low irradiance conditions are shown with the MPP voltage curve. MPP tracker hysteresis window centered on $V_{\rm mpp}$ is depicted at 100 W/m^2.

IV. Harvester Circuit Modeling

In order to optimize the solar harvester design, a simplified model of the pseudo-buck dc–dc input stage is needed to analyze its electrical behavior and to maximize the circuit efficiency.

In steady-state conditions, the PV module works in a quite narrow voltage window centered at $V_{\rm mpp}$, which depends on the comparator hysteresis. Hence, to simplify the circuit model, it is convenient to linearize the electric behavior of the PV module around $V_{\rm mpp}$, thus avoiding more complex and less intuitive formulas. We have

$$v_{\rm pv}(t) = V_{\rm mpp} - R_{\rm mpp}\left(i_{\rm pv}(t) - I_{\rm mpp}\right) \tag{8}$$

$$i_{\rm pv}(t) = I_{\rm mpp} - \frac{v_{\rm pv}(t) - V_{\rm mpp}}{R_{\rm mpp}}. \tag{9}$$

$v_{\rm pv}(t)$ and $i_{\rm pv}(t)$ are the instantaneous values of voltage and current of the PV module, respectively. $R_{\rm mpp}$ is defined as $V_{\rm mpp}/I_{\rm mpp}$.

To optimize the dc–dc input stage efficiency, we adopted the simplified model shown in Fig. 5(a), which is derived assuming that the power consumption of the analog MPPT circuit driving the MOSFET switch is negligible. In the circuit depicted in Fig. 5(a), the switch modeling the MOSFET, the diode and

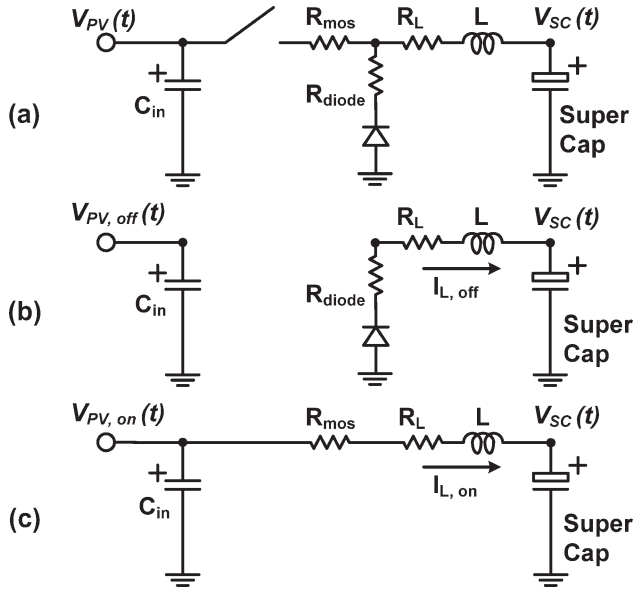

Fig. 5. (a) Equivalent simplified circuit used for the buck analysis. (b) Equivalent circuit in OFF-state condition. (c) Equivalent circuit in ON-state condition.

passives are ideal. The parasitics of real circuit components are included by proper resistances, which are crucial elements to be accounted for to maximize the circuit efficiency. Under typical operating conditions, we verified that the power loss is mostly due to the power dissipated in the inductor (R_L), whereas the MOSFET on-resistance $(R_{\rm mos})$ and the diode $(R_{\rm diode})$ parasitic resistances lead to relatively negligible power losses.

We simplified the circuit analysis separately considering the cases when the MOSFET switch is on and off, respectively.

1) Switch Off: The MOSFET switch remains off at the time that the input capacitor $C_{\rm in}$ is charged from the lower threshold voltage $V_{\rm th\_L}$ to the upper one $V_{\rm th\_H}$. The simplified circuit schematic is shown in Fig. 5(b), and the circuit is modeled by the following differential equation:

$$R_{\rm mpp}C_{\rm in}\frac{dv_{\rm PV}(t)}{dt} + v_{\rm PV}(t) = R_{\rm mpp}I_{\rm mpp} + V_{\rm mpp}. \tag{10}$$

The time the switch is off is derived by solving (10) with the following boundary conditions $v_{\rm PV}(0) = V_{\rm th\_L}$ and $v_{\rm PV}(t_{\rm off}) = V_{\rm th\_H}$, i.e.,

$$t_{\rm off} = R_{\rm mpp}C_{\rm in}\ln\left(\frac{V_{\rm mpp} + R_{\rm mpp}I_{\rm mpp} - V_{\rm th\_L}}{V_{\rm mpp} + R_{\rm mpp}I_{\rm mpp} - V_{\rm th\_H}}\right). \tag{11}$$

The current flowing on the inductor and the parasitic resistances R_L and $R_{\rm diode}$ is given by

$$i_{L,\rm off}(t, V_{\rm SC}) = k_1 \cdot e^{-\frac{R_L + R_{\rm diode}}{L}t} - \frac{V_{\rm SC} + V_D}{R_L + R_{\rm diode}} + k_2. \tag{12}$$

k_1 and k_2 are differential equation solution constants derived from boundary conditions. Once the OFF-state current is

calculated, the energy dissipated by inductor and diode parasitic resistances when the switch is off can easily be calculated as

$$E_{\mathrm{Loss,off}}(V_{\mathrm{SC}}) = \int_0^{t_{\mathrm{off}}} i_{L,\mathrm{off}}^2(t, V_{\mathrm{SC}}) \cdot (R_L + R_{\mathrm{diode}})dt. \quad (13)$$

This way, the impact of inductor and diode losses over the overall harvester efficiency can be estimated.

2) Switch On: The MOSFET switch remains on the time that the input voltage drops from $V_{\mathrm{th\_H}}$ to the lower threshold voltage $V_{\mathrm{th\_L}}$. When the switch is on, the energy stored in C_{in} and coming from the panel is transferred to the SC through the inductor. The electrical behavior of the harvester system can be analyzed using the following differential equation system, obtained by applying Kirchhoff's current and voltage laws to the simplified circuit shown in Fig. 5(c):

$$\begin{cases} v_{\mathrm{PV}}(t) = L\frac{di_L(t)}{dt} + (R_{\mathrm{mos}} + R_L)i_L(t) + V_{\mathrm{SC}} \\ i_L(t) = \frac{1}{L}\int v_{\mathrm{PV}}(t) - (R_{\mathrm{mos}} + R_L) \\ \qquad \times \left[i_{\mathrm{PV}}(t) - C_{\mathrm{in}}\frac{dv_{\mathrm{PV}}(t)}{dt}\right] - V_{\mathrm{SC}}dt \end{cases}. \quad (14)$$

The boundary conditions are $v_{\mathrm{PV}}(t_{\mathrm{off}}) = V_{\mathrm{th\_H}}$ and $v_{\mathrm{PV}}(t_{\mathrm{on}}) = V_{\mathrm{th\_L}}$. Because of its complexity, this system does not lead to an analytical solution for the ON-state time, which is numerically evaluated. As in the OFF-state, the power losses are due to the inductor current flowing through circuit parasitic resistances, i.e., R_L and R_{mos}. In (15) and (16), shown at the bottom of the next page, k_3, k_4, and k_5 are the differential equation solution constants derived from boundary conditions. Once the inductor current is determined, the energy dissipated across the MOSFET and inductor during the time the switch is on is easy to calculate, i.e.,

$$E_{\mathrm{Loss,on}}(V_{\mathrm{SC}}) = \int_{t_{\mathrm{off}}}^{t_{\mathrm{off}}+t_{\mathrm{on}}} i_{L,\mathrm{on}}^2(t, V_{\mathrm{SC}}) \cdot (R_L + R_{\mathrm{mos}})dt. \quad (17)$$

As in the OFF-state, the inductor parasitic resistance plays the most important role in determining the total power dissipation of the circuit.

3) Harvesting Efficiency: In order to calculate the system efficiency, the total energy collected from the PV module E_{PV} should be calculated as

$$E_{\mathrm{PV}} = \int_0^{t_{\mathrm{off}}+t_{\mathrm{on}}} v_{\mathrm{PV}}(t) \cdot \left[I_{\mathrm{mpp}} - \frac{v_{\mathrm{PV}}(t) - V_{\mathrm{mpp}}}{R_{\mathrm{mpp}}}\right] dt. \quad (18)$$

Then, the whole system efficiency is given by

$$\eta(V_{\mathrm{SC}}) = 1 - \frac{E_{\mathrm{Loss,Tot}}(V_{\mathrm{SC}})}{E_{\mathrm{PV}}} \quad (19)$$

where $E_{\mathrm{Loss,Tot}}$ is the sum of energies dissipated during the *switch-on* and *switch-off* times, respectively.

The efficiency is the figure of merit of this system, which allows analyzing the behavior of the solar harvester in a wide range of working conditions. E_{PV} is the input energy that can be collected from the environment during an input stage pseudo dc–dc period. On the contrary, $E_{\mathrm{Loss,Tot}}$ is strongly affected by harvester design choices and circuit implementations, which should be optimized to maximize the efficiency.

TABLE II
POWER LOSSES OF INPUT STAGE COMPONENTS, WITH DEPENDENCES AND EFFECTS

COMPONENT	DEPENDENCE ON	EFFECTS ON
Mosfet, diode	$i_{L,MAX}$, *freq*	*switching losses*
Comparator	*freq*	*power consumption*
Inductor	$i_{L,MAX}$	*conduction losses*
Input Capacitor	*maximum input ripple*	*freq*

V. DESIGN GUIDELINES FOR CIRCUIT OPTIMIZATION

The aim of the harvester circuit is to collect and store into the SC the maximum amount of energy from the environment; hence, the obvious design goal is to increase the circuit efficiency. In particular, we focused on the input stage, whereas we use an off-the-shelf dc–dc converter as the output load.

In this section, we provide some guidelines to optimize the design of a harvester circuit targeted to very-low-power applications. We developed two high-efficiency prototypes demonstrating the effectiveness of the guidelines we proposed.

Optimizing the harvester circuit efficiency requires an iterative process. Harvester efficiency is mainly affected by power losses due to parasitic resistance and switching of the MOSFET and diode to inductor resistance and to comparator power consumption. Generally, these power losses depend on the maximum inductor current $i_{L,\mathrm{MAX}}$ and the operating frequency $freq$ (see Table II). Unfortunately, $i_{L,\mathrm{MAX}}$ and $freq$ also depend on the inductance value and comparator hysteresis, respectively. Thus, the optimum design requires an iterative procedure to select the component values that maximize the circuit efficiency. In the following, we discuss tradeoffs and considerations about component selection.

MOSFET and Diode: The choice of MOSFET and diode has to be performed both to assure reliability operations and to minimize power losses. Reliability constraints force the adoption of MOSFETs and diodes that can safely hold the maximum current, thus fixing their maximum current $I_{\mathrm{DS,MAX}}$. Maximizing the efficiency requires that the MOSFET is selected to simultaneously minimize power losses due to both parasitic resistance, which decreases with $I_{\mathrm{DS,MAX}}$, and switching actions, which depend on the frequency and MOSFET parasitic capacitance, typically increasing with $I_{\mathrm{DS,MAX}}$. This is the typical tradeoff involved in the MOSFET choice. Furthermore, selecting a device with low parasitic capacitance allows to reduce the MOSFET turn-on and turn-off delay, improving the circuit response to the highest frequency. Considering the relatively low frequency of the harvester circuit (up to some hundreds of kilohertz), the switching losses, which we have quantified in Section VI, have a smaller contribution compared to power losses due to parasitic resistance and inductor. Thus, a careful choice of MOSFET and diode should principally be driven in the direction of minimizing both parasitic components. This, in turn, confirms the hypothesis assumed in Section IV.

Comparator: The selection of the comparator implementing the analog MPPT algorithm can be performed considering the

following two options: 1) an ultralow-power (ULP) comparator, dissipating some microwatts and operating up to some tens of kilohertz, and 2) a high-speed (HS) comparator, whose power consumption and maximum frequency are around a few milliwatts and some hundreds of kilohertz, respectively. Despite the higher consumption of the HS comparator, its power dissipation is negligible compared to the total power supplied by the PV module at maximum irradiance conditions, which is ∼500 mW. This justifies the hypothesis assumed in the previous section, i.e., to neglect it when calculating the whole system efficiency. Thus, operating at high frequencies is beneficial for the system efficiency with maximum light irradiance, and an HS comparator can be adopted without significant penalties due to its higher power consumption. Moreover, working at higher efficiency at maximum light conditions allows to collect a greater amount of power considering the energy available during the day, considerably improving the whole system efficiency. On the contrary, the adoption of a ULP comparator becomes more and more convenient with decreasing light irradiance. In fact, the comparator power consumption much more reduces the whole efficiency as the energy collected by the PV module decreases. Therefore, adopting a ULP comparator is beneficial in poor light irradiance. In this regard, it is very important for a proper design to analyze the environment where the harvester will be deployed and to check that the penalty due to the higher power consumption of HS configuration is offset by the efficiency improvement due to higher operating frequencies. In our case, the increment of power consumption using the HS comparator is negligible, confirming the hypothesis assumed in Section IV.

Inductor: Reducing the inductor power loss is key to improving the efficiency. Interestingly, the inductance depends on the maximum current, which must safely be tolerated to prevent component rupture. In order to minimize the inductor power dissipation, small inductors have to be considered since their parasitic resistance is approximately proportional to their value. Unfortunately, reducing the inductance increases the maximum inductor current. Therefore, it is very important for a reliable operation to verify that the maximum current does not exceed the upper limits imposed by inductor specifications, particularly when considering small inductors, desirable also for the small area occupation required for wireless sensor node applications. To reduce the maximum current, the operation frequency should be increased by lowering $C_{\rm in}$, demanding faster comparators. In particular, when the switching frequency exceeds some tens of kilohertz, the HS comparators have to be considered instead of the ULP ones.

Input Capacitor: As shown in Fig. 6, the lowest $C_{\rm in}$ leads to the highest harvester efficiency, whereas the inductor effects are

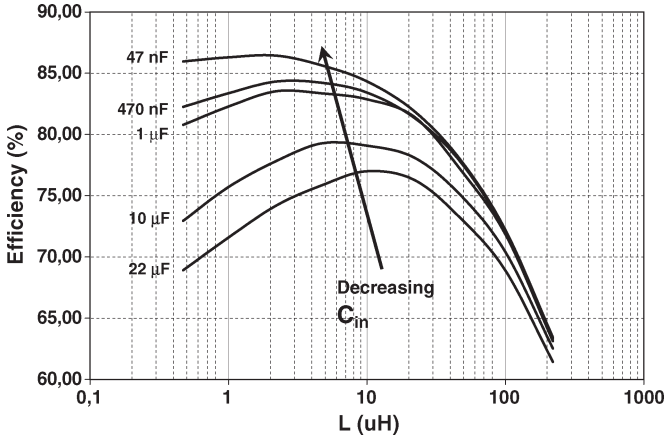

Fig. 6. Variation of efficiency for different values of inductor (L) and input capacitor $(C_{\rm in})$ with SC fully charged.

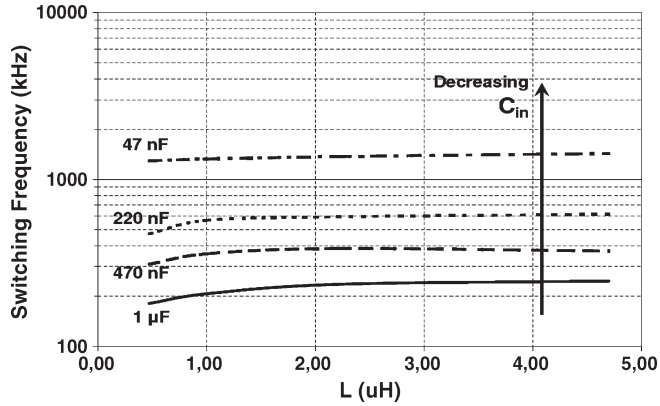

Fig. 7. Variations of circuit switching frequency for different values of inductor (L) and input capacitor $(C_{\rm in})$.

relatively small, particularly when low L values are considered. Reducing $C_{\rm in}$ increases the switching frequency, see Fig. 7.

Moreover, reducing $C_{\rm in}$ decreases the maximum inductor current, which has not to exceed the upper limit due to MOSFET, diode, and inductor specifications, as shown in Fig. 8. The switching frequency is approximately independent of L, whereas it noticeably depends on $C_{\rm in}$ as $t_{\rm off}$ proportionally decreases to $C_{\rm in}$, see (11).

Thus, once selected, the desired configuration (e.g., ULP or HS) $C_{\rm in}$ should be kept as small as possible according to the determined range of operating frequency.

Comparator Hysteresis: Since $t_{\rm on}$ depends only on the comparator voltage hysteresis, $V_{\rm th\_H} - V_{\rm th\_L}$ is crucial for the optimization of the input stage, and it results from a tradeoff between two opposite needs. A smaller voltage hysteresis is better sustainable using the HS configuration, and it is certainly

$$i_{L,\rm on}(t,V_{\rm SC}) = \frac{C_{\rm in}}{2Lb_1} e^{-\frac{[L+(R_{\rm mos}+R_L)b_1+b_2]}{2Lb_1}t} \left\{ k_3\left[b_2 - L + (R_{\rm mos}+R_L)b_1\right] - k_4\left[b_2 + L - (R_{\rm mos}+R_L)b_1\right] e^{\frac{b_2}{Lb_1}t} \right\} + k_5 \quad (15)$$

$$\begin{cases} b_1 = \tau_{\rm in} = C_{\rm in}\cdot R_{\rm mpp} \\ b_2 = \sqrt{L^2 + (C_{\rm in}R_{\rm mpp}(R_L+R_{\rm mos}))^2 - 2LC_{\rm in}R_{\rm mpp}(R_L+R_{\rm mos}+2R_{\rm mpp})} \end{cases} \quad (16)$$

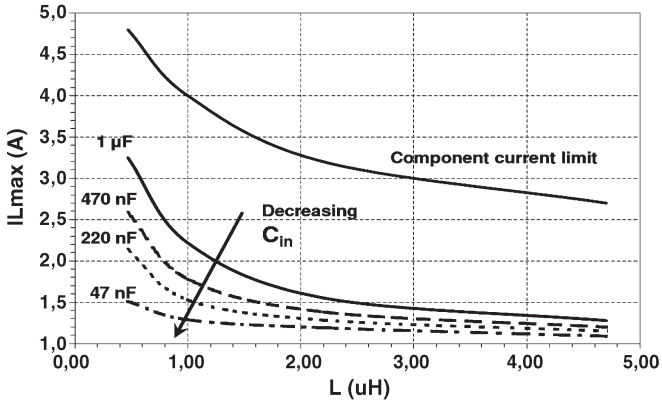

Fig. 8. Maximum current through L, MOS, and diode in solar harvester design with HS comparator. Variations using different values of inductor (L) and input capacitor ($C_{\rm in}$).

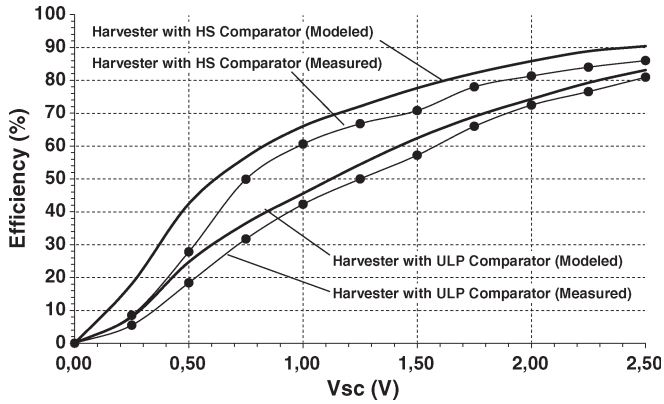

Fig. 9. Efficiency comparison between solar harvester with HS comparator (measured versus modeled) and solar harvester with ULP comparator (measured versus modeled).

beneficial for the efficiency, as the switching frequency is higher and the PV module is forced to operate more closely to the MPP voltage. Unfortunately, with smaller hysteresis, it is difficult for the PV module voltage to follow $V_{\rm mpp}$ when light irradiance conditions rapidly change. In this case, the width of the voltage hysteresis window should be proportional to the $V_{\rm mpp}$ variation range for proper system operation, see Fig. 4. On the contrary, a larger voltage hysteresis allows $v_{\rm PV}(t)$ to keep locked to the estimated $V_{\rm mpp}$ more easily, but the larger PV panel voltage variations and the lower frequency lead to a penalty in the whole system efficiency. The optimum choice of the hysteresis involves a tradeoff between these opposite needs, and a proper design must take into consideration the light irradiance conditions in the deploying environment.

VI. Experimental Results

To validate the proposed methodology, we designed and implemented two harvester circuits following the described guidelines. The first one uses a ULP comparator, $C_{\rm in} = 1.0\ \mu$F and $L = 4.7\ \mu$H, reaching ~60-kHz switching frequency. The second one uses an HS comparator, $C_{\rm in} = 220$ nF and $L = 1.0\ \mu$H, working at a frequency ~300 kHz. Both implementations use the same PV module and the same PV pilot cell implemented with commercial polycrystalline silicon technology.

Several experiments have been performed under different light irradiance conditions. The harvester circuit efficiency obtained from measurements has been compared to simulation results derived from the simplified model described in Section IV. Fig. 9 shows the results obtained with a light irradiance ~700 W/m^2 that forces the PV module to provide ~400 mW. Both harvester circuit prototypes show excellent efficiency performances, particularly if compared to the implementation presented in [12], achieving ~70% efficiency with a ULP comparator when the SC is completely charged, e.g., $V_{\rm SC} = 2.5$ V. Prototypes employing ULP and HS comparators show ~80% and ~85% efficiencies, remarkably outperforming previous results and demonstrating the effectiveness of this design methodology. Moreover, the SC charging time reduces by ~19% and ~11% compared to previous results [12] with HS and ULP comparator implementation, respectively.

Furthermore, Fig. 9 demonstrates that the power losses due to the MOSFET switching at high frequency is negligible provided that MOS and diodes are carefully selected, as outlined in Section V. In fact, a convenient choice of the MOS allows keeping the efficiency reduction due to MOS and diode switching losses below 5% and 2% with HS and ULP comparator implementations, respectively.

VII. Conclusion

In this paper, we have presented an optimization methodology allowing maximizing the efficiency of solar harvester for self-powered WSN devices. This methodology relies on compact models of both the PV module and the harvesting circuit, which implements an analog MPPT technique already proposed in the literature. The model of the PV module is discussed in detail, and a simplified parameter extraction procedure is proposed.

Useful guidelines are presented to optimize the harvester circuit design, which allow to significantly improve the whole harvester efficiency, which is crucial in WSN applications. Noticeably, the harvester implemented using commercial components features a high efficiency (85%), which to our knowledge is the highest ever reported in the literature.

It is worth noting that this methodology is not limited to self-powered WSN nodes; it can easily be applied to embedded systems to extend the battery lifetime, and it can also be used to optimize the design of harvesting ICs. The final goal of this paper will be the implementation of an IC harvester able to efficiently work on a wide range of light conditions. For this reason, design information about the needed passive components is a key aspect, because a tradeoff between harvester performances and physical implementation will be needed to keep the silicon costs below a bearable threshold.

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