國 立 成 功 大 學

電 機 工 程 學 系

碩 士 論 文

以類比積體電路實現太陽能最大發電功率追蹤器

Analog Integrated Circuit Realization for Maximum Power Point Tracking of Solar Energy Systems

研究生：李貞慶

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中華民國九十八年十一月

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Analog Integrated Circuit Realization for Maximum Power Point Tracking of Solar Energy Systems

by

Jen-Ching Lee

A thesis submitted to the graduate division in partial fulfillment of the requirement for the degree of Master Science

at

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以類比積體電路實現太陽能
最大發電功率追蹤器

李貞慶*　郭泰豪**　郭永超**

國立成功大學電機工程研究所

摘要

本論文研發適用於太陽能發電系統之最大功率追蹤轉換器晶片，有別於傳統微處理器結合離散元件的實現方式，針對太陽能發電系統最大功率追蹤轉換器之積體電路化提出新方法，使用精簡類比式電路設計控制結合低複雜度的最大功率追蹤演算法運作即可同時達成高追蹤效率及快速暫態響應的效能，不需要另外增加演算法複雜度、硬體成本及運算量。本篇論文提出一項最適合等效負載線斜率技術，可依實際的太陽能電池輸出特性曲線去決定最適合等效負載線和斜率，因此能與實際應用環境做可適應性的改變。並設計具有高電壓及低電壓兩種模式的結合，適用於太陽能電壓範圍 0V~500V，輸出電流 0~4A 的應用，打破低電壓半導體晶片使用的限制，未來可將此技術移植至超高電壓半導體晶片中。

此類比式最大功率追蹤轉換器是使用台灣積體電路製造股份有限公司所提供的 0.35um 2P4M 3.3V/5V 混合訊號互補式金氧半製程來製造。全晶片面積大約 1.72x1.79mm^2，遠小於傳統以微處理器方法實現的面積。實際量測結果，追蹤效率高達 99.3%以上，其暫態響應參數(暫態追蹤係數)為 0.47ms/W，遠優於現有技術，此轉換器的最大效率為 91%。由量測結果與現有技術比較，本論文研製出目前世界上最小面積成本且最佳效能之太陽能最大功率追蹤轉換器。

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關鍵詞: 太陽能，最大功率追蹤，積體電路

Analog Integrated Circuit Realization for Maximum Power Point Tracking of Solar Energy Systems

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Abstract

The research and invention of a maximum power point tracking converter on chip for solar photovoltaic system is presented in this thesis. It is different from the conventional style which a microprocessor and discrete devices are employed to implement the function. A novel solution is proposed for the integrated circuits of the photovoltaic maximum power point tracking converter. The combination of the analog circuit design and low complex maximum power point tracking algorithm could achieve high tracking efficiency and fast transient response simultaneously without imposing additional algorithm complexity, hardware cost, and major computational load. Adaptive load line slope technique is proposed in this thesis. Under the suggested method, the adaptive load line slope is decided by the output characteristic curves of the real photovoltaic cells, and it will be optimal for the real applications. The design with the hybrid of high voltage mode and low voltage mode is adaptive for the output voltage rating 0~500V of photovoltaic array, and the output current rating 0~4A of the photovoltaic array. The limit of the applicative range on the low voltage CMOS chip is broken by the above method. In the future, these techniques will be transferred onto the ultra high voltage CMOS chip.

This analog maximum power point converter fabricated with TSMC 0.35um 2P4M 3.3V/5V Mixed Signal CMOS process. The total chip area is about 1.72x1.79 mm^2, which is smaller than that in the conventional types. The measured tracking efficiency is 99.3%, the parameter of transient response (Transient Tracking Factor) is 0.47ms/W, being the best in the world, and the power conversion efficiency is 91%. From the comparison between the measurement results and that of other techniques, this thesis presents a photovoltaic maximum power point tracking converter with the smallest area, the lowest cost, and the best performance in the world.

*The author
**The advisor

Keyword: Photovoltaic, Maximum power point tracking, Integrated circuit.

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李貞慶

九十八年十一月

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Chapter 1

Introduction

The increasing concern over energy crisis and environmental issue today, the generation of photovoltaic (PV) is becoming more important as a renewable energy source since many advantages such as cleanness, maintenance-free, no noise, and abundant source of energy. The worldwide-installed photovoltaic power capacity shows a nearly exponential increase over the last ten years [1]. In today's application, there are two principal types of photovoltaic power systems, which are classified by their functions and configuration, named grid-connected systems and stand-alone systems [2]. Their configurations are shown in Fig. 1.1 (a) and Fig. 1.1 (b), respectively. Grid-connected systems, which are in parallel with the electric utility grid and supply solar power to the utility grid, are like Building-Integrated Photovoltaic (BIPV), PV power plant, etc. Oppositively, stand-alone systems which are independent of the electric utility grid, for example, present in portable electronic applications, vehicular electronic applications, and so on. From Fig. 1.1, due to the well-known nonlinear relationship of output characteristics of the solar PV array [3]-[6], maximum power point tracking (MPPT) converter is an essential part needed in both photovoltaic systems. MPPT takes full of available solar energy to the storage device such as a rechargeable battery for overall power efficiency, and also for the economic reasons. It is known that the cost of generating electric power of the photovoltaic is still too high to utilize it generally. The demand, reducing the cost of

generating electric power of the photovoltaic is critical. Therefore, how to design an appropriate MPPT converter to optimum the performance of the PV system will be a development in the future.

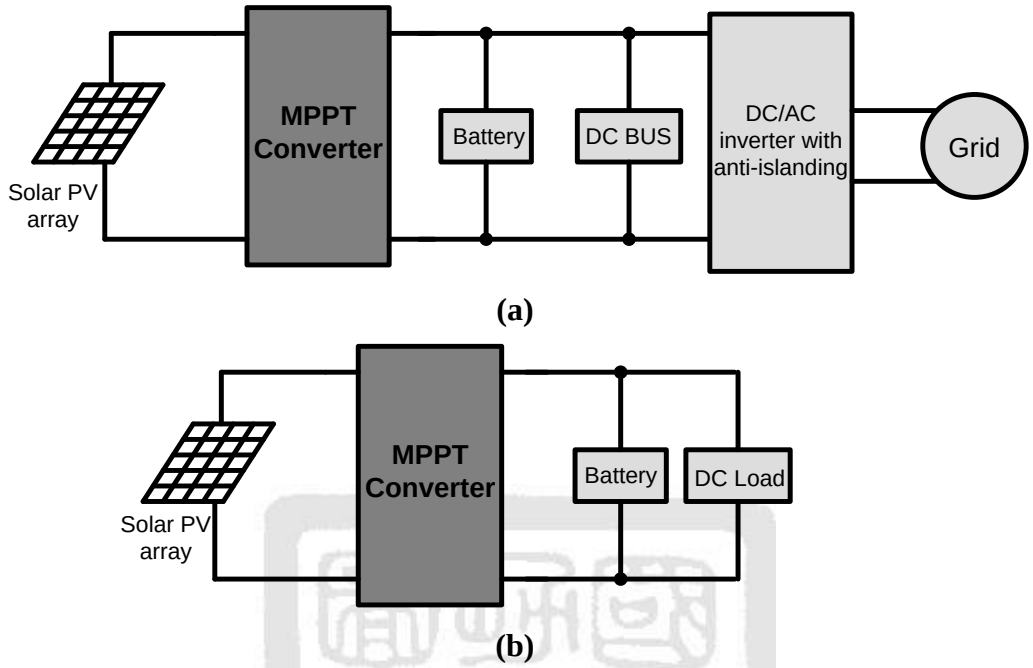


Fig. 1.1 Two types of photovoltaic power systems (a) Grid-connected systems (b) Stand-alone systems

1.1 Motivation

Due to the rapid growth of photovoltaic power, the power management circuits in photovoltaic power systems, including maximum power point tracking converters, inverters for grid-connected systems, and so on, are more and more critical today. Especially, maximum power point tracking converter is an essential part to increase overall power conversion efficiency and to reduce the cost of electric power, because the performance of photovoltaic cells is still below par now. With a great deal of the photovoltaic cell utilized in the world, the demand, which decrease the volume and the cost of power management circuits in photovoltaic power systems, is needed urgently. In the past, many traditional MPPT methods [7]-[20], like Perturb and Observe (P&O) method [7]-[11] and Incremental Conductance (INC) method [12]-[14] are popularly used in the related work and literature. Those methods aim at tracking the maximum power point of a PV module by satisfying the condition $dP_{pv}/dV_{pv} = 0$ in a closed loop regulation, where P_{pv} and V_{pv} are the PV module's power and voltage, respectively. Due to the complexity of the required mathematical operations, a digital

signal processor or a relatively powerful microcontroller is typically needed to compute the MPPT algorithm, and then combine other discrete components for drawing the maximum power from the photovoltaic cells, shown in Fig. 1.2. The traditional scheme relies on measurement of the PV module's voltage and current to

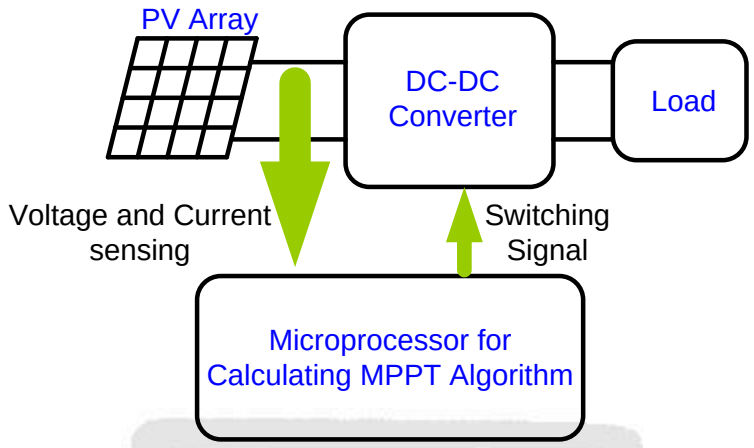


Fig. 1.2 Block diagram of a general MPPT system

adjust a control parameter iteratively. The constant incremental control parameter may be a PV array's voltage variable (ΔV), a PV array's current variable (ΔI), or a converter's duty cycle variable (ΔD). Choosing the incremental value of the controlled parameter becomes a key influence on the performance. If a small incremental value decided, that may decrease the power losses in steady state owing to small perturbations around maximum power point. But the dynamic behavior will be worse in quickly changing irradiation conditions or loads. On the contrary, if a large incremental value decided, that may improve the dynamic behavior in quickly changing irradiation conditions or loads, but the power losses will be worse [15]. The trade-off problem of the tracking efficiency and dynamic response normally exists in the traditional iterative MPPT algorithms. Moreover, the traditional scheme increases the cost of PV energy conversion systems. Therefore, it is not the best solution today. Meanwhile, owing to the rapid progress in the high voltage semiconductor process technology, integrated circuits of maximum power point tracking converters will be a trend in the future [16]. For the reason, this thesis focuses on the CMOS integrated circuit implementation of MPPT converters, that is, power management and mixed-signal circuits can be integrated into a monolithic CMOS chip for low-power and even high-power applications. The concept is shown in Fig. 1.3. In order to provide a low cost and high performance fully integrated MPPT converter for PV energy conversion systems, a monolithic MPPT converter integrated circuit (IC) is

designed with a low-complexity algorithm for breaking the tradeoff mentioned above. Moreover, this IC can be adaptively optimized to fit any kind of photovoltaic modules by following the characteristics. Thus, without imposing additional algorithm complexity, hardware cost, major computational load, high volume size and even a microprocessor, the proposed IC is easy to be employed for wide power range PV modules. An adaptable wide power rating range, high performance, and low power losses maximum power point tracking converter is implemented and integrated on a standard CMOS process in my thesis.

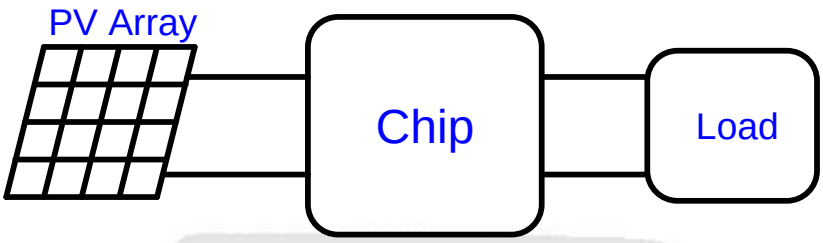


Fig. 1.3 Primary concept of this thesis

1.2 Organization

This thesis is organized as six chapters. The first is introduction. In chapter 2, the fundamentals of photovoltaic maximum power point tracking are introduced, including the characteristic and the model of photovoltaic cell, summary of maximum power point tracking, and specifications of maximum power point tracking. In the chapter 3, the critical techniques proposed in the maximum power point tracking converter are presented. Chapter 4 extends the design into circuit level. Every circuit in the maximum power point tracking converter is described and analyzed. The layout considerations are also shown and described at the end of this chapter. Chapter 5 gives the simulation and measurement result of the designed MPPT converter. Chapter 6 is the conclusion and future work.

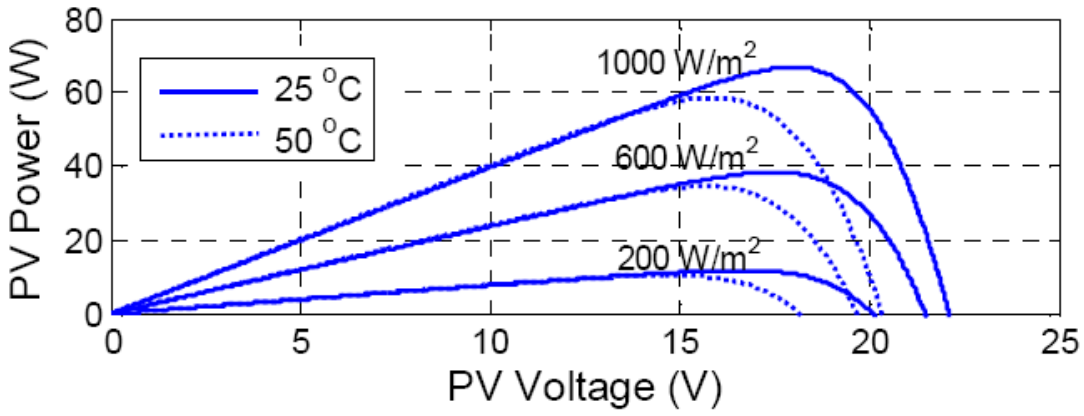
Chapter 2

Fundamentals of Photovoltaic Maximum Power Point Tracking

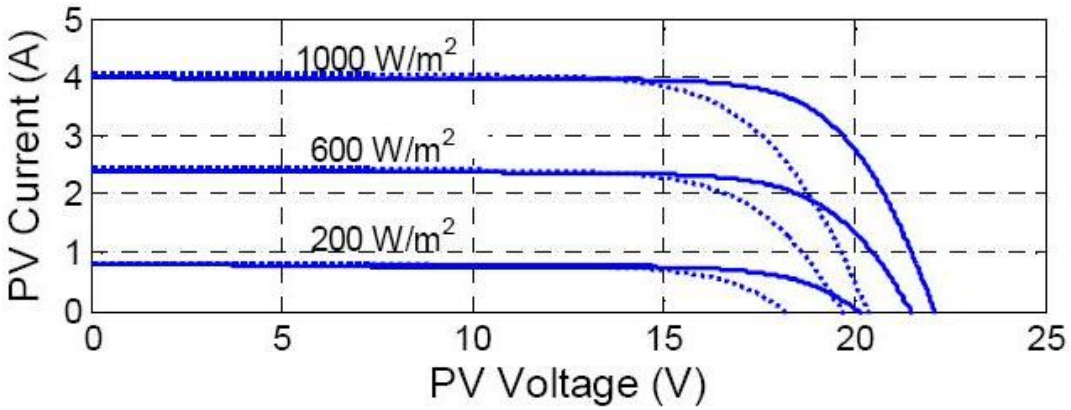
2.1 Fundamentals of Photovoltaic Cell

2.1.1 Typical Photovoltaic Cell Characteristic

General categories of photovoltaic cell are crystalline silicon type, thin film type, high concentration photovoltaic (HCPV), etc. Although different categories of photovoltaic cell are fabricated from different materials, the light-to-electrical energy of them is generated on the similar principle and by low conversion efficiency. They work only for a limited time in one day due to available sunlight and depend heavily on weather conditions, such as solar irradiation and atmospheric temperature. Typical output power- output voltage curves (P-V curves) and output current- output voltage curves (I-V curves) of PV cells are shown in Fig. 2.1 [3]. From Fig. 2.1(a), it can be seen that output power of the PV cells under different solar irradiation and atmospheric temperature is different power rating.



(a)



(b)

Fig. 2.1 P-V and I-V characteristics of a PV module under varying solar irradiances and temperatures (a) P-V curves (b) I-V curves

From Fig. 2.1(b), it maps to different I-V curves under varying solar irradiances and temperatures, and presents the well-know nonlinear relationship between the output current and the output voltage of the photovoltaic cell.

Generally speaking, the electrical characteristics of a PV module consist of maximum power (P_{max}), voltage at P_{max} (V_{mpp}), current at P_{max} (I_{mpp}), open-circuit voltage (V_{oc}), short-circuit current (I_{sc}), etc.

2.1.2 Photovoltaic Cell Model [4]-[6]

Photovoltaic cells consist of a p-n junction that when exposed to light releases electrons around a closed electrical circuit. From this premise the circuit equivalent of a cell can be modeled through the circuit shown in Fig. 2.2. Electrons from the cell are excited to higher energy levels when a collision with a photon occurs and then are free to move across the junction due to the built-in potential and create a current. This is modeled by the light generated current source I_{ph}. The intrinsic p-n junction

characteristic is introduced as a diode in the circuit equivalent. R_{sh} and R_s are the shunt and series resistances, respectively. R_{sh} models the leakage currents in the cell

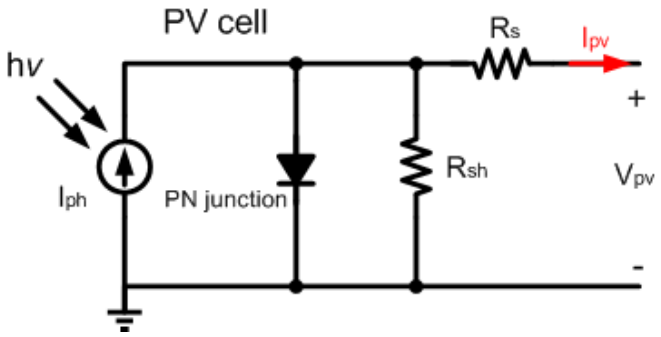


Fig. 2.2 Photovoltaic cells circuit equivalent

while R_s models the intrinsic resistance electrons face before reaching the cell's electrical contacts. Typically, a solar panel comprises n_s well-matched PV cells in series and comprises the number of n_p in parallel. Resistances now become $R_s=n_sR_s'$, $R_{sh}=n_sR_{sh}'$, and the module's voltage is now $V_{pv}=n_sV_{pv}'$, where R_s', R_{sh}' and V_{pv}' are a single cell's series and shunt resistances and voltage, respectively. The relationship between V_{pv} and I_{pv} is known as the I–V characteristic of the photovoltaic module. This is defined by

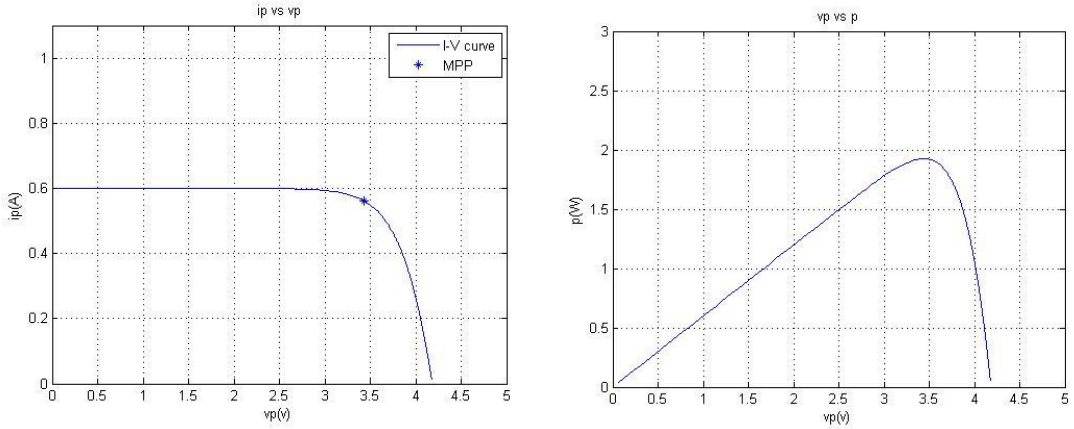
$$I_{pv} = I_{ph} - I_s[\exp(\alpha(V_{pv} + i_{pv}R_s)) - 1] - \frac{(V_{pv} + I_{pv}R_s)}{R_{sh}} \quad (2\text{-}1)$$

where $\alpha = \frac{q}{n_s kT}$, k=1.3807 x 10^{-23} JK^{-1} is Boltzmann's constant, T is absolute temperature, q=1.6022 x 10^{-19} C is electronic charge, and I_s is diode's saturation current. If n_p parallel strings,

$$I_o = n_p I_{pv} \quad (2\text{-}2)$$

where I_o denotes the total output current of PV array.

Circuit model based on this equivalent circuit described above is verified with HSpice. The simulation results are shown in Fig. 2.3.



(a) **(b)**

Fig. 2.3 Simulation results of HSpice model of PV cells (a) I-V curve (b) P-V curve

2.2 Summary of Maximum Power Point Tracking Techniques [7]

Nowadays, maximum power point tracking (MPPT) is shown that at least 19 distinct methods have been introduced in the literature. These methods vary in complexity, sensors required, convergence speed, cost, range of effectiveness, implementation hardware, popularity, and in other respects. The comparison of these MPPT methods is summarized in Table 2.1. [7]

Table 2.1 Major characteristics of MPPT methods [7]

MPPT Technique	PV Array Dependent?	True MPPT?	Analog or Digital?	Periodic Tuning?	Convergence Speed	Implementation Complexity	Sensed Parameters
Hill-climbing/P&O	No	Yes	Both	No	Varies	Low	Voltage, Current
IncCond	No	Yes	Digital	No	Varies	Medium	Voltage, Current
Fractional V_{OC}	Yes	No	Both	Yes	Medium	Low	Voltage
Fractional I_{SC}	Yes	No	Both	Yes	Medium	Medium	Current
Fuzzy Logic Control	Yes	Yes	Digital	Yes	Fast	High	Varies
Neural Network	Yes	Yes	Digital	Yes	Fast	High	Varies
RCC	No	Yes	Analog	No	Fast	Low	Voltage, Current
Current Sweep	Yes	Yes	Digital	Yes	Slow	High	Voltage, Current
DC Link Capacitor Droop Control	No	No	Both	No	Medium	Low	Voltage
Load I or V Maximization	No	No	Analog	No	Fast	Low	Voltage, Current
dP/dV or dP/dI Feedback Control	No	Yes	Digital	No	Fast	Medium	Voltage, Current
Array Reconfiguration	Yes	No	Digital	Yes	Slow	High	Voltage, Current
Linear Current Control	Yes	No	Digital	Yes	Fast	Medium	Irradiance
I_{MPP} & V_{MPP} Computation	Yes	Yes	Digital	Yes	N/A	Medium	Irradiance, Temperature
State-based MPPT	Yes	Yes	Both	Yes	Fast	High	Voltage, Current
OCC MPPT	Yes	No	Both	Yes	Fast	Medium	Current
BFV	Yes	No	Both	Yes	N/A	Low	None
LRCM	Yes	No	Digital	No	N/A	High	Voltage, Current
Slide Control	No	Yes	Digital	No	Fast	Medium	Voltage, Current

In this thesis, the MPPT methods are briefly categorized into the following groups: perturbation and observation (P&O) method, incremental conductance (INC) method, miscellaneous, e.g., fractional V_{oc}, etc. In the following sections, the brief operations about these popular MPPT methods are introduced.

2.2.1 Perturbation and Observation (P&O) Method

[7]-[11]

The P&O MPPT method is mostly used, due to its ease of implementation. It is based on the following criterion: if the operating voltage of the PV array is perturbed in a given direction and if the power drawn from the PV array increases, this means that the operating point has moved toward the maximum power point (MPP) and therefore, the operating voltage must be further perturbed in the same direction. Otherwise, if the power drawn from the PV array decreases, the operating point has moved away from the MPP and, therefore, the direction of the operating voltage perturbation must be reversed. From Fig. 2.4, it can be seen that incrementing (decrementing) the voltage increases (decreases) the power when operating on the left of the MPP and decreases (increases) the power when on the right of the MPP. Therefore, if there is an increase on power, the subsequent perturbation should be kept the same to reach the MPP and if there is a decrease in power, the perturbation should be reversed. This algorithm is summarized in Table 2.2.

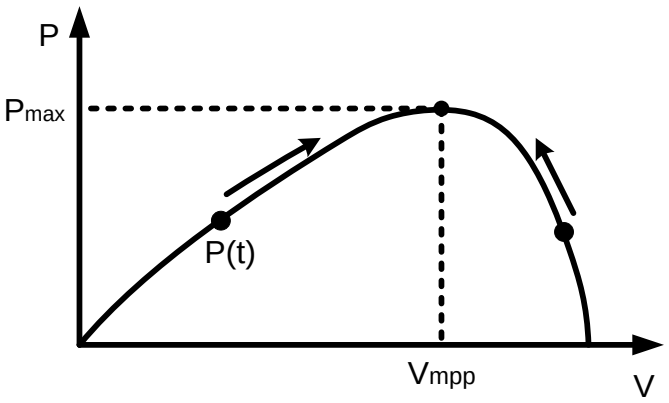


Fig. 2.4 Operation characteristic on P-V curve

Table 2.2 Strategy of P&O algorithm

Perturbation	Change in power	Next perturbation
Positive	Positive	Positive
Positive	Negative	Negative
Negative	Positive	Negative
Negative	Negative	Positive

The process is repeated periodically until the MPP is reached. The system then oscillates about the MPP. The oscillation can be minimized by reducing the perturbation step size. However, a smaller perturbation size slows down the MPPT. This is a trade-off of the speed and accuracy of the conventional P&O method. A drawback of P&O MPPT technique is that it may fail under rapidly changing atmospheric conditions as illustrated in Fig. 2.5. Starting from an operating point A,

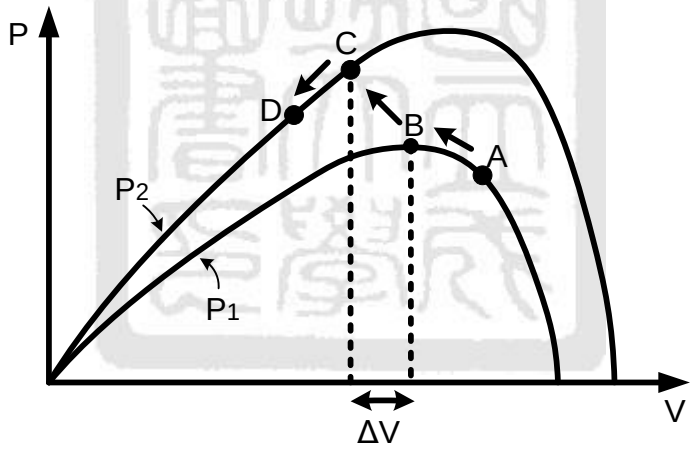


Fig. 2.5 Divergence of P&O from MPP

if atmospheric conditions stay approximately constant, a perturbation ΔV in the PV voltage, V, will bring the operating point to B. However, if the irradiance increases and shifts the power curve from P_1 to P_2 within one sampling period, the operating point will move from B to C and then to D. Consequently, the operating point diverges from the MPP and will keep diverging if the irradiance steadily increases.

Two sensors are usually required to measure the PV array voltage and current. DSP or microcomputer control with discrete analog and digital circuitry is often suitable for P&O.

2.2.2 Incremental Conductance (INC) Method [12]-[14]

The incremental conductance (INC) method is based on the fact that the slope of the PV array power curve (Fig. 2.4) is zero at the MPP, positive on the left of the MPP, and negative on the right, as given by

$$\begin{cases} \dfrac{dP}{dV} = 0, & \text{at MPP} \\ \dfrac{dP}{dV} > 0, & \text{left of MPP} \\ \dfrac{dP}{dV} < 0, & \text{right of MPP} \end{cases} \tag{2-3}$$

Since,

$$\frac{dP}{dV} = \frac{d(IV)}{dV} = I + V\frac{dI}{dV} \cong I + V\frac{\Delta I}{\Delta V} \tag{2-4}$$

(2-3) can be rewritten as

$$\begin{cases} \dfrac{\Delta I}{\Delta V} = -\dfrac{I}{V}, & \text{at MPP} \\ \dfrac{\Delta I}{\Delta V} > -\dfrac{I}{V}, & \text{left of MPP} \\ \dfrac{\Delta I}{\Delta V} < -\dfrac{I}{V}, & \text{right of MPP} \end{cases} \tag{2-5}$$

The MPP can be tracked by comparing the instantaneous conductance (I/V) to the incremental conductance (ΔI/ΔV) as shown in the flowchart in Fig. 2.6. Δ k is the reference incremental value which forces PV array to change output power. Once the MPP is reached, the operation of the PV array is maintained at this point unless a change in ΔI is noted, indicating a change in atmospheric conditions and the MPP. The algorithm decrements or increments Δ k to track the new MPP.

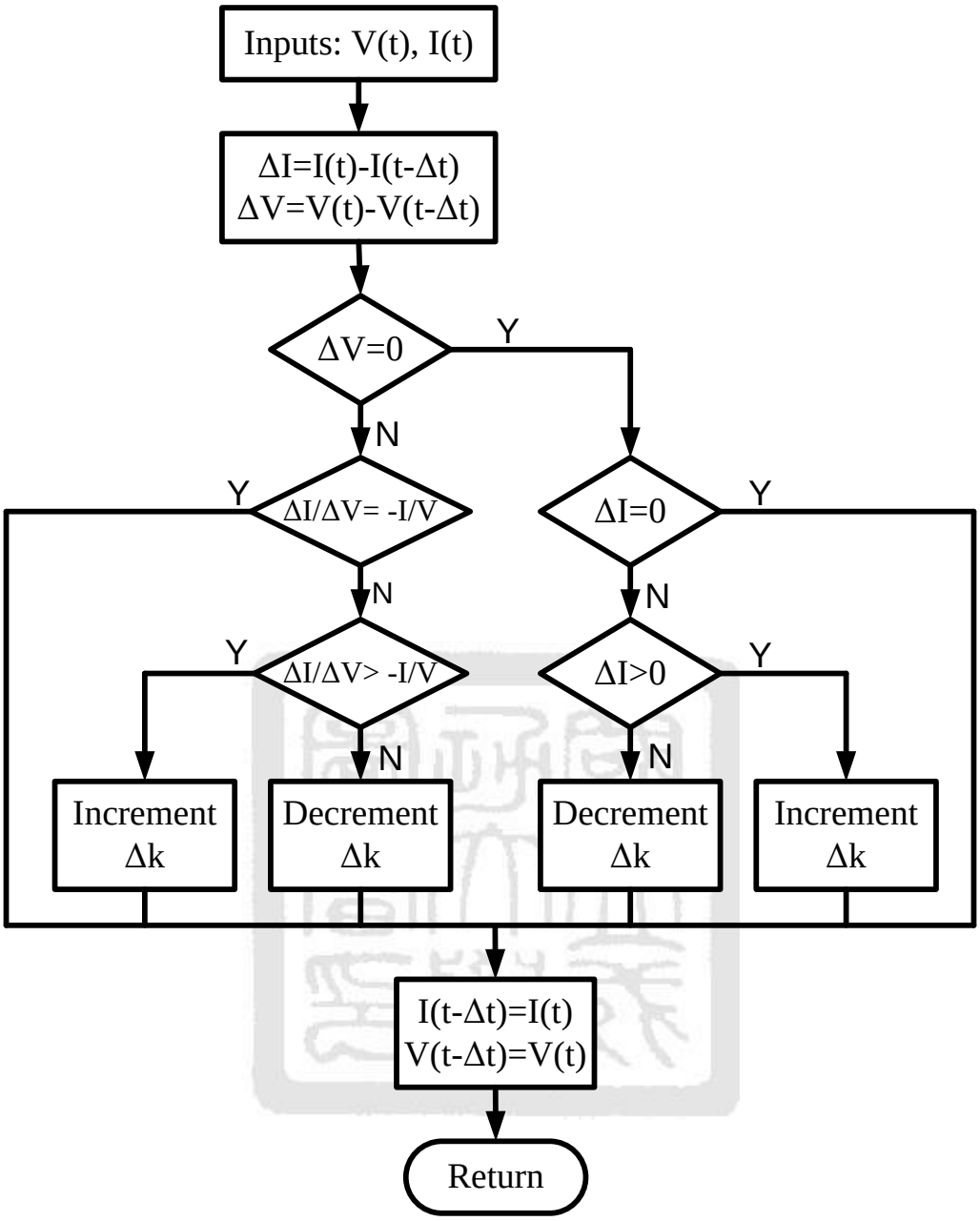


Fig. 2.6 Flow chart of INC algorithm

The increment size determines how fast the MPP is tracked. Fast tracking can be achieved with bigger increments but the system might not operate exactly at the MPP and oscillate about it instead; so there is a tradeoff like as P&O. Indeed, because of noise, measurement and quantization errors, the condition $\frac{\Delta I}{\Delta V} = -\frac{I}{V}$, is in practice never exactly satisfied, but it is usually required that such condition is approximately satisfied within a given accuracy [17]. As a consequence, the INC operating voltage cannot be exactly coincident with the MPP and oscillates across it. Disadvantages of

the INC algorithm, with respect to P&O, are in the increased hardware and software complexity; moreover, leads to increased computation times and to the consequent slowing down of the possible sampling rate of array voltage and current.

Measurements of the instantaneous PV array voltage and current require two sensors. INC method lends itself well to DSP and microcontroller control, which can easily keep track of previous values of voltage and current and make all the decisions.

2.2.3 Miscellaneous Methods

1. Fractional Open-Circuit Voltage [18]

The near linear relationship between V_{mpp} and V_{oc} of the PV array, under varying irradiance and temperature levels, is derived by

$$V_{mpp} \approx KV_{oc} \tag{2-7}$$

where K is a constant of proportionality. Since K is dependent on the characteristics of the PV array being used, it usually has to be computed beforehand by empirically determining V_{mpp} and V_{oc} for the specific PV array at different irradiance and temperature levels. The factor K has been reported to be between 0.71 and 0.78. Once K is known, V_{mpp} can be computed using (2-7) with V_{oc} measured periodically by momentarily shutting down the power converter. However, this incurs some disadvantages, including temporary loss of power. Since (2-7) is only an approximation, the PV array technically never operates at the MPP. Depending on the application of the PV system, this can sometimes be adequate. Even if fractional V_{oc} is not a true MPPT technique, it is very easy and cheap to implement as it does not necessarily require DSP or microcontroller control.

2. Neural Network [19]

Neural networks commonly have three layers: input, hidden, and output layers as shown in next page Fig. 2.7. The numbers of nodes in each layer vary and are user-dependent. The input variables can be PV array parameters like V_{oc} and I_{sc}, atmospheric data like irradiance and temperature, etc. The output is usually one or several reference signals like a duty cycle signal used to drive the power converter to operate at or close to the MPP.

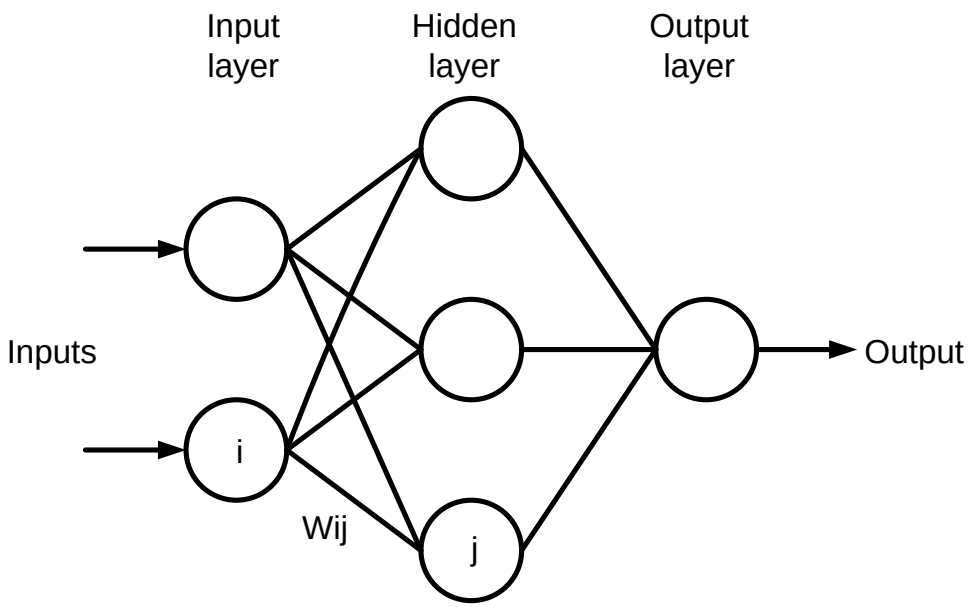


Fig. 2.7 Example of neural network

The link between nodes i and j is labeled as having a weight of Wij. To accurately identify the MPP, the Wij have to be carefully determined through a training process, whereby the PV array is tested over months or years and the patterns between the input(s) and output(s) of the neural network are recorded.

3. Best Fixed Voltage [20]

Statistical data is collected about irradiance and temperature levels over a period of one year and the best fixed voltage representative of the MPP is found. The control sets either the operating point of the PV array to the best fixed voltage or the output voltage to the nominal load voltage. Operation is therefore never exactly at the MPP and different data has to be collected for different geographic regions.

Many other MPPT methods could not be discussed in this thesis. Please consult the reference [7] if needed to know.

2.3 Specifications of Photovoltaic Maximum Power Point Tracking Converter

2.3.1 Tracking Efficiency [21]

An important figure of merit in evaluating MPPT algorithms is tracking efficiency. Generally, the index, tracking efficiency, η_{track}, can be seen in the literature about MPPT algorithm to determine how accurate the MPPT algorithm can achieve under the steady environmental condition. It is defined as

$$\eta_{track} = \frac{\int_{t_1}^{t_2} P_{actual}(t)dt}{\int_{t_1}^{t_2} P_{max}(t)dt} \times 100\% \quad (2\text{-}8)$$

where P_{actual} is the actual power produced by the PV array under the control of the MPPT, and P_{max} is the available maximum power the array could produce under the given temperature and irradiance. Since temperature and irradiance are both functions of time, P_{actual} and P_{max}, are also time varying.

2.3.2 Transient Response

Transient response in MPPT converter is regarded as another important index in evaluating MPPT converter. Transient condition in MPPT converter relates to the magnitude that output power drops and the time for the power tracking to settle down when a rapid change in atmospheric conditions influence photovoltaic array output power rating as shown in Fig. 2.8. It is defined as a variation of output voltage when photovoltaic array output power suddenly changes from one level to another level. The Fig. 2.8 shows that the output capability of PV power available changes from high level to low level at T_1 and from low level to high level at T_2.

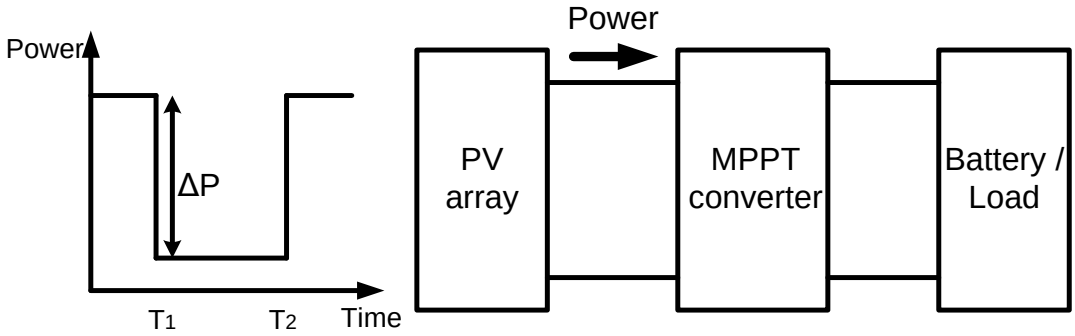


Fig. 2.8 Block diagram of a basic MPPT converter when a rapid change in atmospheric conditions happen

Nowadays, there are not any acknowledged definitions to characterize the transient response of MPPT converter. In this thesis, a novel definition is proposed to compare transient response of any MPPT converters. This index, named Transient Tracking Factor (TTF), is defined as (2-9) and will be explained in Fig. 2.9.

$$TTF = \frac{\text{Transient time}}{\text{Power change during transient time}} = \frac{\Delta T}{\Delta P} \tag{2-9}$$

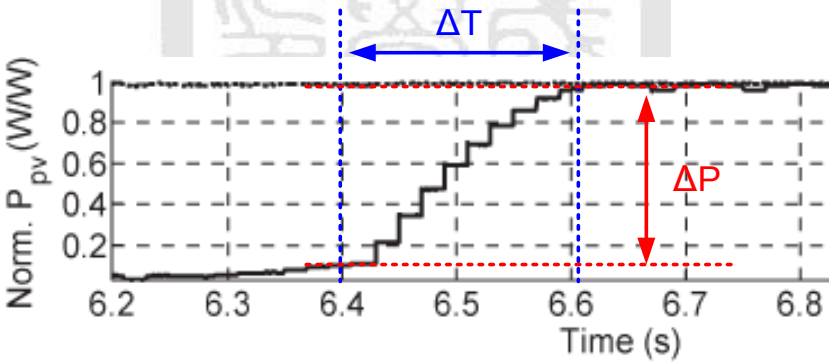


Fig. 2.9 The transient response of MPPT

Fig. 2.9 shows that ΔT is the time of power change from one level to another level. Because of the amount of the power change, ΔP could influence transient speed. It must be normalized in the definition of TTF. Comparison of transient response of MPPT converters is just. From (2-9), it can be known that faster transient response stand for smaller the TTF.

2.3.3 Power Conversion Efficiency

Power conversion efficiency, $\eta_{conversion}$, in MPPT converter highly relates to the implementation of MPPT converter which consists of DC-DC converter, MPPT controller, blocking diode, etc. Power conversion efficiency of MPPT converter is defined as the ratio of load power to PV array output power as follows:

$$\eta_{conversion} = \frac{P_{load}}{P_{in}} \times 100\% = \frac{I_{load} \times V_{load}}{I_{pv} \times V_{pv}} \times 100\% \quad (2\text{-}10)$$

On the other way, it can be seen as the power loss in evaluating MPPT converter. The power loss of MPPT converter may consist of conduction power loss, switching power loss, gate driver loss, inductor power loss, etc. in a DC-DC converter, controller power loss in the MPPT controller, and diode power loss in a blocking diode which protects the PV array from reverse current damage, and so on.

$$\eta_{conversion} = \frac{I_{load} \times V_{load}}{I_{load} \times V_{load} + P_{all\_loss}} \times 100\,\% \quad (2\text{-}11)$$

From (2-11), output power of photovoltaic array is the addition of load power and all power loss. The less the MPPT converter power loss is the more the power conversion efficiency.

2.4 Topology of Photovoltaic Interface for Maximum Power Point Tracking [22]-[24]

This section provides a comparative study with the goal of choosing a suitable converter topology for the applications of the DC-DC MPPT converters. Non-isolated buck and boost DC-DC converters are widely used in photovoltaic power systems because of their simplicity and efficiency. Table 2.3 is the characteristics of the two converter topologies.

Table 2.3 The characteristics of the two converter topologies

Topology	Output vs. Input	Conversion Ratio	Output Polarity
Buck	Step-down	D	Same polarity
Boost	Step-up	1/(1-D)	Same polarity

2.4.1 Buck Converter Topology

A buck DC-DC converter in the photovoltaic power system, as shown in Fig.2.10, has a discontinuous input current and a continuous output current before considering the input filter. The battery symbol represents a constant voltage load. In the steady-state condition, it also keeps the principle of inductor volt-second balance.

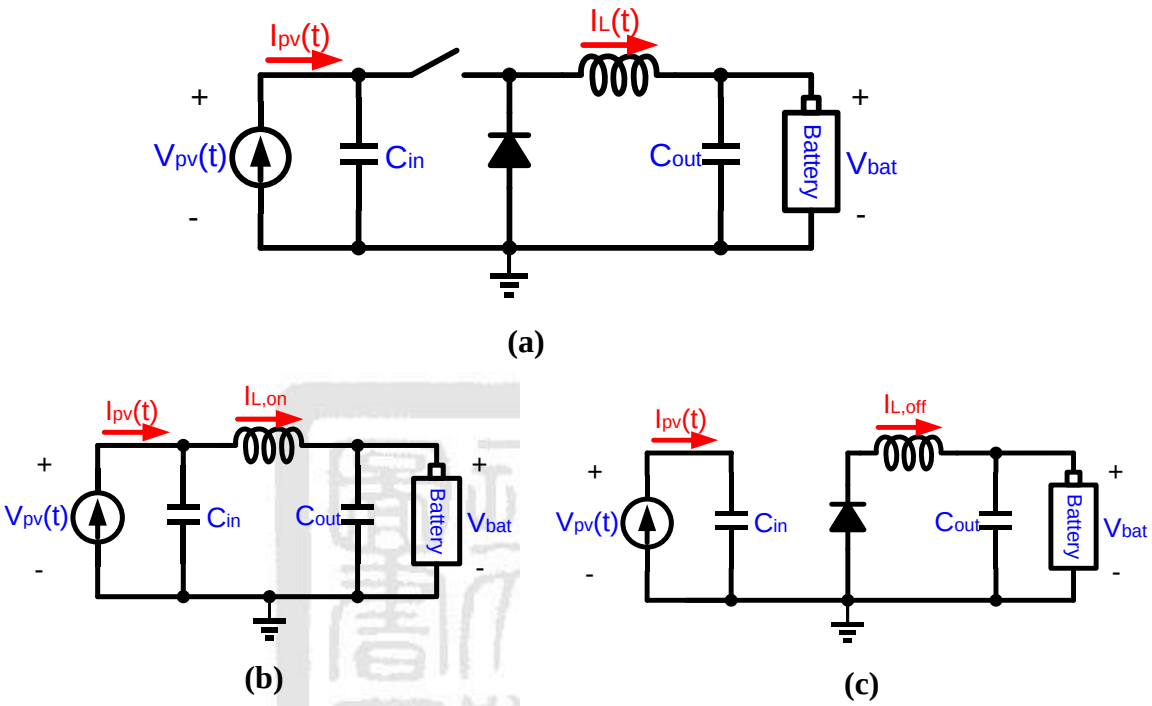


Fig. 2.10 (a) Equivalent simplified circuit of buck converter in photovoltaic power system (b) Equivalent circuit in ON-state condition (c) Equivalent circuit in OFF-state condition

Considering the specifications of the buck converter depends on the passive devices, like input capacitor, inductor, and output capacitor. In the steady-state condition, the inductor current $I_L(t)$ contains a dc component I and the ripple of peak magnitude $\Delta i_L(t)$ as shown in Fig. 2.11.

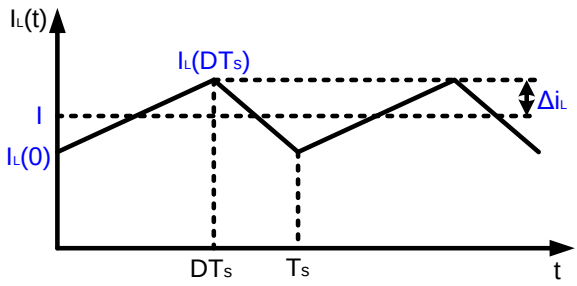


Fig. 2.11 Steady-state inductor current waveform of buck converter

In the boundary between CCM and DCM, the value of inductor could be decided by the inductor current ripple. The average current of the inductor,

$$I = \Delta i_L \tag{2-12}$$

and

$$\Delta i_L = \frac{1}{2}\frac{V_{bat}}{L}(1-D)T_s \tag{2-13}$$

From Eq. (2-12) and (2-13), the value of the inductor can be obtained,

$$L = \frac{V_{bat}(1-D)}{2\Delta i_L \cdot f_{sw}} \tag{2-14}$$

where $f_{sw}=1/T_s$.

The output capacitor provides significant filtering of switching ripple, that the capacitance is chosen large enough that its impedance at the switching frequency is much smaller than the load impedance. Hence, nearly all of the inductor current ripple flows into the output capacitor, and very little flows through load. The output capacitor current is equal to the inductor current without dc component as Fig. 2.12.

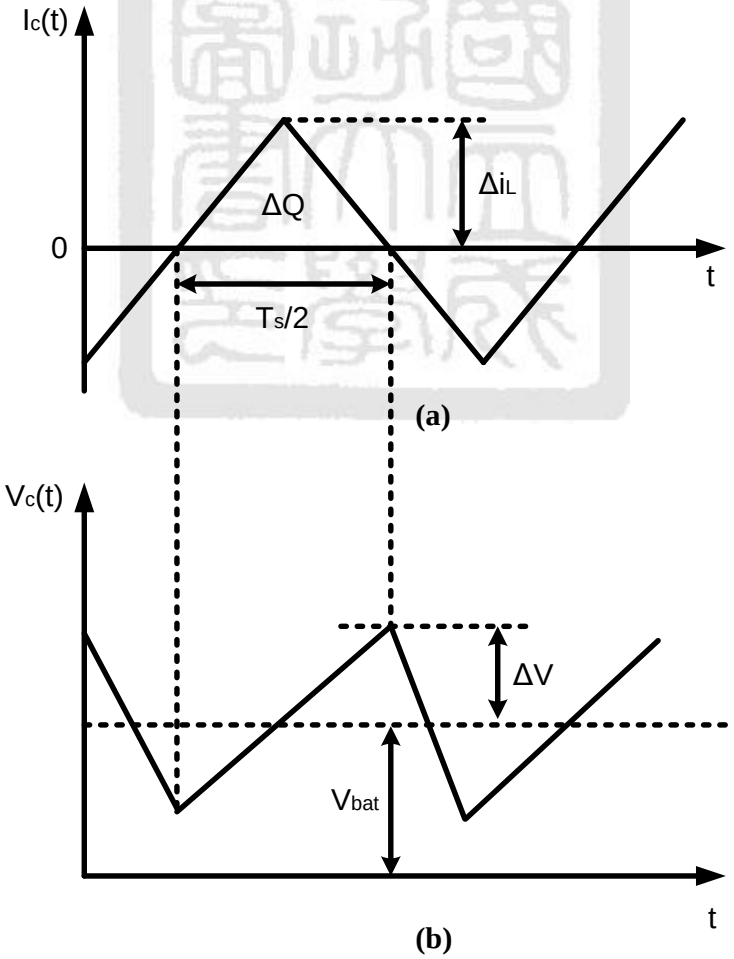


Fig. 2.12 Buck converter (a) output capacitor current waveform (b) output capacitor voltage waveform

Form Fig. 2.12, by the capacitor relation Q=CV, and total charge ΔQ of Fig 2.12 is calculated as follows,

$$\Delta Q = C_{out}(2\Delta V) \text{ and } \Delta Q = \frac{1}{2}\Delta i_L \frac{T_s}{2} \tag{2-15}$$

and then, the solution for the output voltage ripple peak magnitude ΔV.

$$\Delta V = \frac{\Delta i_L T_s}{8C_{out}} \tag{2-16}$$

Hence, we can decide the value of the output capacitor from Eq. (2-17).

$$C_{out} = \frac{\Delta i_L T_s}{8\Delta V} \tag{2-17}$$

The input capacitor is an important role in the buck interface of the photovoltaic power system. It can be decided from the current ripple of the photovoltaic cell flowing through the input capacitor. From Fig. 2.10(c), it can be known that the output current of the photovoltaic cell is equal to the current into the input capacitor during the OFF-state condition. The total charge, q, during the period,

$$q = 2C_{in}\Delta V_{pv} = I_{pv}(1-D)T_s \tag{2-18}$$

Where, ΔV_{pv} is the value of photovoltaic voltage ripple, and I_{pv} is the steady-state photovoltaic current. And then, C_{in} can be decided,

$$C_{in} = \frac{I_{pv}(1-D)T_s}{2 \cdot \Delta V_{pv}} \tag{2-19}$$

2.4.2 Boost Converter Topology

A boost DC-DC converter in the photovoltaic power system, illustrated in Fig.2.13, has a continuous input current and a discontinuous output current before considering the input filter. The battery symbol represents a constant voltage load. In the steady-state condition, it also keeps the principle of inductor volt-second balance.

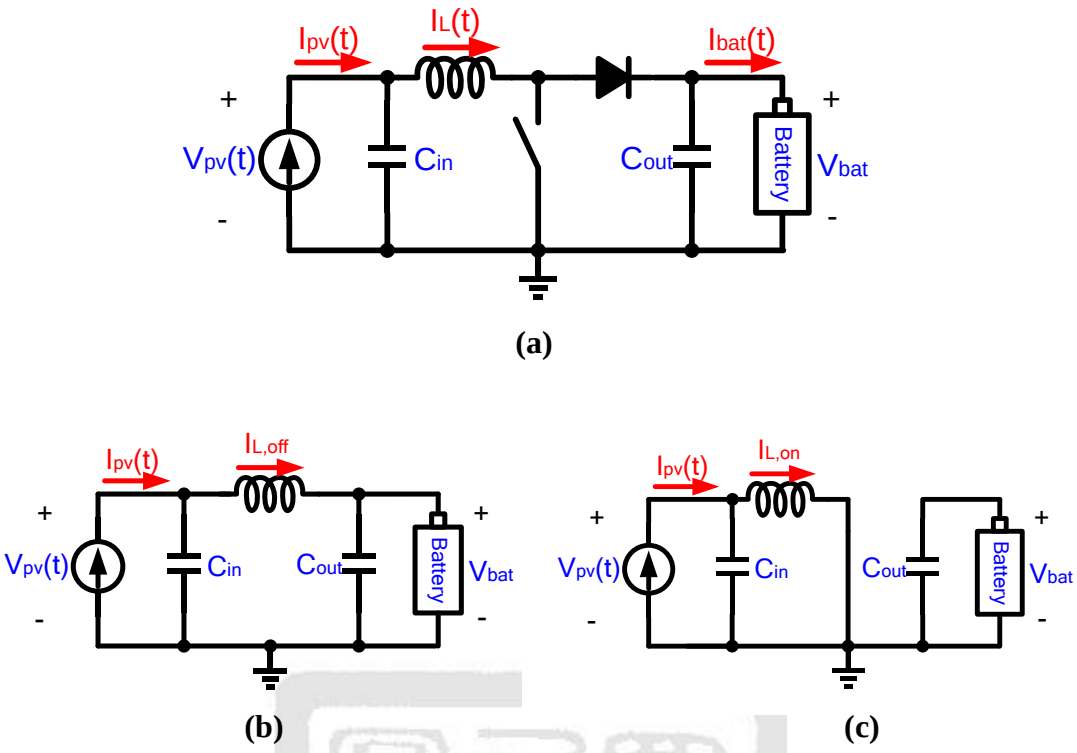


Fig. 2.13 (a) Equivalent simplified circuit of boost converter in photovoltaic power system (b) Equivalent circuit in OFF-state condition (c) Equivalent circuit in ON-state condition

The values of the inductor, the input capacitor, and the output capacitor of the boost converter can be decided by the analysis as same as that of the buck converter. The value of the inductor is

$$L = \frac{V_{pv} D T_s}{2 \cdot \Delta i_L} \tag{2-20}$$

The value of the output capacitor is

$$C_{out} = \frac{I_{bat} D T_s}{8 \cdot \Delta V} \tag{2-21}$$

where ΔV is the value of output voltage ripple and I_{bat} is the steady-state output ripple.

Finally, the value of the input capacitor is

$$C_{in} = \frac{\Delta i_L T_s}{8 \cdot \Delta V_{pv}} \tag{2-22}$$

where ΔV_{pv} is the value of photovoltaic voltage ripple.

Chapter 3

Techniques of CMOS Photovoltaic MPPT Converter

In this chapter, some proposed techniques are presented and described to improve some issues of photovoltaic maximum power point tracking converter, such as high tracking efficiency, fast transient response, and so on. On the other hand, the power rating range is limited for low-voltage applications by the CMOS process. Here, a wide power rating range CMOS maximum power point tracking converter is proposed with a hybrid high-voltage-mode (HV-mode) and low-voltage-mode (LV-mode) structure.

3.1 Techniques for Breaking the Trade-Off of Conventional MPPT

3.1.1 Issues Statement

Two of the commonly MPPT algorithms are perturb and observe (P&O), and the incremental conductance (INC). In the implementation, both they rely on measurement of the PV module's voltage and current, and then iteratively adjust a control parameter, typically a constant incremental value, to adjust the output resistance of the PV module. On the other words, a variable resistance device, like a DC-DC converter, would be connected between the PV module and load, and controlled by a constant parameter. Maximum power point of the PV module could be tracked by the principle. The implementation of this principle is shown in Fig. 3.1. A controller of the dc-dc converter implements the decision of the maximum power point tracking for the successive iteration. The basic scheme is shown in Fig. 3.2.

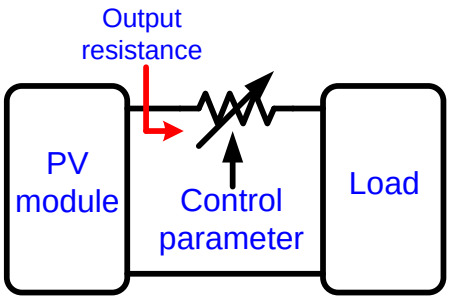


Fig. 3.1 The basic implemented concept of the MPPT principle

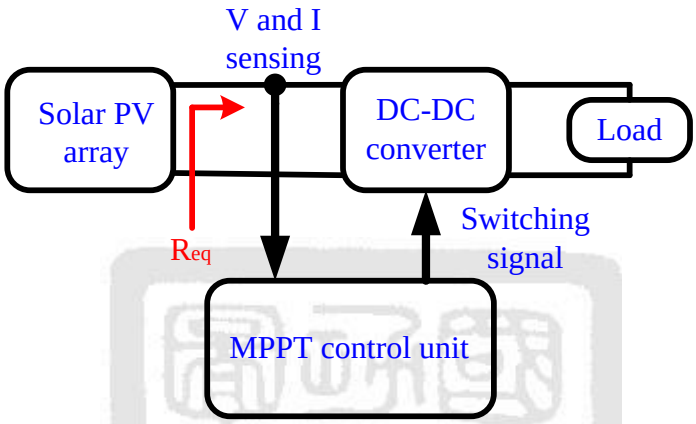


Fig. 3.2 The basic scheme of P&O and INC

The constant incremental control parameter can be the PV array's voltage (ΔV), or the PV array's current (ΔI), or the dc-dc converter's duty cycle (ΔD). This implies a tradeoff in choosing the incremental value by which the controlled parameter is adjusted. If a small value decided, it could decrease the power losses in steady state due to small perturbations around maximum power point. On the contrary, if a large value decided, it could improve the dynamic behavior in situations including quickly changing irradiation conditions or loads [15]. In the following, we will discuss the difference of three constant incremental parameters control mapping on the current–voltage characteristic curves of the PV array, respectively.

It can be observed that the dc-dc converter is controlled so as to reflect a variable load towards the PV array. The first kind of constant incremental control parameter, the PV array's voltage (ΔV), is that the equivalent load line is intersected with the PV array output characteristics [15][25] as shown in Fig. 3.3.

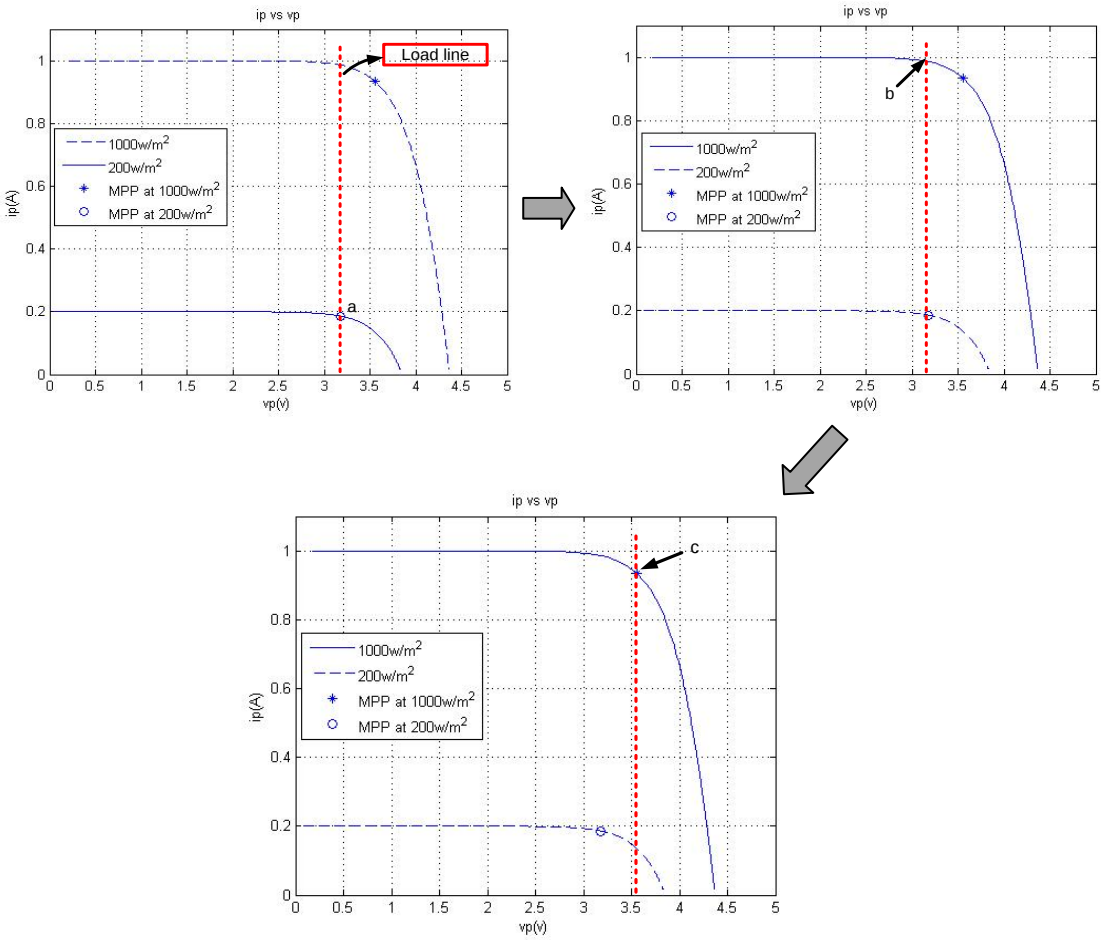


Fig. 3.3 The convergence process of the control parameter ΔV after a rapid change in irradiation

In the Fig. 3.3, it can be seen that the equivalent load line presents a vertical line in the constant ΔV control, and it presents the convergence process after a rapid change in irradiation. In this case, operation at MPP prior to the irradiation change is marked by 'a'. Operation point 'b' represents the operation point right after the irradiation change, before the response and convergence of the maximum power point tracking takes place. After some cycles, operation point 'c' is the final operation point reached due to the tracking of MPP already under another irradiation. In the conclusion, the tracking path is 'a'→'b'→ … →'c'.

The second kind of constant incremental control parameter, the constant dc-dc converter's duty cycle (ΔD) [25], is shown in Fig. 3.4.

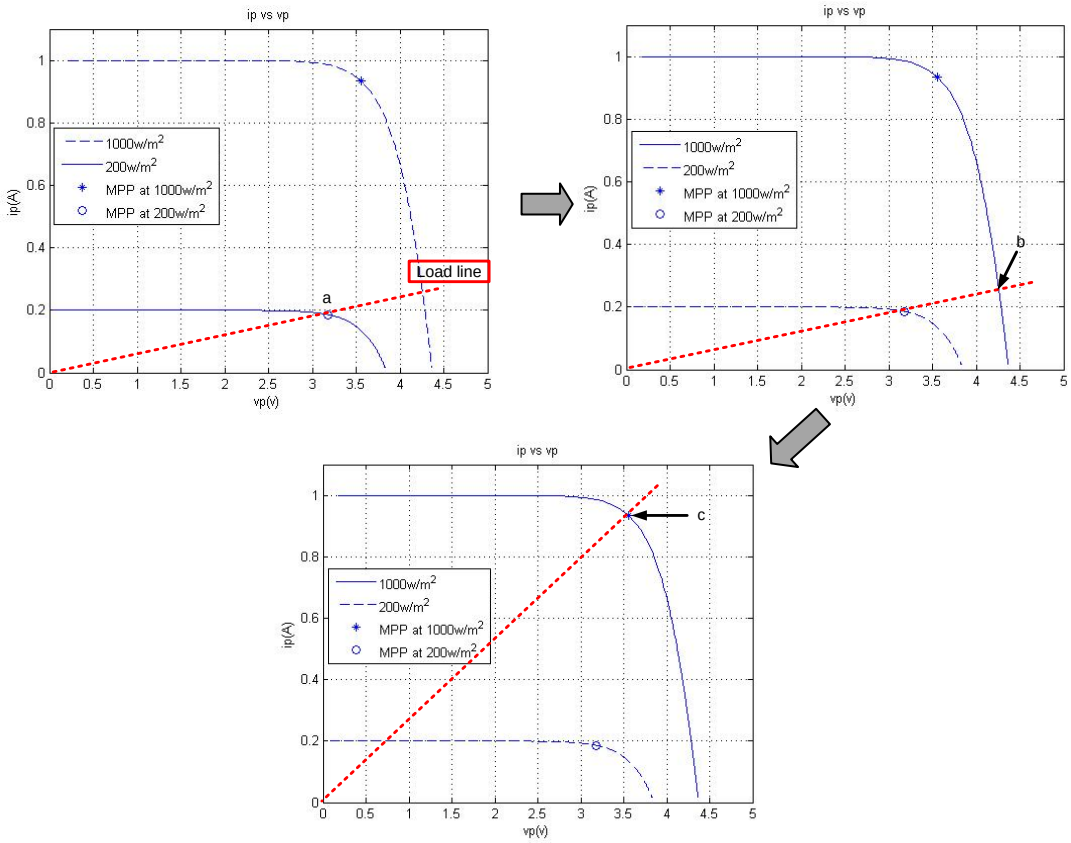


Fig. 3.4 The convergence process of the control parameter ΔD after a rapid change in irradiation

The equivalent load line in the constant dc-dc converter's duty cycle control presents an oblique line through the origin, and the relationship between the equivalent load line and the duty cycle derives from the following equation [25].

$$R_{eq} = \frac{R_{load}}{D^2} \tag{3-1}$$

Where "R_{eq}", "R_{load}", "D", represent the equivalent load toward the PV array, the output load, and duty cycle, respectively. The slope of the equivalent load line is varied by changing the duty ratio and equals to $1/R_{eq}$. While the duty cycle is kept constant, the load is reflected toward the PV array through the converters transfer ratio as if it was a dc transformer. In the Fig. 3.4, it also presents the convergence process after a rapid change in irradiation. The steps is as the above mention, and the tracking path is 'a'→'b'→ … →'c'.

The last kind of constant incremental control parameter, the PV array's current (ΔI) [19], is shown in Fig. 3.5.

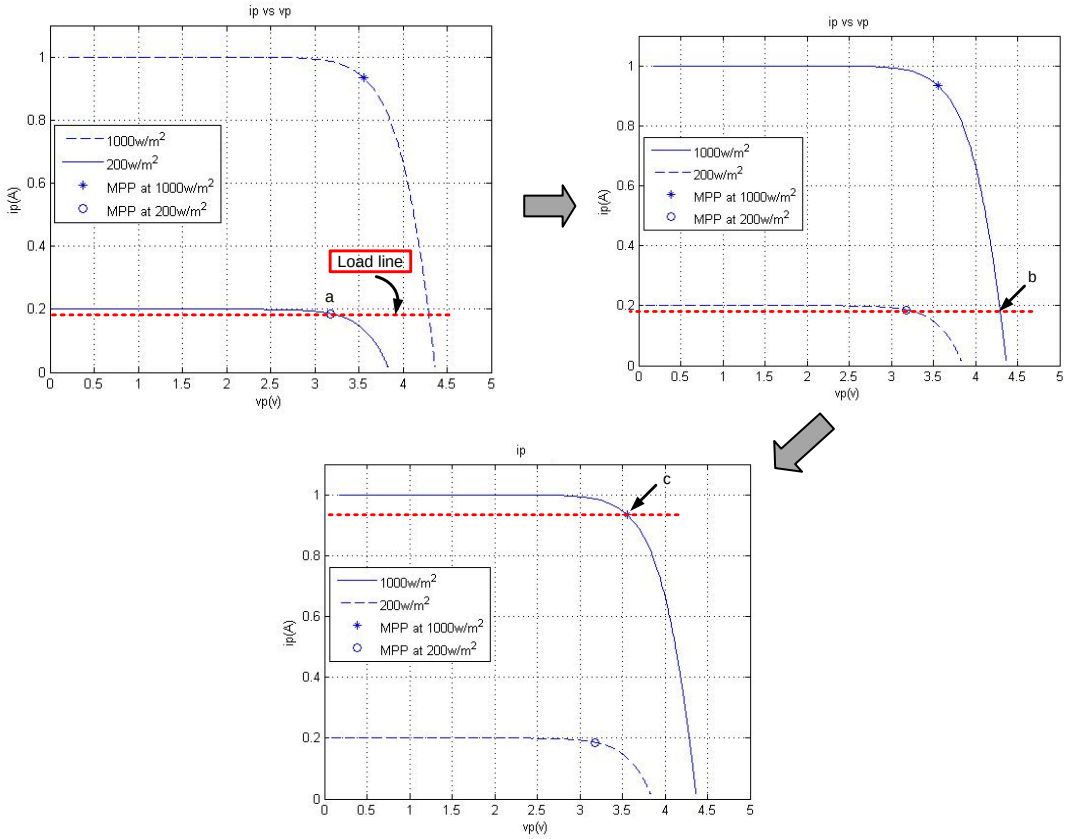


Fig. 3.5 The convergence process of the control parameter ΔI after a rapid change in irradiation

The equivalent load line in the constant PV array's current control presents a horizontal line and it also presents the convergence process after a rapid change in irradiation. The tracking path is 'a'→'b'→ … →'c'.

The implementations of three methods mentioned above have a tradeoff between the speed and the accuracy. Conventionally, some techniques in the recent literatures attempt to decrease the influence of the tradeoff, such as implementing MPPT algorithms with varying step size [15]. But, they impose additional algorithm complexity and hardware and also imply a great deal of computational load. And this is not easy to implement via the simple analog circuits.

3.1.2 Adaptive Load Line Slope (ALLS) Technique

Firstly, we observe the Fig. 3.6, which it shows the I-V characteristics of a PV plane, and presents separated the MPP and the non-MPP regions [26]. If it could be operated only in the MPP region, it would be effective to track the maximum power point.

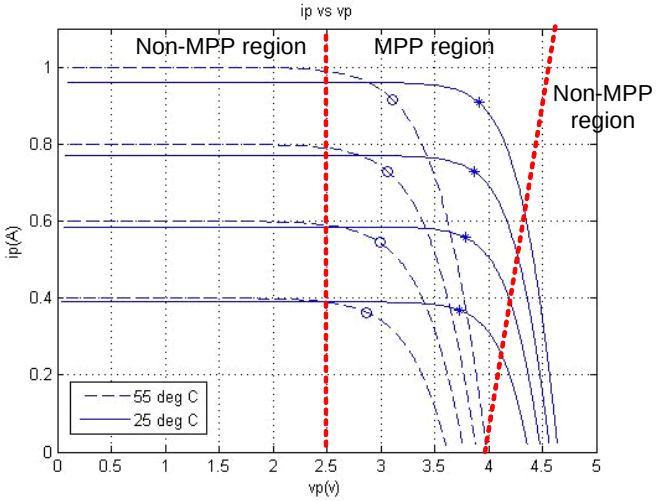


Fig. 3.6 PV array I-V characteristics and regions [26]

Therefore, a simple and effective approach is proposed to accelerate convergence time of conventional MPPT algorithms without sacrificing accuracy. This approach, named adaptive load line slope technique, provides an optimized equivalent load line intersecting in the I-V curve of the PV array, such as Fig. 3.7. The adaptive load line is determined by fitting the MPP of the actual PV array under the different irradiations.

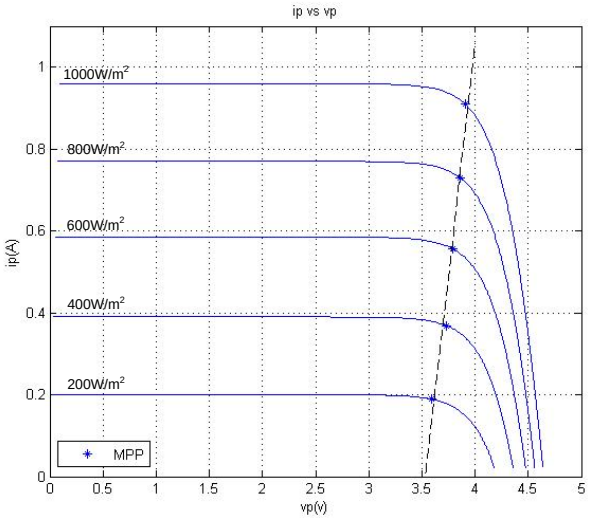


Fig. 3.7 Adaptive load line intersecting with the PV array's I-V curves

The linear equation of this line can be expressed,

$$V_{pv} - kI_{pv} - V_{ref} = 0 \tag{3-2}$$

where V_{pv} is the output voltage of the PV array, I_{pv} is the output current of the PV array, V_{ref} is a constant value crossing on the x-axis and k is the inverse value of the slope.

This line could be implemented by following the equation and controlling through the parameters, V_{pv}, I_{pv}, and V_{ref}. The scheme is shown in Fig. 3.8. Since the true MPP locus is not on a straight line, the value of V_{ref} is also tuned by the MPPT algorithm, so that the adaptive load line moves to different locations, while maintaining the same slope.

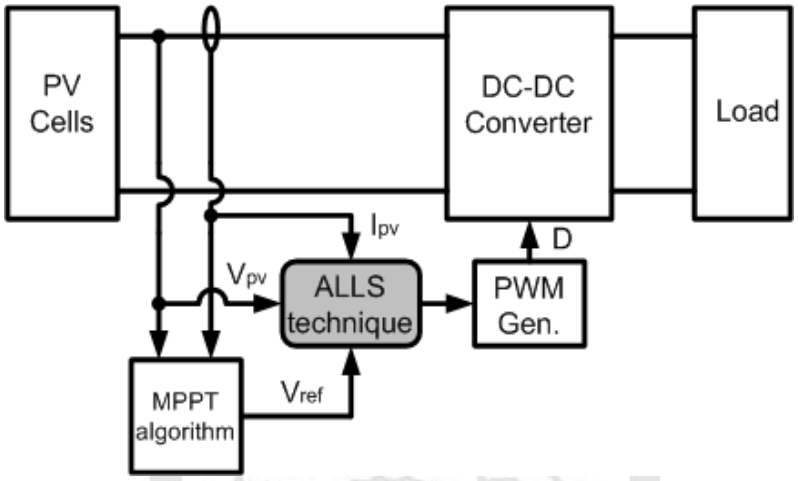


Fig. 3.8 The adaptive load line slope technique scheme

In this way, the PV module is passively operated at the vicinity of the actual maximum power point at any given irradiation. Automatic adjustment of V_{ref} through the MPPT algorithm may be regarded as a steady state fine tuning, bringing the operation point from the vicinity of MPP to the exact MPP. Thus, fast tracking in response to rapid variations of irradiation level is achieved by the adaptive load line matching. Furthermore, since the power around the MPP is quite insensitive to variations of the operation voltage, very little power is lost during the tuning of V_{ref}. Fig. 3.9 describes the operation before and immediately after a rapidly changing in irradiation level. If the PV module was operating at MPP 'a' under the 200W/m^2 irradiation firstly, and then after the irradiation changed to 1000W/m^2 irradiation, the operation point would be at point 'b'. Point 'b' is close to the MPP 'c' under the 1000W/m^2 irradiation, and eventually, fine tuning the V_{ref} is to attain to the exact MPP 'c' accurately. The tracking path is 'a'→'b'→'c'.

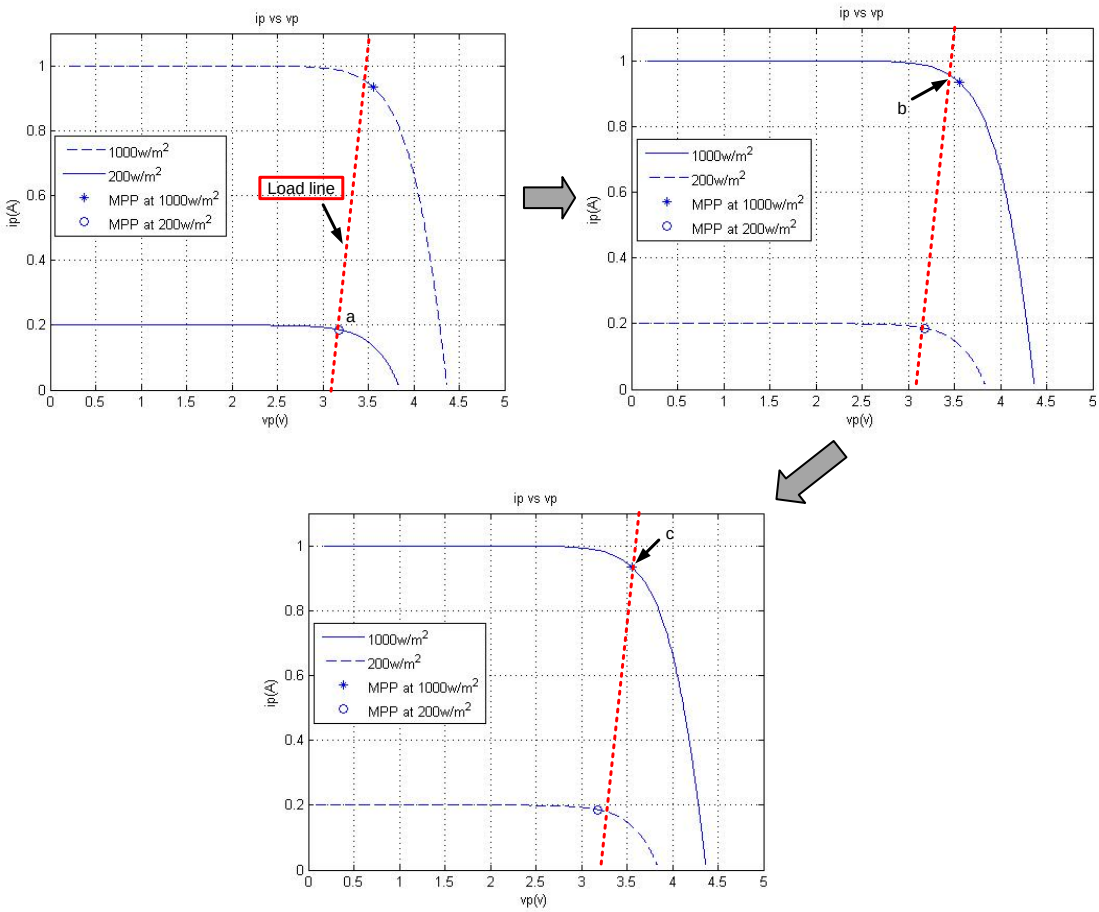


Fig. 3.9 The convergence process of the adaptive load line slope technique after a rapid change in irradiation

3.1.3 Strategy of Transient-State Detecting and Variable Frequency Control

Due to the above mention that the true MPP locus is not on a straight line and the PV module's output may be influenced by the temperature, such as Fig. 2.1 in the chapter 2, the adaptive load line slope technique could not manage well in large change of the PV module's output. In this thesis, the strategy of variable frequency control is proposed to assist in the shortcoming of the adaptive load line slope technique. In the brief, we accelerate the system frequency when the violent transient state happening, and slow down the system frequency as steadily tracking the neighborhood of the MPP. Therefore, how to know if the transient state happens now plays a key role in the strategy of variable frequency control. According to PV module's output power,

$$P_{pv} = V_{pv} \times I_{pv} \tag{3-3}$$

PV module's output voltage will not change large amount immediately due to the adaptive load line slope technique as the rapid change in the PV module's output power happening. Consequently, the PV module's output current change more violently than the PV module's output voltage as the rapid change in the PV module's output power happening due to the PV module's output current proportional to the PV module's output power. As a result, the change rate of the PV module's output current will be a condition to determine if the transient state happens now. Transient states are classed as the positive change and negative change according to the power increasing or decreasing. Fig. 3.10 shows the PV module's output current changing when the negative change in power.

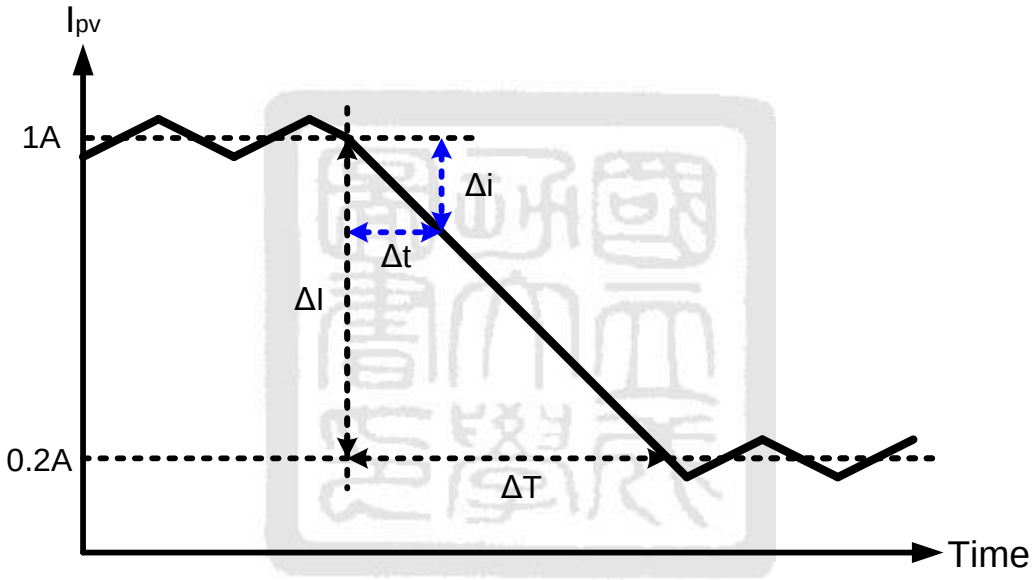


Fig. 3.10 PV module's output current changing when the negative change in power

The definition of the transient condition consists of two parts. One is a fast transient rate and the other is a large change level in power. From Fig. 3.10, the transient rate means the transient time, ΔT, and the change level means the current change, ΔI. We know,

$$\left|\frac{\Delta I}{\Delta T}\right| = \left|\frac{\Delta i}{\Delta t}\right| \tag{3-4}$$

Therefore, if the absolute value of Δi/Δt was greater than a constant value designed over the actual condition, the transient state happens, and then it speeds up the system frequency. In other words, it will speed up the auto-tuning frequency of the step voltage, V_{ref}.

3.2 Wide Power Rating Range MPPT Converter

3.2.1 Low Voltage Mode Structure

The proposed fully chip design is adaptive for the low voltage and low power solar photovoltaic modules. Fig. 3.11 shows the low voltage mode (LV-mode) structure.

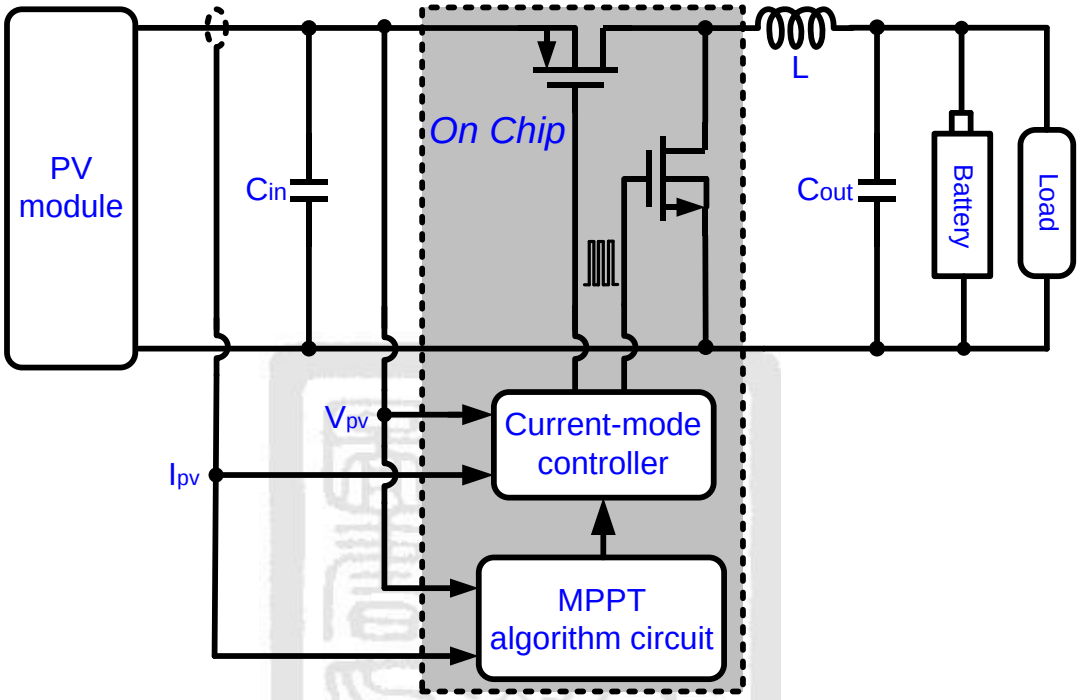


Fig. 3.11 The LV-mode structure

The LV-mode structure includes buck converter with the synchronous power stage on chip. The power flow will deliver to the output load/battery through the chip. However, it must be careful with the limit of power rating of the chip to avoid extensive damage because of the larger power flow through the chip. In this thesis, the LV-mode structure is for the low power PV module within 5V and within about 5 Watt.

3.2.2 High Voltage Mode Structure

For the high power rating applications which occupy important place in the PV system today, the high voltage mode (HV-mode) structure with the CMOS process chip is proposed to achieve the maximum power point tracking and it is shown in Fig. 3.12.

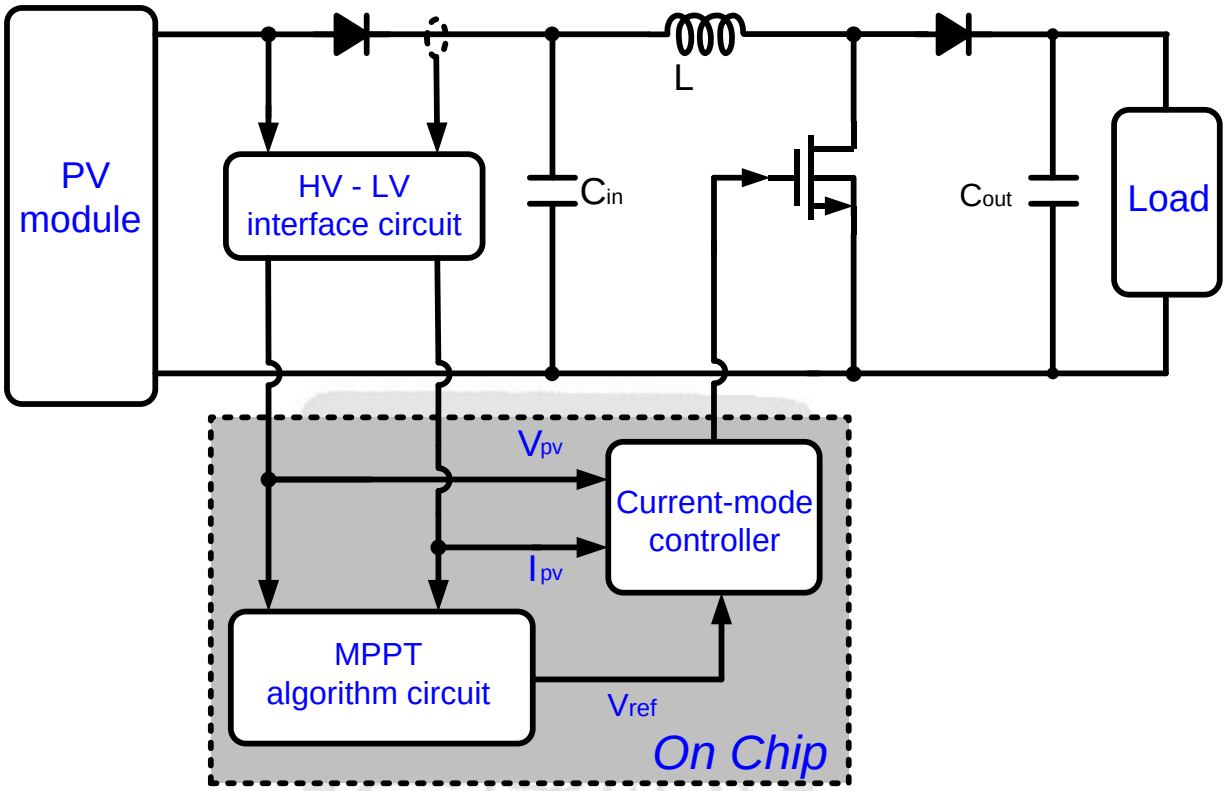


Fig. 3.12 The HV-mode structure

There are some different concerns in the HV-mode structure. The power rating of the solar PV array is large beyond the limit of the chip. So the large power can't flow in the chip directly, in other words, the large power flow must deliver to load through an extra power conditioner, such as a boost converter with a power MOSFET here. For the selection of the power conditioner, the current rating of power MOSFET is lower in the boost topology than in the buck topology. The buck converter requires a high-side MOSFET driver, which is more complex and expensive, but the boost converter needs the low-side driver, which is adaptive to build in the chip. On the other hand, the photovoltaic current in the boost converter is as smooth as its inductor current without any input capacitor. A small and cheap capacitor can further smooth the photovoltaic current and voltage, not like that the buck converter requires a large and expensive capacitor to smooth the discontinuous photovoltaic current and to handle the significant current ripple. However, it must be careful with the connection

between the high voltage part and the chip. The HV-to-LV interface circuits, such as off chip current sensor and voltage sensor, are to connect the high voltage part and the chip, and it protects the chip to avoid the high voltage damage for reliability issues. In this thesis, the HV-mode structure is for the high power PV module within 500V and within about 1 k-Watt.

Chapter 4

Circuit Design

4.1 Architecture of Monolithic MPPT Converter

The design of entire system in this thesis is presented in this chapter. The system block diagram of this MPPT converter is shown in Fig. 4.1.

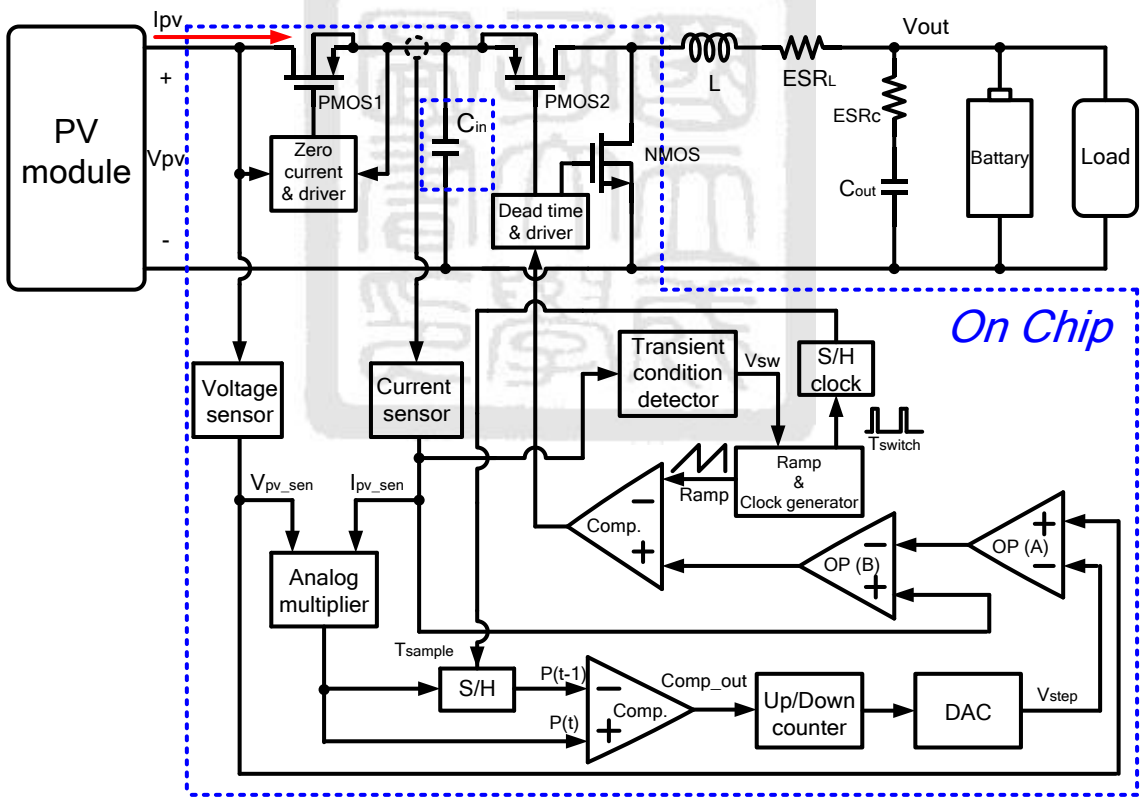


Fig. 4.1 Block diagram of monolithic MPPT converter

In the following several sections, each function block will be discussed in detail and the simulation results are presented.

4.2 Power Transistors of Buck Power Stage

The buck power stage transforms input dc voltage V_{in} into a lower output dc voltage V_{out}. The two power transistors including power PMOS and power NMOS are regarded as switching elements, as shown in Fig.4.2. The buck power stage is a bridge between photovoltaic source and load circuits or a dc-bus. Theoretically, it is desired that power stage dissipates no power and power from PV module will completely delivers to load circuits, but it's impossible because all the components are not ideal. From description mentioned above, we know that reducing the power dissipation of MPPT converter to obtain higher conversion efficiency is an essential objective in circuit design.

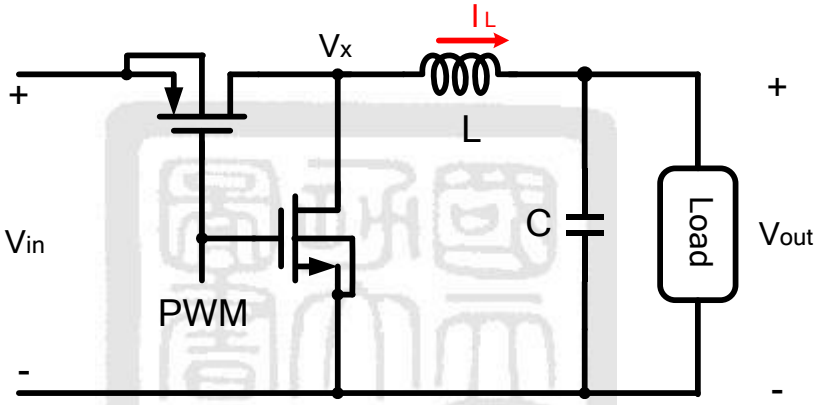


Fig. 4.2 Power transistors of buck power stage

When the power transistor conducts, the large current will flows through it to cause power dissipation. The power dissipation due to the on-resistance of power transistor is expressed as follows:

$$P_{conduction} = D \cdot I_{load}^2 R_{on,p} + (1-D) \cdot I_{load}^2 R_{on,n} \quad (4\text{-}1)$$

where

$$R_{on,p} = \frac{1}{\mu_p C_{ox} \left(\frac{W}{L}\right)_p \left|V_{gs} - V_t\right|}; \quad (4\text{-}2)$$

$$R_{on,n} = \frac{1}{\mu_n C_{ox} \left(\frac{W}{L}\right)_n \left|V_{gs} - V_t\right|} \quad (4\text{-}3)$$

In order to diminish this power dissipation, the only way is to reduce the $R_{on,p}$ and $R_{on,n}$. By the efficiency requirement larger than 80%, the ratio W/L must be several ten thousands. The huge size of power transistors usually occupy approximately half

to two-thirds of whole chip layout area. As a results, I design the $R_{on,p}=R_{on,n}\fallingdotseq 0.2\Omega$, and the W/L ratio of PMOS and NMOS can be calculated. After considering the 20% process variation, the W/L ratio, $\left(\frac{W}{L}\right)_p=\left(\frac{60000}{0.5}\right)$(μ m/μ m) and $\left(\frac{W}{L}\right)_n=\left(\frac{24000}{0.5}\right)$(μ m/μ m) are decided.

4.2.1 Distributed and Weighted Conduction [27]

The driving circuit of output stage with distributed and weighted conduction is as shown in Fig. 4.3.

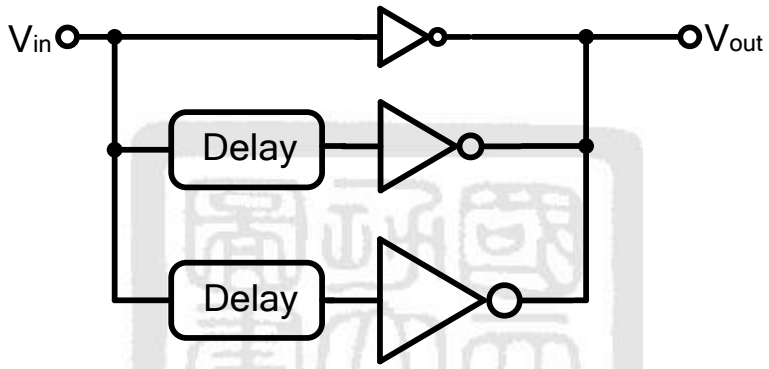


Fig. 4.3 The general idea of distributed and weighted conduction

Fig. 4.3 shows that signal flow is via many buffers, which are different sizes, from V_{in} to V_{out}. The delay circuits designed adaptively can conduct different output stages in time. This will decrease the di/dt of the output current as input signal changing. On the other word, down slope of the output waves will be smooth, not steep and be a solution of the decrease of ringing or supply bounce.

In this thesis, utility of the conception is to decrease of supply bounce and to increase reliability. When the large size of power transistor is turned off by the duty cycle signal control, the input current of PMOS is down to zero steeply and the di/dt of current is large. It could cause to the problem of supply bounce or even EMI possibly.

As a result, I will divide a large size p-type transistor into some small sizes p-type transistors paralleled each other. As the following equation:

$$\left(\frac{W_{total}}{L}\right)_p=\left(\frac{W_1}{L}\right)_{p1}+\left(\frac{W_2}{L}\right)_{p2}+\left(\frac{W_3}{L}\right)_{p3}+\left(\frac{W_4}{L}\right)_{p4}+\left(\frac{W_5}{L}\right)_{p5}+\left(\frac{W_6}{L}\right)_{p6} \qquad (4\text{-}4)$$

where

$$W_{total} = W_1 + W_2 + W_3 + W_4 + W_5 + W_6 \quad \text{and} \quad W_1 >> W_2, W_3, \ldots$$

Design the delay circuits to conduct these small size p-type transistors in different time. As similar as p-type transistor is conducted by one to one as shown in Fig. 4.4

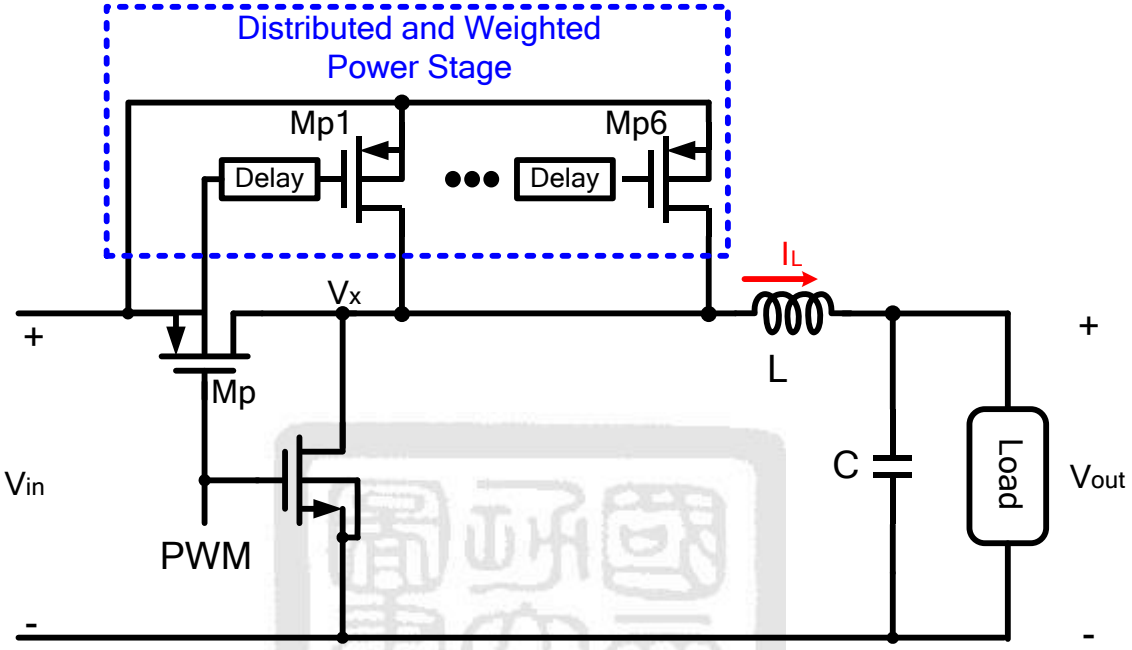


Fig. 4.4 Power stage with distributed and weighted

The simulation result is shown as Fig. 4.5

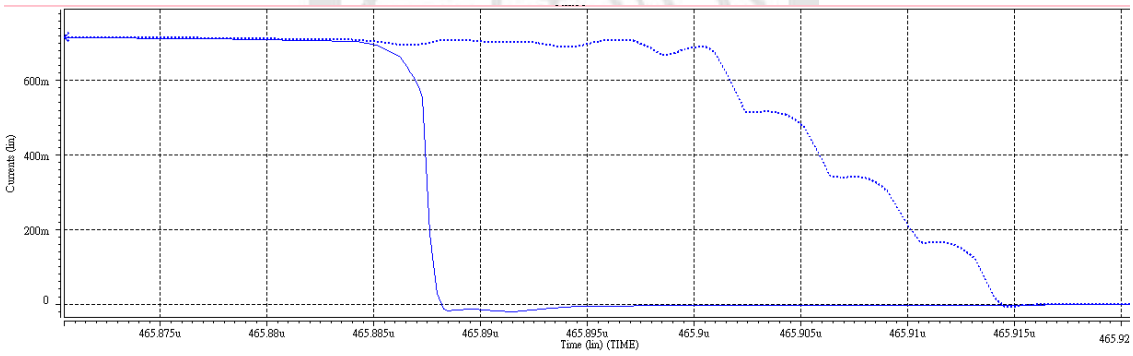


Fig. 4.5 Input current of PMOS with distributed and weighted and without distributed and weighted

Form the Fig. 4.5, it can be seen that the solid line stands for the input current of PMOS without distributed and weighted function and it has a steep change in current as the PMOS turning off. On the other hand, the dotted line stands for the input current of PMOS with distributed and weighted function and the smoother change in current than the solid line as the PMOS turning off. Fig. 4.6 shows the comparison

with the di/dt of input current of PMOS with and without distributed and weighted, and it presents the improvement about five times in the instantaneous current change.

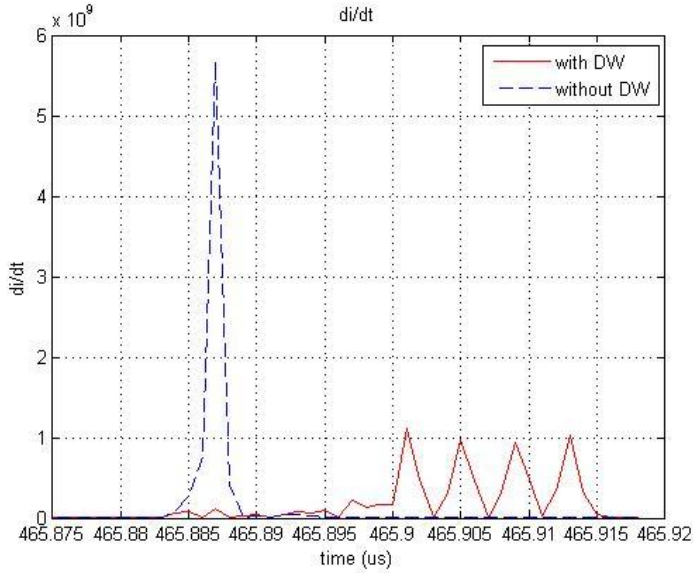


Fig. 4.6 The comparison with di/dt of input current of PMOS with distributed and weighted and without distributed and weighted

4.3 Current Sensor and On Chip Blocking Diode

For the MPPT converter with current-mode control and MPPT algorithm, it is necessary to obtain the information of PV output current. As the above mention in the chapter 2, buck topology used in MPPT converter requires a large capacitor to smooth the discontinuous input current from the photovoltaic module, and to handle significant current ripple. For the reason, the PV current sensing is difficult to sense from inductor current of buck topology. As the Fig. 4.7, it can be seen that inductor current is not equal to the PV output current according to KCL.

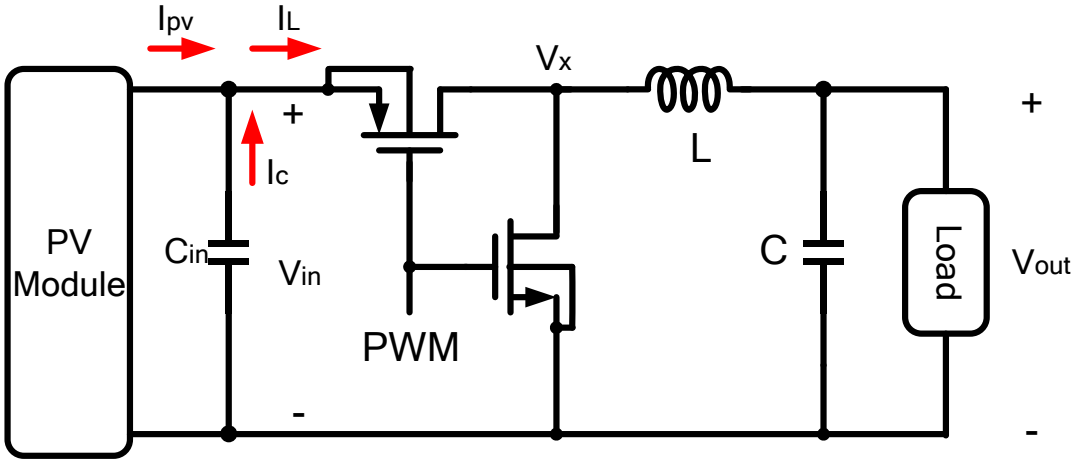


Fig. 4.7 Relationship between inductor current and PV output current

The inductor current is

$$I_L = I_{pv} + I_c \tag{4-5}$$

where I_{pv} is PV output current and I_C is discharge current. Because I_C is the time function of the PV output current, the instantaneous value of I_C is not known. The inductor current does not be known well and not adaptively be sensed in MPPT converter. Therefore, an additional current sensing circuit is needed to sense the PV output current signal in MPPT converter. Conventional current-sensing method is to insert a sensing resistor in the path of the current to be sensed. This method incurs significant power loss, especially when the current sensed is high. Therefore, a CMOS on-chip current sensing circuit with low power dissipation shown in Fig. 4.8 is adopted in this thesis.

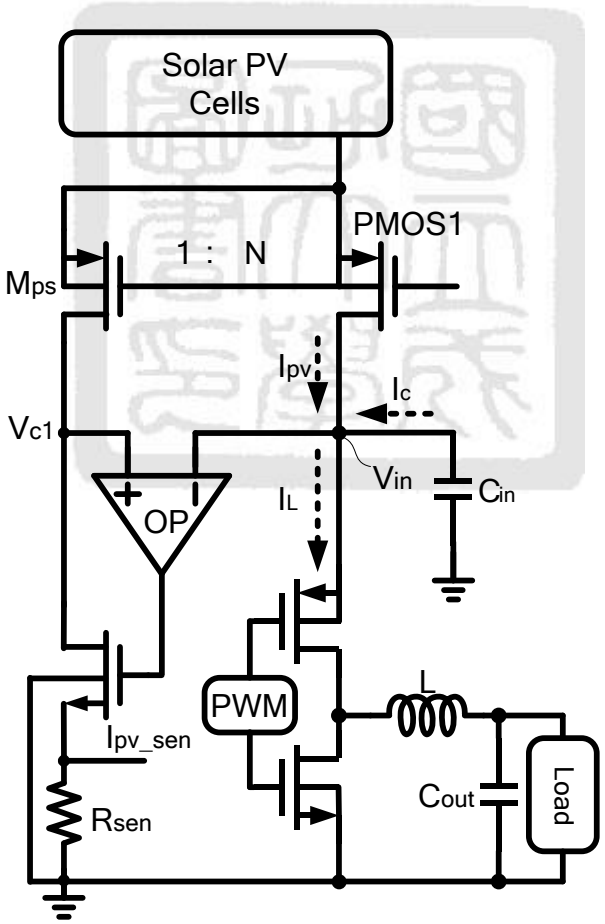


Fig. 4.8 The current sensing circuit

As a result, directly sensing I_{pv} with another transistor between PV module and the large input capacitor is a convenient method. The method here is also called

"SenseFETs" technique. The main idea is to build a current sensing FET M_{ps} in parallel with the transistor 'PMOS1', which is always turned on under the generally operating condition, and use its measuring capabilities for sensing the PV output current. The effective width of the current sensing FET M_{ps} is significantly smaller than the large size transistor PMOS1 to guarantee that the power dissipation in the current sensing FET M_{ps} is low. The width ratio of M_{ps} to PMOS1, 1: N is 1:1000 in my design. The voltages of nodes V_{in} and V_{c1} should be equal to eliminate the current mirror non-idealities from channel-length modulation. The operation amplifier (OP) is used to force voltage of nodes V_{in} and V_{c1} to be equal. The sensing signal I_{pv_sen} is given by

$$I_{pv\_sen} = \frac{I_{pv}}{N} \cdot R_{s\,e} \tag{4-6}$$

where N=1000 and R=1kΩ in my design.

As the N increases, the accuracy of the circuit decreases as the matching accuracy of MOSFETs degrades. Hence, the adequate value of N is acceptable.

While the addition of the transistor PMOS1 will incurs the conduction power losses, even if it has a small $R_{ds,on}$, the motivation of the device is good to use in the photovoltaic MPPT converter. It is also as a special protecting circuit, well-known a blocking diode, in the photovoltaic system. In most applications, the photovoltaic array acts as a power source to energize devices capable of storing electricity or a utility grid. However, the capacity of solar generation systems depends heavily on the presence of light. At night, a current could flow back into photovoltaic cells from the bus; however, reverse current must be avoided because it causes leakage loss, extensive damage, or could even cause a fire [22]. Blocking diodes are effective to prevent reverse current flows. However, in the buck interface, the blocking diode is an additional discrete component conventionally that is needed to conduct the full photovoltaic current as shown in Fig. 4.9. This results in an increase in cost and additional power loss due to the forward voltage drop.

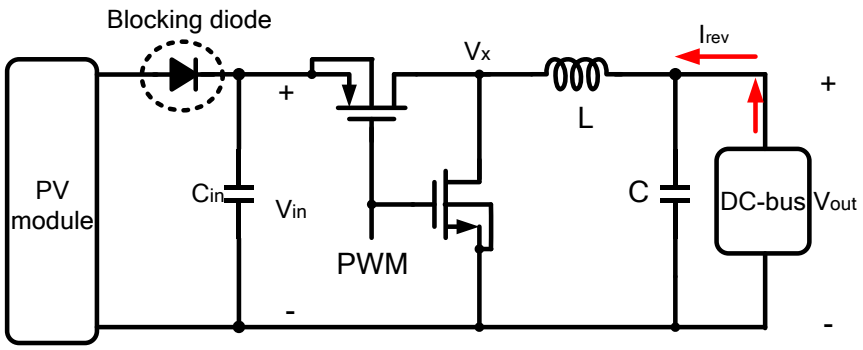


Fig. 4.9 Conventional blocking diode in PV system

In this thesis, transistor PMOS1 is also regarded as the capacity of diode and as an active rectifier on chip. It is shown in Fig. 4.10 and the technique is named CMOS-control rectifier (CCR) [28].

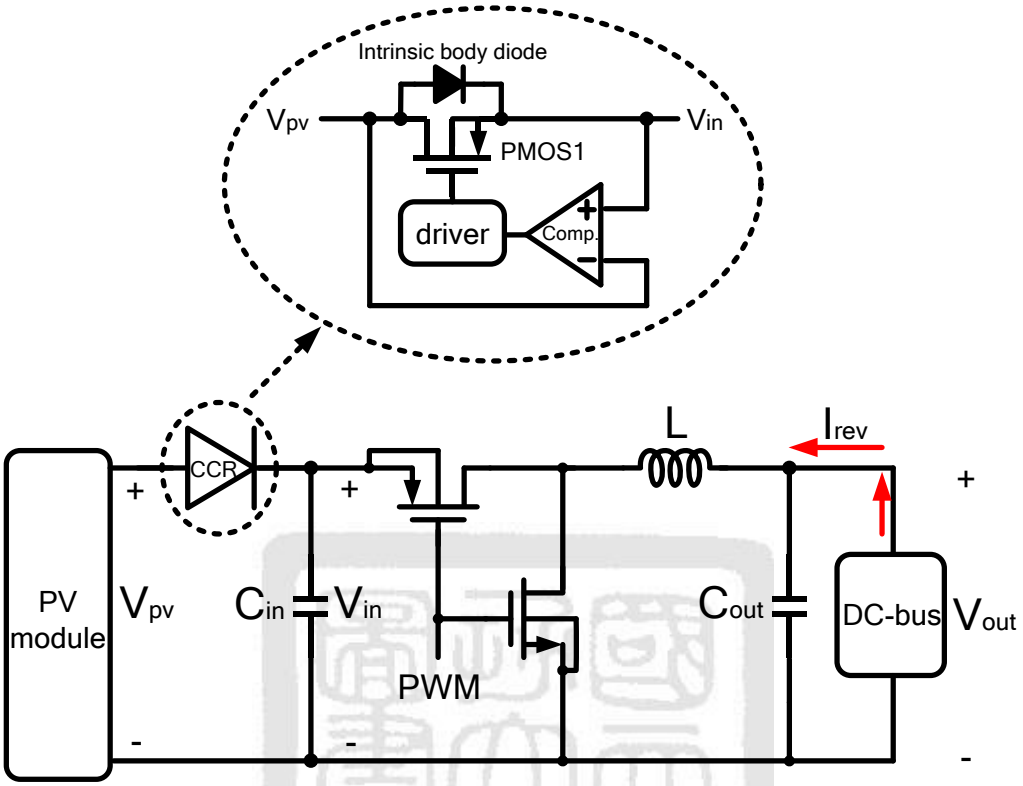


Fig. 4.10 On chip blocking diode with CCR

A CMOS-control rectifier (CCR) is proposed to prevent reverse current flows from the DC-bus as PV module outage and provide mV-range forward-voltage drop for highly efficient MPPT converters. The body terminal of PMOS1 is connected to the output terminal of the CCR to prevent any unwanted reverse current through the intrinsic body diode of PMOS1.

4.4 MPPT Algorithm Circuits

MPPT algorithm circuit is an essential part in the monolithic system. It must execute the simple MPPT algorithm, like P&O, as the flow chart Fig. 4.11 and decide the correct perturbation direction in every cycle. The detail block diagram of MPPT algorithm circuits is shown in Fig.4.12.

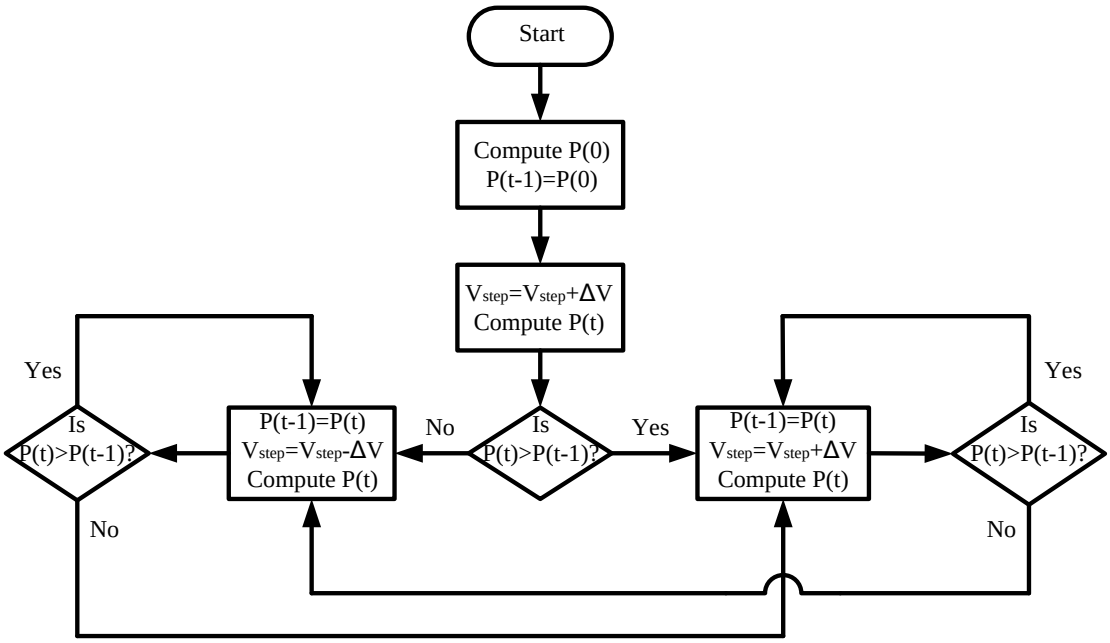


Fig. 4.11 The flow chart of MPPT algorithm

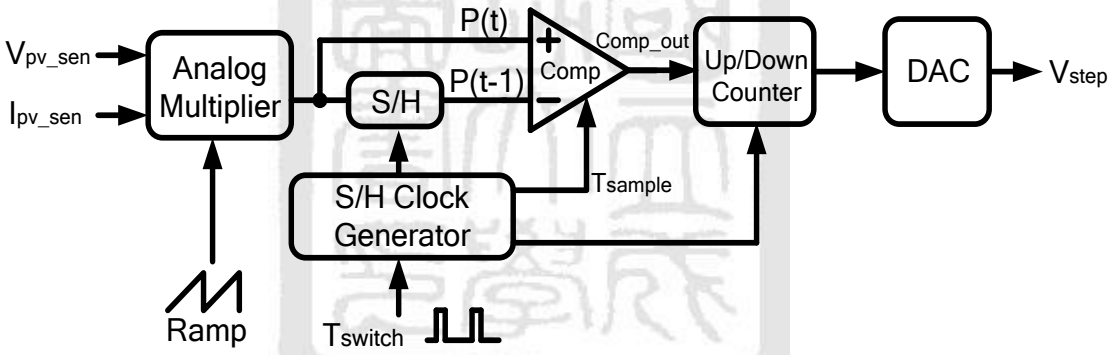


Fig. 4.12 The block diagram of MPPT algorithm circuits

The detail circuit design will be discussed respectively in the following sections.

4.4.1 Analog Multiplier

The first step of MPPT algorithm is needed to get the product of the current sensing signal and voltage sensing signal. Therefore, there is a multiplier needed here, and process the current sensing signal and voltage sensing signal. Conventionally, the implementation of MPPT algorithm circuit uses a microprocessor to achieve the MPPT calculation. The multiplier unit in the microprocessor is a digital multiplier. Firstly, the sensing signals are converted to digital signals by analog-to-digital converter, and secondly, multiplying these digital signals is executed by digital multiplier. Because the amount of digital circuits is too huge, it is not adaptive in my

design. On the contrary, the selection of simpler multiplier is analog style. The analog multiplier of my MPPT algorithm circuit is shown Fig. 4.13.

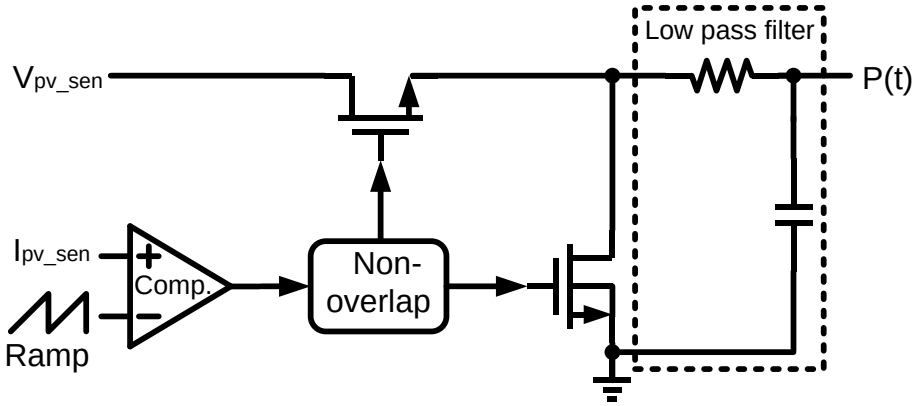


Fig. 4.13 Analog multiplier circuit

A configuration produces a two-quadrant product of analog signals but uses no log amplifiers. The voltage sensing signal V_{pv_sen} and the current sensing signal I_{pv_sen} are the multiplier inputs. The ramp signal is produced from ramp generator of current mode control circuit, mentioned at next section. V_{pv_sen} and I_{pv_sen} may assume both positive values. Fig. 4.14 shows the waveforms.

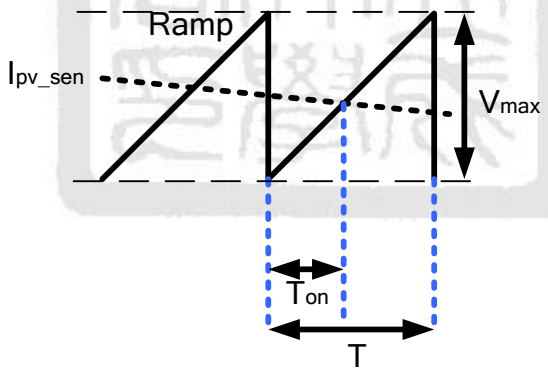


Fig. 4.14 Ramp waveform and I_{pv_sen} waveform

The comparator allows the V_{pv_sen} signal to reach the RC low-pass filter only when I_{pv_sen} exceeds the amplitude of the ramp wave supplied by the ramp generator. The lowpass-filtered signal at the output is P(t), derived as follow.

$$\frac{T_{on}}{T} = \frac{I_{pv\_sen}}{V_{max}}$$

$$P(t) = \frac{1}{T}\int V_{pv\_sen}dt = V_{pv\_sen}\frac{T_{on}}{T} = \frac{V_{pv\_sen}\cdot I_{pv\_sen}}{V_{max}} \quad (4\text{-}7)$$

From Eq. 4-7, the output of this multiplier, P(t), is proportional to the product of the V_{pv_sen} and I_{pv_sen}.

4.4.2 Sample and Hold (S/H) Circuit and Comparator

The output of multiplier, P(t), is delivered to the one input of MPP comparator, and then compares with the other input, P(t-1), held by a capacitor in the sample and hold (S/H) circuit. Fig. 4.15 shows the circuits.

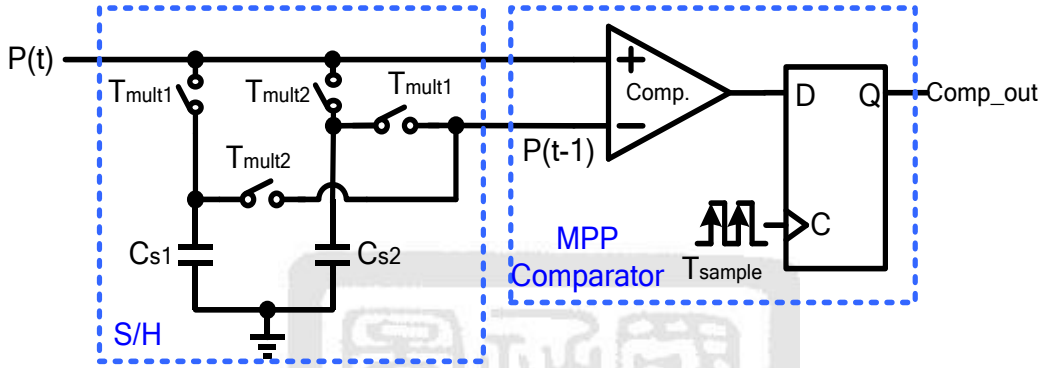


Fig. 4.15 S/H circuit and MPP comparator

Where the sample and hold circuit employs two capacitors to sample and hold the value of P(t) simultaneously. Four switches controlled by the clock signals T_{mult1} and T_{mult2} from the S/H clock generator achieve the operation of sampling and holding data. When the phase of the T_{mult1} is on and T_{mult2} is off, C_{s1} is sampling P(t) and P(t-1) held in C_{s2}, delivers to negative input of the comparator. If P(t) > P(t-1) at the positive trigger of the clock T_{smaple}, the output of MPP comparator, Comp_out, does not change. Relatively, if P(t) < P(t-1), the output of MPP comparator, Comp_out, should change to the opposite phase.

The clock signals, T_{smaple}, T_{mult1}, and T_{mult2}, are shown in Fig. 4.16.

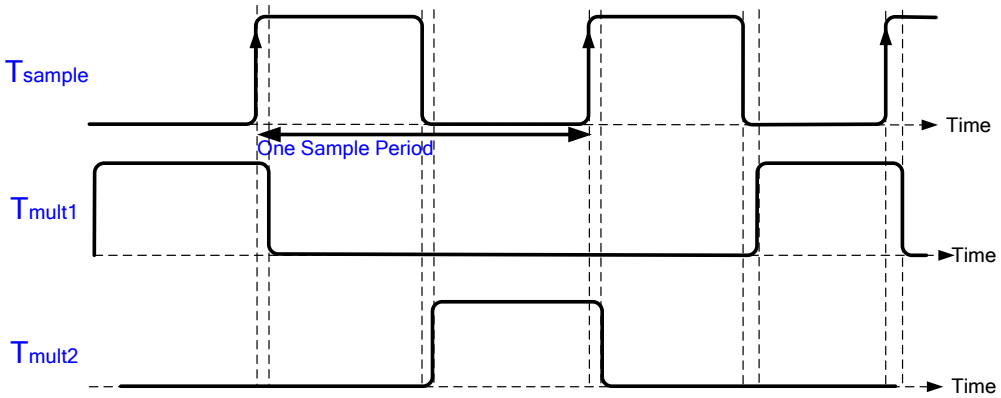


Fig. 4.16 Clock waveforms produced by S/H clock generator

The number of sampling data in every one period is only one time. The clock signals, T_{smaple}, T_{mult1}, and T_{mult2}, are generated by the S/H clock generator shown in Fig. 4.17.

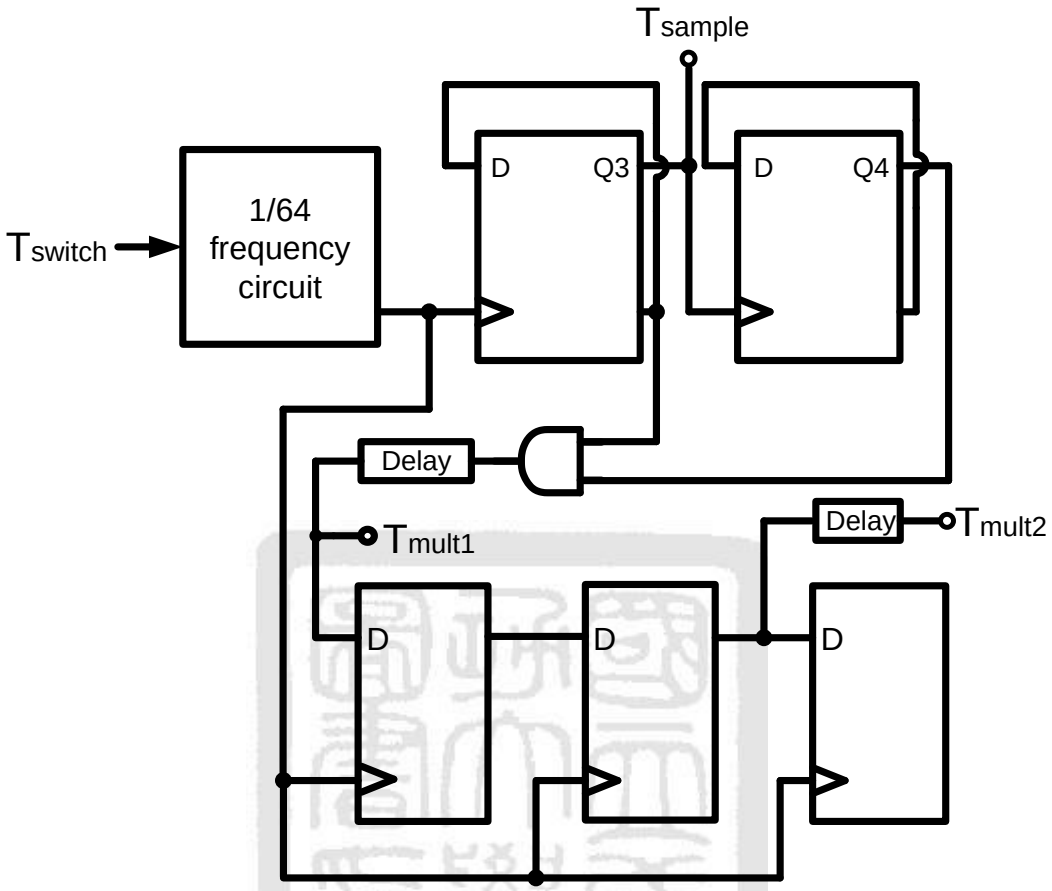


Fig. 4.17 S/H clock generator

From the Fig. 4.17, it can be seen that the S/H clock generator is made of many D flip flops as frequency dividers and some logic circuits. The S/H clock generator is a dependent clock generator relating to the high frequency signal, T_{switch}, which is switching frequency of buck power stage. Because of the changing rate of the PV output, T_{sample} does not need to be as fast as the switching frequency. The T_{sample} must to slow down from the switching frequency. The simulation results are shown in Fig.4.18.

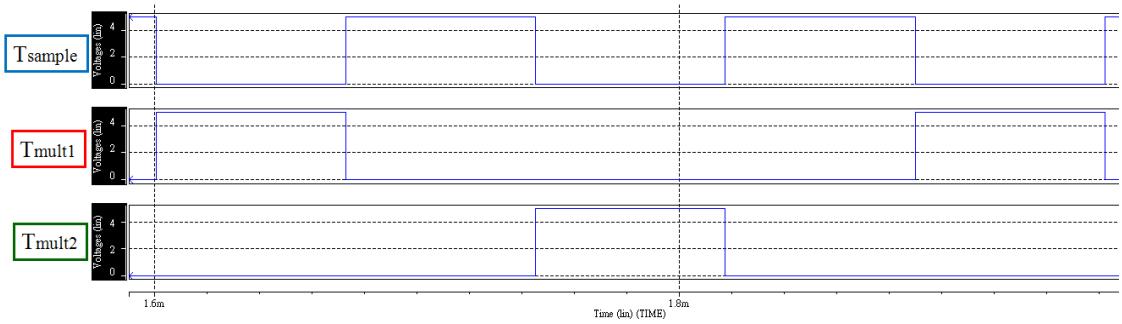


Fig. 4.18 The simulation results of T_{sample}, T_{mult1}, T_{mult2}

4.4.3 Up/Down Counter

The purpose of the counter is to execute the correct direction of the perturbation in MPPT algorithm. Up counting and down counting stand for increasing perturbation and decreasing perturbation, respectively. A 5-bit synchronous up/down counter is employed here as shown in Fig. 4.19.

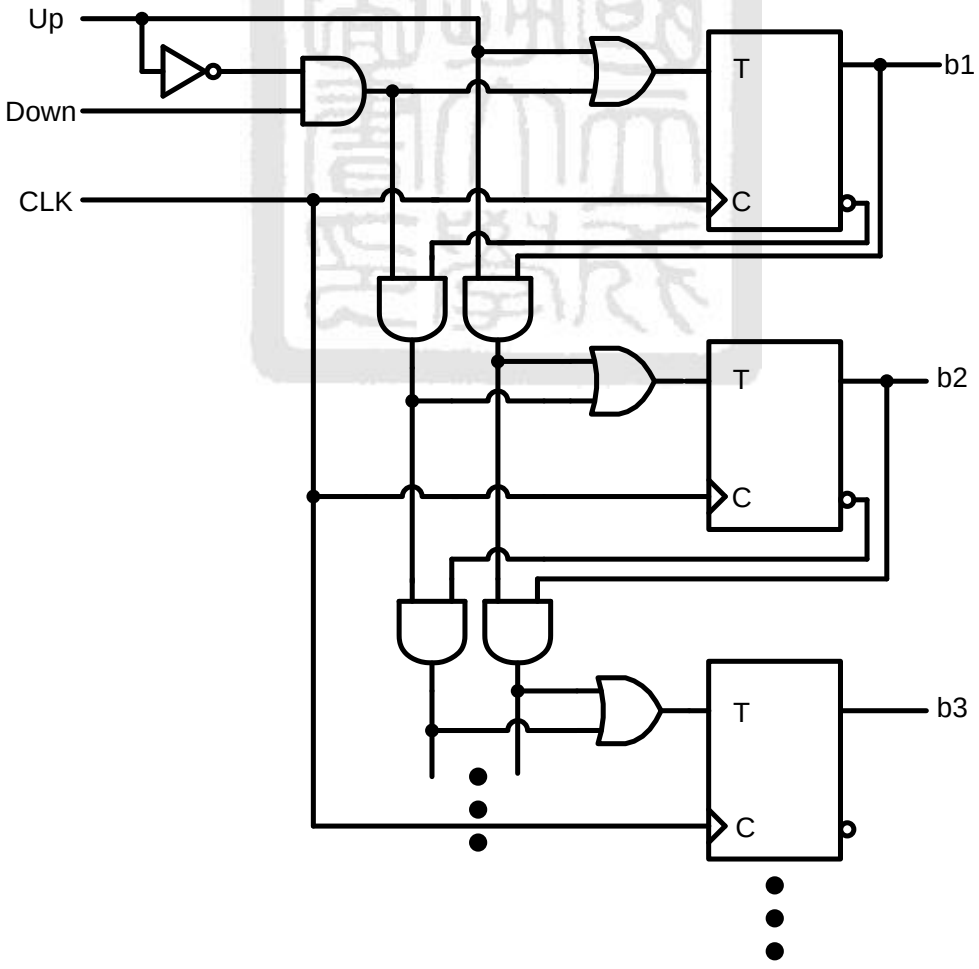


Fig. 4.19 5-bit up/down counter

The up/down counter can reverse order from the maximum number of binary code down to the minimum number of binary code and back to the maximum number to repeat the count. But the characteristic of the up/down counter is not adaptive in my design. The phenomenon of counting reversely must be prevented. Counting reversely would cause the failure of maximum power point tracking. Fig. 4.20 is shown as following, and the proposed up/down counter in my design.

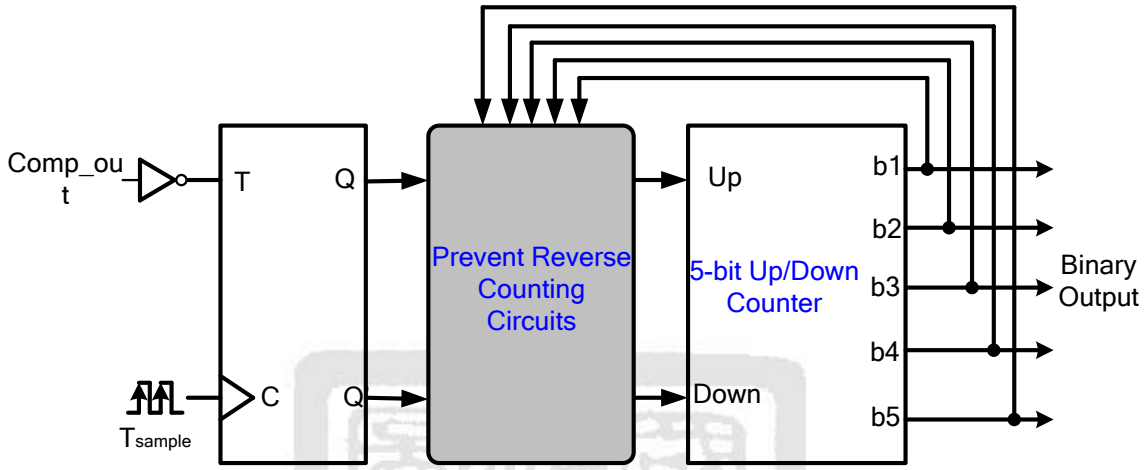


Fig. 4.20 The proposed up/down counter

The proposed up/down counter consists of a T flip flop, prevent reverse counting circuits and 5-bit up/down counter. The input signal, Comp_out, is produce from the output of the MPP converter. T flip flop is a toggle with the input signal, Comp_out, and the characteristic table of the operation is as the Table 4.1

Table 4.1 Characteristic table of the T flip flop's operation

Comp_out	Q(t+1)	Q'(t+1)
0	Q'(t)	Q(t)
1	Q(t)	Q'(t)

Prevent reverse counting circuits are formed by some logic gates with a truth table and to avoid reverse counting. This circuit is too simple that it doesn't show details in this thesis.

4.4.4 Resistor String DAC [29]

In this MPPT algorithm, an analog reference value, needed to be produced, is an important parameter and then is delivered to the proposed current mode control circuit,

named adaptive load line slope control circuit. So a digital to analog converter (DAC) is used to convert the binary output of up/down counter to an analog value. In my design, a resistor string DAC is selected due to its simple structure, low power, and guaranteed monotonicity. The 5-bit resistor string DAC is shown Fig. 4.21.

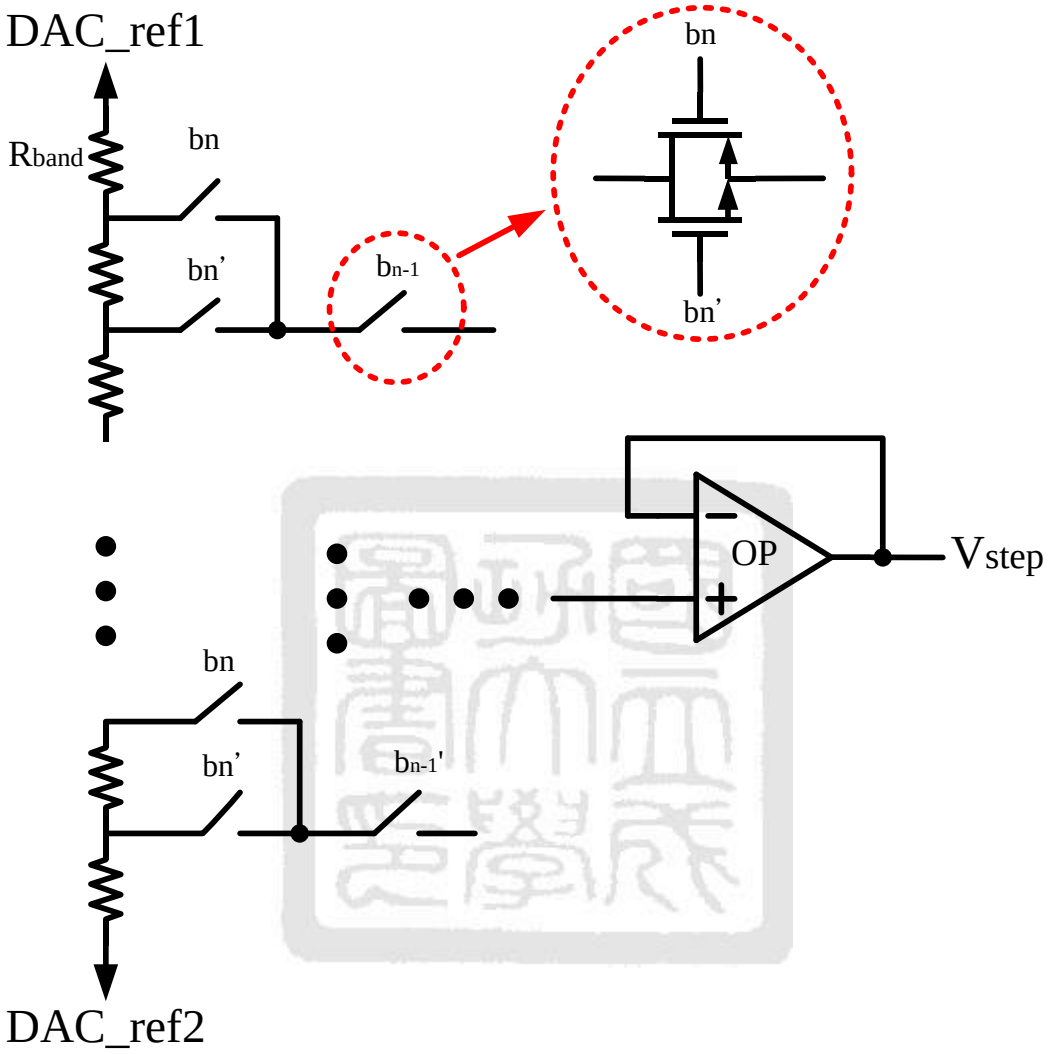


Fig. 4.21 5-bit resistor string DAC

Where it consists of the resistor string, switches controlled by the binary output of up/down counter, and a buffer, the output signal, V_{step}, is between the reference voltage DAC_ref1 and DAC_ref2, which are designed for real conditions. A resistor of the resistor string, R_{band}, is a large resistance for the concern of low power loss. A cross voltage of a resistor of the resistor string is the voltage of one LSB, and the V_{step} will increase (decrease) one LSB voltage every cycle. Transmission gates might be used rather than n-channel switches for reducing switch resistance, and the minimum size of a transmission gate is designed for reducing the layout area.

4.5 Proposed Current-Mode Control Circuits

The proposed current-mode control circuits are the implementation of the adaptive load line slope control method which was discussed in the chapter 3. We expect that an adaptive load line slope is implemented by PWM modulation through some given parameters like the voltage sensing signal, the current sensing signal and the output of MPPT algorithm. The circuits design will be discussed in detail in the following sections.

4.5.1 Adaptive Load Line Slope Control Circuit

For implementing the linear equation of the adaptive load line, that the linear equation is derived as follow,

$$V_{pv} - kI_{pv} - V_{ref} = 0 \tag{4-8}$$

It can be converted to

$$I_{pv} - \frac{1}{k}(V_{pv} - V_{ref}) = 0 \tag{4-9}$$

where V_{ref} are the voltage value as I_{pv} is zero. Here V_{ref} will be substituted by the output signal V_{step} of the controllable MPPT algorithm circuit as the Eq. (4-10),

$$I_{pv\_sen} - \frac{1}{k}(V_{pv\_sen} - V_{step}) = 0 \tag{4-10}$$

The proposed circuit is shown in Fig. 4.22.

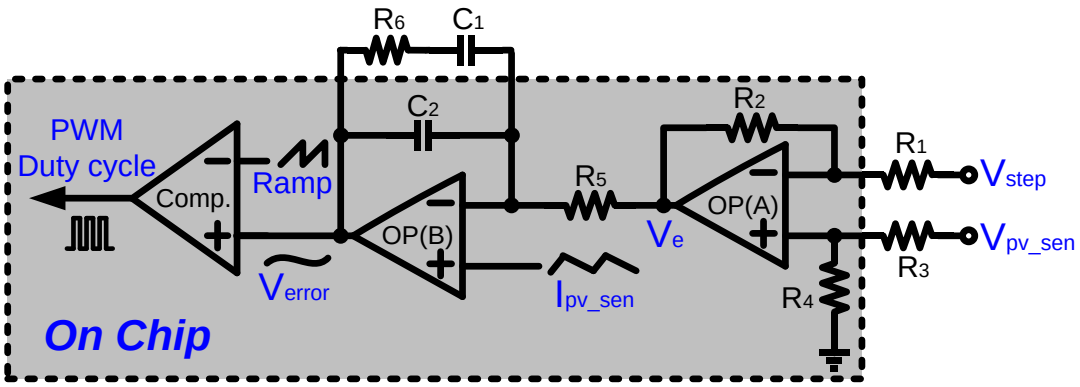


Fig. 4.22 Adaptive Load Line Slope Control Circuit

From Eq. (4-10), it can be seen that the slope of the linear equation is 1/k, and multiplies the difference of PV voltage V_{pv} and V_{step}. In the Fig. 4.22, a fully

differential operational amplifier (OP) is used here to calculate the difference of V_{pv_sen} and V_{step}, and the gain of this operational amplifier stands for the slope of the linear equation, which means that the gain should be equal to 1/k. However, the slope of the adaptive load line may be different from the IV-curves of the different PV modules. Therefore, the gain of this operational amplifier must be adjustable for the actual PV module's IV-curves. Resistor R_1 and R_3 are designed off chip to decide the gain of the operational amplifier.

$$\frac{R2}{R1}=\frac{R4}{R3}=\frac{1}{k} \tag{4.11}$$

The second part of the linear equation is to subtract the output of the operational amplifier, V_e, from the sensing current signal, I_{pv_sen}, and the value has zero if tracked to maximum power point already. Another operational amplifier would be used here to execute the subtraction, but the signals V_e and I_{pv_sen} both have unwanted high frequency noise on them because of the PWM modulation switching noise. The noise will cause the instable output of the subtraction and then the failure on MPPT function. Therefore, type-II compensator is employed here as a low-pass filter to keep from the pass of high frequency noise. It is shown in Fig. 4.23 and its transfer function can be calculated as:

$$\frac{V_{error}(s)}{V_e(s)}=-\frac{1+sR_6C_1}{sR_5(C_1+C_2)(1+sR_6\frac{C_1C_2}{C_1+C_2})} \tag{4-12}$$

If C1>>C2, the transfer function becomes:

$$\frac{V_{error}(s)}{V_e(s)}=-\frac{1+sR_6C_1}{sR_5(C_1+C_2)(1+sR_6C_2)} \tag{4-13}$$

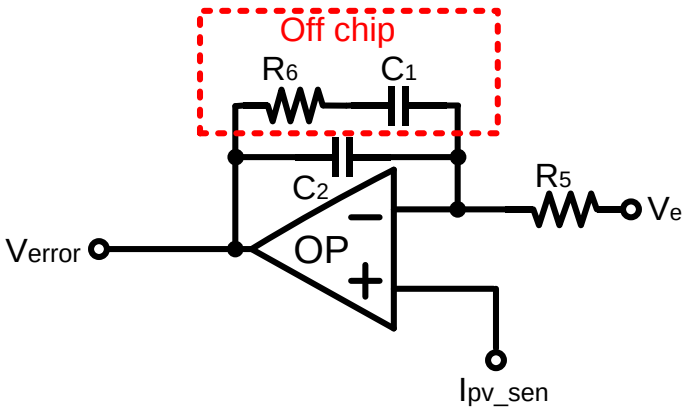


Fig. 4.23 Type-II compensator

The poles locate at the origin and frequency $f_p = \frac{1}{2\pi \cdot C_2 R_6}$. The zero locates at frequency $f_z = \frac{1}{2\pi \cdot R_6 C_1}$. The gain and phase of type-II compensator is shown in Fig. 4.24.

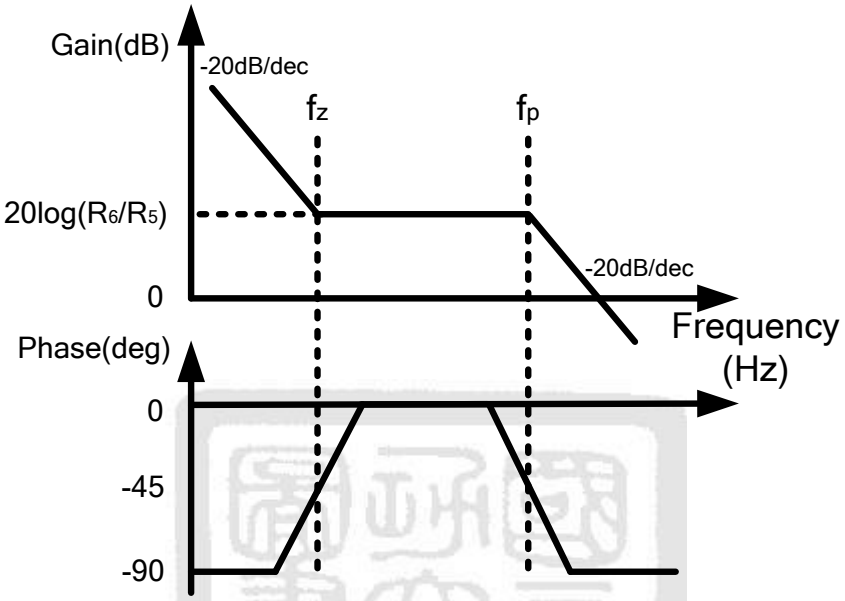


Fig. 4.24 Bode plot of type-II compensator

In the control theory, type-II compensator is one kind of proportional-plus-integral compensator, and it adds a pole at the origin and a zero close to the pole. Let steady-state error close to zero [30]. When designing the compensator, I set the zero f_z close to the origin, the pole f_p around 1/10 f_{sw} and select R_6/R_5 ratio decide the unit-gain frequency of this compensator, as R_6/R_5 is too large to cause SNR decreasing, and too small to cause small bandwidth. Therefore, the values of R_6 and C_1 are too large like MΩ level and μF level respectively that they are designed off chip.

The last, it compares the output of the compensator, V_{error} and a ramp signal to decide the duty cycle controlling the power switches. The implementation of the adaptive load line is achieved.

4.5.2 Ramp and Clock Generator

There is an independent clock generator in this system shown in Fig. 4.25, which generate the ramp signal for PWM control and the clock for S/H clock (MPPT algorithm calculation), respectively.

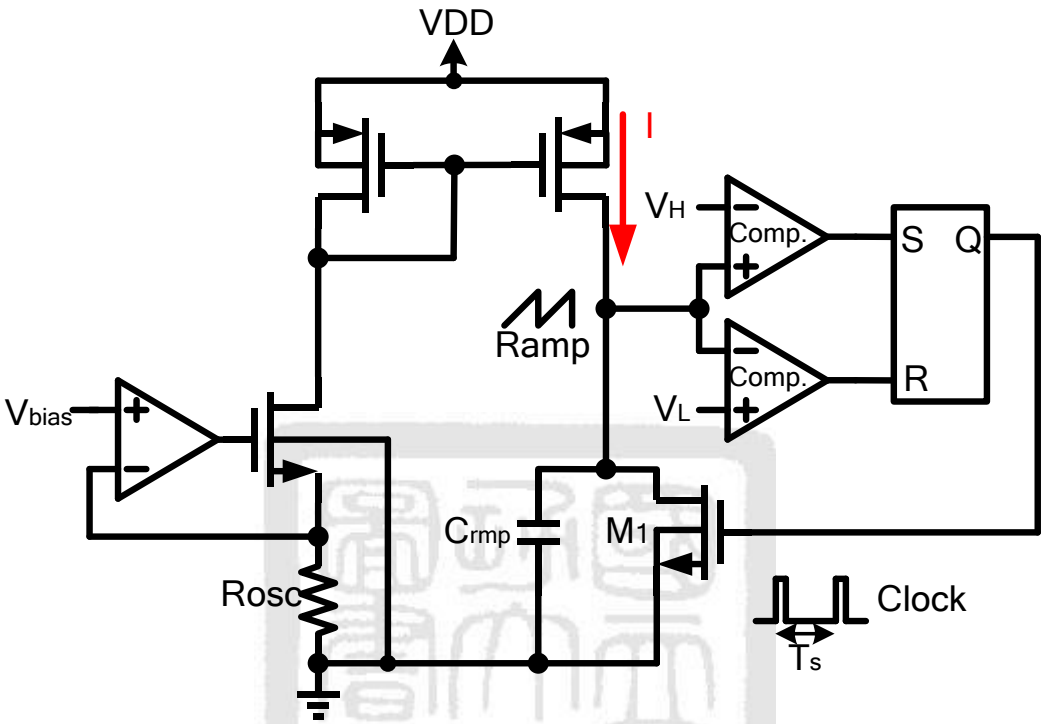


Fig. 4.25 Ramp and clock generator

The circuit has two states, one is charging state and the other is discharging state. During the charging state, the constant current I, which mirrored from a fixed current V_{bias}/R_{osc}, charges the capacitor C_{rmp}, thereby the ramp signal ramping up. When the ramp signal reaches V_H, the comparator changes state and the transistor M_1 turns on to discharges the capacitor C_{rmp} to start the discharging state. Normally, the discharging current is much larger than the charging current. During the discharging state, the ramp signal drops until it reaches V_L and the comparator changes state and the transistor M_1 turns off. Consequently, the clock frequency and the ramp signal is synchronized with each other. These actions will repeat periodically to generate the clock with fixed frequency and it can be expressed as follow.

$$f_{sw} = \frac{I}{C_{rmp}(V_H - V_L)} \tag{4-14}$$

Due to the process variation, temperature, and so on, the deviation of capacitor Crmp is approximately equal to -20%~20%. Therefore, the actual clock frequency

distributes over the range of 120 kHz to 180 kHz in the low-voltage mode design, but this deviation is tolerable in my design.

4.5.3 Dead-Time Control Driver

In the switching buck converter, the size of the two power transistors as switching elements must be large in order to diminish conduction loss. Because of their large gate capacitance, it does not have enough driving capability to drive them only by the PWM duty cycle signal. Hence, a buffer with enough driving capability is needed. The buffer is commonly composed of a simple inverter chains. This inverter chains consist of the cascade inverter stage designed with a tapering factor 3 or 4. If the buffer stage is poorly designed with a simple inverter chain to let two power transistors conduct simultaneously, a shoot-through current will occur and a large current will pass through the two power transistors during each switching transition. The current may damage the inner component and dissipate extra large power loss. Accordingly, the buffer with dead-time that avoids the shoot-through current is needed. The driver with dead-time control used in this thesis is shown in Fig. 4.26.

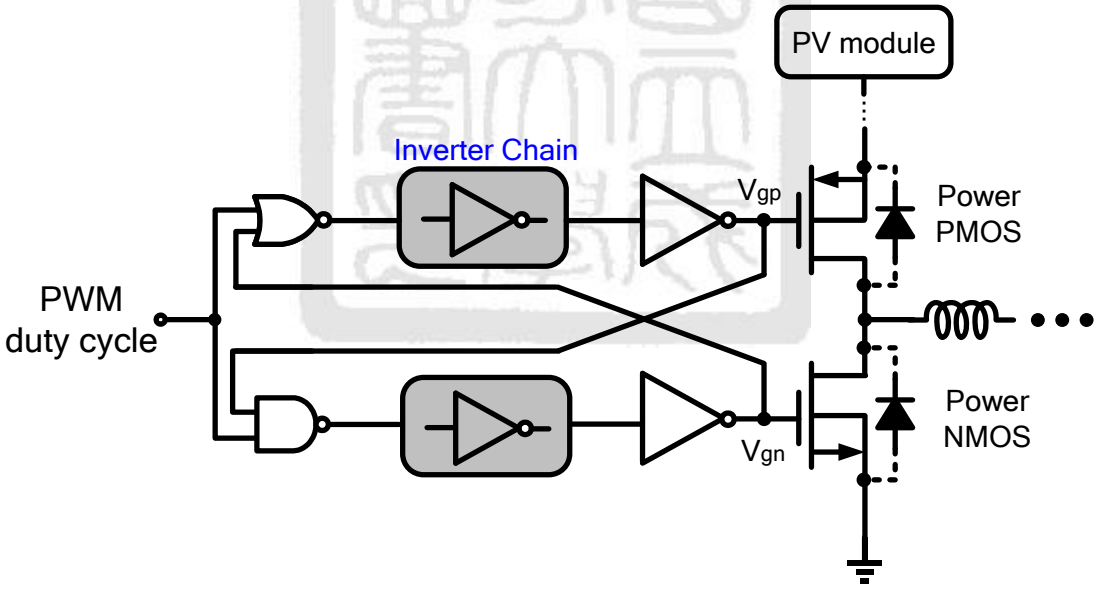


Fig. 4.26 Dead-time control driver

When the power PMOS turns off gradually, the body diode of the power NMOS will conduct some current to the inductor because the power PMOS can't provide enough current to the inductor this moment. If the power NMOS can't turn on promptly to provide current to inductor when the power PMOS turns off gradually, the body diode of the power NMOS will play an important role to provide current to inductor. Because the power loss of body is larger than the power NMOS for the same current,

the less time of body diode conduction will make this power dissipation smaller. Generally speaking, the dead time is usually designed from 10ns to 100ns. Fig. 4.27 is shown that the simulation results of dead time in my design, and the dead time are 28ns and 38ns, respectively.

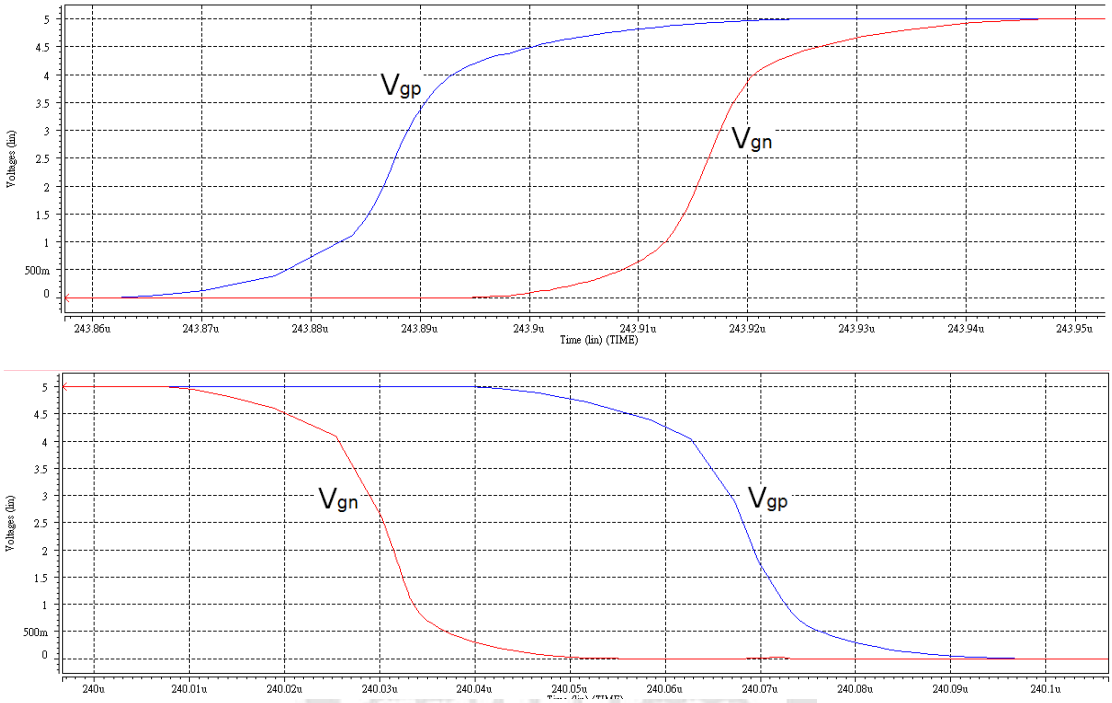


Fig. 4.27 The simulation results of fixed dead control signal

4.6 Transient/Steady Condition Detector

We discussed how to detecting transient condition and the strategy of variable frequency control in the chapter 3. In this section, the implementation of the proposed transient condition detector and variable frequency control circuit will be presentation in detail. In the first of the strategy is to detect if transient condition happening or not and the transient condition detector and its operating clock signal is shown as Fig. 4.28 and Fig. 4.29, respectively.

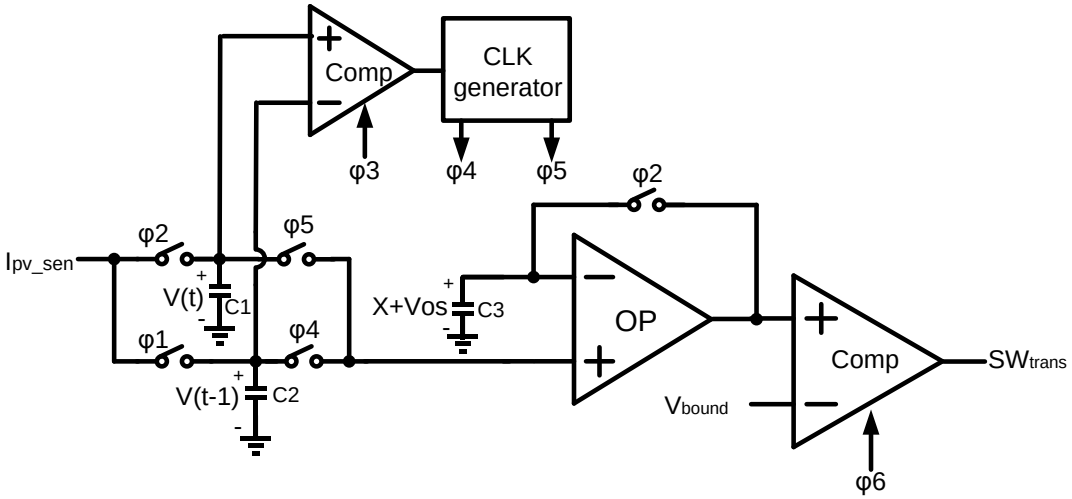


Fig. 4.28 Transient condition detector

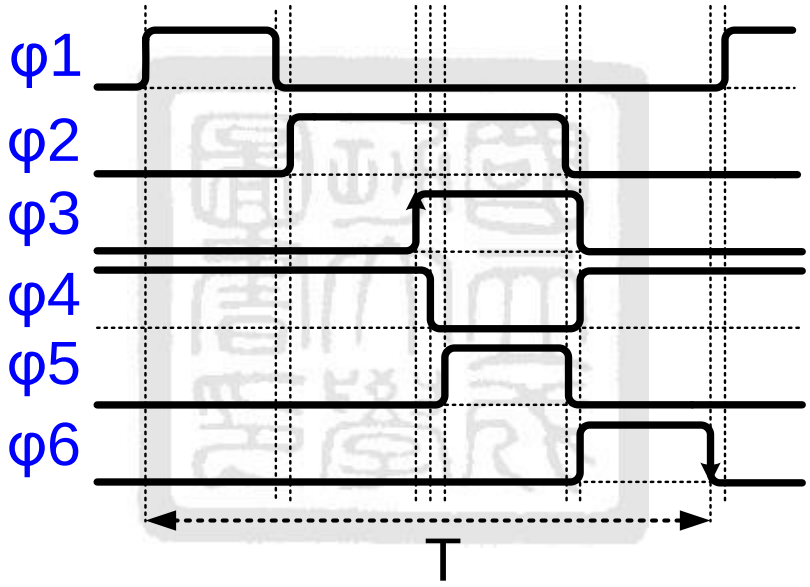


Fig. 4.29 Operating clock signal of transient condition detector

Its main principle is detecting the difference of the change of the current sensing signal I_{pv_sen} during ΔT, and as the amount of the change is bigger than the reference value designed by us, the output voltage of the transient condition detector, SW_{trans}, is high standing for transient condition happening. The operations are described in the following.

The first, the switch φ1 also controlled by clock signal φ1 would sample I_{pv_sen} and hold the value, V(t-1), in the capacitor C2 as the switch turning off before clock signal φ2 turning on. When the clock signal φ2 turns on, the switch φ2 would sample I_{pv_sen}, and clock signal φ3 is turned on within on-state of the clock signal φ2. It is determined what direction of the change of the current sensing voltage, I_{pv_sen} by the

comparison of the V(t) crossing on C1 and V(t-1) held on C2. And then the clock signal φ4 and φ5 are generated simultaneously by the CLK generator to decide which value, V(t) or V(t-1), would store in the C3. On the other hand, When the clock signal φ2 turns on, the offset voltage of the OP is also stored in the C3 for offset cancellation. The above operations are summarized as following Table 4.2.

Table 4.2 The operational table of transient condition detector

Transient direction	**The storage of C3 (X+V_{os})**	**The change of I_{pv_sen} (ΔV)**
Positive	$V(t-1) + V_{os}$	V(t) - V(t-1)
Negative	$V(t) + V_{os}$	V(t-1) - V(t)

The last operation is as the Table 4.3, where the ‘G’ stands for the gain of the OP.

Table 4.3 The final operation of transient condition detector

Condition	**Compare**	**SW_{trans}**
Transient	$G\Delta V > V_{bound}$	1
No transient	$G\Delta V < V_{bound}$	0

In the strategy of variable frequency control, detecting steady condition is important to slow down the frequency of the system under the steady condition which is at the vicinity of the maximum power point. The output signal of the MPP comparator in the MPPT algorithm circuit, Comp_out, is selected to determine whether at the vicinity of the maximum power point or not. First, we observe the change of power and Comp_out, which is as Fig. 4.30

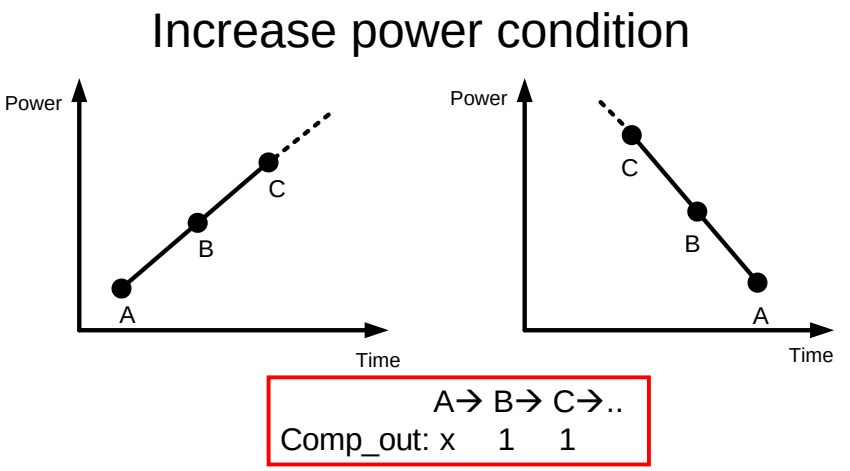


Fig. 4.30 The relationship between the power and the signal Comp_out

It can be seen that the changing situations of the signal Comp_out would be a regular change at the vicinity of maximum power point. A digital circuit with a truth table is designed in the follow.

Table 4.4 The truth table of steady condition detector

Comp_out(t-2)	Comp_out(t-1)	Comp_out(t)	Re
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	0

Where the output signal of steady condition detector, Re, is high state which stands for power tracking at the vicinity of the maximum power and could slow down the frequency of the system. The Boolean function of Re,

$$\begin{aligned} Re = {} & Comp\_out(t-2)\overline{Comp\_out(t-1)}Comp\_out(t) \\ & + \overline{Comp\_out(t-2)}Comp\_out(t-1)\overline{Comp\_out(t)} \end{aligned} \tag{4-15}$$

and the circuit,

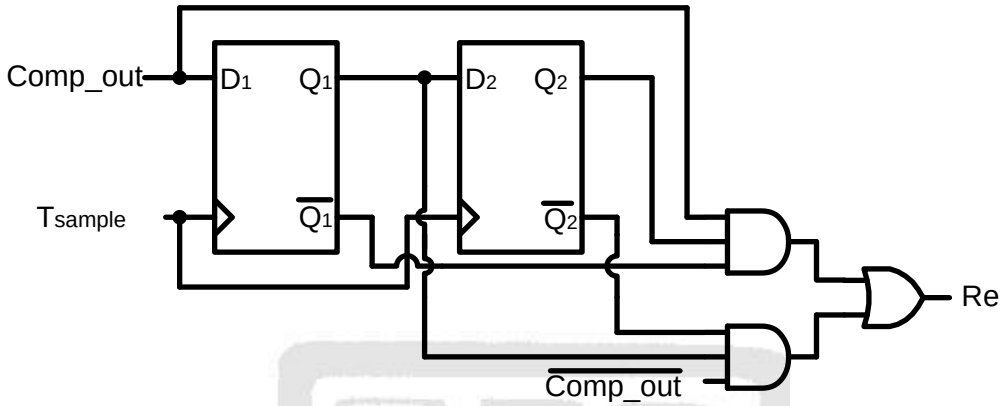


Fig. 4.31 Steady condition detector

The last step of the strategy of variable frequency control is to collect the output signal of transient condition detector, SW_{trans}, and the output signal of steady condition detector, Re for decide whether speeding up the frequency or not. A truth table is in the follow,

Table 4.5 The truth table of variable frequency

SW_{trans}	Re	Output control signal	Function
0	0	X	Don't care
0	1	0	Slow-down frequency
1	0	1	Speed-up frequency
1	1	1	Speed-up frequency

and the circuit,

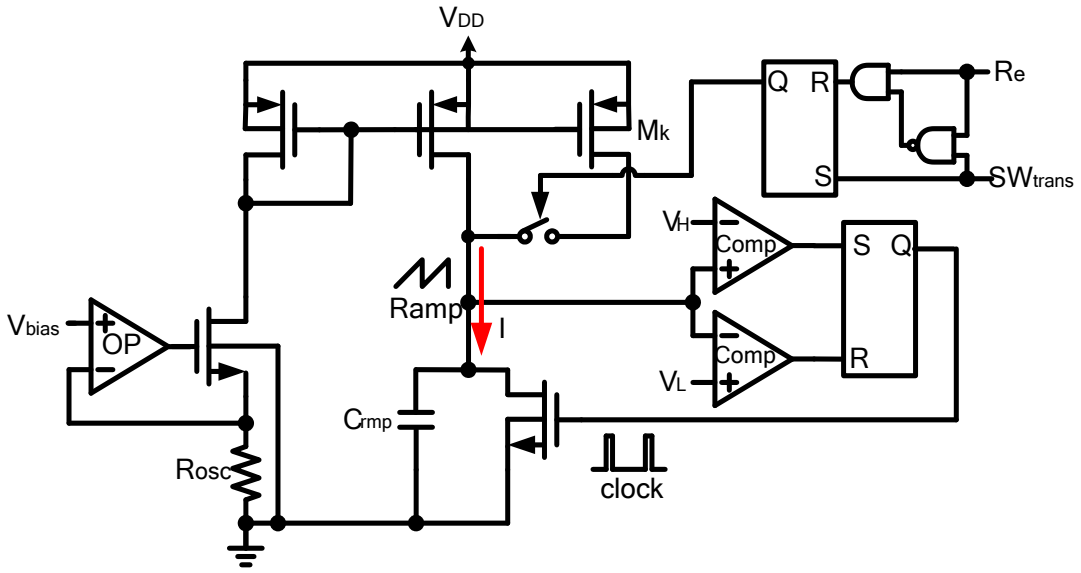


Fig. 4.32 Variable frequency generator

where adding an another constant current source, M_k, and a switch to the ramp and clock generator, will accelerate the clock frequency as the switch is turned on. Due to the addition of the extra current, the charging current I is increased and the clock frequency is accelerated. On the contrary, the charging current I is decreased as the switch is turned off, and the clock frequency is slow down to the original frequency.

4.7 Operational Amplifier

The operational amplifier is employed in the monolithic system. A two-stage operational amplifier [23] is used in my design. The schematic of typical two-stage operational amplifier is shown in Fig. 4.33. “Two-stage” refers to the number of gain stages in the operational amplifier. The first gain stage is a differential-input single-ended output stage. The second gain stage is normally a common-source gain stage that has an active load. Capacitor C_C is included to ensure stability when the operational amplifier is used with feedback. Because C_C is between the input and the output of the second stage, it is called ”Miller capacitance” since its effective capacitive load on the first stage is large than its physical value.

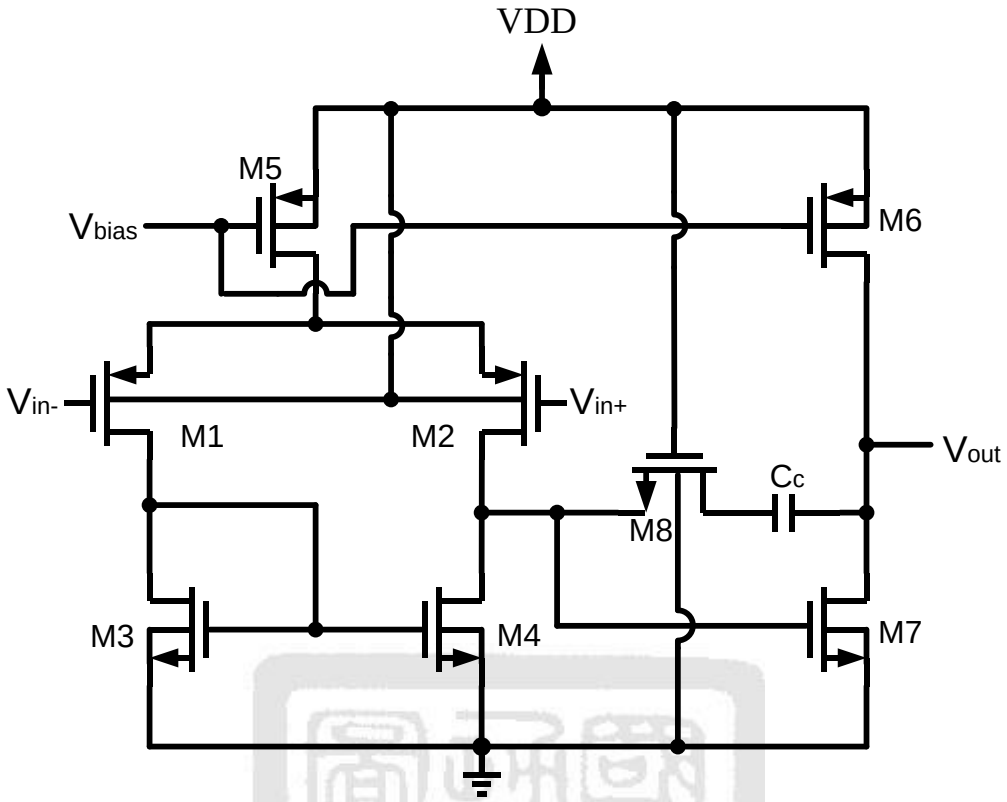


Fig. 4.33 Two-stage operational amplifier

The gain of first stage is

$$A_{v1} = g_{m1}(r_{ds2} \| r_{ds4}) \tag{4-16}$$

The second gain stage is simply a common-source stage with a p-channel active load 'M6', and its gain is

$$A_{v2} = -g_{m7}(r_{ds6} \| r_{ds7}) \tag{4-17}$$

Where the approximation value $g_{mp} = \sqrt{2\mu_p C_{ox}(\frac{W}{L})I_D}$, $g_{mn} = \sqrt{2\mu_n C_{ox}(\frac{W}{L})I_D}$ and $r_{dsi} = \alpha \cdot \frac{L_i}{I_{Di}}\sqrt{V_{DGi} + V_{ti}}$ are used to estimate the desired gain value. Where α is a technology-dependent parameter of around $5\times10^6\ \sqrt{V}/m$. Secondly, the frequency response of operational amplifier is discussed. The second stage introduces primarily a capacitive load on the first stage due to the Miller effect of the capacitor Cc. By this relation and some calculations, we can obtain a simple overall gain in middle frequency as follows.

$$A_v(s) = \frac{g_{m1}}{sC_c} \tag{4-18}$$

This equation can be used to find the approximate unity-gain frequency.

$$\omega_t = \frac{g_{m1}}{C_c} \tag{4-19}$$

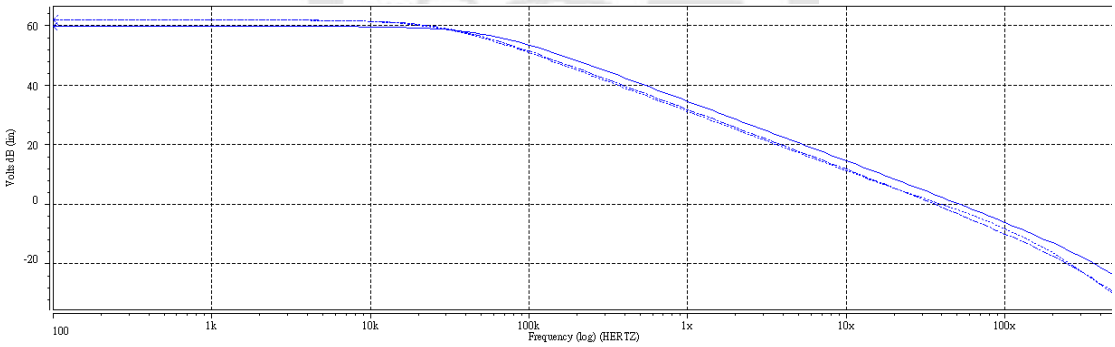
Note here that the unity-gain frequency is directly proportional to g_{m1} and inversely proportional to C_c. By the equation of gain and unity-gain frequency, we can obtain the approximate size values of all transistors except M8. This transistor operates in triode region and as a resistor. The resistance is given by

$$r_{ds8} \approx \frac{1}{\mu_n C_{ox}\left(\frac{W}{L}\right)_8 (V_{GS} - V_t)_8} \tag{4-20}$$

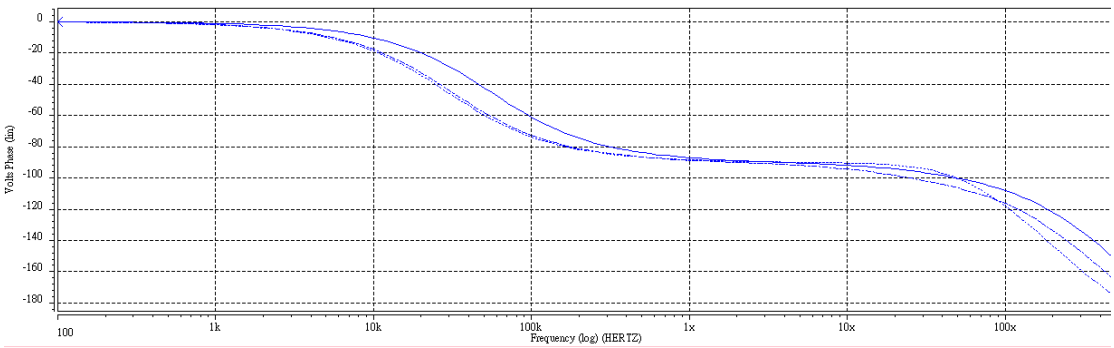
It is induced in order to realize a left-half-plane zero at frequency around or slightly above unity-gain frequency. Without the transistor M8, there is a left-half-plane zero which make the compensation much more difficult. The addition of such an extra left-half-plane zero is what is commonly called "lead-compensation". The common choice of rds8 according to

$$r_{ds8} = \frac{1}{1.2 g_{m1}} \approx \frac{1}{1.2 \omega_c C_c} \tag{4-21}$$

The gain and phase plot of operational amplifier under TT/55℃, FF/25℃ and SS/125℃ corner is shown in Fig. 4.34



(a)



(b)

Fig. 4.34 (a) Gain and (b) phase plot of operational amplifier under TT/55℃, FF/25℃ and SS/125℃ corner

Some frequency characteristic about gain and phase of operational amplifier are shown in Table 4.6

Table 4.6 The frequency characteristic of the operational amplifier under TT/55℃, FF/25℃ and SS/125℃ corner

Corner/Temperature	FF/25℃	TT/55℃	SS/125℃
DC gain	60.1dB	61.9dB	61.8dB
Unity-gain frequency	51.9 MHz	36.1MHz	39.8 MHz
Phase margin	79.4°	76.7°	79.4°

4.8 Comparator

Comparators are needed in the monolithic system. For example, it used in the current-mode control to generate the duty cycle for deciding when to turn off the power PMOS. The comparator used in this thesis is shown in Fig. 4.35.

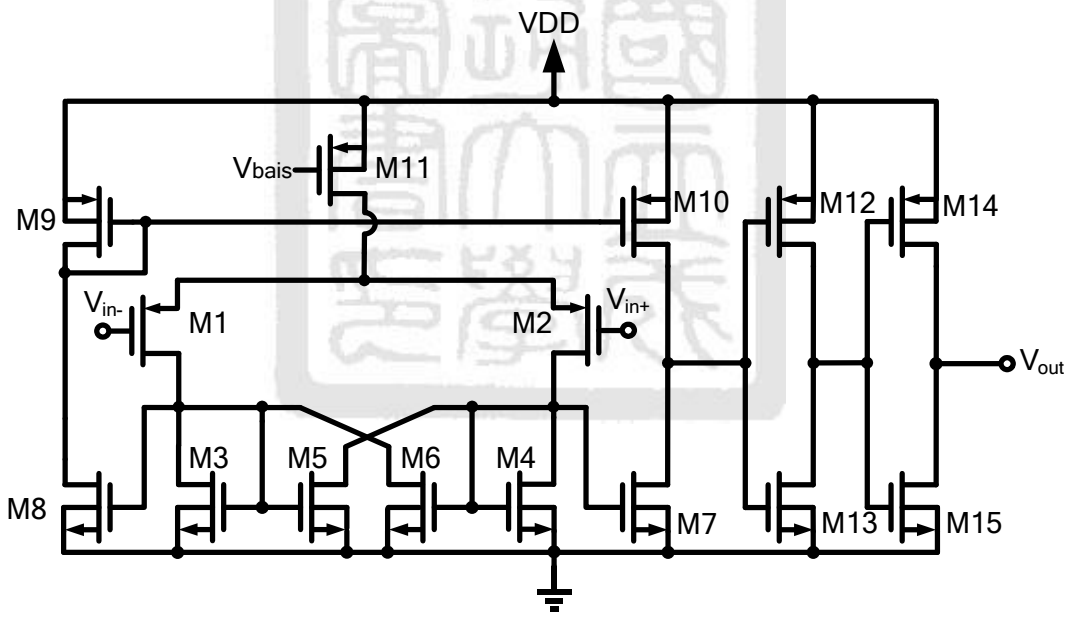


Fig. 4.35 Latch comparator

It is composed of three stages. The first stage is implemented by a source-coupled differential pair with positive feedback to provide a high gain. The transistors M3, M4, M5, and M6 make up the positive feedback gain stage and the gain is given by

$$A_{v1} = \sqrt{\frac{\mu_p (W/L)_{M1}}{\mu_n (W/L)_{M3}}} \cdot \frac{1}{1-\alpha} \quad , \quad \alpha = \frac{(W/L)_{M5}}{(W/L)_{M3}} \tag{4-22}$$

where α is the positive feedback factor which is responsible for increasing the gain.

The second stage is composed of a n-channel differential pair with an p-channel current mirror active load. The gain of second stage is given by

$$A_{v2} = g_{m7}(r_{ds7} \parallel r_{ds10}) \tag{4-23}$$

The third stage is composed of the inverter chains M12~M15 and these are used to increase the response of the comparator output signal. This inverter chain can also act as a driver stage such that the transistors M7 and M8 can be made smaller to reduce the parasitic capacitance at the gates of M7and M8 for a faster response.

The simulation results are shown in Fig. 4.36 and Fig. 4.37. The offset voltage of the comparator is approximately 1.2mV and the delay time is around 13ns, which is tolerable for my application with the switch frequency 200 kHz.

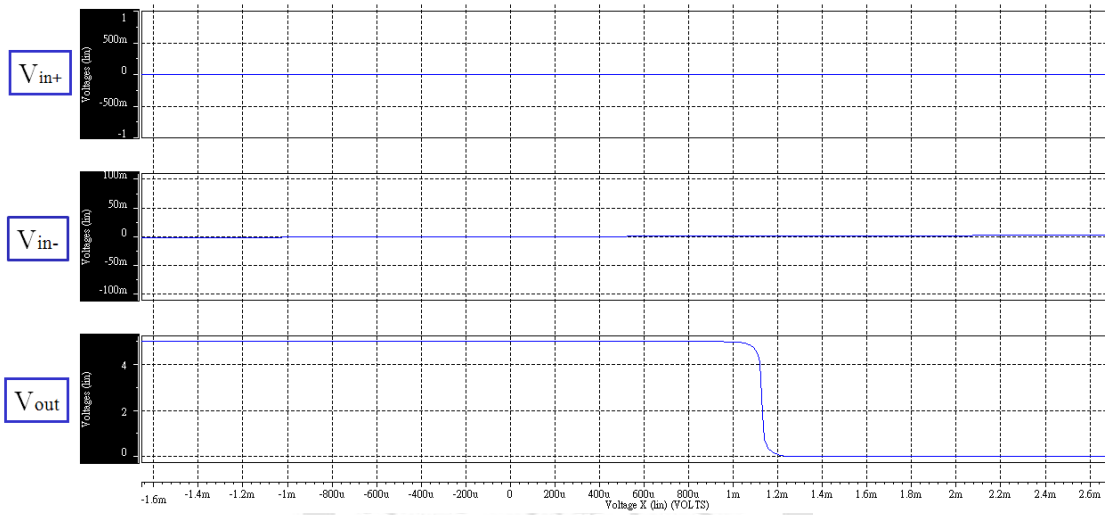


Fig. 4.36 DC characteristic of the comparator

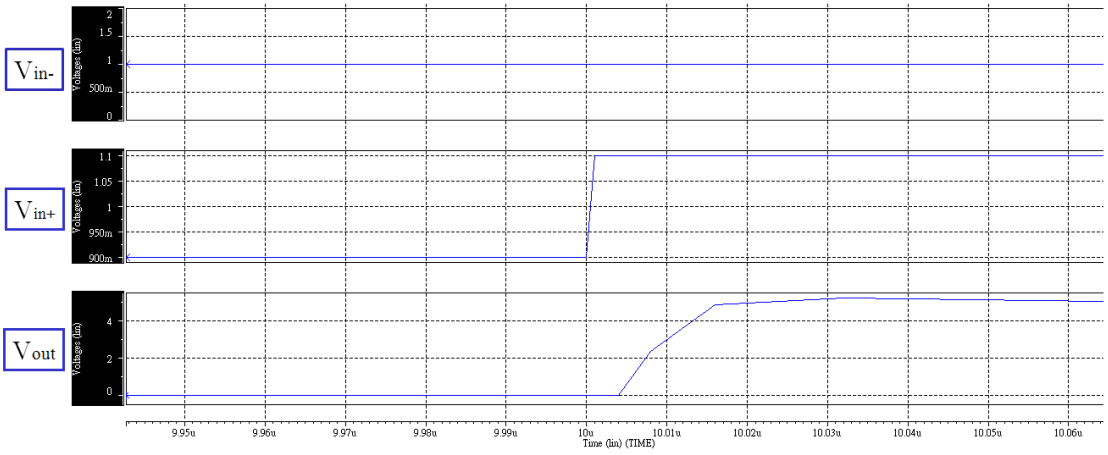


Fig. 4.37 Transient characteristic of the comparator

4.9 Layout Consideration

The layout floor plan of the designed chip is shown in Fig. 4.38, and the floor plan is mainly divided into two parts.

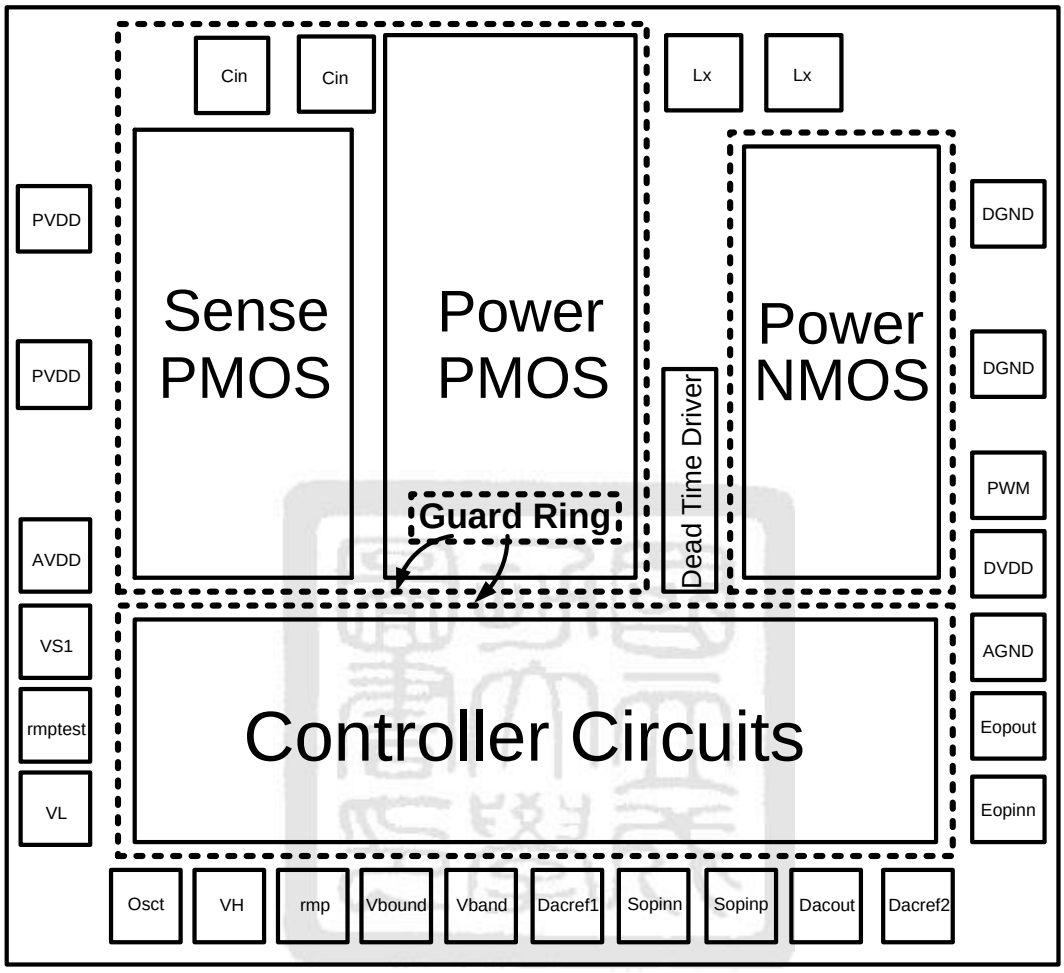


Fig. 4.38 The floor plan of chip layout

One is composed of power transistors and driver, and the other is composed of the control circuits. It is separated two parts by the guard ring to alleviate the noise effect on the control circuits because the power transistors and drivers belong to high noise region. The large amount of current through the power transistor and switching are the main sources of high noise. The guard ring could also avoid the latch up of the big size power transistor. Finally, the metal line connected to the power source, ground, and switch node 'Lx' must be wide and short as possible as one can sustain large current and reduce the parasitic effect.

The layout photograph is showed in Fig. 4.39. The chip is fabricated by 0.35um 2P4M 3.3/5V Mixed Signal CMOS process. The active area is around 1.456 x 1.571 mm^2 and the total area is around 1.718 x 1.796 mm^2.

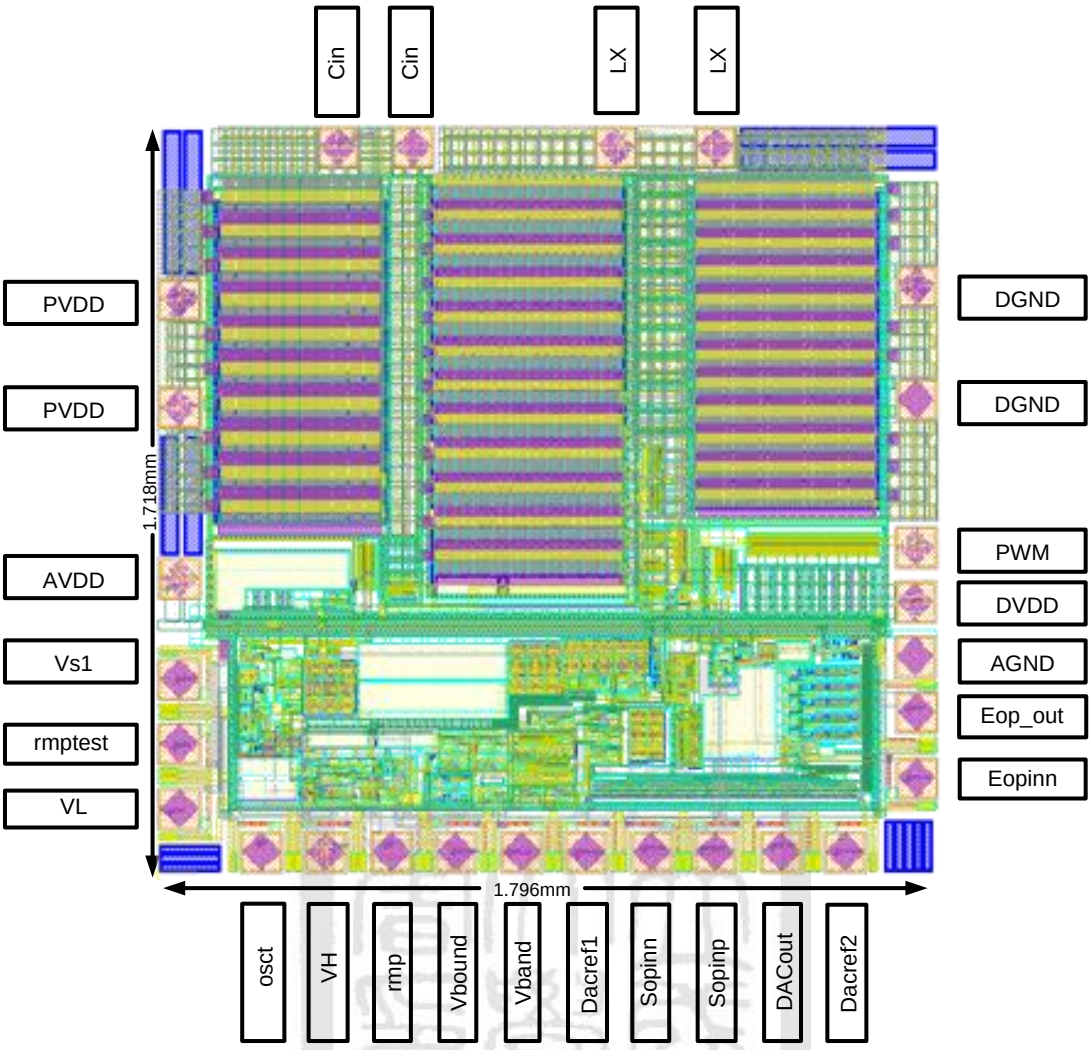


Fig. 4.39 The layout photograph of whole chip

Chapter 5

Simulation and Measurement Results

5.1 Simulation Results

This section shows some crucial simulation results of the MPPT converter with LV-mode and HV-mode structure. From these simulation results of Hspice, the functions and specifications of the MPPT converter can be verified mostly. In all following simulation results, the adaptive Spice model of photovoltaic source are established according to the principle mentioned in the chapter 2. These results are as follows.

1. LV-mode structure simulation result in steady-state (Illumination: 600W/m^2)

Fig. 5.1 shows the output of the low power rating photovoltaic with the LV-mode MPPT converter under the steady-state irradiation level 600W/m^2, and the upper part in Fig. 5.1 is the output voltage of the photovoltaic, and the bottom part in Fig. 5.1 is the output current of the photovoltaic. Fig. 5.2 and Fig. 5.3 are the verification of maximum power point tracking. The variant condition of output power of the photovoltaic in the time is shown in Fig. 5.2. The variant condition of output power of the photovoltaic, relative to the output voltage of the photovoltaic, is shown in Fig. 5.3. it can be seen that the thin line presents the power-to-voltage curve of the photovoltaic under the irradiation level 600W/m^2, and the thick line presents the variant condition of output power of the photovoltaic with the LV-mode MPPT converter.

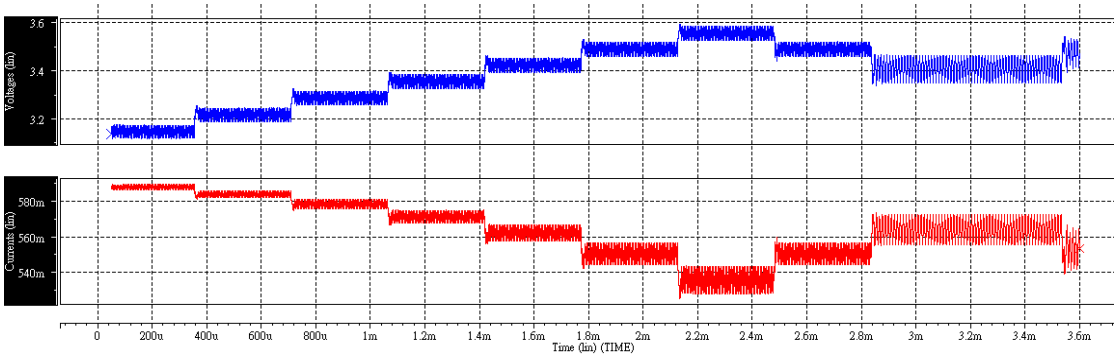


Fig. 5.1 Output voltage and current of the low power rating photovoltaic under the steady-state irradiation level 600W/m^2

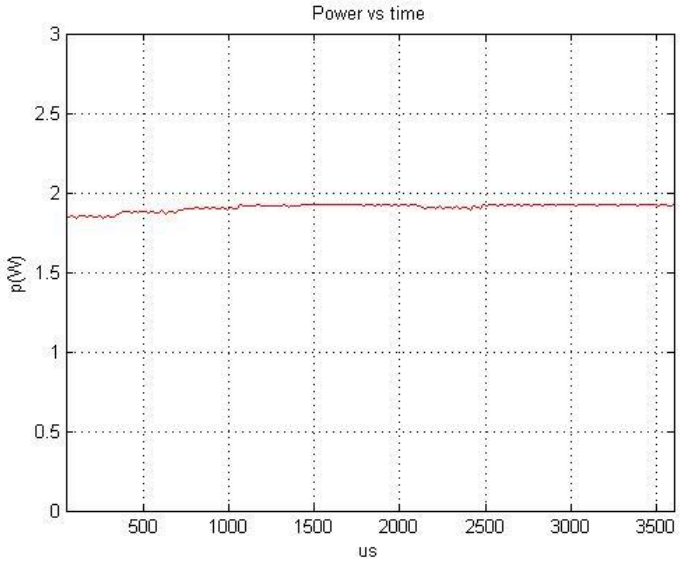


Fig. 5.2 Output power of the low power rating photovoltaic under the steady-state irradiation level 600W/m^2

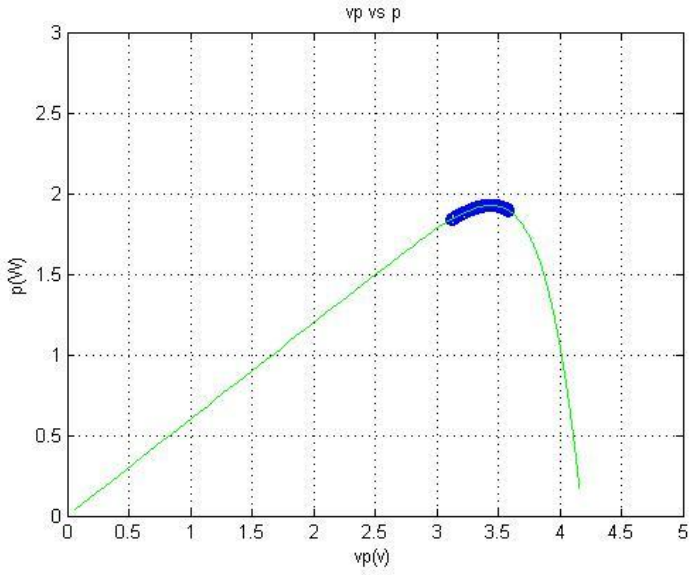


Fig. 5.3 Output power variability with the output voltage of the low power rating photovoltaic under the steady-state irradiation level 600W/m^2

2. LV-mode structure simulation result in dynamic-state (Illumination: 600W/m^2 ➔200W/m^2)

In this part, addition to a transient condition changing in the irradiation is to observe the good transient response of the proposed MPPT converter. Fig. 5.4 shows the output of the low power rating photovoltaic with the LV-mode MPPT converter, and the upper part in Fig. 5.4 is the output voltage of the photovoltaic, and the bottom part in Fig. 5.4 is the output current of the photovoltaic. We can see that a change in

the irradiation at 1.8ms from 600W/m^2 to 200W/m^2. At about 3ms, it achieves the maximum power point under the irradiation 200W/m^2. The variant condition of output power of the photovoltaic in the time is shown in Fig. 5.5. The variant condition of output power of the photovoltaic, relative to the output voltage of the photovoltaic, is shown in Fig. 5.6. In this figure, two thin lines stand for the power-to-voltage curves of the photovoltaic under the irradiation level 600W/m^2 and 200W/m^2, respectively, and the thick line presents the variant condition of output power of the photovoltaic with the LV-mode MPPT converter. The order of the tracking path is 1 ➔ 2 ➔ 3.

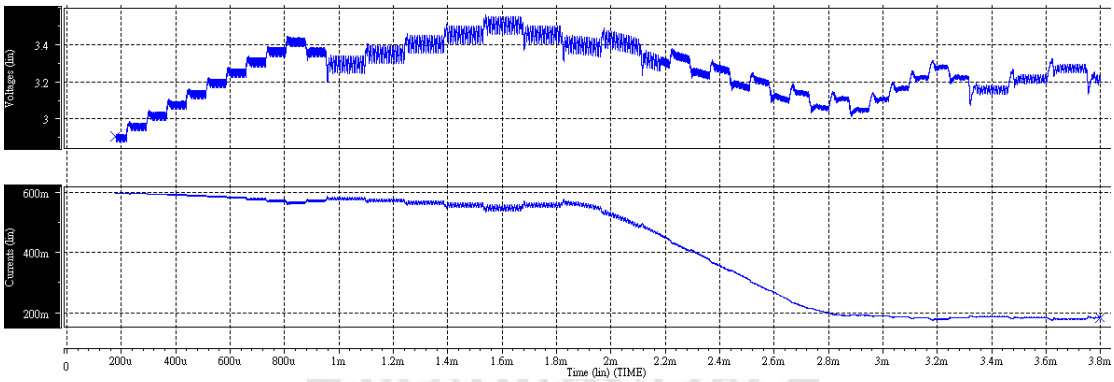


Fig. 5.4 Output voltage and current of the low power rating photovoltaic under the dynamic-state irradiation level 600W/m^2 ➔ 200W/m^2

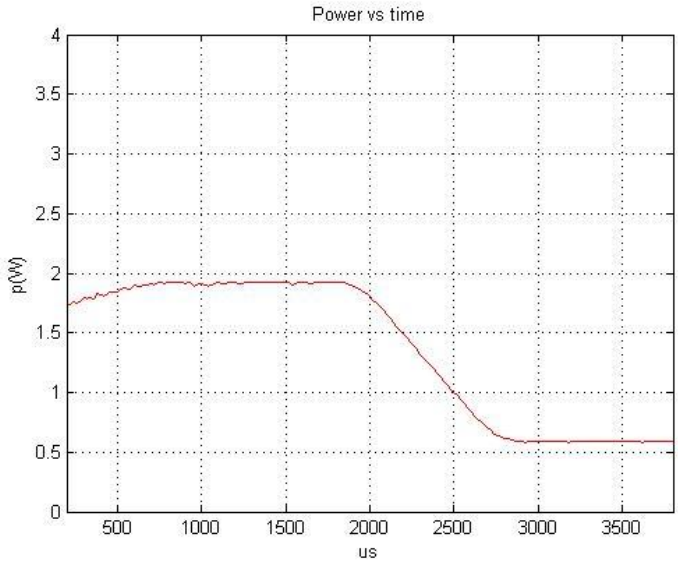


Fig. 5.5 Output power of the low power rating photovoltaic under the dynamic-state irradiation level 600W/m^2 ➔ 200W/m^2

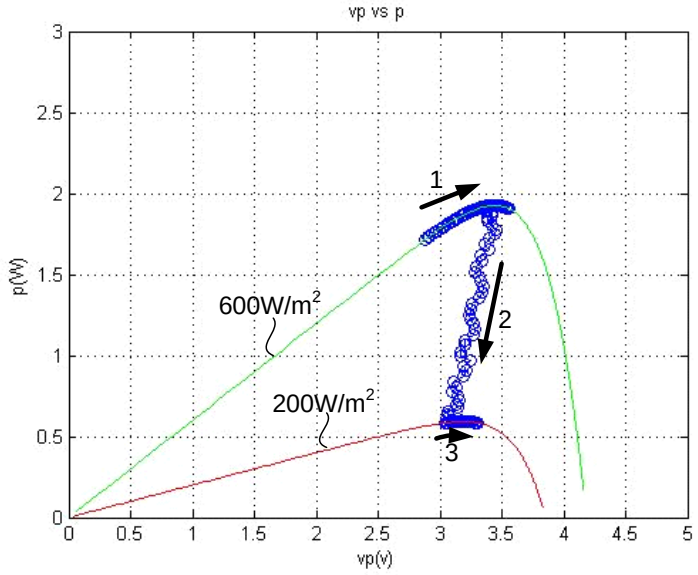


Fig. 5.6 Output power variability with the output voltage of the low power rating photovoltaic under the dynamic-state irradiation level 600W/m^2 ➔ 200W/m^2

3. Transient Tracking Factor (TTF) verification (Illumination: 600W/m^2 ➔200W/m^2 ➔600W/m^2)

In this part, addition to a step-changing transient condition in the irradiation is to observe the good transient response of the proposed MPPT converter. Fig. 5.7 shows the output of the low power rating photovoltaic with the LV-mode MPPT converter, and the upper part in Fig. 5.7 is the output voltage of the photovoltaic, and the bottom part in Fig. 5.7 is the output current of the photovoltaic. We can see that a change in the irradiation at 6ms from 600W/m^2 to 200W/m^2. At the same time, it could achieve the maximum power point under the irradiation 200W/m^2. The variant condition of output power of the photovoltaic in the time is shown in Fig. 5.8. The variant condition of output power of the photovoltaic, relative to the output voltage of the photovoltaic, is shown in Fig. 5.9. In this figure, two thin lines stand for the power-to-voltage curves of the photovoltaic under the irradiation level 600W/m^2 and 200W/m^2, respectively, and the thick line presents the variant condition of output power of the photovoltaic with the LV-mode MPPT converter. A practical PV system will not exhibit voltage steps because the irradiance doesn't step change and even if it did, the capacitor across the panel's output limits the rate of voltage change. Even so, an artificial such step was employed in order to explain the proposed control operation and to calculate the TTF for comparing MPPT converters' performance. Table 5.1 shows the TTF of the proposed MPPT.

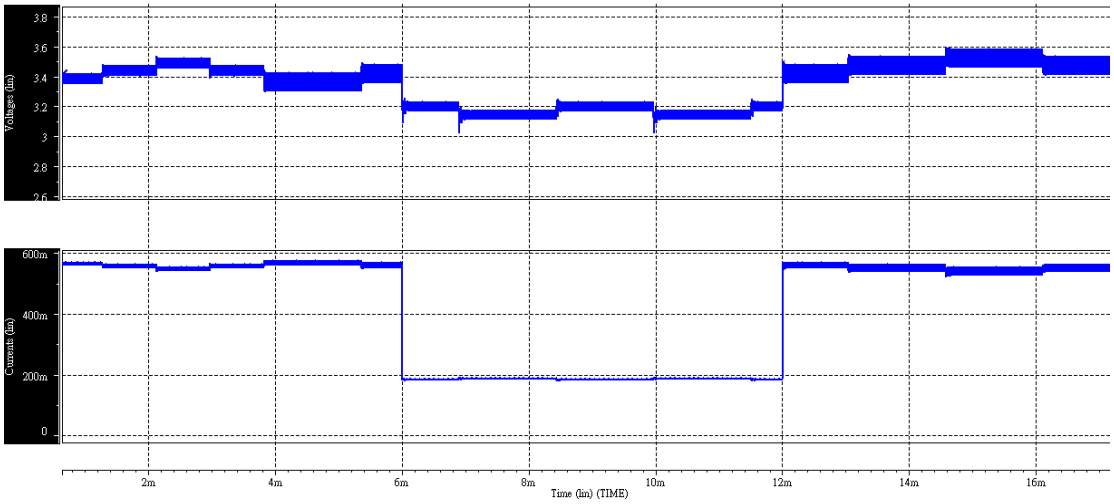


Fig. 5.7 Output voltage and current of the low power rating photovoltaic under the step change of irradiation level 600W/m^2 ➔ 200W/m^2 ➔600 W/m^2

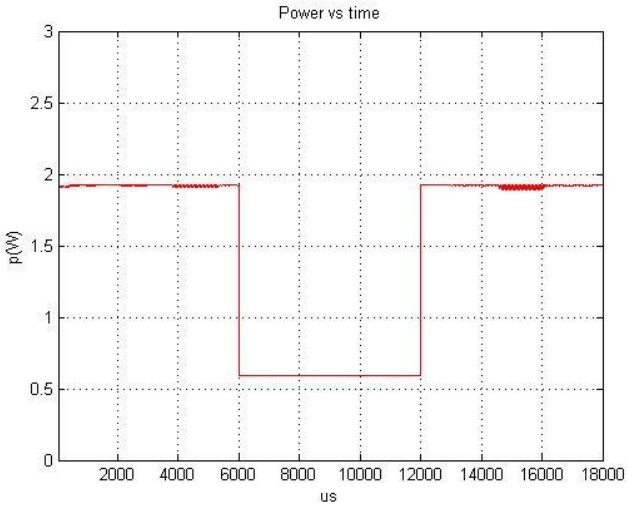


Fig. 5.8 Output power of the low power rating photovoltaic under the step change of irradiation level 600W/m^2 ➔ 200W/m^2 ➔600 W/m^2

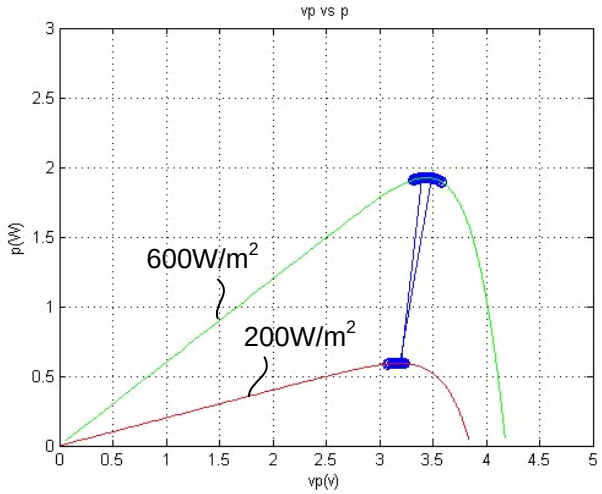


Fig. 5.9 Output power variability with the output voltage of the low power rating

photovoltaic under the step change of irradiation level 600W/m^2 ➔ 200W/m^2 ➔600 W/m^2

Table 5.1 TTF of the proposed MPPT

Transient Tracking Factor (TTF)	
600 ➔200(W/m^2)	**200 ➔600(W/m^2)**
0.22 (ms/ W)	**0.15(ms/ W)**

4. HV-mode structure simulation result in steady-state (Illumination: 1000W/m^2)

Fig. 5.10 shows the output of the high power rating photovoltaic with the HV-mode MPPT converter under the steady-state irradiation level 1000W/m^2, and the upper part in Fig. 5.10 is the output voltage of the photovoltaic, and the bottom part in Fig. 5.10 is the output current of the photovoltaic. Fig. 5.11 and Fig. 5.12 are the verification of maximum power point tracking. The variant condition of output power of the photovoltaic in the time is shown in Fig. 5.11. The variant condition of output power of the photovoltaic, relative to the output voltage of the photovoltaic, is shown in Fig. 5.12. it can be seen that the thin line presents the power-to-voltage curve of the photovoltaic under the irradiation level 1000W/m^2, and the thick line presents the variant condition of output power of the photovoltaic with the HV-mode MPPT converter.

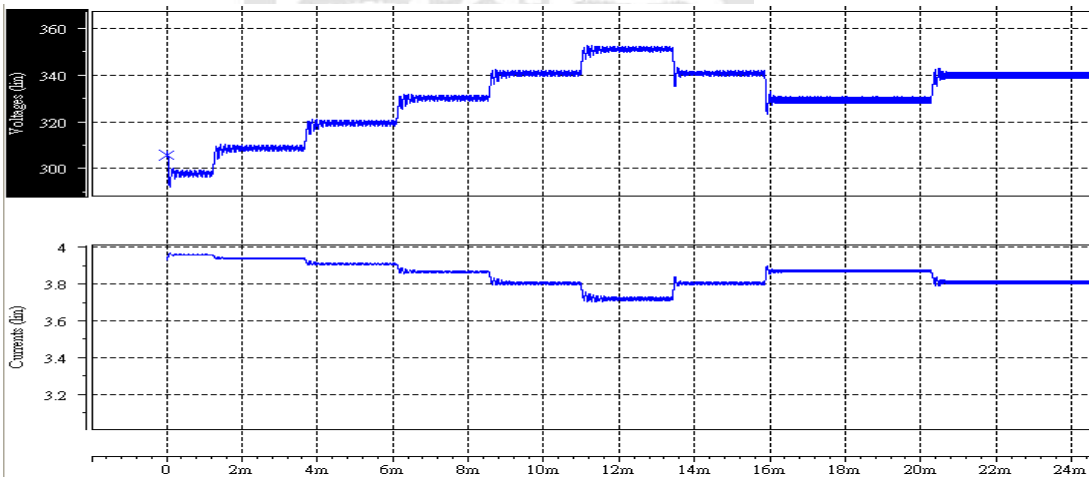


Fig. 5.10 Output voltage and current of the low power rating photovoltaic under the steady-state irradiation level 1000W/m^2

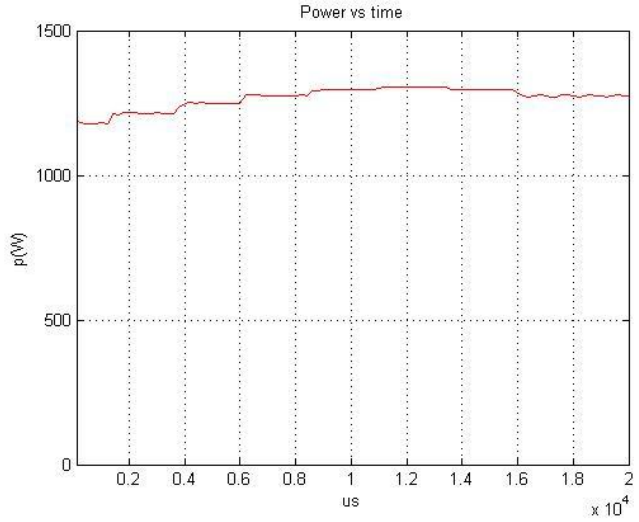


Fig. 5.11 Output power of the high power rating photovoltaic under the steady-state irradiation level 1000W/m^2

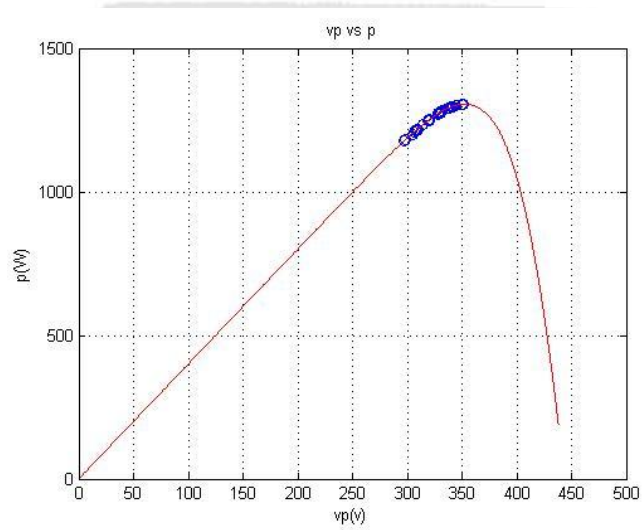


Fig. 5.12 Output power variability with the output voltage of the high power rating photovoltaic under the steady-state irradiation level 1000W/m^2

5. HV-mode structure simulation result in dynamic-state (Illumination: 1000W/m^2 ➔500W/m^2)

In this part, addition to a transient condition changing in the irradiation is to observe the good transient response of the proposed MPPT converter. Fig. 5.13 shows the output of the high power rating photovoltaic with the HV-mode MPPT converter, and the upper part in Fig. 5.13 is the output voltage of the photovoltaic, and the bottom part in Fig. 5.13 is the output current of the photovoltaic. We can see that a change in the irradiation at 24ms from 1000W/m^2 to 500W/m^2. The variant condition of output power of the photovoltaic in the time is shown in Fig. 5.14. The variant

condition of output power of the photovoltaic, relative to the output voltage of the photovoltaic, is shown in Fig. 5.15. In this figure, two thin lines stand for the power-to-voltage curves of the photovoltaic under the irradiation level 1000W/m^2 and 500W/m^2, respectively, and the thick line presents the variant condition of output power of the photovoltaic with the HV-mode MPPT converter.

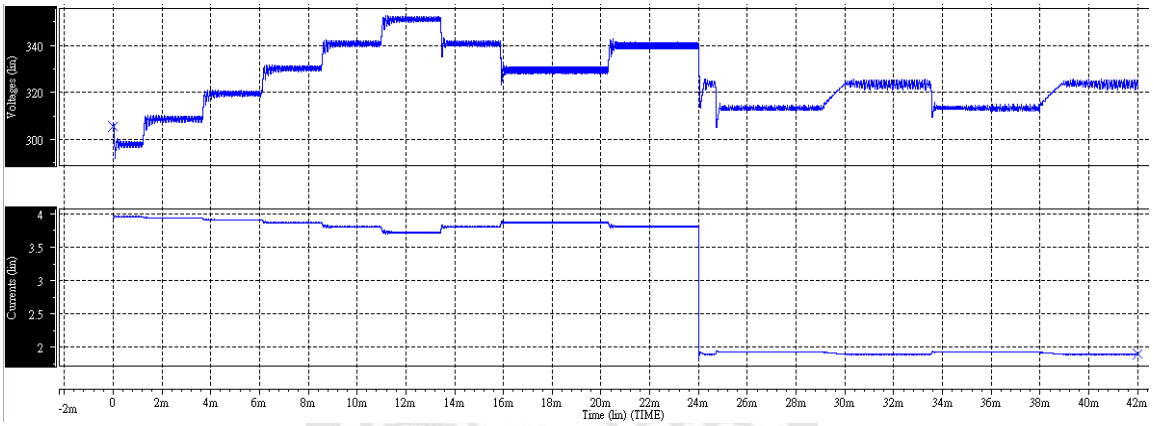


Fig. 5.13 Output voltage and current of the high power rating photovoltaic under the dynamic-state irradiation level 1000W/m^2 ➔ 500W/m^2

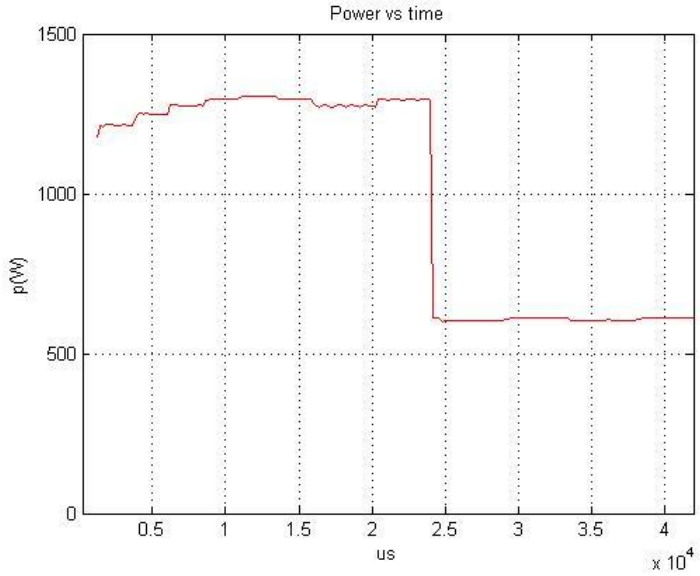


Fig. 5.14 Output power of the high power rating photovoltaic under the dynamic-state irradiation level 1000W/m^2 ➔ 500W/m^2

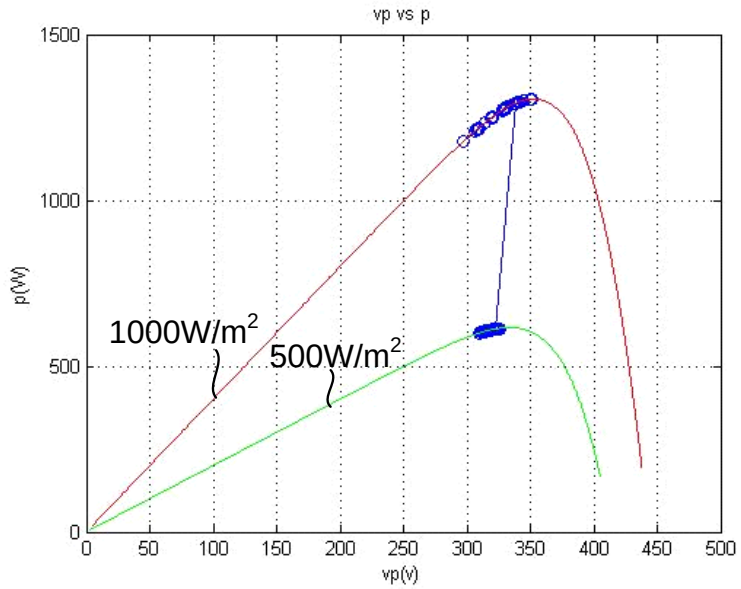


Fig. 5.15 Output power variability with the output voltage of the high power rating photovoltaic under the dynamic-state irradiation level 1000W/m^2 ➔ 500W/m^2

6. Tracking Efficiency (η_{track})

The tracking efficiency versus different irradiations is shown in the following Fig. 5.16. The lower tracking efficiency happens under the lower irradiations due to the insensitivity in the peak of the smooth P-V curve under the lower irradiations. The maximum tracking efficiency is 99.83%.

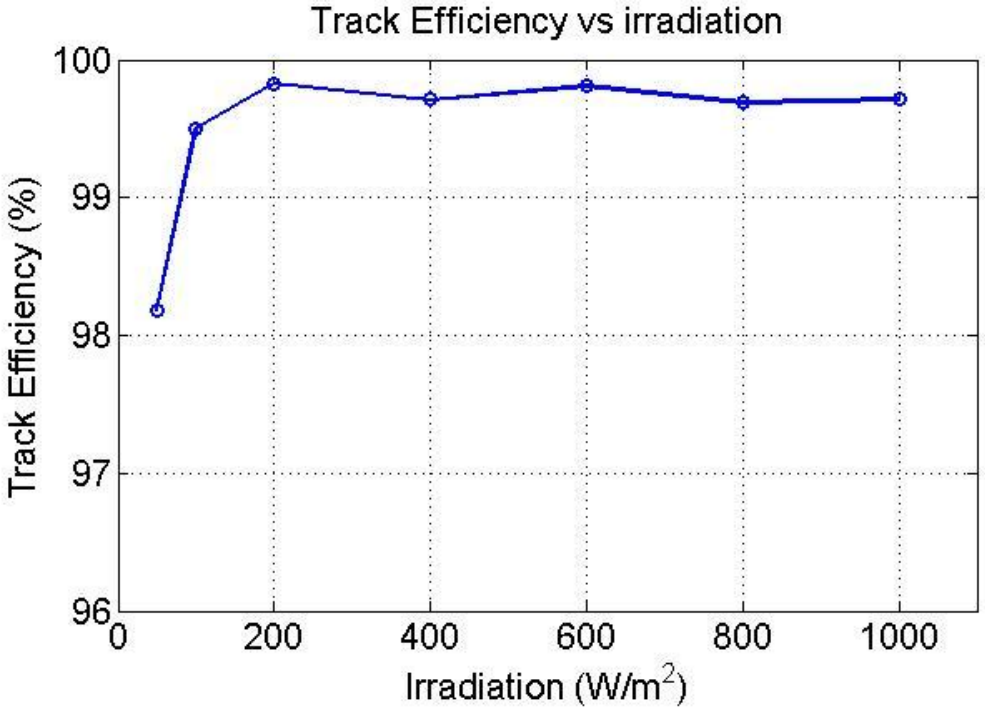


Fig. 5.16 Tracking efficiency vs. irradiation variation

7. Power Conversion Efficiency ($\eta_{conversion}$)

The power conversion efficiency versus different irradiations is shown in the following Fig. 5.17 and Fig. 5.18. The maximum power conversion efficiency is 91.04% in the LV-mode and 96.19% in the HV-mode structure.

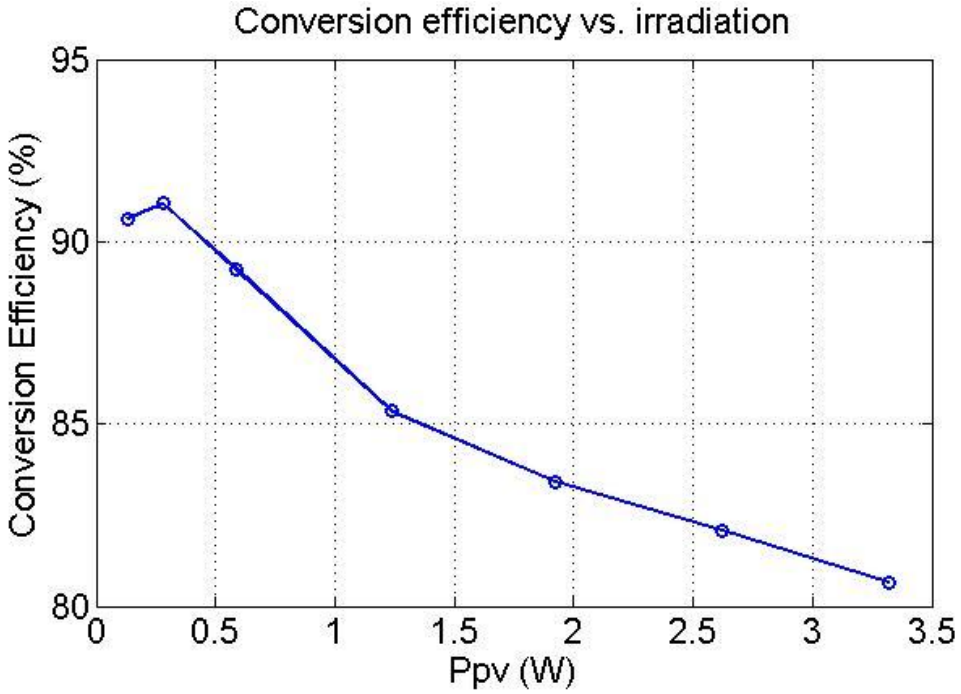


Fig. 5.17 Power conversion efficiency of LV-mode vs. irradiation variation

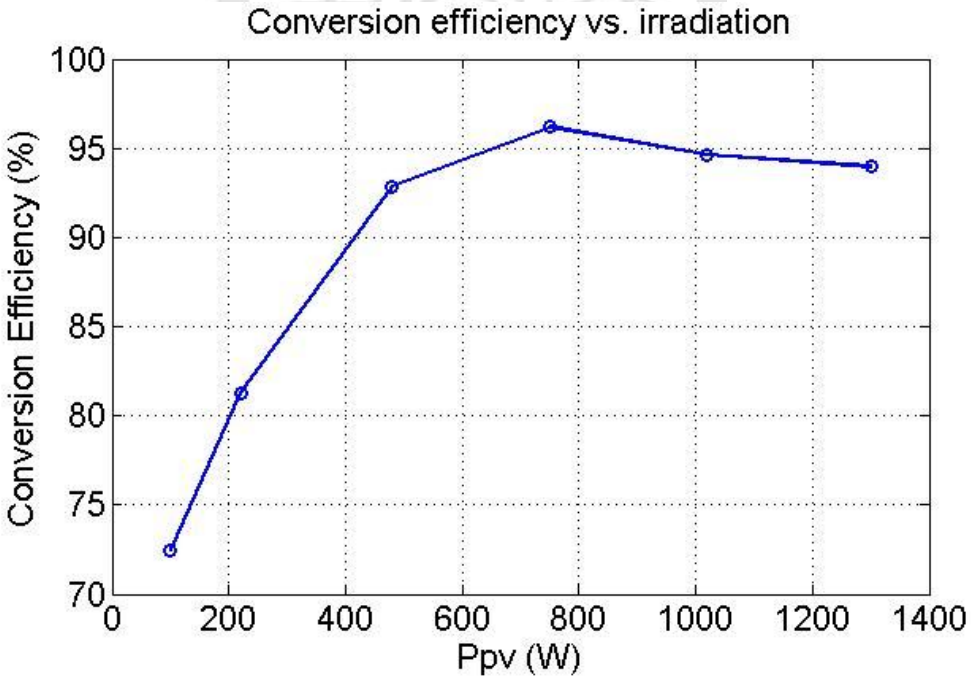


Fig. 5.18 Power conversion efficiency of HV-mode vs. irradiation variation

8. Performance summary

Table 5.2 Performance table

Classification	Descriptions
Technology Process	TSMC 0.35 μm 2P4M 3.3V/5V Mixed Signal CMOS Process
Supply Voltage	5V
Suitable Photovoltaic Voltage Rating Range	LV-mode: 0V~5V HV-mode:5V~500V
Suitable Photovoltaic Power Rating Range	LV-mode: 0W~5W HV-mode: 5W~1kW
Load Voltage	Battery/DC-bus dependent
Load Current	LV-mode: Max 1A HV-mode: Max 4A
Switching Frequency	LV-mode: 100kHz~200kHz HV-mode: 25kHz~50kHz
Tracking Efficiency	Max 99.83%
Transient Tracking Factor	0.15 (ms/W)
Power Conversion Efficiency	LV-mode: Max 91.04% (PV current=139mA, PV power=0.434W) HV-mode: Max 96.19% (PV current=2.215A, PV power=750W)
Chip Area	Active Area: 1.456 x 1.571 mm^2 Total Area: 1.718 x 1.796 mm^2

5.2 Measurement Setup

Fig. 5.19 shows the measurement setup for the LV-mode structure of the MPPT converter. Referring to Fig. 5.19, the Agilent E4361A solar array simulator used in the "SAS mode" of this simulator approximates the actual PV curves. Agilent E3630A is used to provide the power supply of this chip. Agilent N3301A and N3302A constitute the electric load. The voltage probe and current probe belong to the Tektronix MSO2024 oscilloscope and are used to measure the output voltage and output current of PV simulator. As for some external passive components, they are organized according to the requirement shown in Fig. 5.19. On the other hand, Fig. 5.20 shows the measurement setup for the HV-mode structure of the MPPT converter. It needs extra application circuits, such as the boost converter, resistor-type current sensor, etc., to connect to the high voltage terminal. The solar PV array is practical

with the high power rating. The chip of MPPT converter is as the proposed controller for the entire structure. Table 5.3 and Table 5.4 are the other components' summary of the LV-mode and the HV-mode, respectively.

Table 5.3 The values of components used in the LV-mode structure

Items	***Description***
Inductor of buck converter	22μH (ESR_L=0.2Ω)
Output capacitor of buck converter	10μF (ESR_C=0.15Ω)
Input capacitor	10μF (ESR_C=0.15Ω)

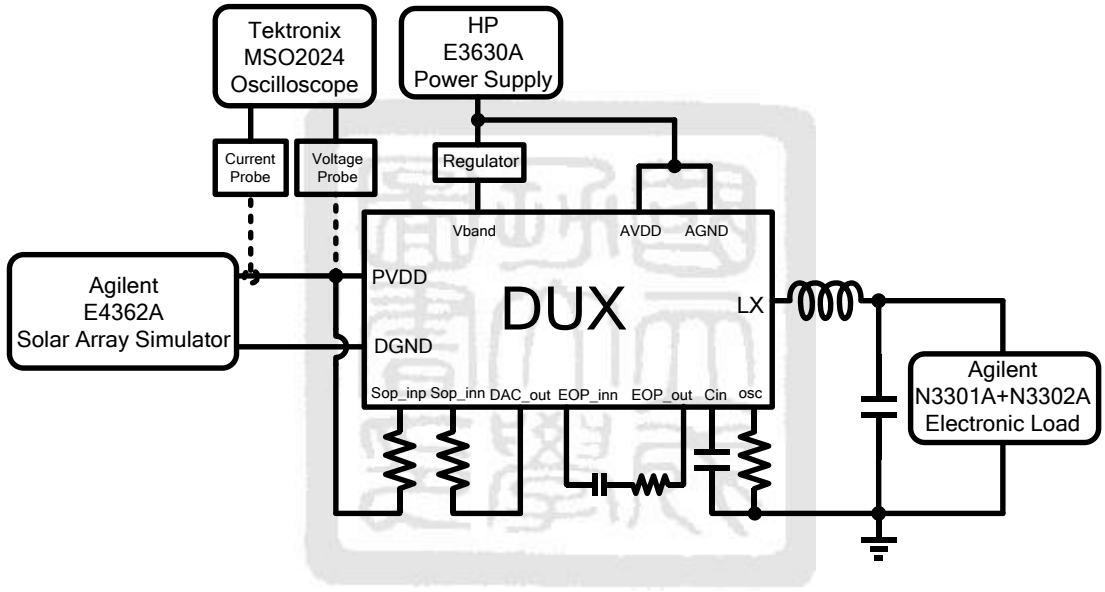


Fig. 5.19 The measurement setup of LV-mode structure of the MPPT converter

Table 5.4 The values of components used in the HV-mode structure

Items	***Description***
Inductor	1mH (ESR_L=1Ω)
Power NMOS	$R_{ds,on}$=0.1Ω, C_g=8nF
R_{sen}	0.1Ω
V_{fw} of diode ($^*V_{RRM}$=1000V)	1.48V
Output capacitor	100uF (ESR_c=1Ω)

* Repetitive peak reverse voltage

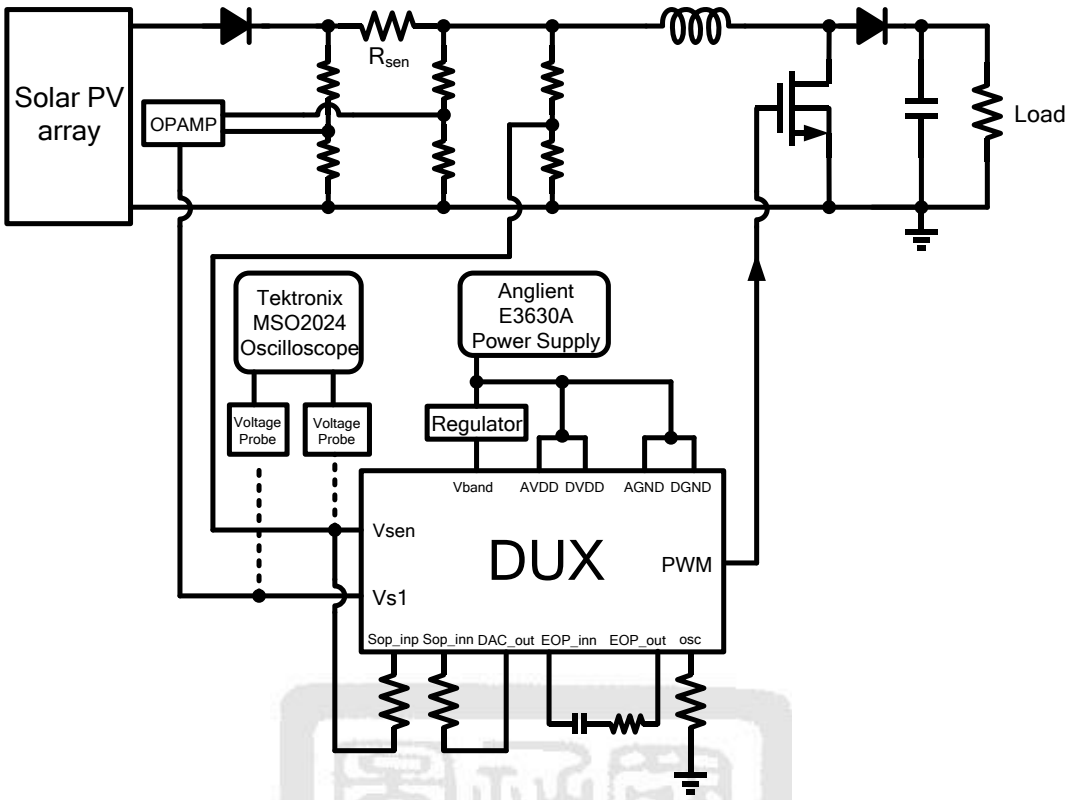


Fig. 5.20 The measurement setup of HV-mode structure of the MPPT converter

5.3 Comparison

In order to comparing the MPPT converter fairly, we define the specifications of the MPPT converter in the chapter 2. The well-known concept of MPPT is to achieve a high tracking efficiency and a good transient response, simultaneously. Therefore, the parameters of tracking efficiency and transient tracking factor (TTF) are regarded as a comparison between the MPPT converters. Table 5.5 is the comparison between this work and other published IEEE papers within late three years. We can observe that the MPPT converter designed in this work has the best TTF and tracking efficiency. Switching frequency of this work is faster than others in order to reduce the filtering value of inductor and capacitor in the dc-dc converter. Inductor 22μH and capacitor 10μF are used in this work. On the contrary, inductor 100μH~1mH and capacitor 100μF~3mF are used in the other reference. Fig. 5.21 plots the tracking efficiency versus TTF based on the data listed in table 5.5. It can be seen that the design plotted on the lower right position of Fig. 5.21 performs better tracking

accuracy and speed.

Table 5.5 Comparison between published IEEE papers and this work

Characteristic	[31]	[32]	[33]	[34]	[5]	**This work**
Tracking Efficiency	99.2%	98.8%	98.5%	99%	99%	**99.83%**
TTF (ms/ W)	2.19	369.7	7.44	16.1	52.4	**0.15**
On-chip implementation	No	No	No	No	No	**Yes**
Microprocessor	Yes	Yes	Yes	Yes	Yes	**No**
Switching frequency(kHz)	20	10	20	10	10	**LV-mode: 200** **HV-mode: 25**

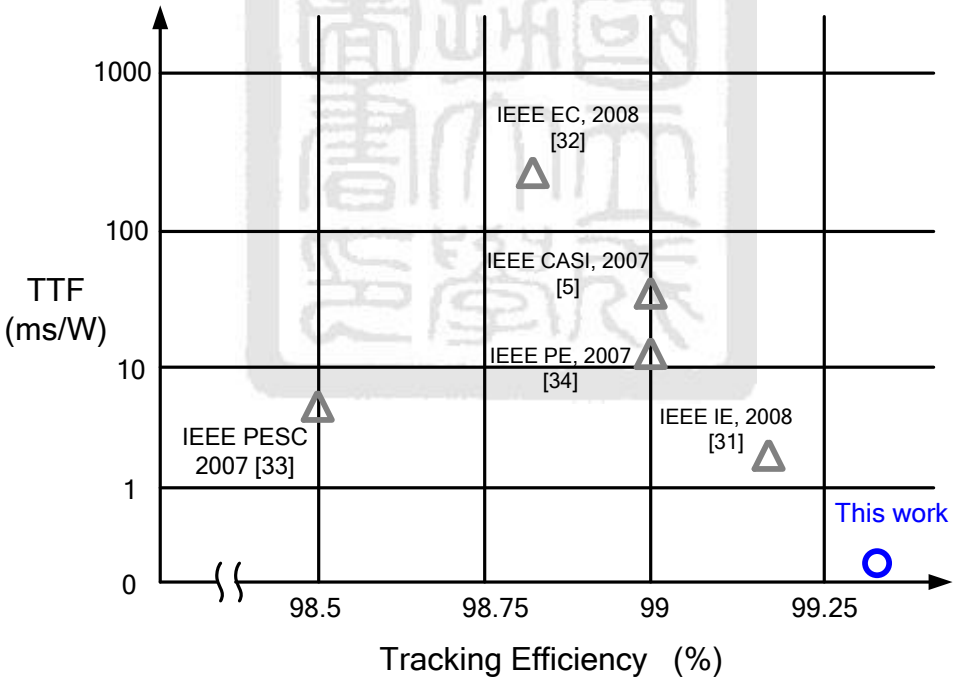


Fig. 5.21 Tracking Efficiency vs. TTF

5.4 Measurement Results

Some measurement results will be described in the section, including the waveforms of circuits and performance.

1. Functional waveforms

The functional waveforms including pin LX (PWM), pin PVDD (the output voltage of solar array simulator), and ramp signal are shown in the Fig. 5.22. These waveforms can prove the operation which is not a failure. The waveforms are measured under the setup of the solar array simulator E4362A SAS mode are V_{mp} 3.8V, I_{mp} 0.2A, V_{oc} 5V, I_{sc} 0.25A. How to operate the E4362A could see the user's guide [35].

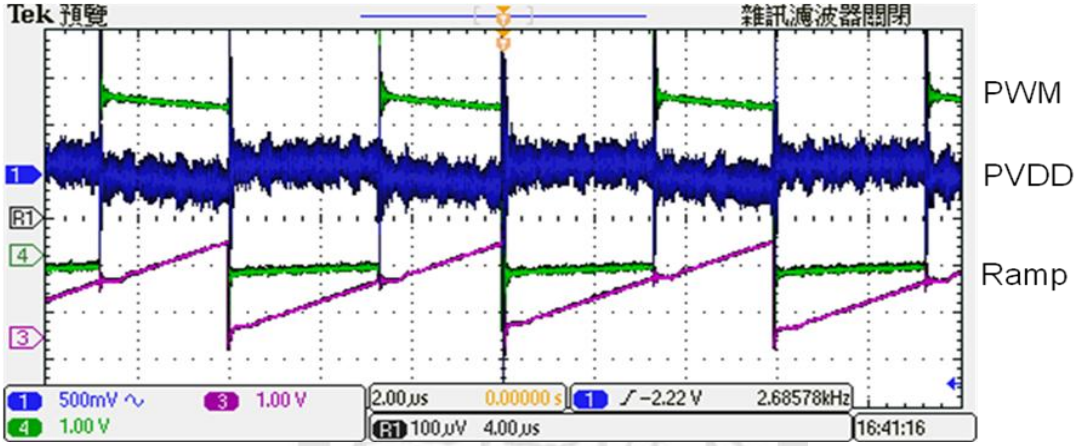


Fig. 5.22 Waveforms of PWM (1V/div), PVDD (0.5V/div), Ramp (1V/div)

From Fig. 5.22, it can be seen that the switching frequency is 167 kHz, and the voltage ripple is within the 500 mV (~10%) which is bigger than that in the post-simulation. Increasing the value of the capacitor on the pin Cin, the voltage ripple will be decreased within 200 mV (~4%), shown in the Fig. 5.23. It is the limit of the simulator [35]. Fig. 5.24 shows the output of the DAC under the stable state.

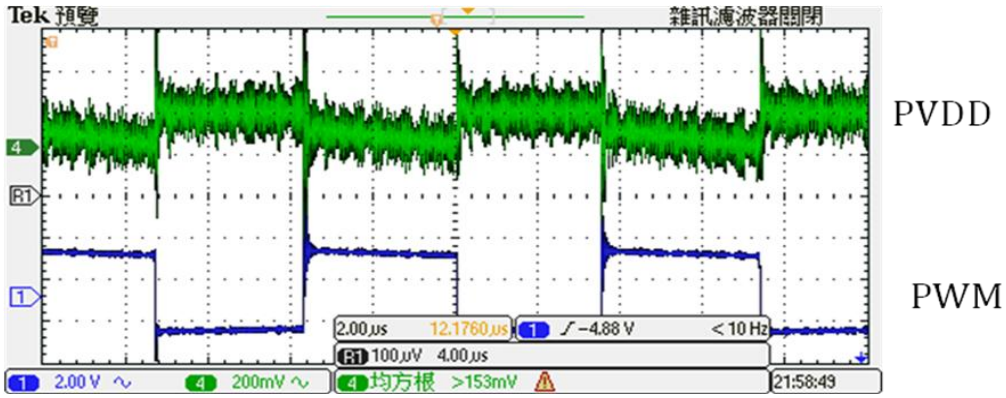


Fig. 5.23 Improved waveforms of PVDD (0.2V/div), PWM (2V/div)

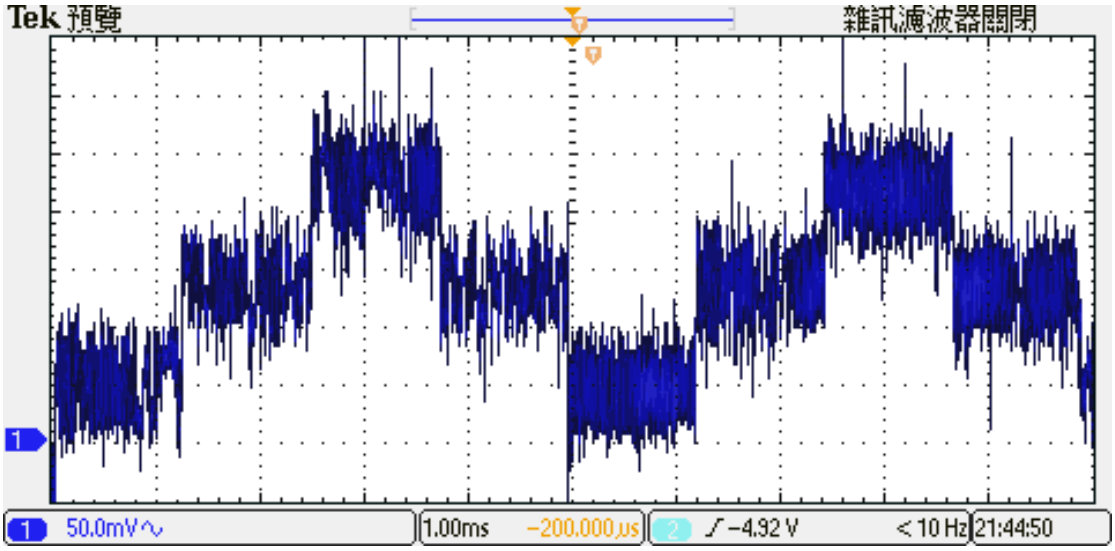


Fig. 5.24 The waveform of DAC output at the stable state (50mV/div)

2. Measurement of the tracking efficiency

The tracking efficiency is measured by the oscilloscope to get the RMS value of the photovoltaic output voltage and photovoltaic output current, and then we get RMS value of the photovoltaic output power. For example, like the Fig. 5.25, the RMS value of photovoltaic output voltage is 3.81V, and the photovoltaic current is 0.199mA. The channel M is the math functional waveform, which is the multiplication with output voltage and output current. It is equal to the photovoltaic output power, and the RMS value is 755mW. The setup of the solar array simulator E4362A SAS mode is V_{mp} 3.8V, I_{mp} 0.2A, V_{oc} 4.5V, I_{sc} 0.3A. Consequently, the tracking efficiency is 99.34%.

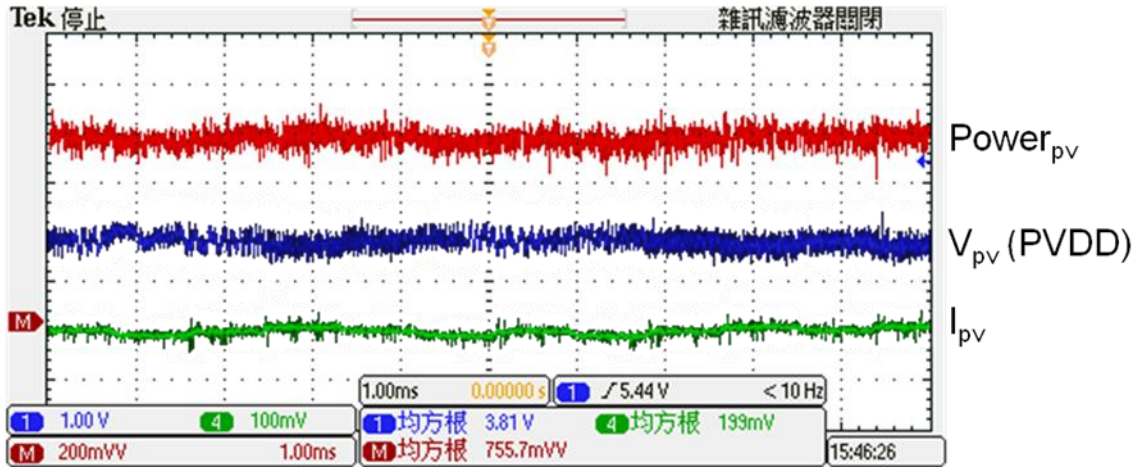


Fig. 5.25 Waveforms and RMS values of photovoltaic output voltage (1V/div), photovoltaic output current (100mV/div), and photovoltaic output power

(200mV/div), time (1ms/div)

From the Fig. 5.26, the maximum tracking efficiency is 99.34% under the irradiation 200W/m^2. There is a conclusion here that the tracking efficiency is a little bit worse than that in the post-simulation shown in Fig. 5.16. But the trend of tracking efficiency measured is as similar as that in the post-simulation.

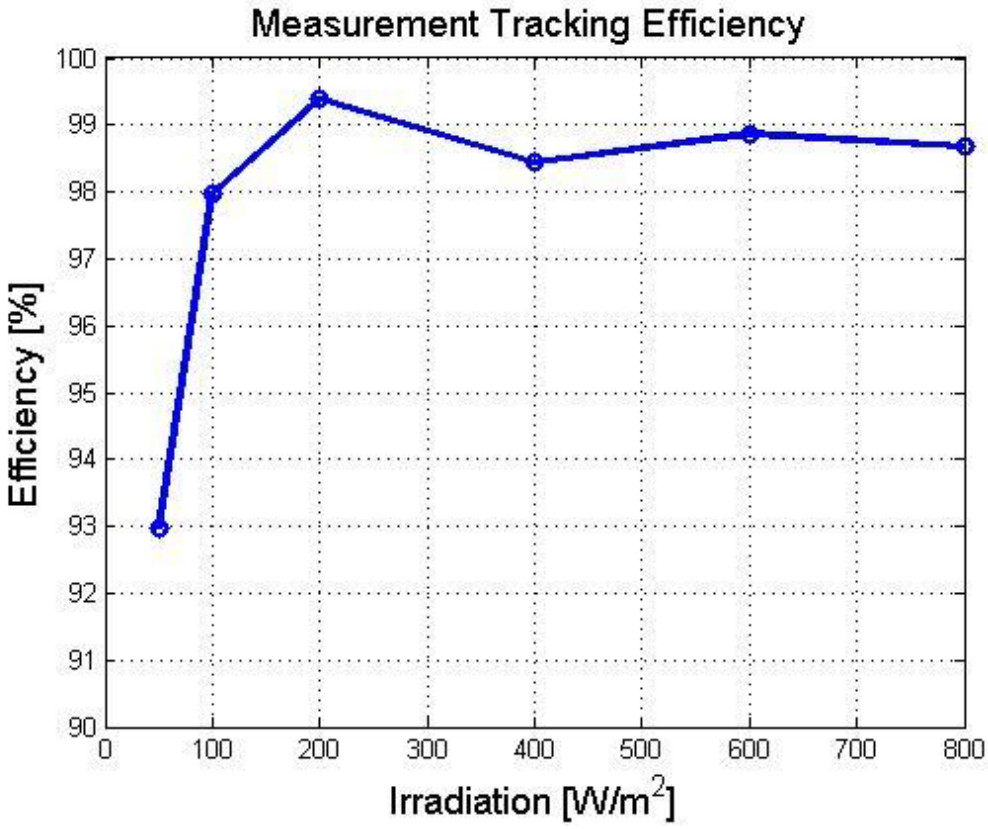


Fig. 5.26 Measurement of tracking efficiency

3. Transient response and measurement of the TTF

The measurement results of the transient response are shown in the following graphs. The condition, which we set, simulates the irradiation from 600W/m^2 to 200W/m^2. In other words, the maximum output power of SAS is set from 2W to 0.7W, shown in the Fig. 5.27. And then, the state of the irradiation from 200W/m^2 to 600W/m^2 is shown in the Fig. 5.28. The measurement of the TTF is shown in the Table 5.6.

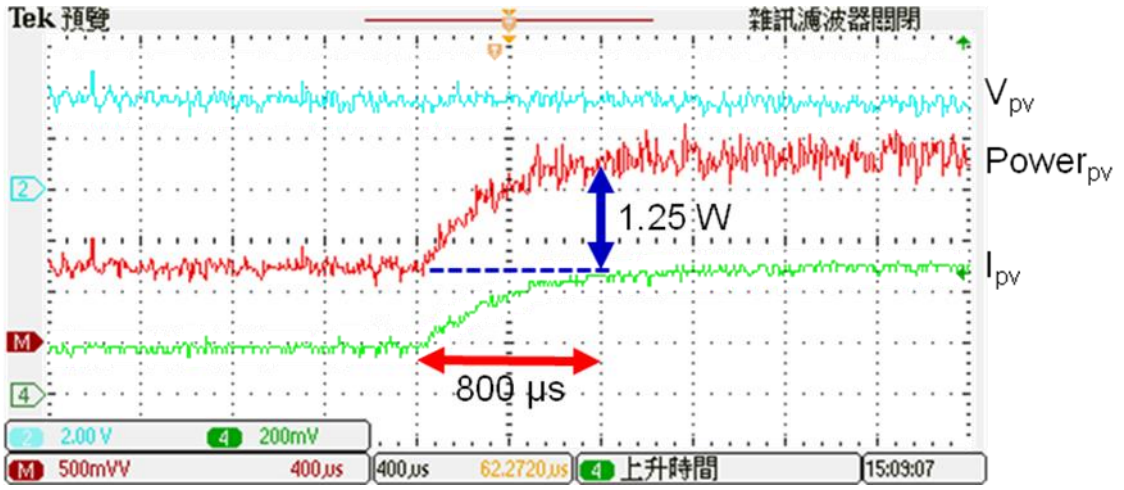


Fig. 5.27 Transient response of irradiation level 600W/m^2 ➔ 200W/m^2, V_{pv}(2V/div), I_{pv}(0.2V/div), $Power_{pv}$(0.5V/div), Time (400 μ s/div)

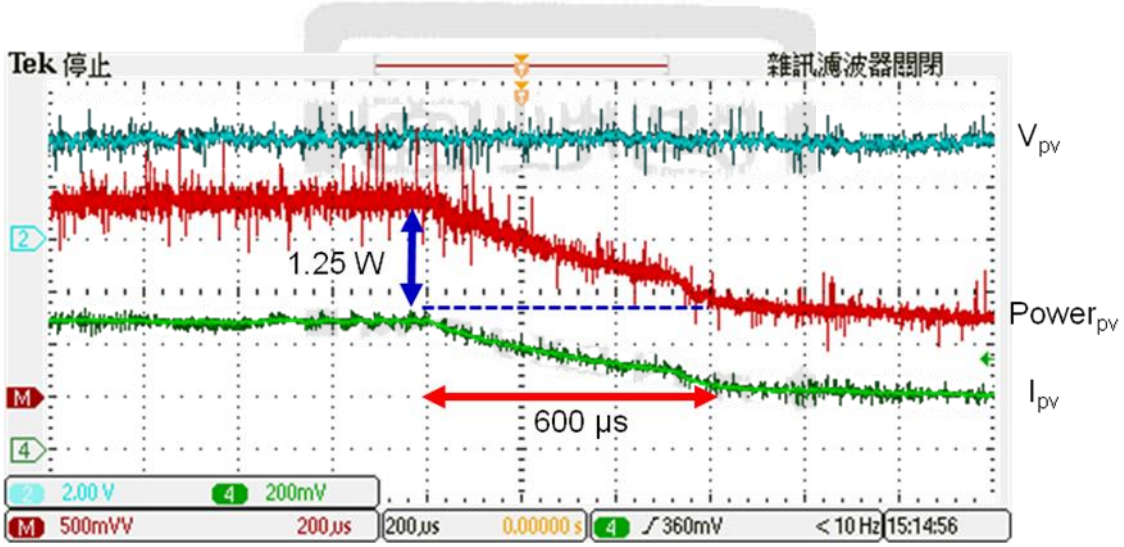


Fig. 5.28 Transient response of irradiation level 200W/m^2 ➔ 600W/m^2, V_{pv}(2V/div), I_{pv}(0.2V/div), $Power_{pv}$(0.5V/div), Time (200 μ s/div)

Table 5.6 Measurement results of the TTF

Transient Tracking Factor (TTF)	
600 ➔200(W/m^2)	**200 ➔600(W/m^2)**
0.47 (ms/ W)	**0.63(ms/ W)**

4. Measurement results of power conversion efficiency

The result of power conversion efficiency is shown in the Fig. 5.29. The maximum efficiency is 91.04% at the input power 0.8W. The trend measured is as similar as that in the post-simulation.

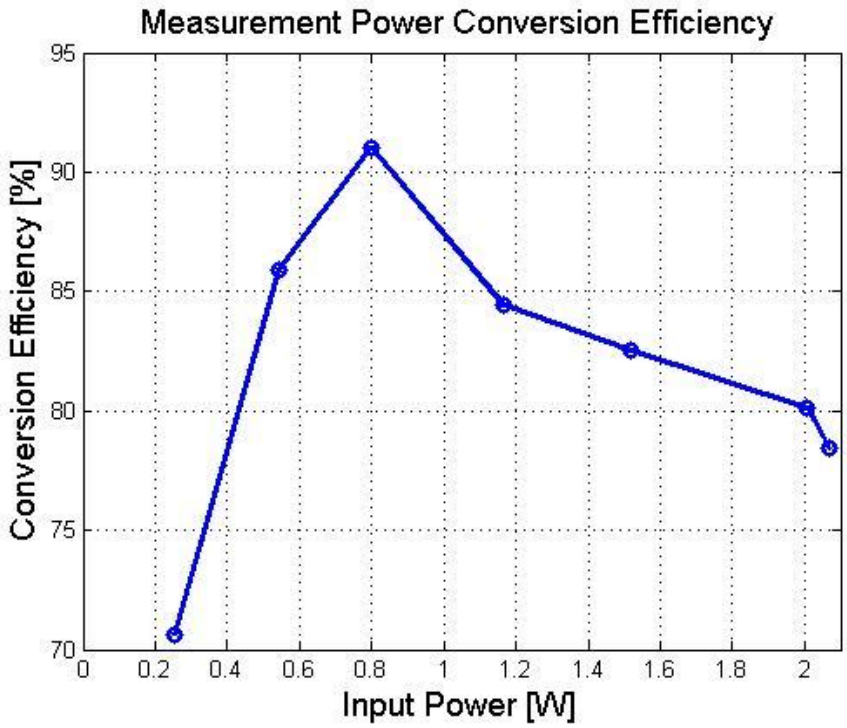


Fig. 5.29 Measurement results of power conversion efficiency

5. Measured performance summary

Table 5.7 Measured performances summary

Classification	Descriptions
Supply Voltage	5V
Suitable Photovoltaic Voltage Rating Range	0V~5V
Suitable Photovoltaic Power Rating Range	0W~5W
Load Voltage	Battery/DC-bus dependent
Load Current	Max. 1A
Switching Frequency	100kHz~200kHz
Tracking Efficiency	Max. 99.34%
Transient Tracking Factor	0.47 (ms/W)
Power Conversion Efficiency	Max. 91 %

Chapter 6

Conclusion

In this thesis, an innovative CMOS MPPT converter with a hybrid high-voltage-mode and low-voltage-mode structure for a wide PV power rating range is implemented, including the analysis, circuit implementations and verification. This MPPT converter is fabricated by TSMC 0.35 μm 2P4M 3.3V/5V Mixed Signal CMOS Process. The measured maximum tracking efficiency is 99.3%, TTF is 0.47ms/W, being the best in the world, and the maximum power conversion efficiency could achieve 91% and 96% at the low-voltage-mode and high-voltage-mode, respectively. From the comparison between the measurement results and that in other techniques, this work presents a photovoltaic maximum power point tracking converter with the smallest area, the lowest cost, and the best performance in the world. Besides, it is adjustable for real photovoltaic modules to optimal performance. Therefore, it can be embedded in many applications widely, such as portable applications, vehicular applications, and building-integrated photovoltaic systems and so on. However, it still exists that some parts of this work could be improved again in the future like circuit more simplicity, increasing efficiency, etc. This concept will be a developmental trend of the future in the green energy industry.

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