INTEL® SERIAL VOLTAGE IDENTIFICATION (SVID) PROTOCOL TRAINING-101

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Warm-up

A Real Case: System Hang with MSMI_N(or CATERR#) triggered during enter/exit PkgC6

- Any error log?
- Power issue?
  - SVID transaction error?
  - SVID DC electrical parameter or AC timing violated ?
  - VRTT test passed or failed?
  - What kind of SVID decoder tool can use?

Note: SVID = Intel® Serial Voltage Identification

Agenda

1. Overview
2. SVID specification
   - Physical Layer
   - Data Link Layer
   - Function Layer
3. SVID issue debug tool and flow

Note: SVID = Intel® Serial Voltage Identification

What SVID can be used to?

The SVID interface can be connected to multiple slaves. Slaves are identified by a unique address. The SVID master can address a command to either an individual slave or it can broadcast a command to multiple slaves.

The SVID interface is used primarily to

- Control dynamic voltage regulators (VRs)-DVID
- Read back telemetry information from VRs or dedicated power sensors-Monitor current/power
- Configure the VRs or dedicated power sensors-Configure VR
- Communicate alert-conditions interrupts the SoC-Alert response

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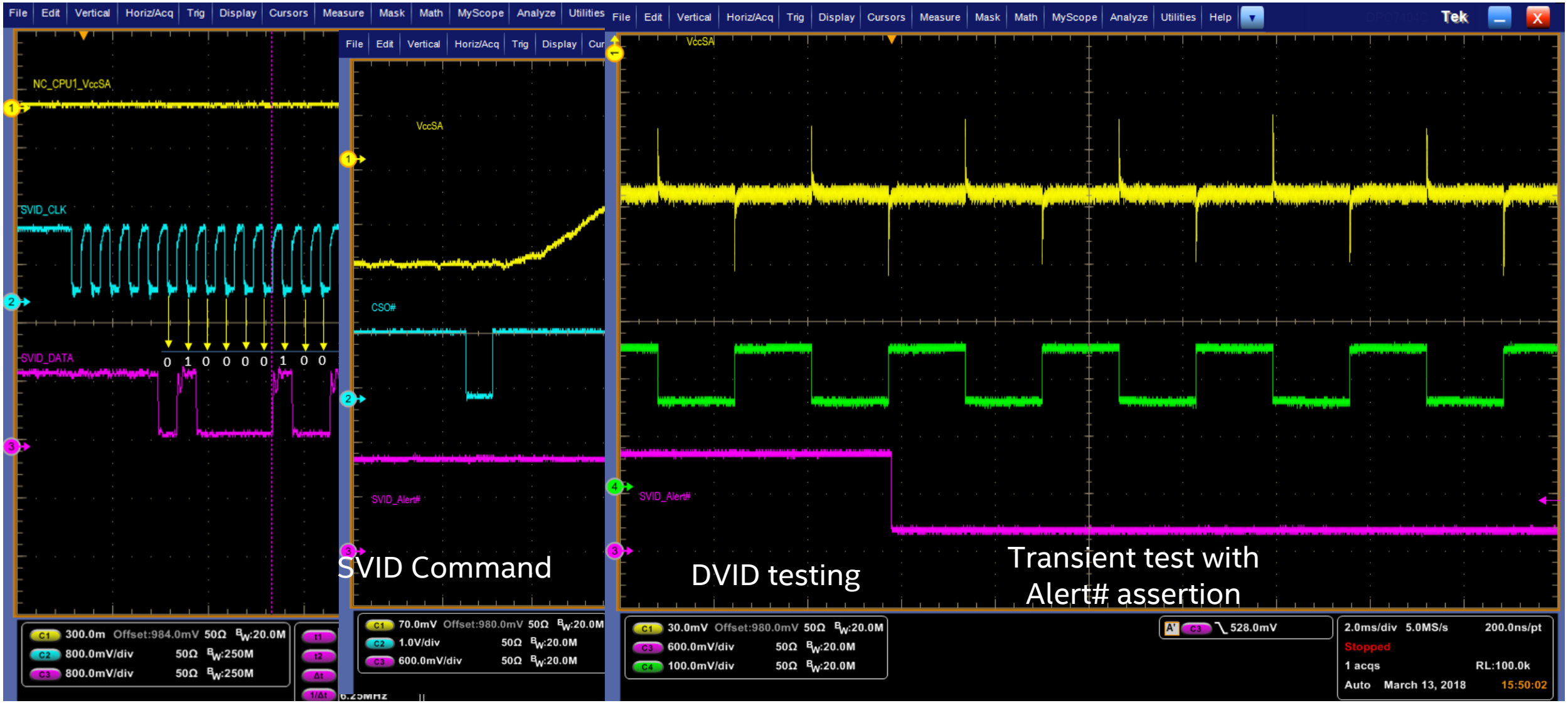
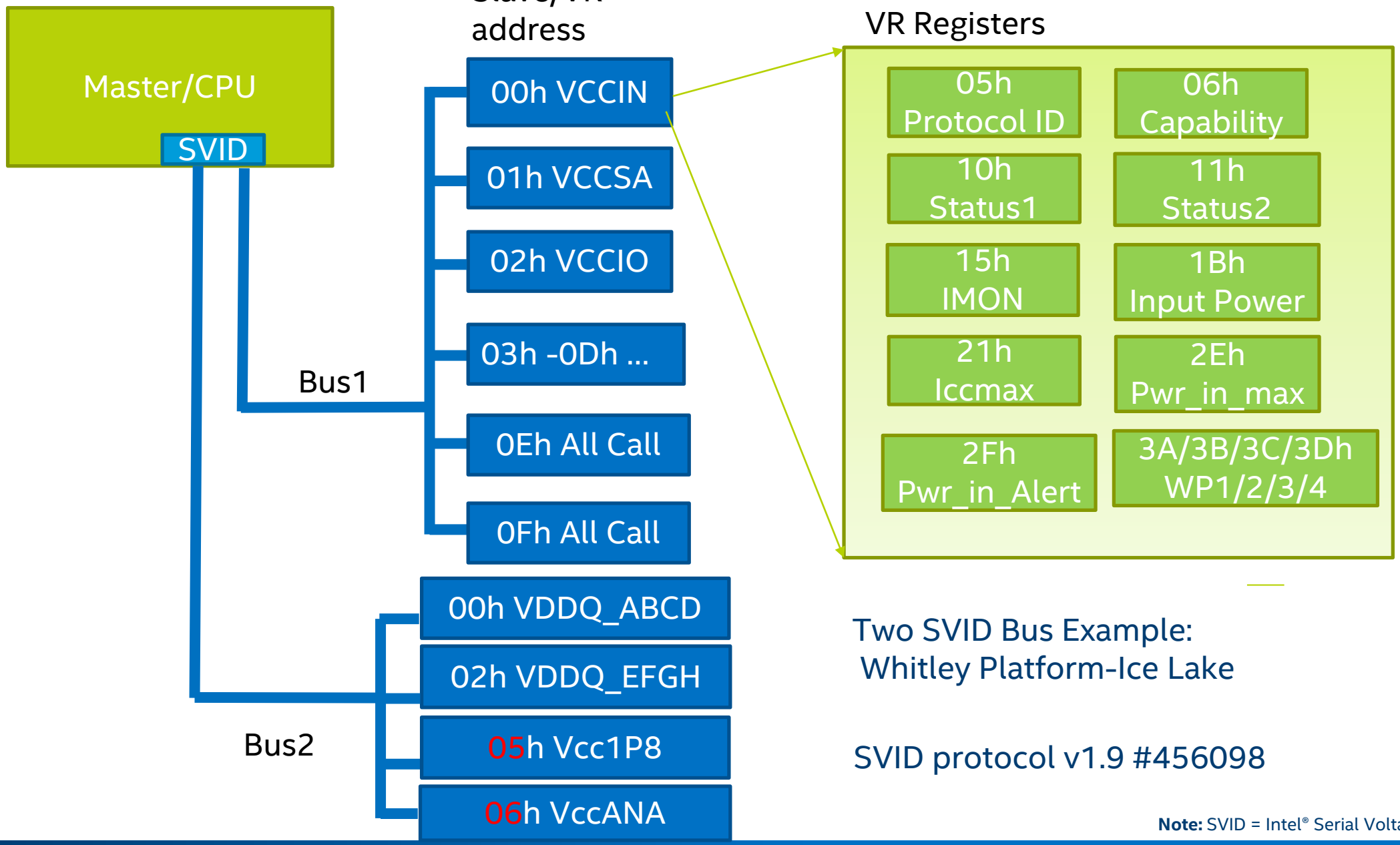
Waveform during debug or VRTT test



Note: SVID = Intel® Serial Voltage Identification

SVID overview



Two SVID Bus Example:
Whitley Platform-Ice Lake

SVID protocol v1.9 #456098

Note: SVID = Intel® Serial Voltage Identification

SVID SPECIFICATION

Note: SVID = Intel® Serial Voltage Identification

Physical/Data/Function Layer

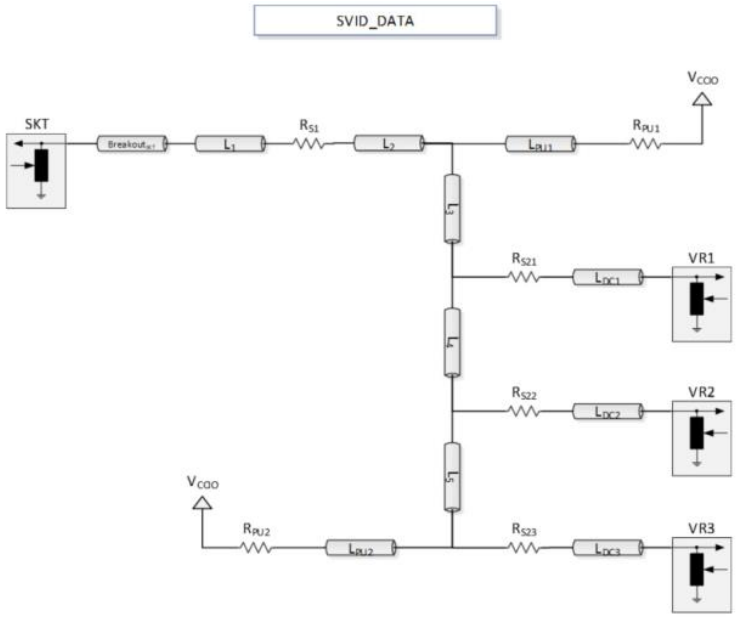
The SerialVID specification is separated into layers, patterned after the Open Systems Interconnection (OSI) network model. The layers are:

- **Physical Layer** – specifies how individual bits are communicated across the SerialVID link. The physical layer specifications are found in the **PWM specifications**.
- **Data Link Layer** – specifies how bits are bound together into transactions that are used to send the command and response data between the SVID master and the SVID slaves.
- **Functional Layer** – specifies how the commands are interpreted by the slave VRs and the responses are interpreted by the master. (**Command Set**)

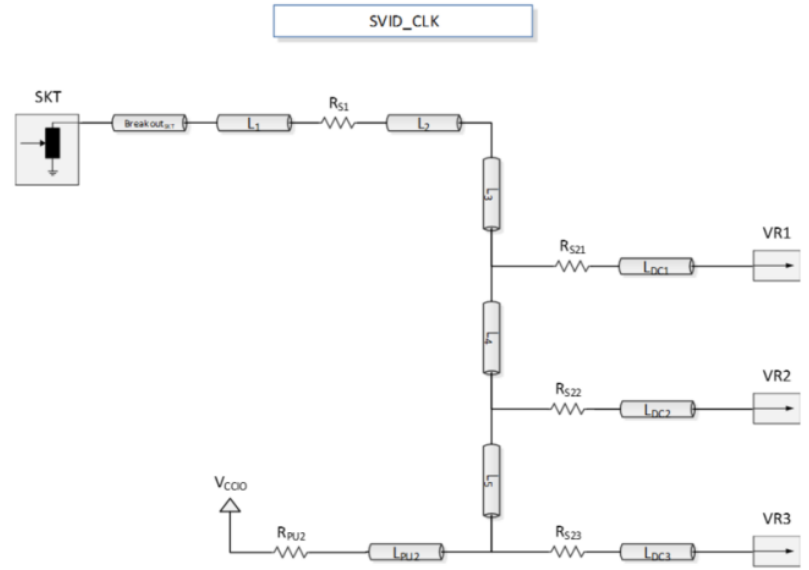
Note: SVID = Intel® Serial Voltage Identification

PHYSICAL LAYER

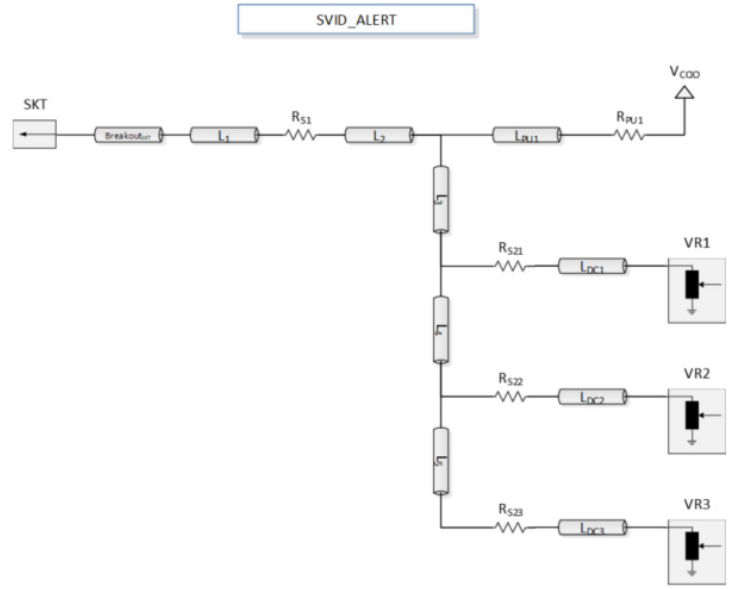
Typical SVID Daisy Chain Topologies



$Breakout_{SKT}$	$Breakout_{SKT} + L_1$	L_2	$L_{DC\#}$	$L_{PU\#}$	$L_3 + L_4 + L_5$	R_{S1}	$R_{S2\#}$	R_{PU1}	R_{PU2}	V_{CCIO}
< 4"	< 4.5"	< 0.2	< 1"	< 0.2"	< 27"	0 Ohms	0 Ohms	100 Ohms	100 Ohms	1.0 V



$Breakout_{SKT}$	$Breakout_{SKT} + L_1$	$L_{DC\#}$	L_{PU2}	$L_2 + L_3 + L_4 + L_5$	R_{S1}	$R_{S2\#}$	R_{PU2}	V_{CCIO}
< 4"	< 4.5"	< 1"	< 0.2"	< 27"	0 Ohms	150 Ohms	50 Ohms	1.0 V



$Breakout_{SKT}$	$Breakout_{SKT} + L_1$	L_2	$L_{DC\#}$	L_{PU1}	$L_3 + L_4 + L_5$	R_{S1}	$R_{S2\#}$	R_{PU1}	V_{CCIO}
< 4"	< 4.5"	< 0.2"	< 1"	< 0.2"	< 27"	0 Ohms	0 Ohms	50 Ohms	1.0 V

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SVID Routing Guide

- Refer to SVID routing guide in PDG (for Purley, Chapter 6.9 of PDG #546835)

- Highlight:
  - ✓ SVID must be ground reference. Do not route SVID bus signals under phase nodes or high side MOSFET nodes that generate electrical noise.
  - ✓ Low inductance path for VIO termination voltage to termination resistors (10 mils is the minimum trace width allowed). Bypass termination voltage as close as possible to termination resistor with 10 µF and 0.1 µF capacitors to ground (bypass is required unless supplied from a full plane).
  - ✓ Trace length matching must be used between the Clock and Data lines to ensure a length difference of no more than 250 mils;
    Microstrip (MS) and Stripline (SL) routing are allowed. Spacing of 13.5 mils on MS and 12 mils on SL within the Clock and Data signals, and 15 mils to all other non-static lines. For 10 mils of spacing on SL, do not exceed this spacing for more than 2.5 inches. An exception is for the breakout regions where spacing between lines can drop to 4 mils for coupling lengths less than 0.5 inches.

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Model and Collaterals

- SKL MISC SI Models/Decks
  - Document RDC# : 566889-skl-misc-si-model-566889-rev0-9
  - Folders : SVID_Lowloss and SVID_Midloss under “\miscio_decks \miscio_purley\”
  - Deck : Hspice format “purley_svid_daisy_3vr_clk_data_r1p0a.sp”
  - Model User Guide (MUG) : SKL_MISC_IO_556993_Rev0.9.pdf
    - SVID Data Daisy Chain Topology
    - Suggest to do SI post-layout simulation (Use third tool to extract PCB models of VCLK, VDIO and VALT_N nets).

SVID DC Electrical Parameters

544905_VR13_and_VR13HC_rev_1.3

546834-skx-eds-vol3

Symbol	Parameter	Min	Typ	Max	Units
VccIO	CPU I/O voltage (also known as VccIO)	0.90	0.95 to 1.05	1.1	V
V_{IL}	Input low voltage	-	-	0.45	V
V_{IH}	Input high voltage	0.65	-	-	V
Vhyst	Hysteresis voltage	0.05	-	-	V

VR

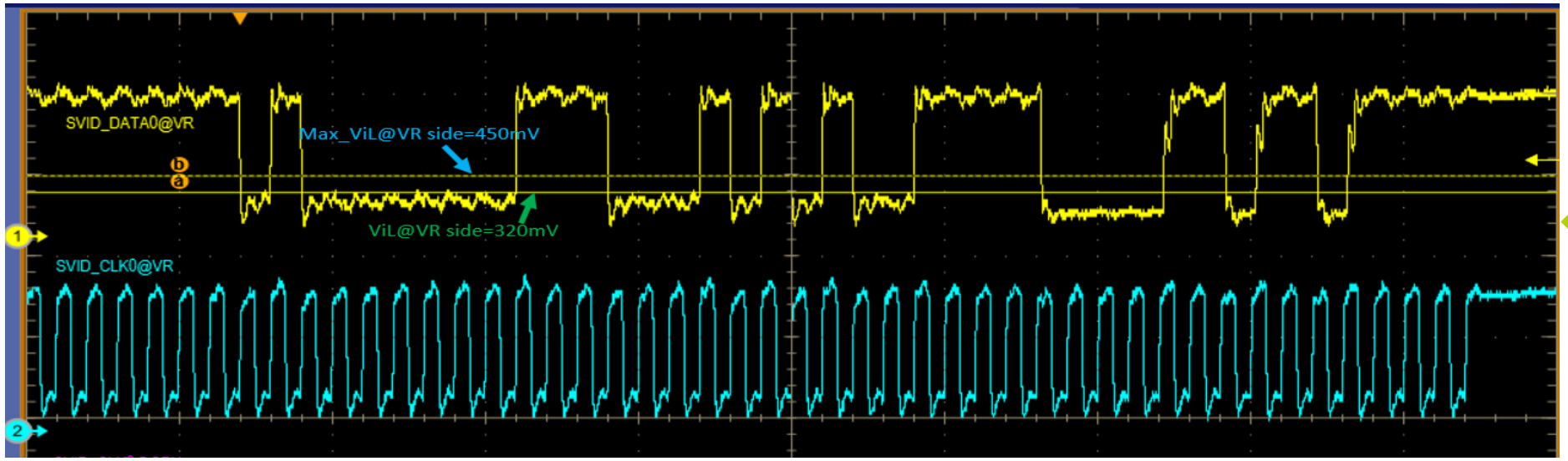
Symbol	Parameter	Min	Typ	Max	Units
VccIO	CPU I/O voltage (also known as VccIO)	VccIO-5%	1.0	VccIO+5%	V
V_{IL}	Input low voltage	-	-	0.3*VccIO	V
V_{IH}	Input high voltage	0.7*VccIO	-	-	V
Vhyst	Hysteresis voltage	0.1*VccIO	-	-	V

CPU

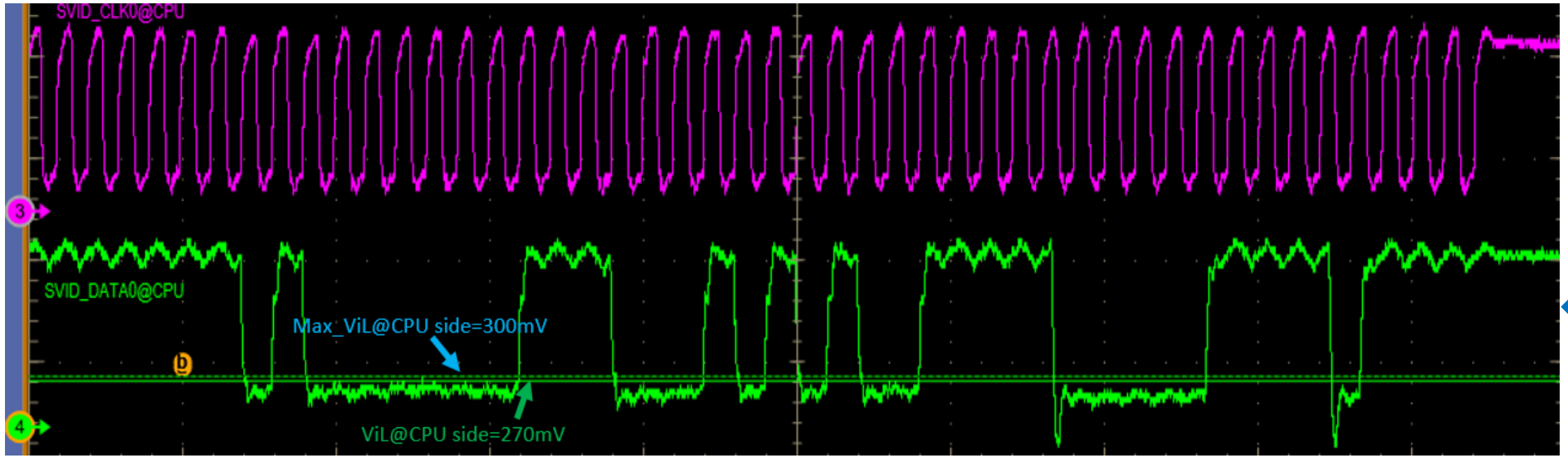
VIL, VIH are critical parameters that need to be measured and verified on the customer board. If there is a violation of VIL, tune the pullup and termination resistors.

Note: SVID = Intel® Serial Voltage Identification

Waveform Example of VIL

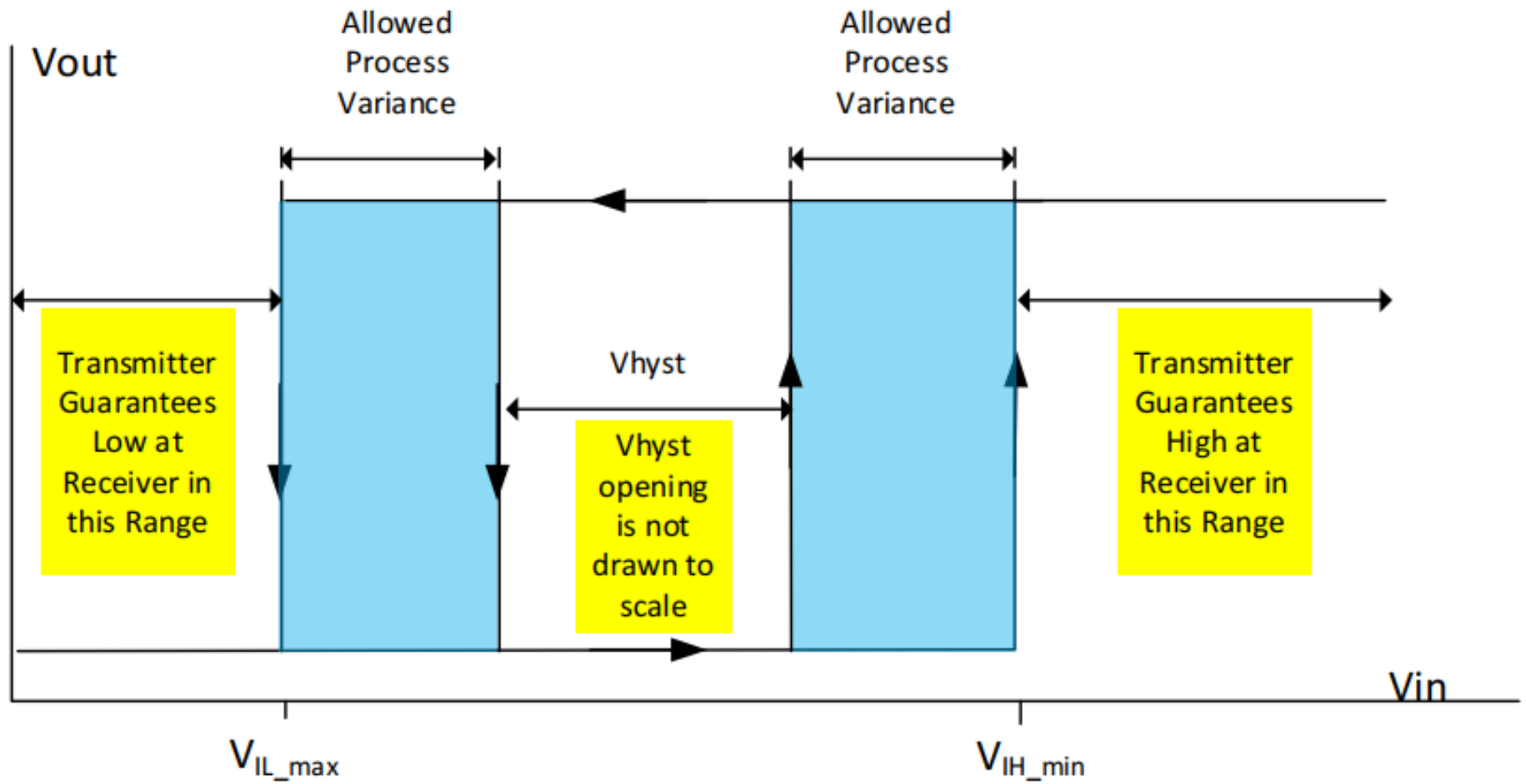


VR



CPU

Input Buffer Variance and Hysteresis

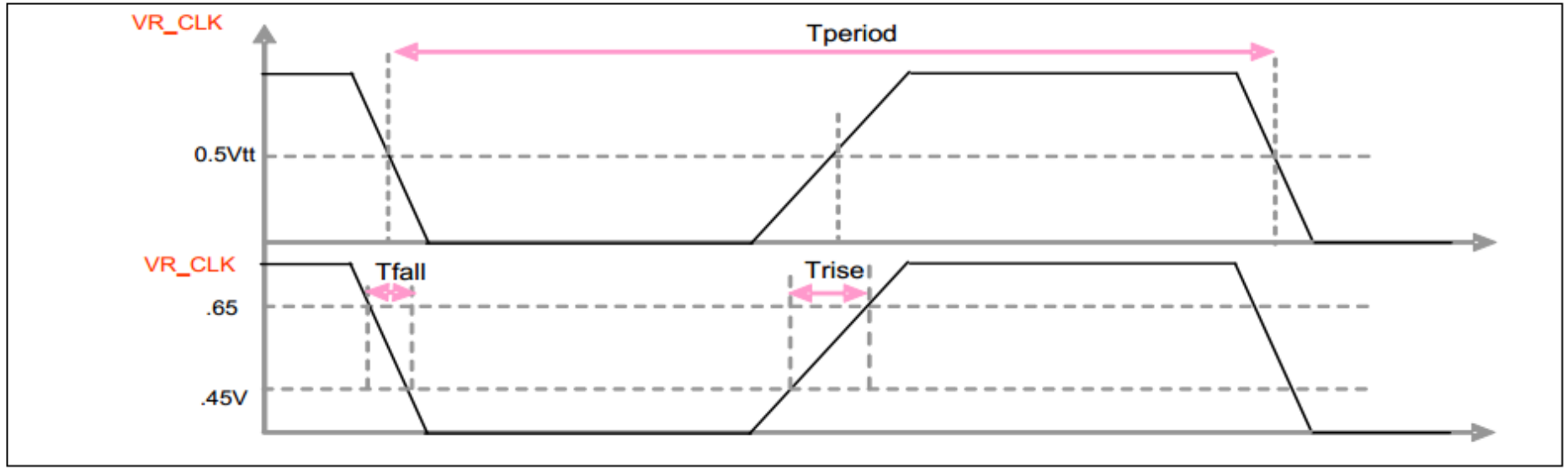


SVID CLK AC timing

Table 3-3 VCLK AC Timing Parameters 100ns 40ns 38.1ns

Symbol	Parameter	Min	Typ	Max	Units	Notes
	VCLK Frequency based on system BCLK/4, BCLK/6, BCLK/8	10	25	26. 25	MHz	1, 4,5, 6
Trise	VCLK Rise Time (@VR Pad)	0.25		5.5	ns	2
Tfall	VCLK Fall Time (@VR Pad)	0.25		5.5	ns	2
	Duty Cycle	40		60	%	1, 4

Figure 3-2 Measurement Points for VCLK high, low, rise, and fall time, Tperiod

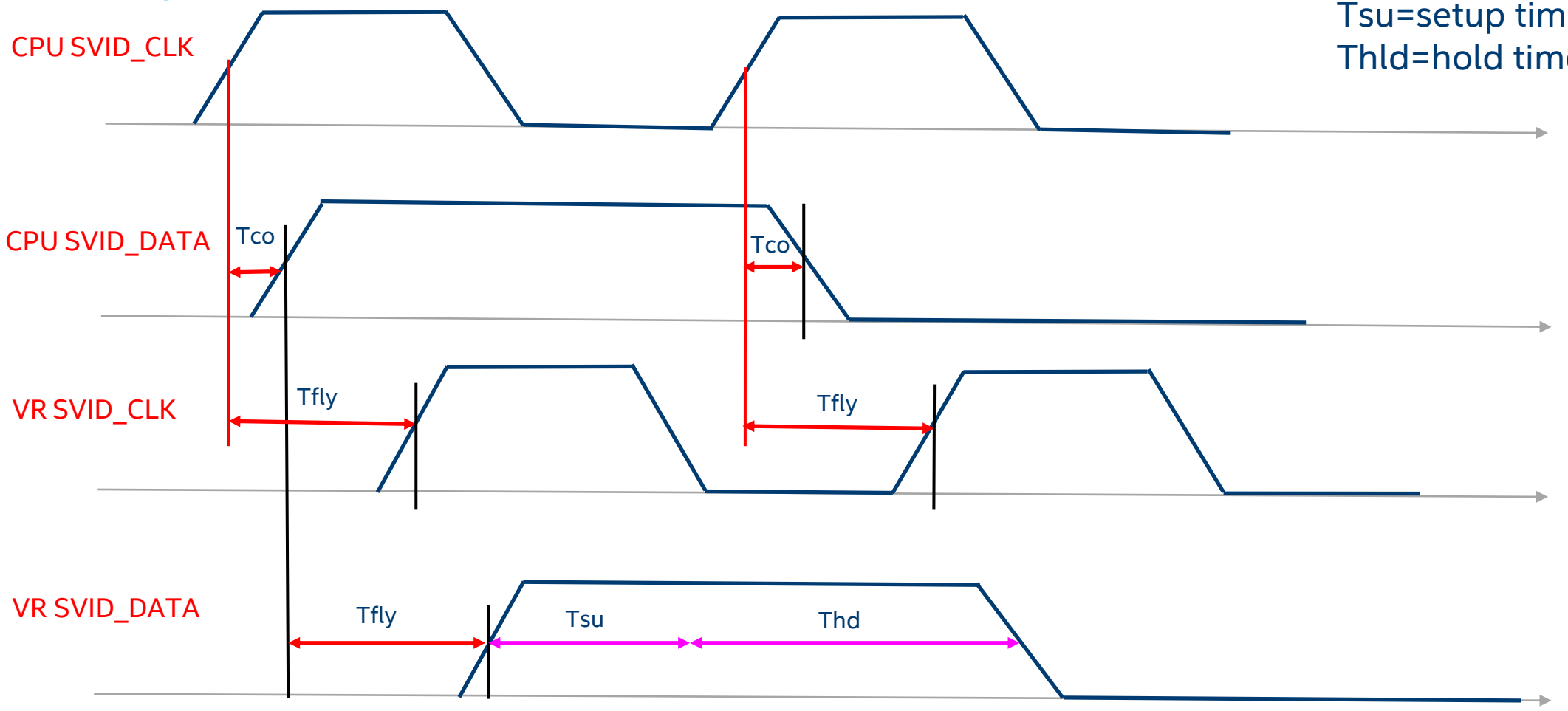


Note: SVID = Intel® Serial Voltage Identification

Platform Bus Timing-all market segments

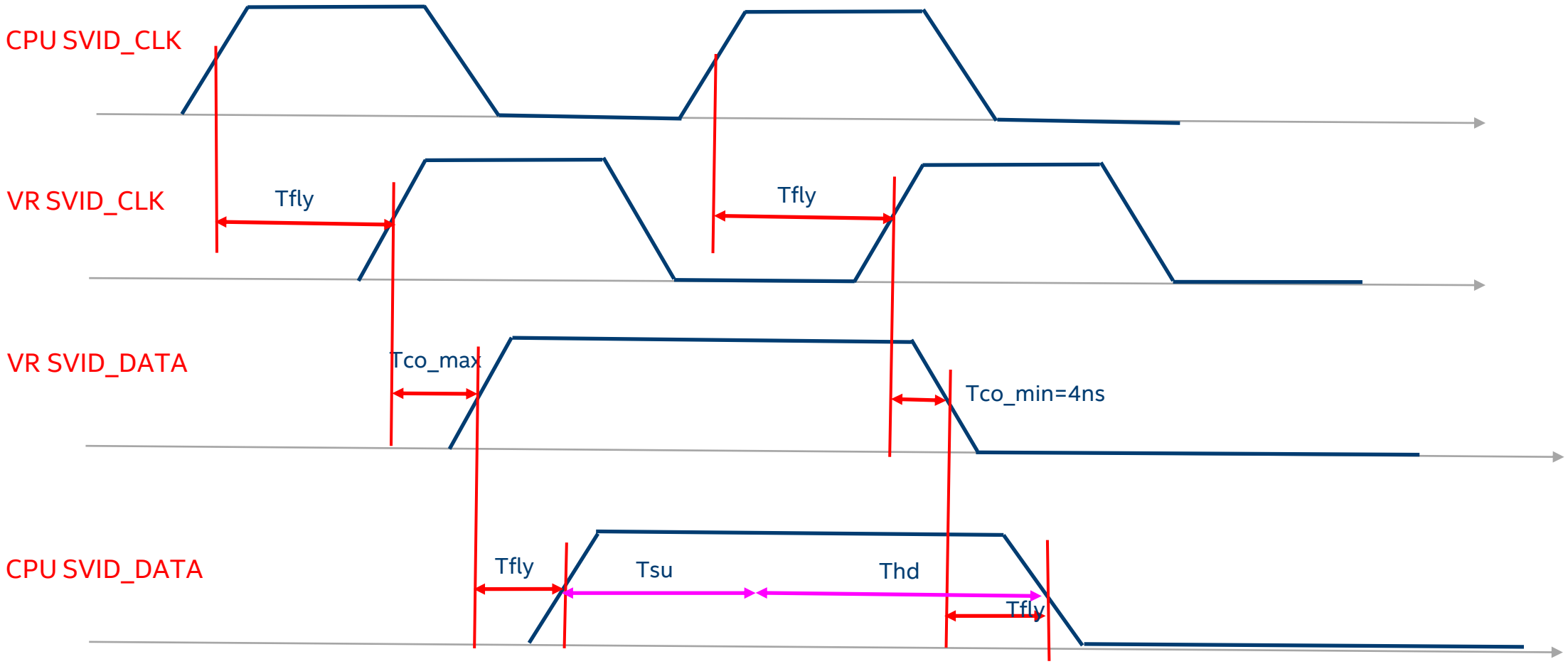
CPU driving

Tco =clock to output
Tsu=setup time
Thld=hold time



Platform Bus Timing-all market segments (Cont.)

VR driving



Platform Bus Timing-all market segments (Cont.)

- Tco_max_VR Clock to data delay = 12 ns
- Tco_min VR clock to data delay = 4 ns
- Tsu_VR - Setup time of signal VDIO at VR side = 7 ns
- Thld_VR - Hold time of signal VDIO at VR side = 14 ns

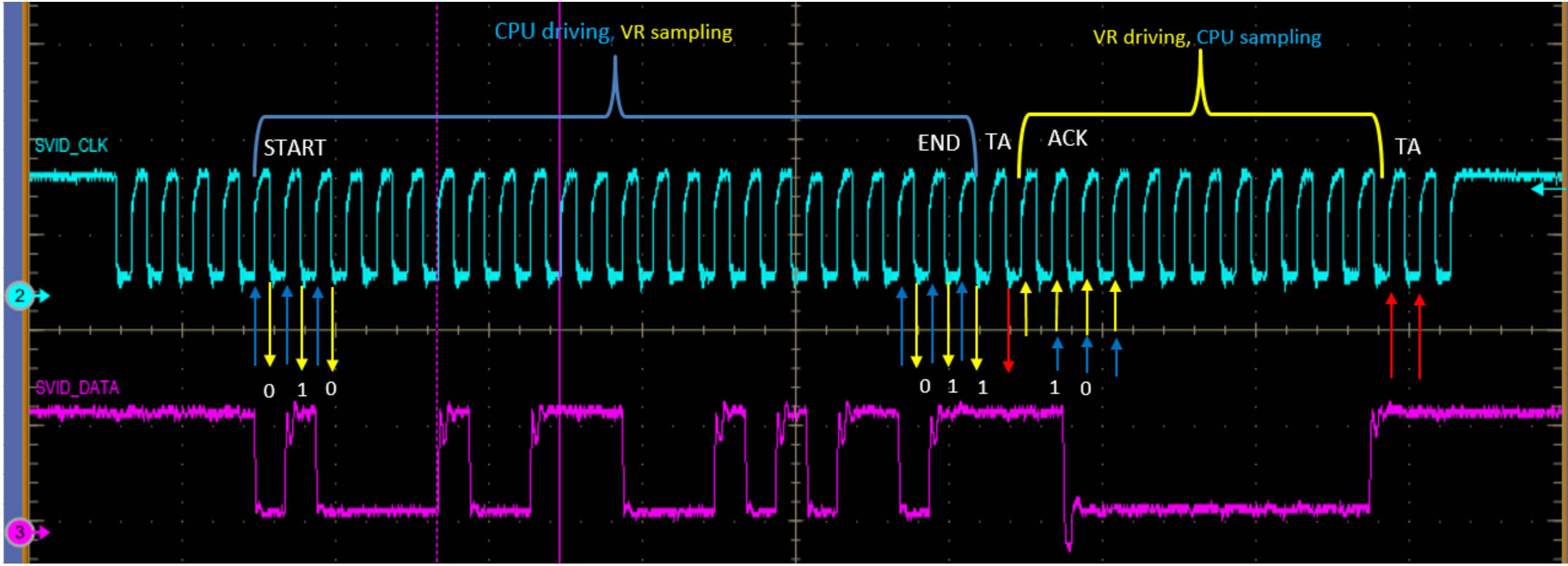
VR

- Tco_max_CPU Clock to data delay @bump = 0.65 ns
- Tco_min_CPU Clock to data delay @bump= -3.6 ns
- Tsu_CPU - Setup time of signal VDIO at CPU side = 1 ns
- Thld_CPU - Hold time of signal VDIO at CPU side = 3 ns

CPU

DATA LINK LAYER

SVID link Layer-Clock and Data Driving



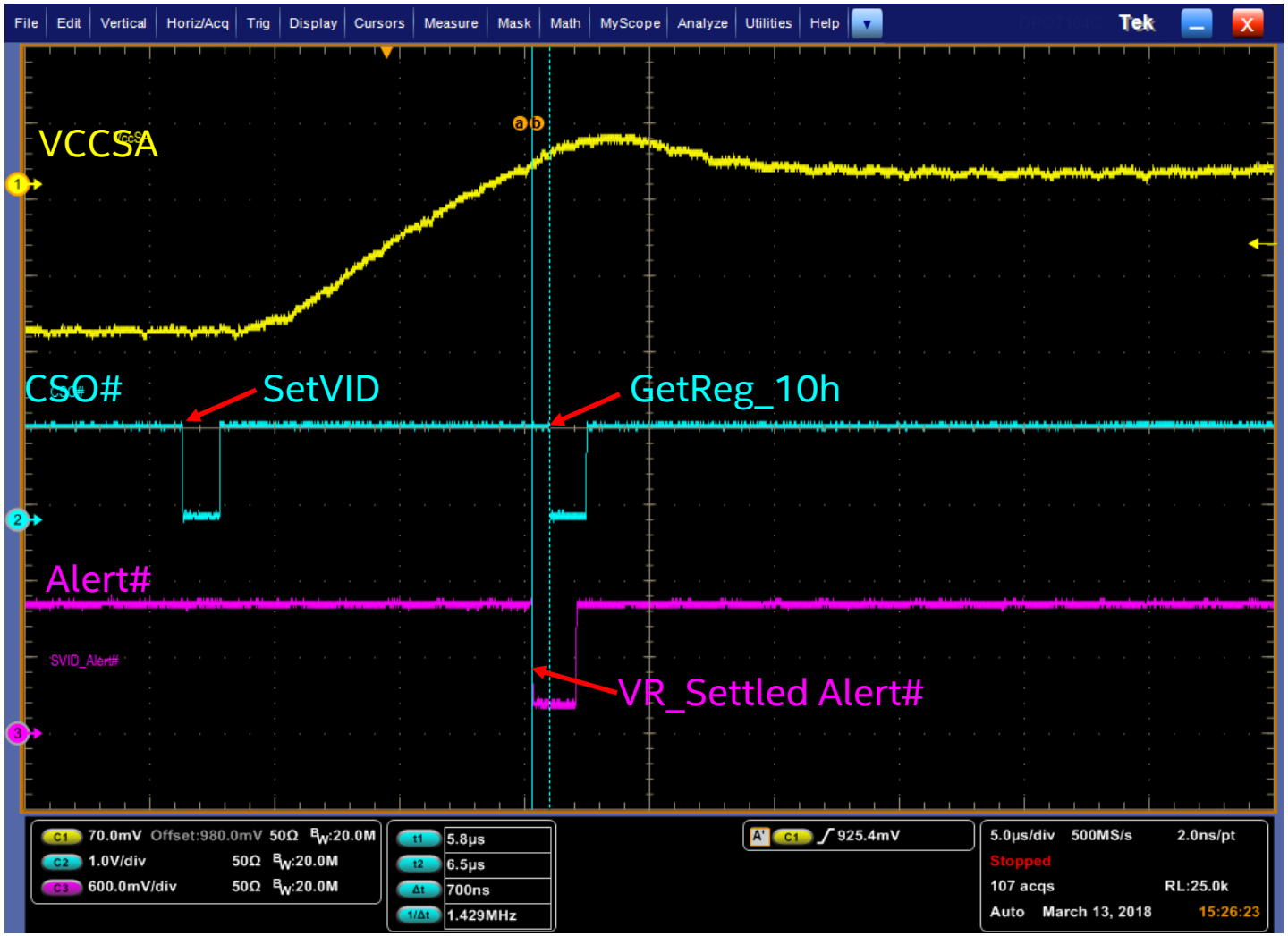
Command CPU to VRC, Response VRC to CPU

- **Command**: CPU drive on **rising** edge, VR sample on **falling** edge
- **Response**: VR driving at rising edge , CPU sample on next rising edge

Note: SVID = Intel® Serial Voltage Identification

SVID link Layer- Alert Line

- VR_SETTLED Alert and VID setting commands



VID setting (31h)
-present VID value(tracking)

Status1 Register (10h) 1

Bit0=

0, VR is not at target voltage;

1, VR is at target voltage

Note: SVID = Intel® Serial Voltage Identification

SVID link Layer- Alert Line

Thermal Alert and IccMAX Alert

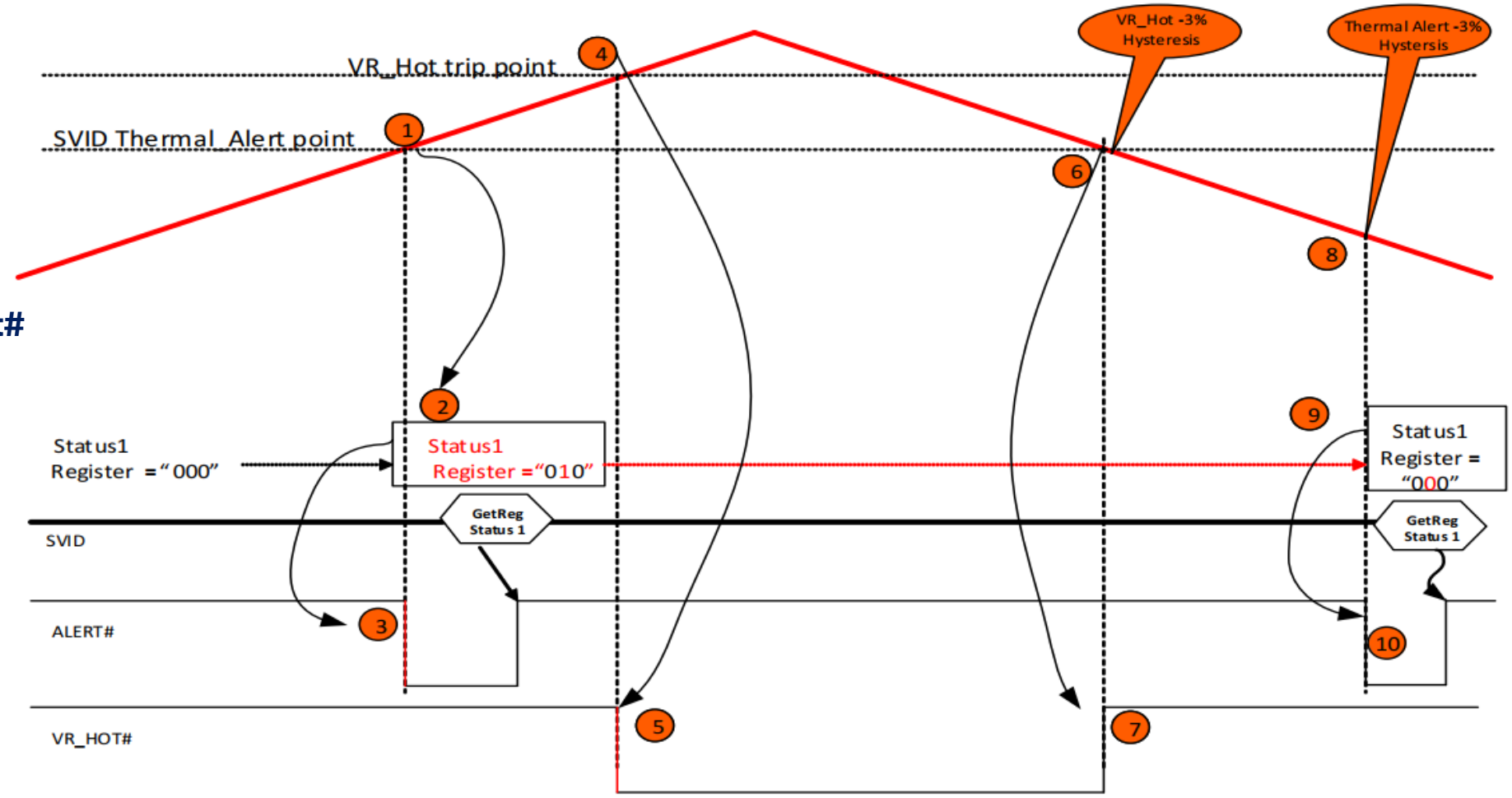
- Status1 Register (10h)
  - Bit1->Thermal
  - Bit2->Iccmax

- **Thermal Monitoring(12h)**
- **VR Thermal Alert#-> VR Hot#**

2

- **Iccmax(21h)**
- **IMON(15H)**

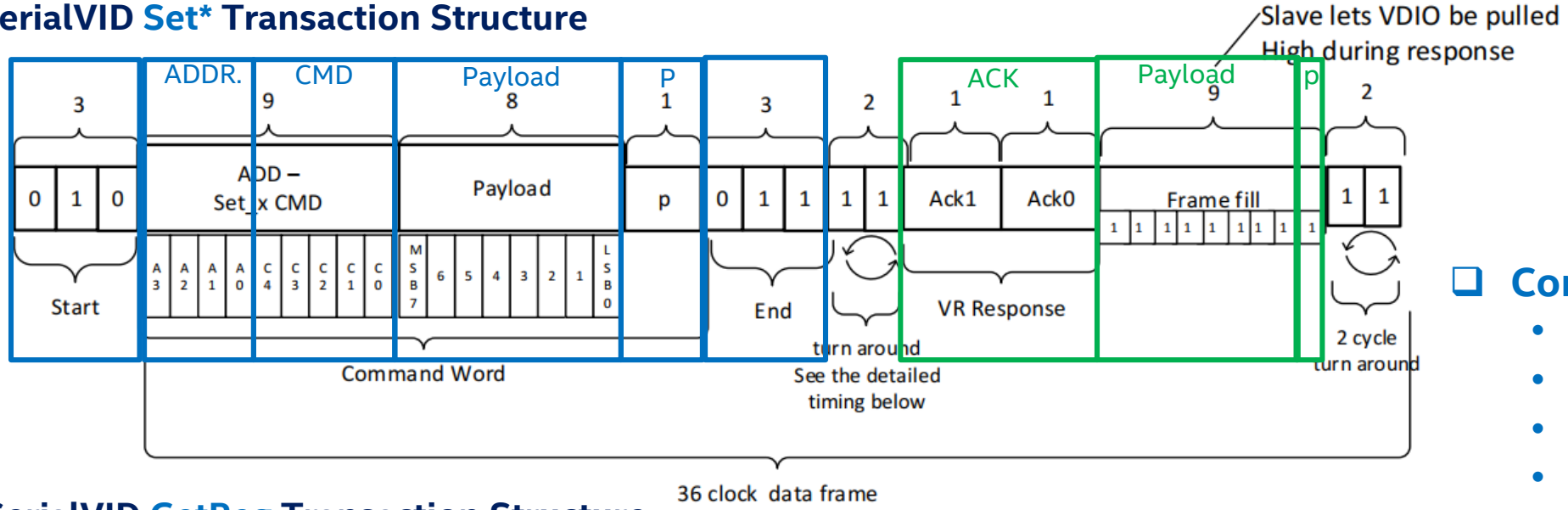
3



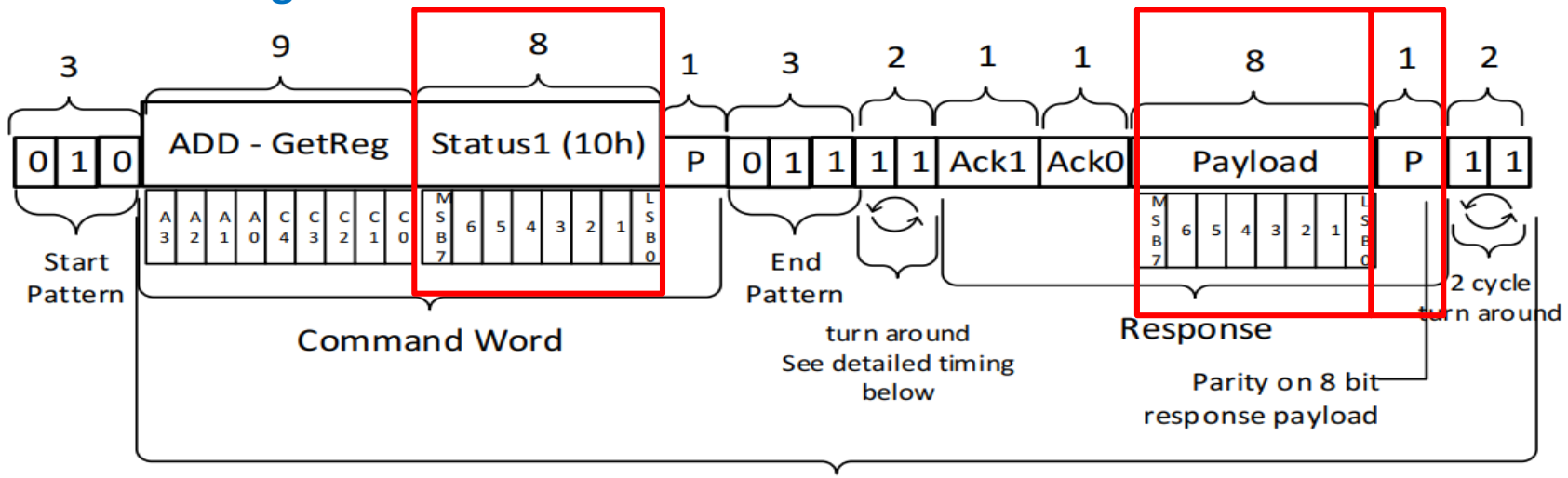
Note: SVID = Intel® Serial Voltage Identification

Data Link Layer- Command Structure

SerialVID Set* Transaction Structure



SerialVID GetReg Transaction Structure



Note: SVID = Intel® Serial Voltage Identification

- **Command Word Encoding**
  - 3-bit Start pattern(010)
  - 4-bit Slave address
  - 5-bit command index
  - 8-bit command payload
  - 1-bit of parity
  - 3-bit End pattern(011)
- **Response Encoding**
  - 2-bit acknowledgement
  - 8-bits response data
  - 1-bit of parity

Data Link Layer-Structure(cont.)-Acknowledge Type

Acknowledge Type	Ack1	Ack0
MIXED Error on an All-Call rail access, such as SetWP Results from wired-AND of simultaneous NAK and ACK responses being driven onto the open-drain SVID bus by two or more SVID slaves. ACK-ing slaves executes the command NAK-ing slaves do not execute the command	0	0
NAK (Not-Acknowledge) Returned on transmission error, parity error, an unsupported command request to an All-Call address, or a GetReg, SetRegAddr, or SetRegData command to an All-Call address Slave may log parity or frame error if applicable, does not execute command.	0	1
ACK (Acknowledge) Transmission received correctly, Slave carries out command	1	0
REJ (Reject) Returned for either Inactive SVID slave address or individually addressed SVID slave with command or register not supported. Cannot be used in most active All-Call address response since an ACK would hide any REJ after the wired-AND. Exceptions allow for an active All-Call command to REJ exist for (a) when LockVIDPS == 1, (b) for unset working point (WP), and (c) Unknown command number. Slave does nothing, does not execute command	1	1

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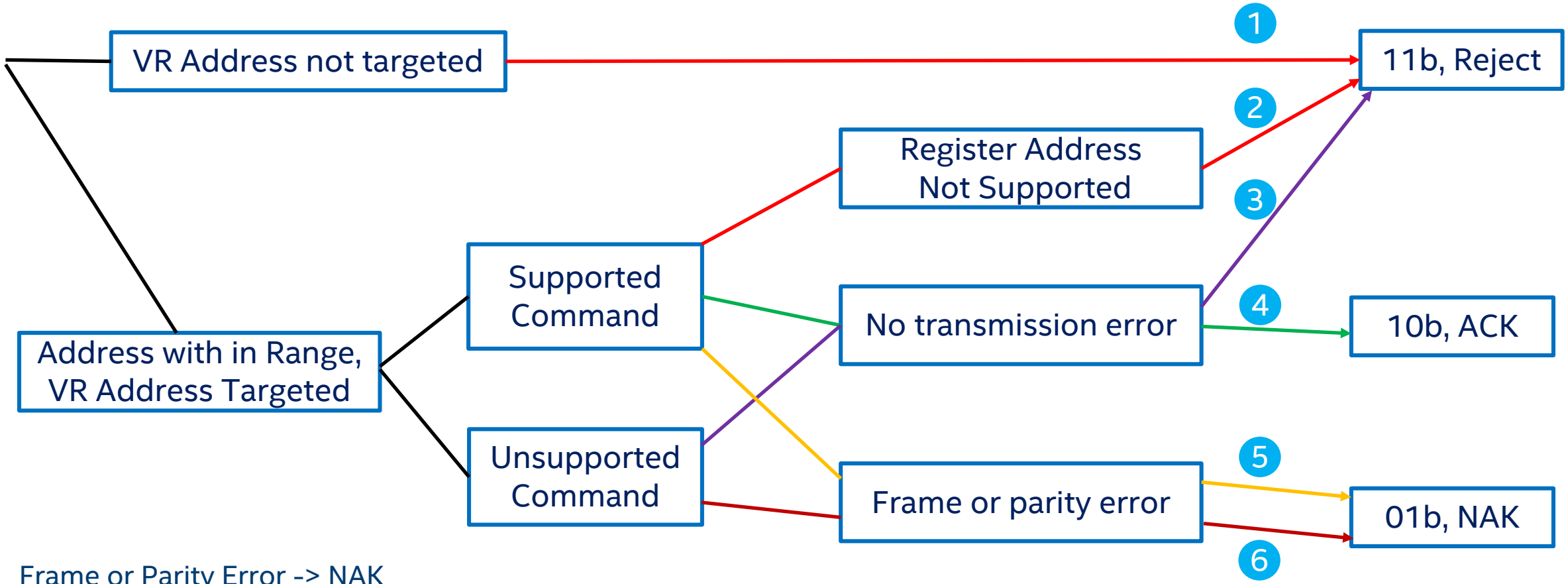
Acknowledge Type(Cont.)

SVID



Frame or Parity Error -> NAK
Invalid VR Address -> such as Skylake-SP SVID BUS0 VR04
Unsupported Command ->such as command 0Ah
Unsupported Register Address- such as Register 7A

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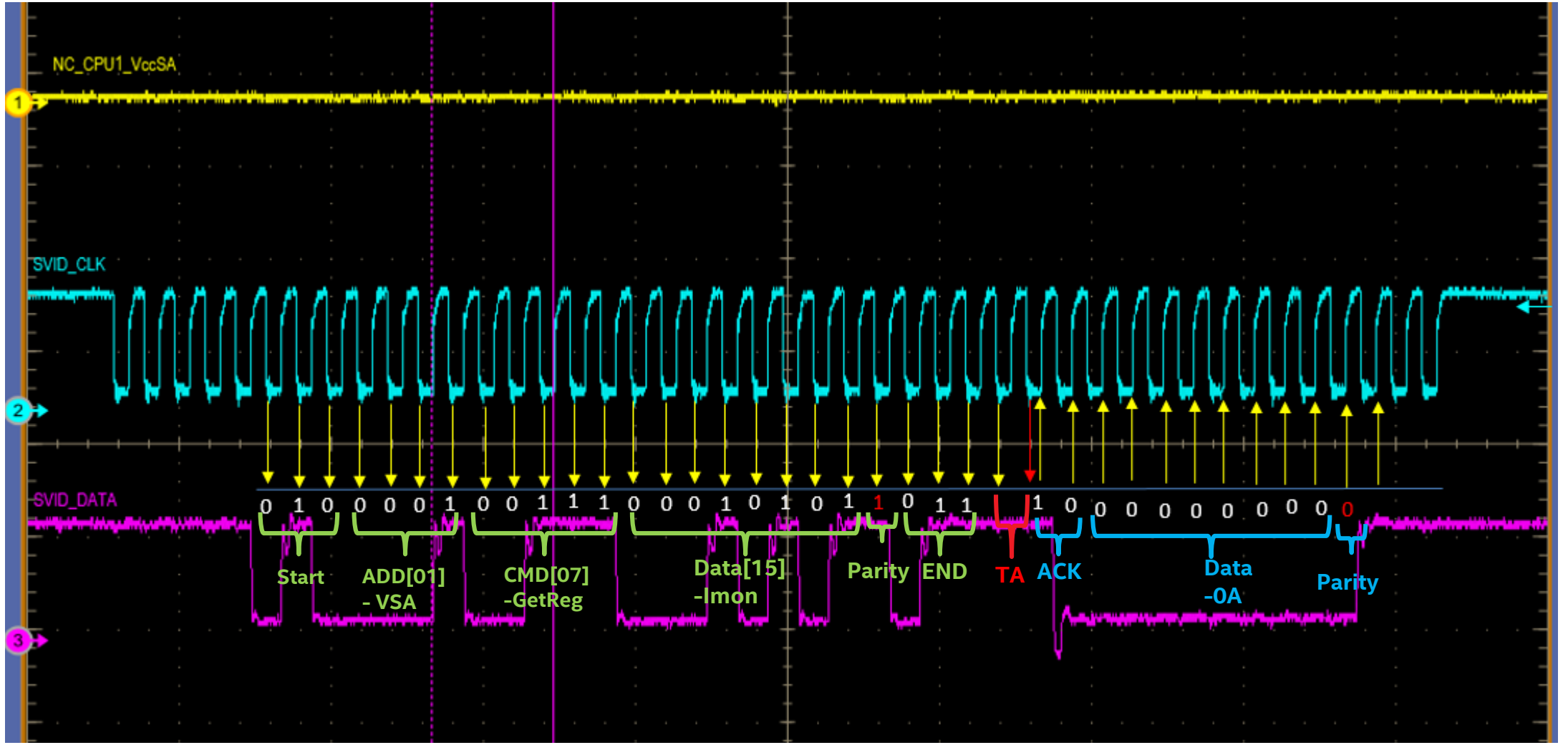
Exercise

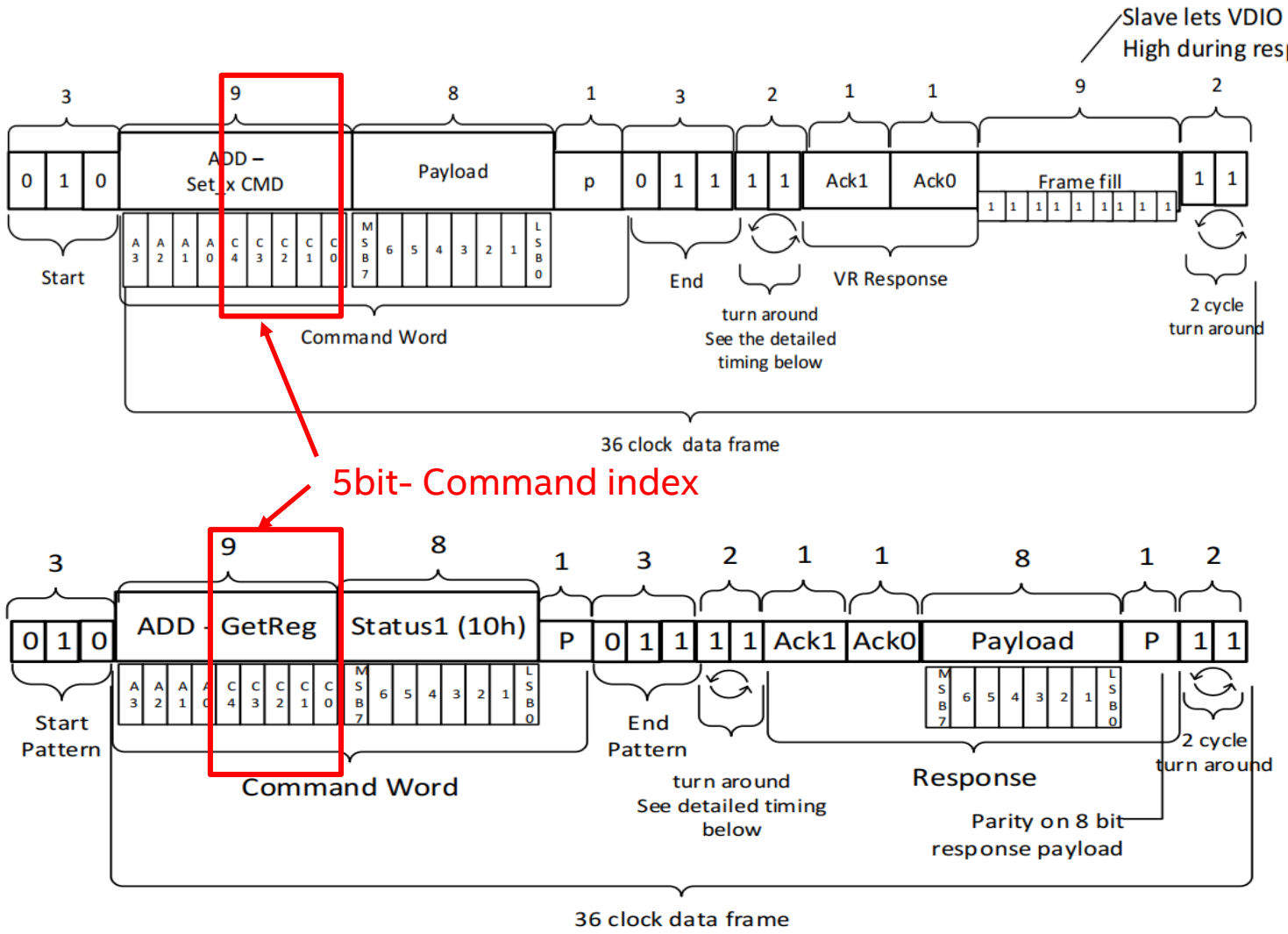


Test point at VR side

FUNCTION LAYER

SVID function Layer-command set

1. SetVID_Fast (01h)
2. SetVID_Slow (02h)
3. SetVID_Decay (03h)
4. SetPS (04h)
5. *SetRegAddr variants (05h)*
6. *SetRegData variants (06h)*
7. ***GetReg*** variants (07h)
8. TestMode (08h)
9. SetWP (09h)



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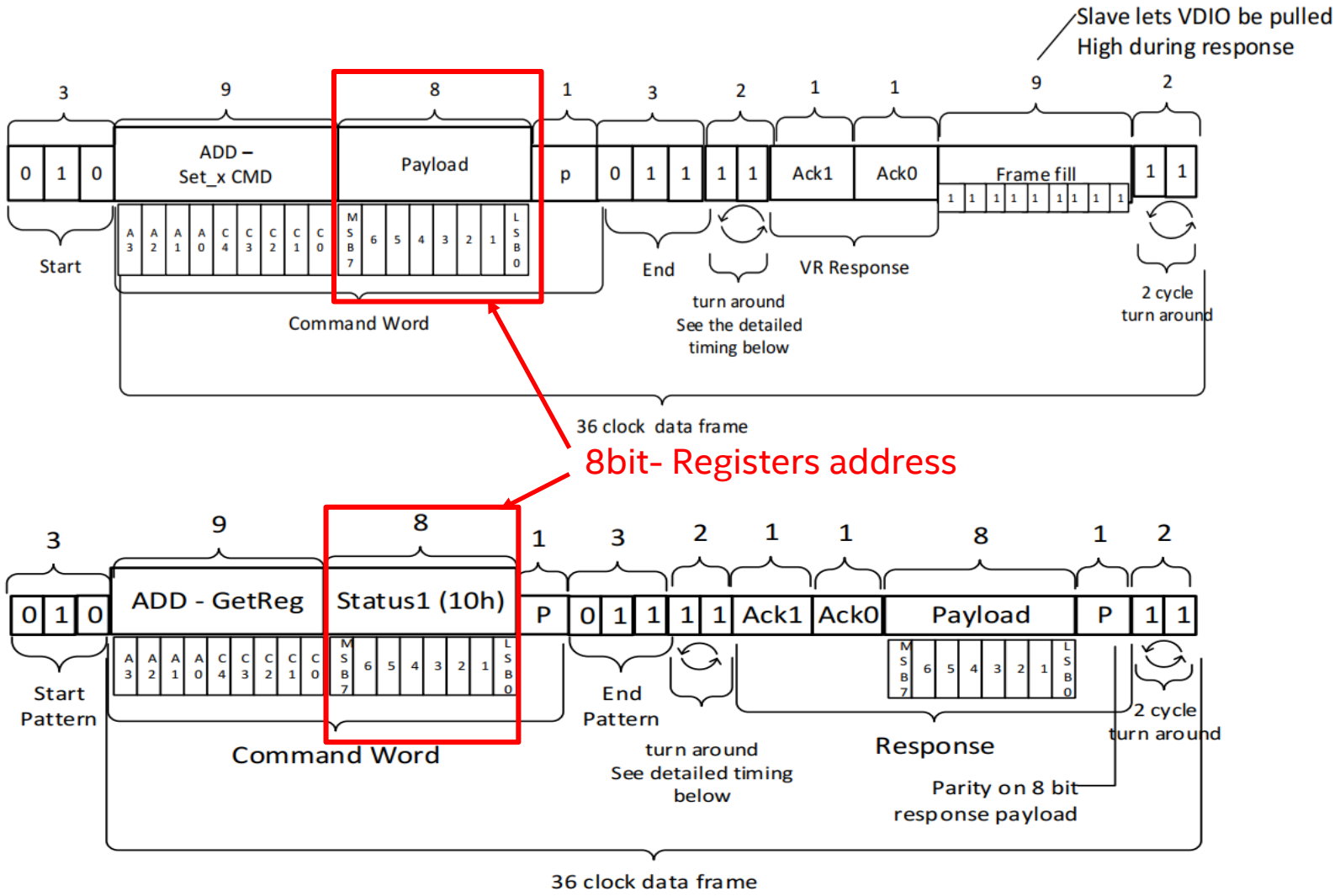
Main Address Space Registers

05h Protocol ID	06h Capability
10h Status1	11h Status2
12h Thermal Monitor	2Ah Slow Slew Rate
15h IMON	1Bh Input Power
21h Iccmax	2Eh Pwr_in_max
2Fh Pwr_in_Alert	3A/3B/3C/3Dh WP0/1/2/3

Main Register Address Examples



Protocol ID (05h)

This 8-bit read-only register identifies the protocol ID by which the slave address is communicating. It is possible that this may be reconfigurable via NVM or other means for a given product to make it applicable to a larger market segment.

Protocol ID[7:0]	Definition
01h	VR12.0, IMVP7
02h	VR12.5
03h	VR12.6
04h	VR13, 10mV VID table
05h	IMVP8
06h	VR12.1
07h	VR13, 5mV VID table
08h	IMVP9
09h	VR14 VR 5mV VID table
0Ah	VR14 VR 10mV VID table
0Bh	VR14 VR custom VID table
0Ch	VR14 Psys device
0Dh	IMVP9 Psys device

Capability (06h)

Capability Register, a 1b indicates digitize data is supported							
b7	b6	b5	b4	b3	b2	b1	b0
Iout/ Jout format (15h)	Tempe rature (17h)	input P (1Bh)	input V (1Ah)	input I (19h)	Pout (18h)	Vout (16h)	Iout (15h)

Description	Intel® Xeon® Server CPU domains			Memory	Microserver SOC 1	Notes
	00h	01h	02h & 03h	Multiple addresses	Multiple addresses	
Capability (06h)	X 1x1x xxx1b	X 1xxx xxx1b	X 1xxx xxx1b	X 1x1x xxx1b	X 1x1x xxx1b	Bit 5 = Pin supported Bit 7 = IMON supported Refer to the SVID protocol specification for additional information.

Status1 Register (10h)

Table 7-13. SVID Status1 Register

Bit	Name	Description
7	ReadStatus2	0= No need to read Status2 register 1= Go read status2 register
6:5	Reserved	Return 0
4	(VR14) CalOpComplete (Others) Reserved	(VR14) 0= No status update from IMON calibration 1= Check IMON calibration status registers (Others) Return 0
3	VID_DAC_high	0= VID DAC is not >30mV above VID target 1= VID DAC is >30mV above VID target
2	IccMaxAlert	0= I_out in normal current range 1= I_out is over-current (latched value)
1	ThermAlert	0= Not over-temperature 1= Over-temperature
0	VR_Settled	0= VR is not at target voltage 1= VR is at target voltage

Note: Default values for each bit are 0, indicating flag not set.

Note: SVID = Intel® Serial Voltage Identification

IMON (15h) /ICC_MAX(21h)

Index	Register Name	Description Note see detailed paragraph for each register	Access	Default	Generational VR Usage
15h	Output Current (Iout)	Averaged output current. For averaging and update/read rates see VR PWM specification. Left justified, scaled to Icc_max = ADC full range. IE 8 bit ADC, FFh=Icc_max or a 6 bit ADC, 3Fh = Icc_max, **TABLET** lower 8 bits of 10 BIT ADC,	R-M W-PWM	Actual Iout measured after start up Note 2	VR12 server Required IMVP7 Optional VR12.5 Required VR12.6 Required VR13/IMVP8 Required Tablet Required
21h	ICC_MAX	Data register containing the Icc max the platform supports. The platform design engineer programs this value during the design process. Binary Coded Decimal format in amps, IE 100A = 64h. This data is used with the Iout (15h) register scaling	RO platform	00h Note 2	VR12/IMVP7 Required VR12.5 Required VR12.6 Required Tablet Undefined VR13/IMVP8 Required

$$Imon = Iout(15h) \times \frac{IccMax(21h)}{255}$$

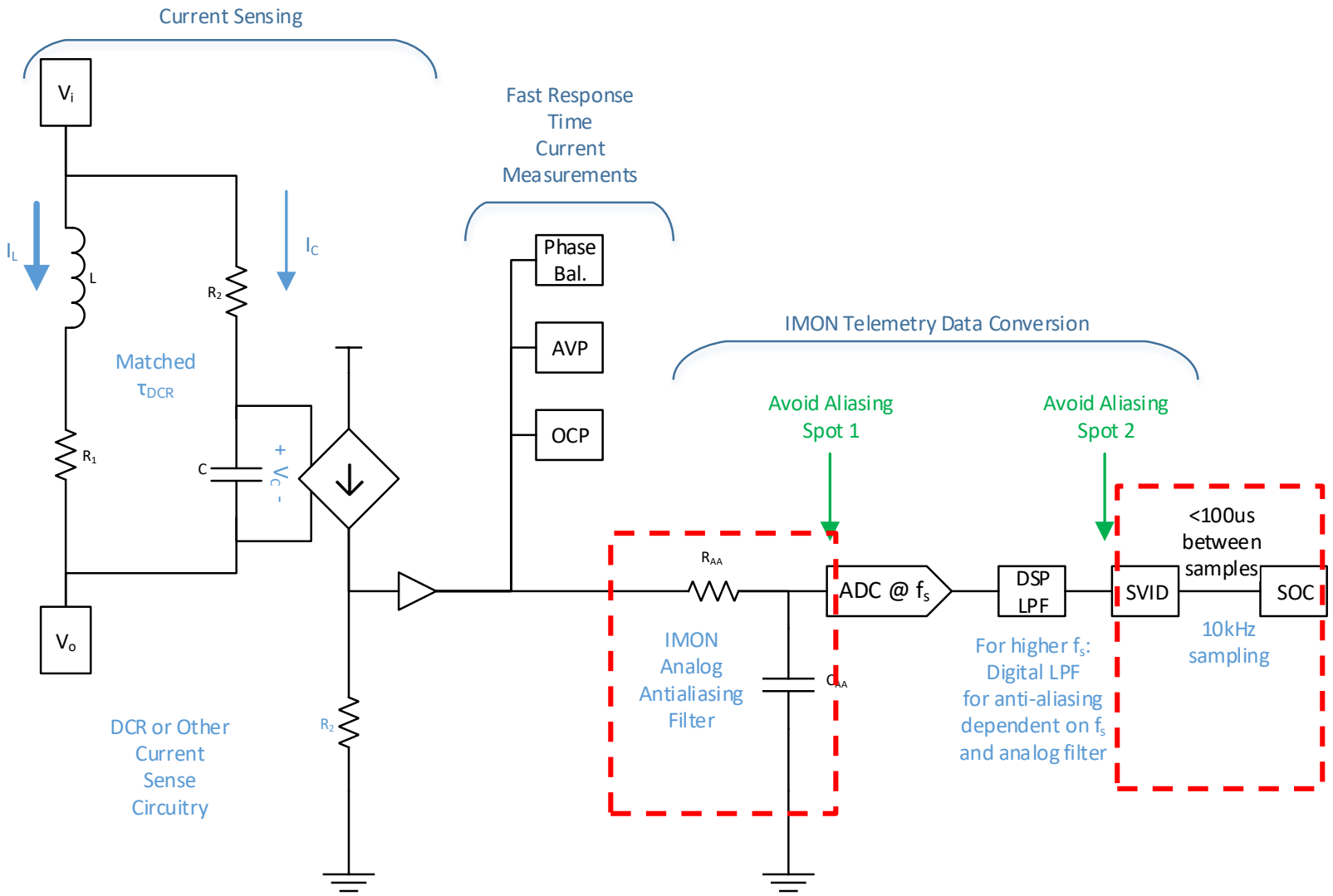
IMON Accuracy Targets

Accuracy is a function of the PWM internal circuits, and measurement technique: either external inductor (or shunt) and NTC temperature coefficient matching network, or integrated MOSFET sensing in the power stage

- Typical RSS 3 sigma platform accuracy targets
- **Tighter tolerance** on current reporting will yield a platform with better turbo performance.
- IMON accuracy is needed for RAPL consistency. If accuracy is poor, the spread for PL1 and memory RAPL will be greater than a board with tighter IMON distribution curve. It is up to the ODM/OEM designer to do the cost, performance tradeoff between inductor sensing and MOSFET sensing.
- CPU power management regulation points such as PL1 (TDP) and PL2 depend on the IMON accuracy. Wide variation in IMON tolerance will have a direct impact on customer's TDP level. **Underreporting IMON results in higher CPU thermal dissipation**; **over-reporting IMON results in lower thermal dissipation and lower CPU performance**. The accuracy targets at lighter loads are important for RAPL power capping algorithms

Telemetry Anti-aliasing Example

- Platform Power Management requires the VR to report a digitized value of output current over the SVID bus.
- The output current is to be sensed in a similar manner as **VR load line** and **phase current balance**.
- IMON support is required in **all power states** and **every VID** including 0V.
- Aliasing can be avoided by a proper combination of analog filtering and digital filtering prior each of the two points.



PWR_IN (1Bh) /Pwr_in_Max (2Eh)

Index	Register Name	Description Note see detailed paragraph for each register	Access	Default	Generational VR Usage
1Bh	Input Power PWR_IN **Tablet** Input Power L	Averaged Input Power or Psys. For averaging and update/read rates see VR PWM specification. Averaging, update interval same as Iout (15h) Left justified, scaled to Pwr_In_max (2Eh) = ADC full range. **Tablet** lower 8 bits of 10 BIT ADC of Pin data	R-M W-PWM	Note 2	VR12.0/IMVP7 Optional Note 3 VR12.5 Optional VR13 Required IMVP8 Required Tablet Required
2Eh	Pwr_in_Max	Input power sensor scaling for Input Power(1Bh) register Programmed by Platform designer to the rating of the Input Power Sensor. Programmed as 2W/LSB			VR12/IMVP7 Undefined VR12.5 Undefined VR12.6 Undefined IMVP8 undefined VR13 required

Thermal Monitoring (12h)

VR_Hot# and Thermal Alert

- Bit6- Thermal Alert#, Bit7 VR_Hot#
- **VR_Hot#** is required to be routed to the processors **PROCHOT#** input pin for all market segments, to initiate thermal throttle low power state of the CPU to protect the VR from overheating.
- **VR_Hot#** may also be routed to various system thermal management controllers

Temperature zone register and example

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
100 %	97 %	94 %	91 %	88 %	85 %	82 %	75 %
VR_HOT#	ThermAlert	Thermal indicator assertions occur as zone increases into the range bits 6 and 7.					
Example thresholds for 100°C temp max.							
100°C	97°C	94°C	91°C	88°C	85°C	82°C	75°C
Example register contents for 95°C temperature, 100°C temp max.							
0	0	1	1	1	1	1	1

Input Power sensor(1Bh)

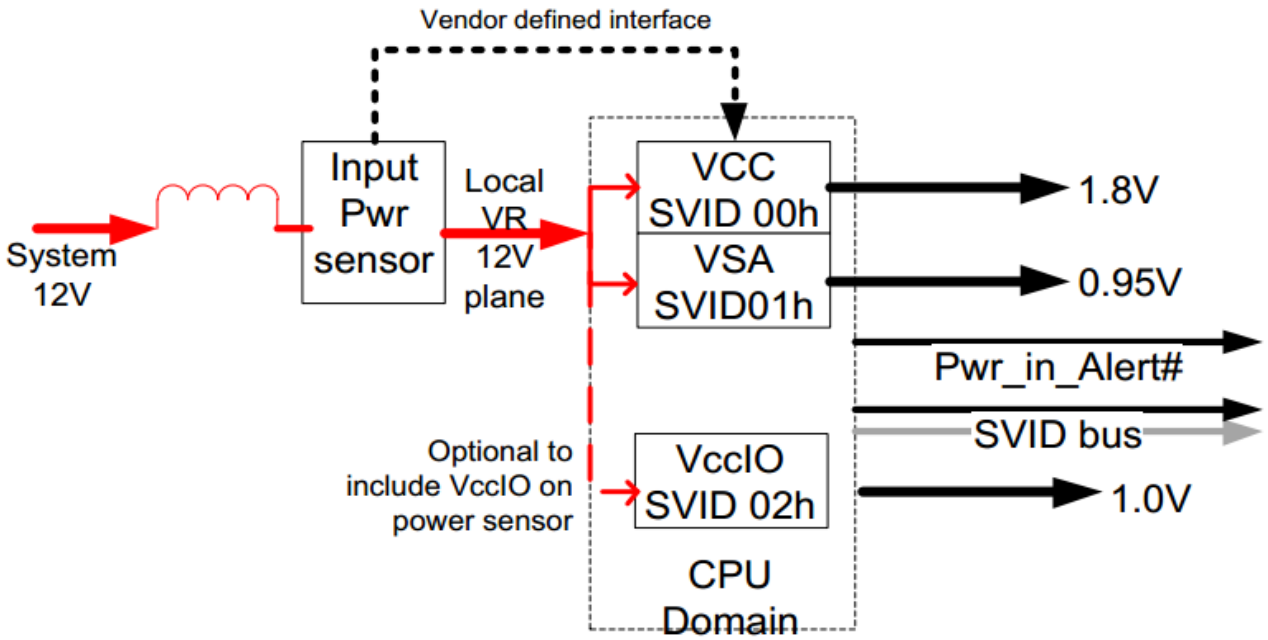
This requirement applies to **both** CPU domains and memory domains. The sense element will be placed between the 12 V input filter inductor and bulk capacitors placed on the local 12 V plane feeding the domain voltage regulator circuits

- Pwr_in Alert# used to change the state of the CPU from a PMax condition down to PL2 condition
- The goal of the PWR_in Alert# is to reduce the PMax detection interval from 600us (3X IMON averaging time constant) to typical < 100 µs to reduce peak power stress on the input power supply 12V and the amount of 12V buffering capacitance.
- Provide single point for RAPL power measurement for memory systems that mix both 12V NVDIMMs and standard DDR4 DIMMs

Note: CPU uses IMON data on the various rails and not the input sensor for RAPL and power limit calculations.

Pwr_in_alert (2Fh)

This 8-bit read-write register is by default the same value Power In Max(address 2Eh), but can be set by the SVID master to any value lower than Power In Max. If an attempt is made to set the effective Power In Alert threshold higher than the effective Power In Max value, it will be acknowledged and stored, but the PWR_IN_ALERT# function will be disabled.



Slow slew rate and VR13.HC support (2Ah)

Bit	Mode	Name	Default	Definition
7	Read-only	HC_SUPPORT*	See Right	0=VR13.HC mode not supported 1=VR13.HC mode supported
6	Read-write	HC_ACTIVE*	0	0=VR13.HC mode not active 1=VR13.HC mode activated
5	Rsvd	Reserved	0	Default to 0
4	Rsvd	Reserved	0	Default to 0
3:0	Read-Write	SlowSR_Ctrl	2h	1XXX = Set Slow SR to Fast SR/16 01XX = Set Slow SR to Fast SR/8 001X = Set Slow SR to Fast SR/4 0001 = Set Slow SR to Fast SR/2 0000 = Leave Slow SR at its prior setting

VR13 High Current Support (VR13.HC)

- Existing VR13.0 platforms (ex. Purley) are capped at IccMax = 255A (IMON limit)
- Desired Objectives:
  - IccMax > 255A would enable additional performance in future processors
  - Minimize enabling work required to provide such a feature
  - Maintain backwards compatible to the existing VR13.0 CPU (even if it's unaware of VR13.HC mode)
- Solution: Adds FIVE new registers to the SVID Protocol
  1. **HC Support bit (2Ah bit7)** – Indicates if VR can support beyond 255A
  2. **HC Mode Active bit (2Ah bit6)** – Write 1 bit to switch IMON I_{out} and P_{in} scaling from 255A to IccMax
  3. **IccMaxAdditional (50h)** – Amount of max(I_{out}) beyond 255A, encoded at 2A/LSB. Iccmax(21h)
  4. **PwrInMaxAdditional (51h)** – Amount of max(P_{in}) beyond 510W, encoded at 4W/LSB. PwrInMax(2Eh)
  5. **PwrInThreshAdditional (52h)** – Amount to add to P_{jn} threshold beyond 510W, encoded at 4W/LSB. PwrInTresh(2Fh)

Note: SVID = Intel® Serial Voltage Identification

New in VR13.HC

The VR13.HC specification is designed to support up to 765A output current and 1530W input power telemetry.

VR13 High-Current mode example

Setting	HC_ACTIVE==0	HC_ACTIVE == 1
Output Current Full Range	IccMax Amps	(IccMax + 2* IccMaxAdd) Amps
Input Power Full Range	(2*PwrInMax) Watts	(2*PwrInMax + 4*PwrInMaxAdd) Watts
Input Power Alert Threshold	(2*PwrInAlert) Watts	(2*PwrInAlert + 4*PwrInAlertAdd) Watts

Where:

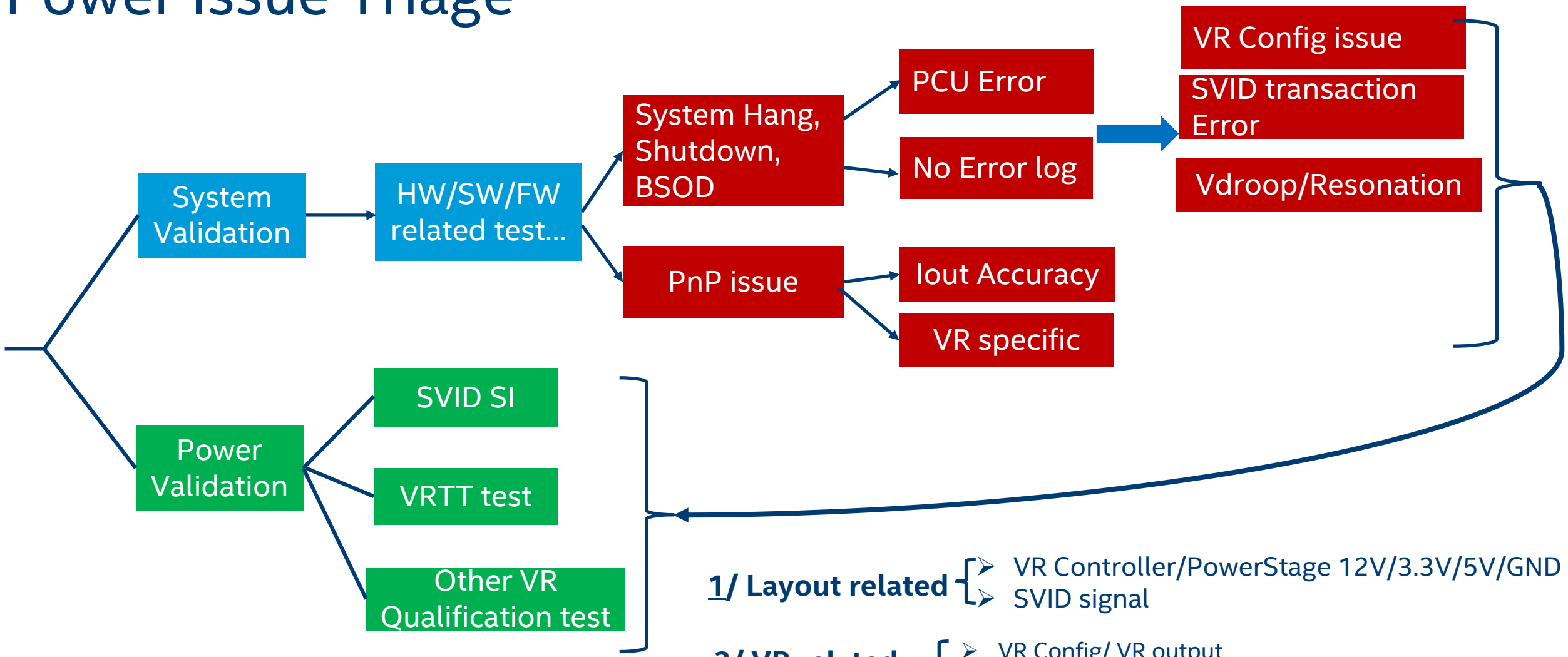
- IccMax = Register 21h.
- PwrInMax = Register 2Eh.
- PwrInAlert = Register 2Fh.

IccMaxAdd = Register 50h (VR13.HC only)
PwrInMaxAdd = Register 51h (VR13.HC only)
PwrInAlertAdd = Register 52h (VR13.HC only)

SVID DEBUG TOOL AND COMMON ISSUE

Note: SVID = Intel® Serial Voltage Identification

Power Issue Triage



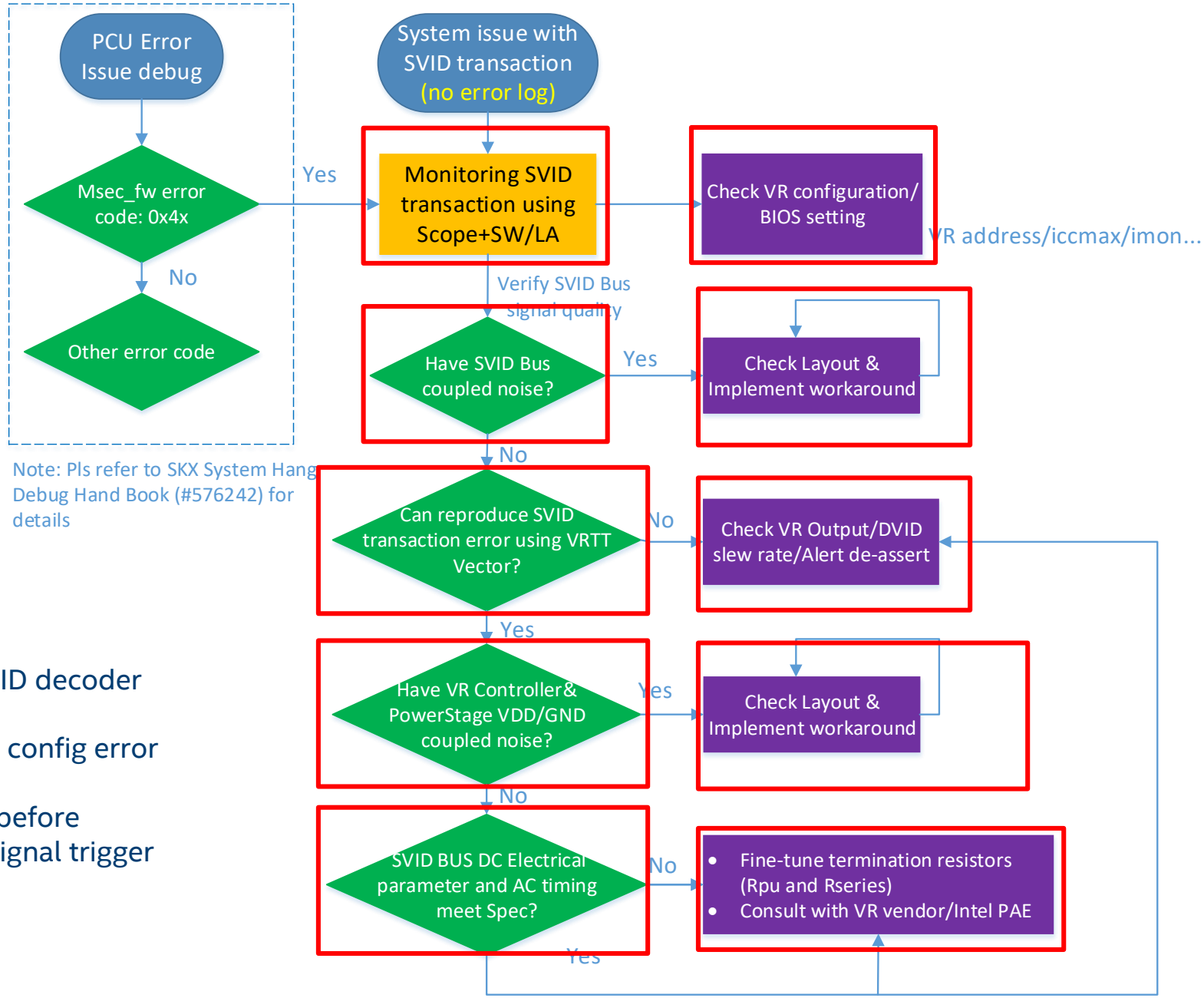
1/ Layout related
- VR Controller/PowerStage 12V/3.3V/5V/GND
- SVID signal

2/ VR related
- VR Config/ VR output
- VR Silicon

3/ CPU related
- Firmware/BIOS setup
- Pcode issue

Note: SVID = Intel® Serial Voltage Identification

Suggested SVID Debug Flow



Note:

1. "SW" in Scope+SW means Scope SVID decoder or Intel SVID decoder checker;
2. PCU error can help to filter out its VR config error or SVID transaction error
3. Longer duration of SVID transaction before Processor Asynchronous Sideband Signal trigger need to be monitoring.

Note: SVID = Intel® Serial Voltage Identification

PCU errors- MCA bank4 mc-status registers: Bits[31:24] (**msec_fw)**

0x40 = MCA_SVID_VCCIN_VR_ICC_MAX_FAILURE; Fused CPU Icc-max exceeds Vccin VR's limit

0x41 = MCA_SVID_COMMAND_TIMEOUT; SVID command timeout (busy bit was not cleared fast enough)

0x42 = MCA_SVID_VCCIN_VR_VOUT_FAILURE; Fused CPU boot voltage exceeds Vccin VR's limit

0x43 = MCA_SVID_CPU_VR_CAPABILITY_ERROR; A CPU VR found that does not support IOUT (IMON polling)

0x44 = MCA_SVID_CRITICAL_VR_FAILED; Failure of critical VR detected during reset.

0x45 = MCA_SVID_SA_ITD_ERROR; Failure updating SA VR VID for ITD

0x46 = MCA_SVID_READ_REG_FAILED; SVID command to read a register failed

0x47 = MCA_SVID_WRITE_REG_FAILED; SVID command to write a register failed

0x48 = MCA_SVID_PKGC_INIT_FAILED; SVID initialization of PkgC support (at reset) failed

0x49 = MCA_SVID_PKGC_CONFIG_FAILED; SVID enable/disable of PkgC support (at runtime) failed

0x4a = MCA_SVID_PKGC_REQUEST_FAILED; SVID Pkgc request failed

0x4b = MCA_SVID_IMON_REQUEST_FAILED; SVID IMON request failed

0x4c = MCA_SVID_ALERT_REQUEST_FAILED; SVID ALERT request failed

0x4d = MCA_SVID_MCP_VR_RAMP_ERROR; MCP VR failed to ramp

SVID debug tools

1. 540269_SVID_Decoder_Protocol_Checker

- **CSV or txt file from Scopes**

2. Scopes support SVID protocol Firmware

- **Contact local vendor's FAE for support**

3. Third Party Logic Analyzer

- **Support long data streams and triggering models**
- **More flexible to decode**

These tools can be used to monitor the SVID signals and convert SVID binary traffic into readable format to aide in SVID or platform debug

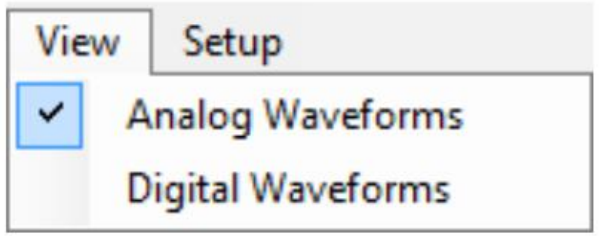
Note: SVID = Intel® Serial Voltage Identification

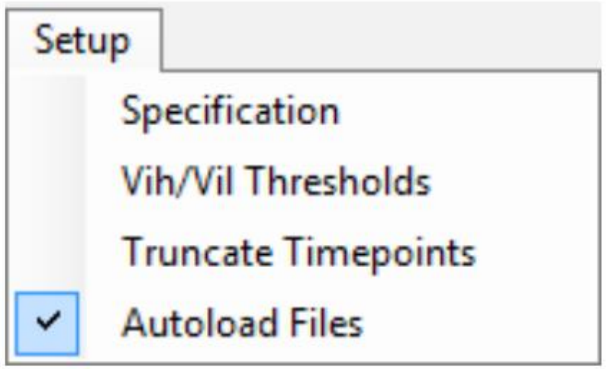
How to decode the SVID protocol?

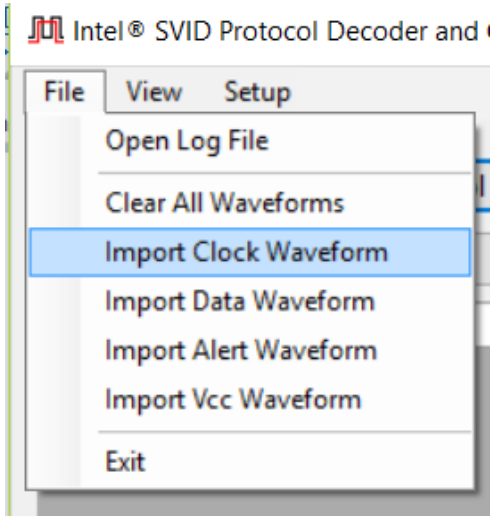
- Logic Analyzer Only
  - More details in following slides
  - Pros: easy, simple to use
  - Cons: signal quality not able to check
- Scope Only
  - How to calculate by eye balls correctly?
  - Rising edge or falling edge?
  - Pros: signal quality can be checked
  - Cons: One protocol at a time and takes time to decode by eye ball check
- Scope+LA
  - Use LA to do protocol trigger and can check signal quality at the same time

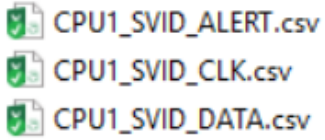
Note: SVID = Intel® Serial Voltage Identification

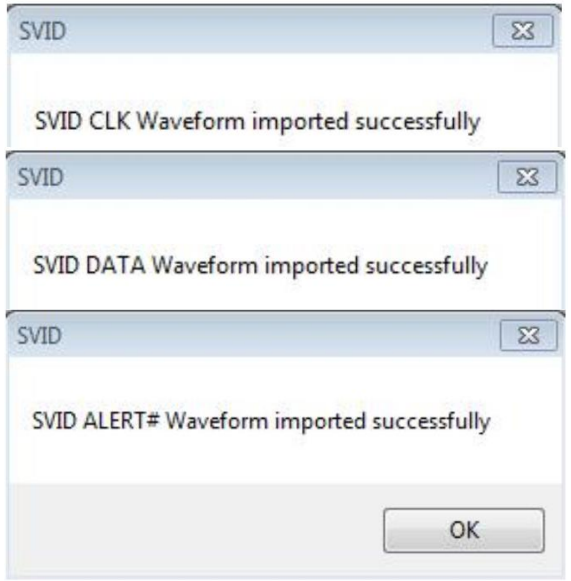
Intel® Serial Voltage Identification Decode Tool Use Steps

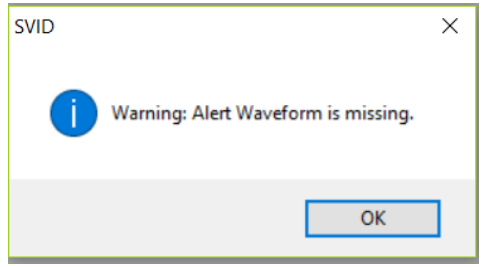


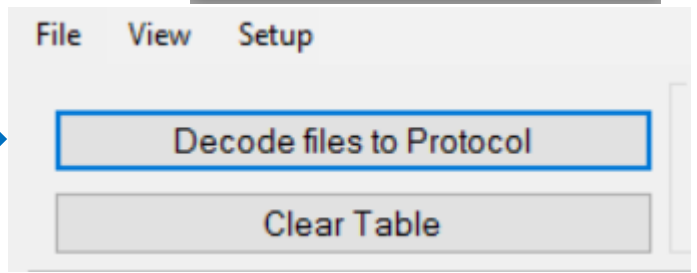




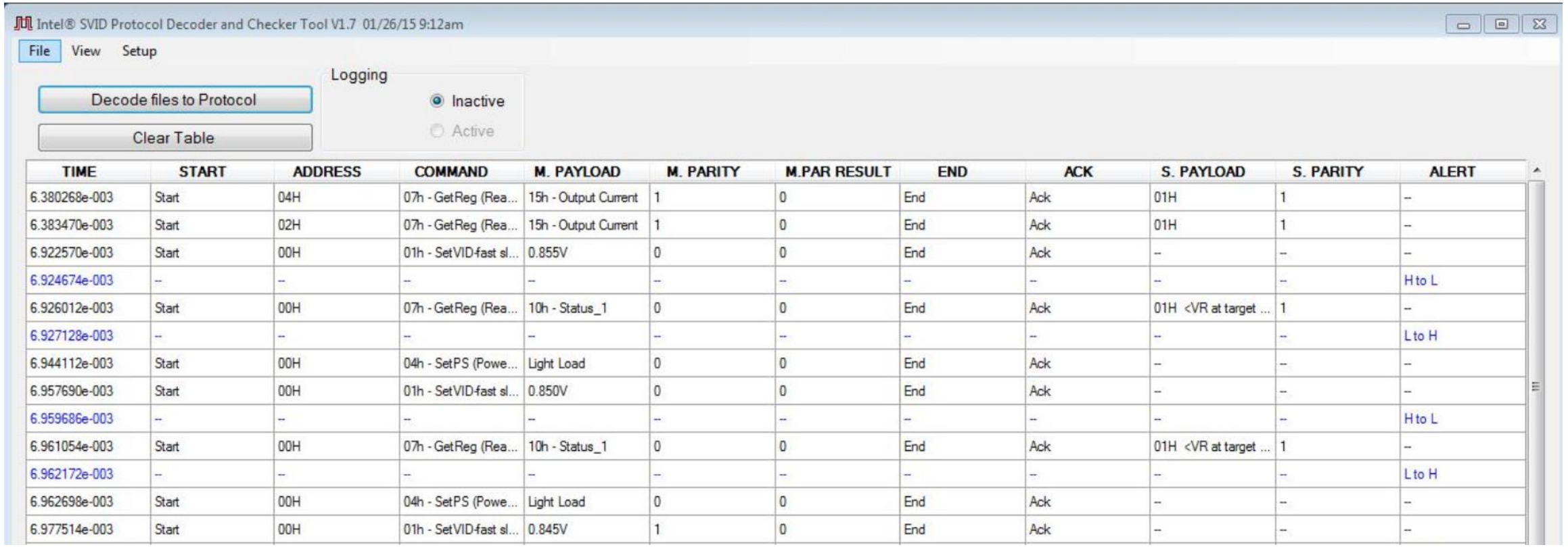








Intel® Serial Voltage Identification Decode Tool Result Example

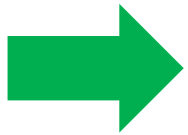


TIME	START	ADDRESS	COMMAND	M. PAYLOAD	M. PARITY	M.PAR RESULT	END	ACK	S. PAYLOAD	S. PARITY	ALERT
6.380268e-003	Start	04H	07h - GetReg (Rea...	15h - Output Current	1	0	End	Ack	01H	1	--
6.383470e-003	Start	02H	07h - GetReg (Rea...	15h - Output Current	1	0	End	Ack	01H	1	--
6.922570e-003	Start	00H	01h - SetVID-fast sl...	0.855V	0	0	End	Ack	--	--	--
6.924674e-003	--	--	--	--	--	--	--	--	--	--	H to L
6.926012e-003	Start	00H	07h - GetReg (Rea...	10h - Status_1	0	0	End	Ack	01H <VR at target ...	1	--
6.927128e-003	--	--	--	--	--	--	--	--	--	--	L to H
6.944112e-003	Start	00H	04h - SetPS (Powe...	Light Load	0	0	End	Ack	--	--	--
6.957690e-003	Start	00H	01h - SetVID-fast sl...	0.850V	0	0	End	Ack	--	--	--
6.959686e-003	--	--	--	--	--	--	--	--	--	--	H to L
6.961054e-003	Start	00H	07h - GetReg (Rea...	10h - Status_1	0	0	End	Ack	01H <VR at target ...	1	--
6.962172e-003	--	--	--	--	--	--	--	--	--	--	L to H
6.962698e-003	Start	00H	04h - SetPS (Powe...	Light Load	0	0	End	Ack	--	--	--
6.977514e-003	Start	00H	01h - SetVID-fast sl...	0.845V	1	0	End	Ack	--	--	--

SVID Transactions During System Boot up and Running

- GetReg*
  - Vendor ID (Reg 0x00)
  - Product ID (Reg 0x01)
  - Product Revision (Reg 0x02)
  - Product Date Code (Reg 0x03)
  - Lot Code (Reg 0x04)
  - Protocol ID (Reg 0x05)
  - Capability ID (Reg 0x06)
  - ICC Max (Reg 0x21)
  - Loadline resistance (Reg 0x23)
  - Fast/slow VID slopes (Regs 0x24 0x25)
  - **Pin_MAX(Reg 0x2E)- BUS2/Memory**
  - Vout max VID (Reg 0x30)
  - Status1 (Reg 0x10) -- clearing Alert# from Vboot
- SetRegADR/SetRegDAT
- SetVID_Slow

Boot Up

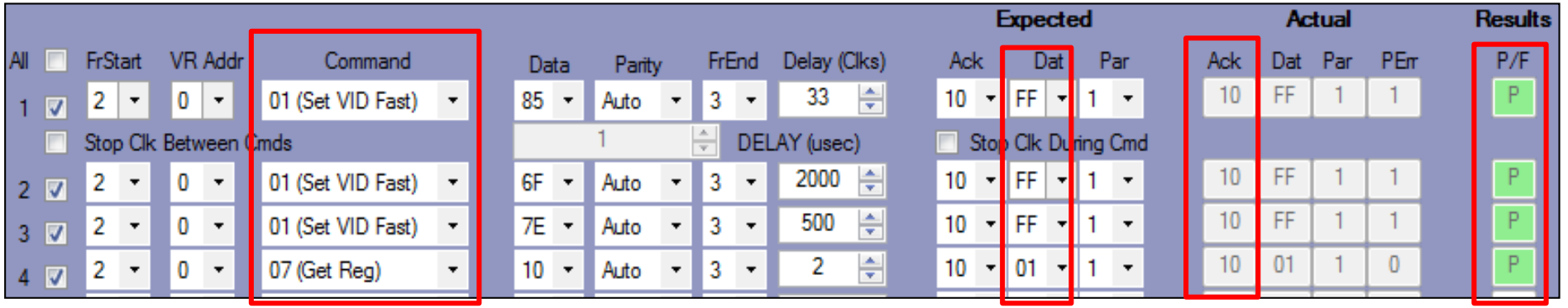


- GetReg 15h
- SetVID_Slow/Fast
  GetReg 10h
- SetWP1/2
  GetReg 10h

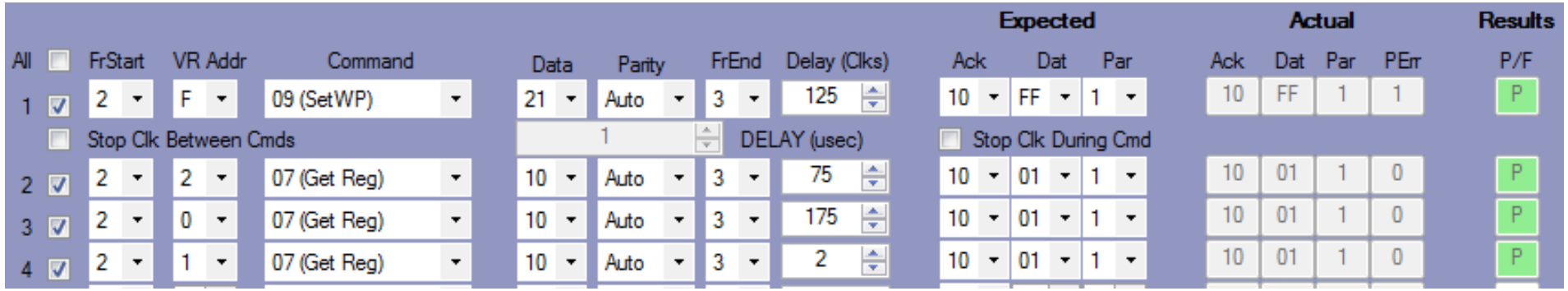
System Running

Note: SVID = Intel® Serial Voltage Identification

Replicate SVID Transaction using VRTT Vector Features



SetVID



SetWP

Tips:

1. Increase static current loading to target rails
2. Adjusting output voltage to target rails

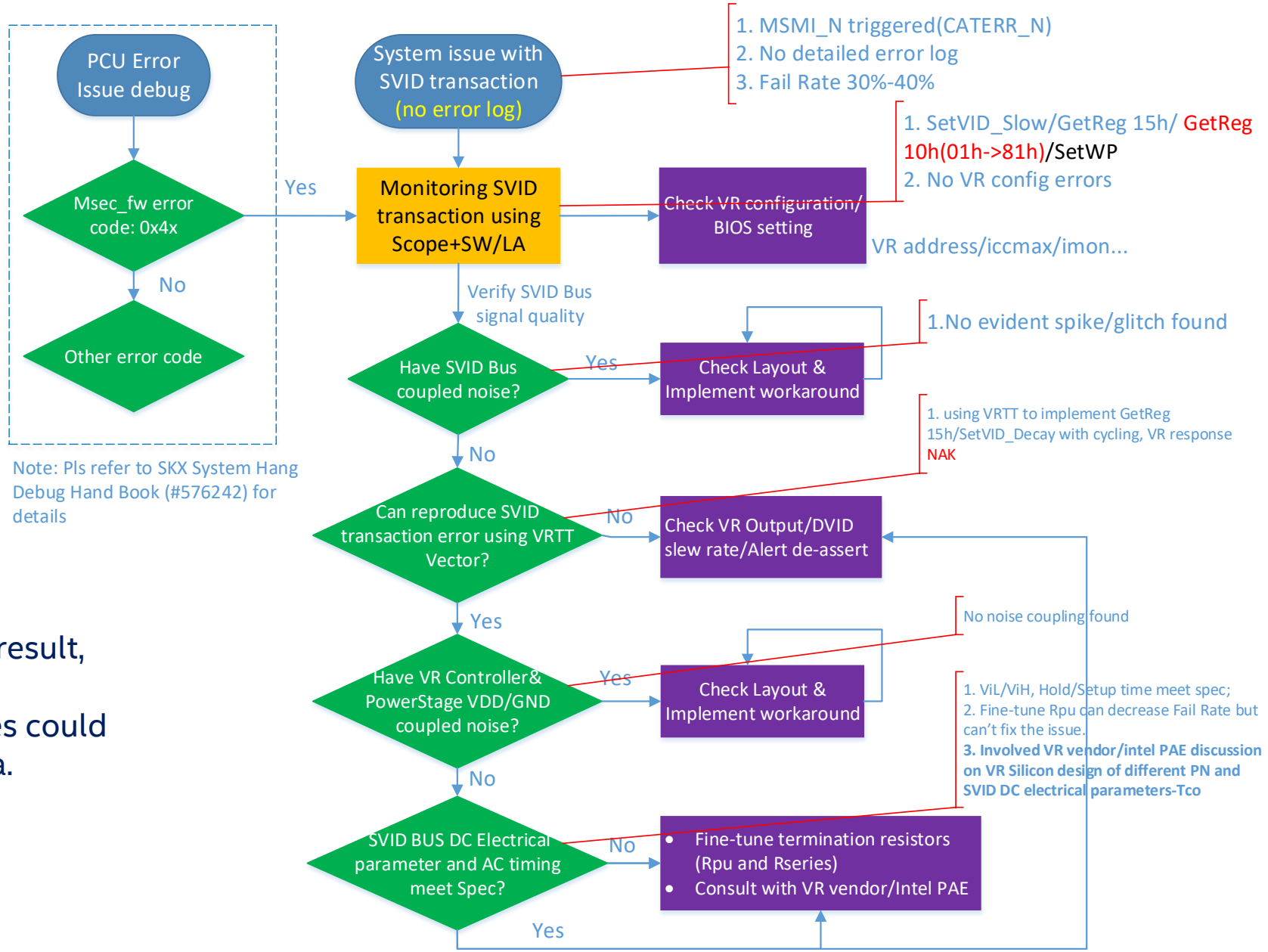
Note: SVID = Intel® Serial Voltage Identification

Real case

Case1. System Hang with MSMI_N(or CATERR_N) triggered during enter/exit PkgC6

Case2. System hang issue with IERR during OS installation

Case3. Purley EP2S system hang during C state transition



Notes:

1) Take note of each experiment, test result, waveforms
2) Hypothesis, experiment and theories could be revised based on actual test data.

Note: SVID = Intel® Serial Voltage Identification

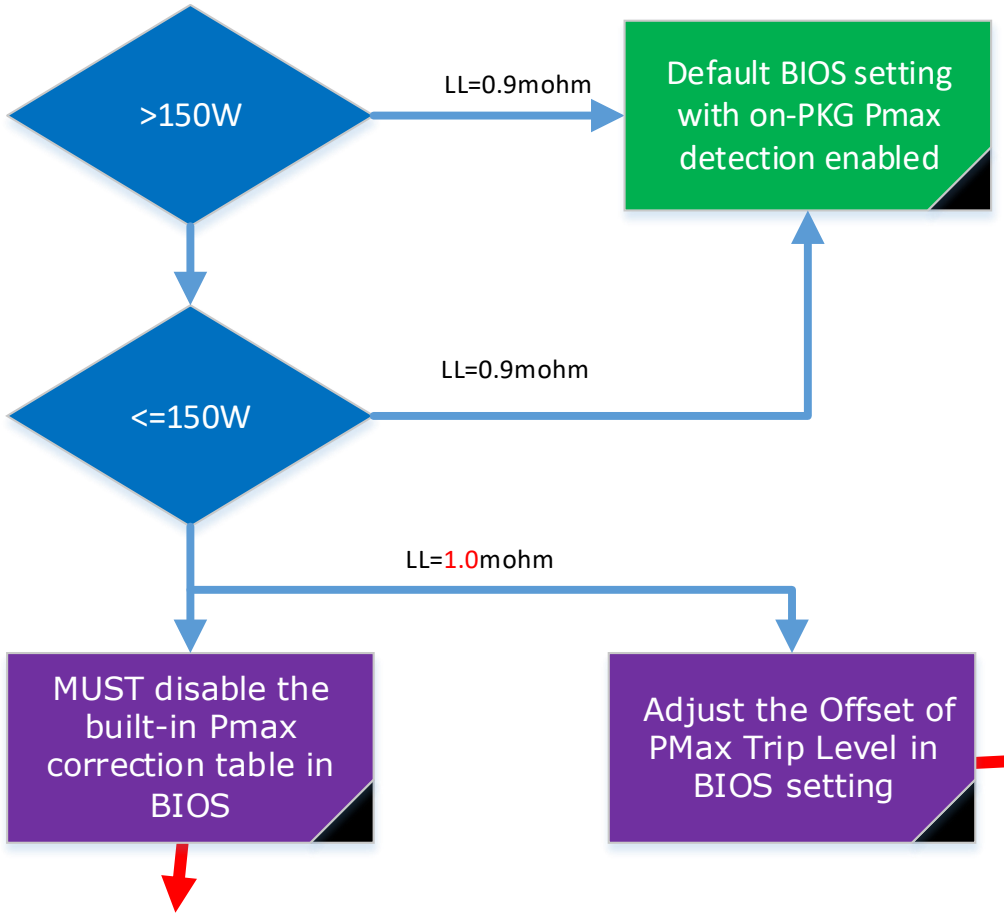
SVID Errors That Cause CPU to Hang

- REJ/NAK of initial SVID GETREG on VccIN VR
  - No VR present or bus not working, CPU halt
- Icc_Max (21h) mismatch to CPU rating during initialization
  - CPU halts, issues CATERR# (Catastrophic Error Signal)
- SVID communication error checking
  - Occurs when CPU receives NAK or REJ or parity error
  - CPU retries same command 3 times, if all fail CPU halts, issues CATERR# signal
  - If multiple retries are observed, check SVID bus signal integrity and pull-up values to meet VIO, VIL levels
- VR failing to return Alert# after a SetVID_Fast or SetVID_Slow command from low voltage to higher voltage
  - CPU may hang or stay in low performance mode, no CATERR# issued

Note: SVID = Intel® Serial Voltage Identification

BACKUP

BIOS setting for On-Package Pmax detection at different SKU -Purley

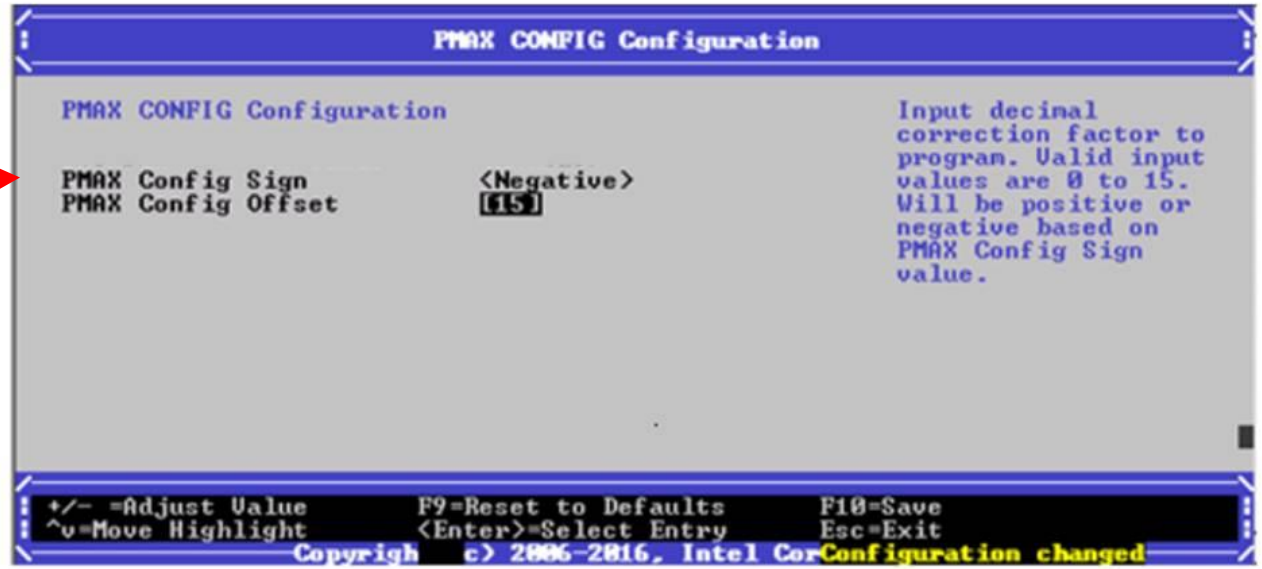


TDP	Loadline	Built-in Pmax correlation Table
>150W	0.9mohm	Enable(default)
<=150W	0.9mohm	
<=150W	1.0mohm	Disable

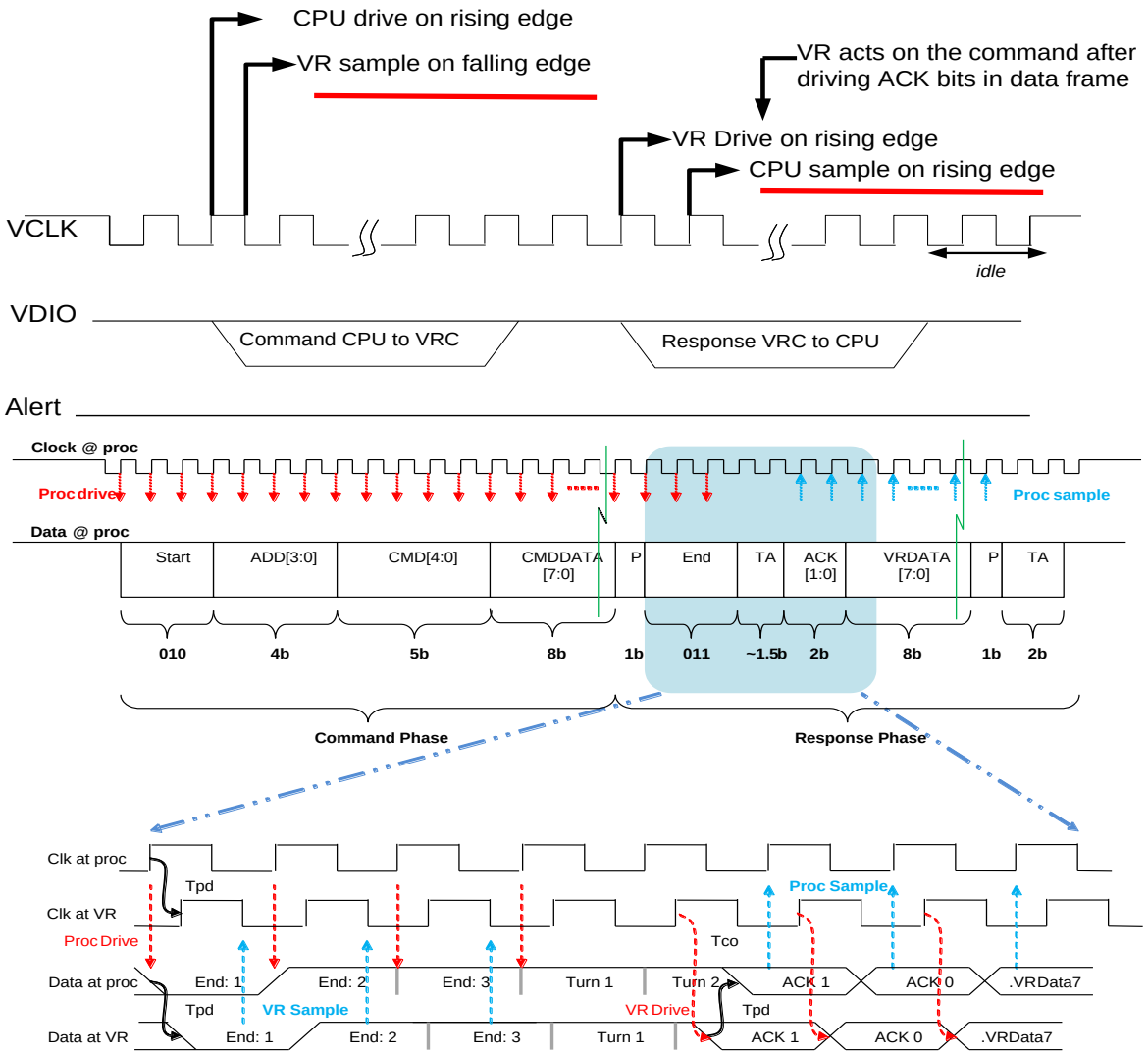
```
// Hardcoding value to always use offset table for 0.70mohm boards

// Customers may re-enable Setup question tied to this or change hardcode value as
needed

//SetupData.SocketConfig.PowerManagementConfig.UsePmaxOffsetTable = 1;
```



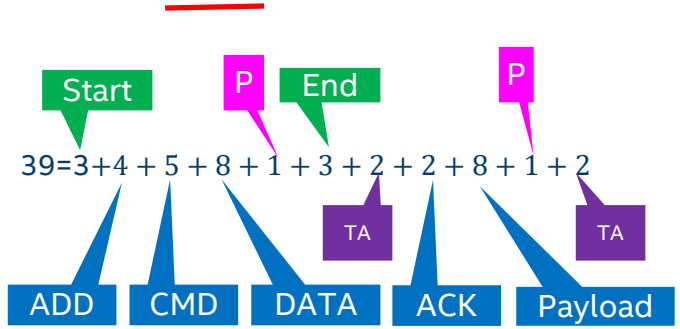
Data Sampling and Timing Analysis



- CPU drive on rising edge, VR sample on failing edge
- VR acts on the command after driving ACK bits in data frame
- VR drive on rising edge, CPU sample on failing edge

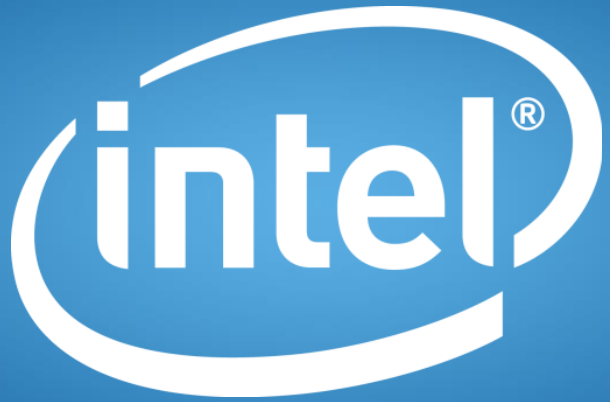
Measurement tips:

- Probe SVID signals at VR side or CPU side?



Tco = clock to data delay
Tpd= propagation delay on clk/data signal trace

Note: SVID = Intel® Serial Voltage Identification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