



FSL91030M chip

30G Layer 2 Ethernet switch chip

Register Description

Manual version: **D**

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1 Register Overview

1.1 Chip Introduction

FSL91030M is a 30G bandwidth Layer 2 Ethernet switch chip. Its service interface supports 8-way Gigabit adaptive electrical port, 2-way 10G optical port, 4 Gigabit optical ports and 2 RGMII/GMII/MII interfaces. Internally integrated RISC CPU, supports 16-bit DDR3 Interface, and UART, JTAG, GPIO, QSPI and I2C interfaces. The chip supports complete layer 2 network protocol processing, each port Scheduling function for 8 queues, synchronous Ethernet and 1588 functions.

This document mainly introduces the registers of the FSL91030M chip and the description of each bit field, the addresses of all table entries and registers. The jumps are all performed in units of words. For table entries, the minimum index value, maximum index value, and base value of the table entry are defined. The address of each entry in the table is obtained by the table base address and offset address; for registers, the address of the register is defined. site.

In this document, the following abbreviations are used:

RO: Read-only

WO: Write Only

RW: Readable and writable

RC: Read Clear

RW/WC: Readable/Writable/Write Clear

RW/W1C: Readable and writable/Write 1 Clear

WO/W1C: Write Only/Write 1 Clear

1.2 Block Division

The addresses of table entries and registers in this chip are obtained by adding the addresses of each subsystem to the offset address of the table entry or register.

The address ranges of various subsystems are shown in Table 1-1 and Table 1-2.

Table 1-1 Address mapping table of each subsystem

category	Modules		Base address description	
Global	CpBlock	top_cfg_reg	32'h0000_0000	Top-level configuration registers
		mdio_initiator_reg	32'h0200_0000	MDIO Configuration Register
	PKT_DMA		32'h0780_0000 Transmit and receive packet DMA configuration register	
	DP2REG		32'h0780_0020	Packet Configuration Registers
	CPU_CFG		32'h0400_A000	CPU Configuration Registers
	DDR		32'h0400_B000	DDR Configuration Registers
Interface	IpBlock	sd1g0_reg	32'h0400_1000	Serdes0 Configuration Register
		sd1g1_reg	32'h0400_2000	Serdes1 Configuration Register
		sd1g2_reg	32'h0400_3000	Serdes2 Configuration Registers
		sd1g3_reg	32'h0400_4000	Serdes3 Configuration Registers

		sd1g4_reg	32'h0400_5000	Serdes4 Configuration Registers
		sd1g5_reg	32'h0400_6000	Serdes5 Configuration Registers
		gphy0_reg	32'h0400_7000	GPHY0 Configuration Register
		gphy1_reg	32'h0400_8000	GPHY1 Configuration Register
PcsBlock		eth_fx100_0_reg	32'h0400_0000 100M electrical port 0PCS configuration register	
		eth_fx100_1_reg	32'h0400_0100 100M electrical port 1PCS configuration register	
		eth_fx100_2_reg	32'h0400_0200 100M electrical port 2PCS configuration register	
		eth_fx100_3_reg	32'h0400_0300 100M electrical port 3PCS configuration register	
		eth_fx100_4_reg	32'h0400_0400 100M electrical port 4PCS configuration register	
		eth_fx100_5_reg	32'h0400_0500 100M electrical port 5PCS configuration register	
		eth_xsgmii0_reg	32'h0400_0600 10G XGMII PCS Configuration Register	
		eth_xsgmii1_reg	32'h0400_0700 10G XGMII PCS Configuration Register	
		eth_xsgmii2_reg	32'h0400_0800 10G XGMII PCS Configuration Register	
		eth_xsgmii3_reg	32'h0400_0900 10G XGMII PCS Configuration Register	
		eth_xsgmii4_reg	32'h0400_0A00 10G XGMII PCS Configuration Register	
		eth_xsgmii5_reg	32'h0400_0B00 10G XGMII PCS Configuration Register	
		eth_xsbi0_reg	32'h0400_0C00 10G XSBII PCS Configuration Register	
		eth_xsbi1_reg	32'h0400_0D00 10G XSBII PCS Configuration Register	
MacBlock		eth_top_reg	32'h0700_0000 Ethernet top-level configuration register	
		eth_cmacrx_reg	32'h0700_4000 Ethernet RX configuration register	
		eth_cmactx_reg dp_reg	32'h0700_8000 Ethernet TX configuration register	
DP			32'h068E_0000 Datapath top level configuration register	
		traffic_write_reg	32'h068A_0000	Write Cache Configuration Register
		traffic_rep_reg	32'h0688_0000 Traffic replication configuration register	
		traffic_drop_reg	32'h0686_0000	Packet Drop Configuration Register
		traffic_queue_reg	32'h0684_0000 Queue management configuration register	
		traffic_schedule_reg	32'h0682_0000 Queue scheduling configuration register	
		traffic_read_reg	32'h0680_0000	Read Cache Configuration Register
		ptp_reg	32'h068D_0000	PTP Configuration Register
		oam_transmit_reg	32'h068C_0000 OAM message generation configuration register	
		dma_adapter_reg	32'h068C_8000 DMA adapter interface configuration register	
PP		pptop_reg	32'h0660_0000 Packet processing top-level configuration register	
		ipr0_reg	32'h0600_0000 Packet analysis module configuration register	
		ivt_reg	32'h0608_0000 Ingress Vlan conversion configuration register	
		inet_reg	32'h0610_0000 Entry Vlan Configuration Register	
		ifwd_reg	32'h0618_0000	L2 Switch Configuration Register
		iacl_reg	32'h0620_0000 Entry ACL Configuration Register	
		ipol_reg	32'h0628_0000 Entry policing configuration register	
		idst_reg	32'h0630_0000	Multicast Configuration Register
		eee_reg	32'h0638_0000 Egress VLAN conversion configuration register	
		epf_reg	32'h0640_0000 Egress	Egress vlan configuration register
		eacl_reg	32'h0648_0000	ACL Configuration Register
		epol_reg	32'h0650_0000 Egress policing configuration register	
		edst_reg	32'h0658_0000	Queue Configuration Register

Table 1-2 SOC address mapping table

category	Modules	Base	describe
SOC (System Peripherals)	GPIO	address 0x1001_1000 ~ 0x1001_1FFF	GPIO module register address range
	UART 0	0x1001_3000 ~ 0x1001_3FFF	The first UART module register address range
	UART 1	0x1001_2000 ~ 0x1001_2FFF	Second UART module register address range
	I2C	0x1001_8000 ~ 0x1001_8FFF	I2C module register address range
	QSPI	0x1001_4000 ~ 0x1001_4FFF	XPI QSPI module register address range
	QSPI0	0x1001_6000 ~ 0x1001_6FFF	QSPI0 module register address range
	DMA	0x1001_7000 ~ 0x1001_7FFF Note:	DMA module register address range

When using SOC, the first digit of the base address of each subsystem (Table 1-1) needs to be added with 5.

2 Global

2.1 CpBlock

2.1.1 top_cfg_reg

The top_cfg_reg register module contains 23 32-bit registers, as shown in the following table:

Register Offset	Register Name	Description
5'b0_0000	work_mode_cfg	Chip working mode configuration register
5'b0_0001	pcs_switch_mode_cfg	PCS and Switch Subsystem Mode Configuration Registers
5'b0_0010	ti_mode_cfg	TI Subsystem Configuration Registers
5'b0_0011	sys_pll_divisor	System PLL parameter configuration register
5'b0_0100	sdxg_pll_divisor	10G SerDes PLL parameter configuration register
5'b0_0101	sd1g_pll_divisor	1G SerDes PLL parameter configuration register
5'b0_0110	ptp_pll_divisor	PTP PLL parameter configuration register
5'b0_0111	rgmii_csr	RGMII Module Control and Status Registers
5'b0_1000	pll_pd_ctrl	PLL power down control register
5'b0_1001	sync_eth_cfg	Synchronous Ethernet Configuration Registers
5'b0_1010	reset_global	Reset Register: Global reset control
5'b0_1011	reset_serdes	Reset register: SerDes module reset control
5'b0_1100	reset_serdes_pcs	Reset Register: PCS Subsystem Reset Control
5'b0_1101	reset_switch_ephy	Reset Register: Switch subsystem and gephy module reset control
5'b0_1110	reset_pcs_adpt	Reset register: PCS adapter module reset control
5'b0_1111	reset_misc	Reset register: reset control of LED and other modules
5'b1_0100:5'b1_0110 5'b1_1000	axi_cp_cfg	axi_cp module configuration registers
5'b1_1001	soc_pll_divisor	soc PLL parameter configuration register
5'b1_0001	efuse_csr	Control and status registers of the efuse module
	tdc_cfg	TDC Module Configuration Register
5'b1_1010:5'b1_1011 5'b1_1100	chip_intr	Chip interrupt information and its mask
5'b1_1101	rgmii_alm_csr	RGMII module warning information and interrupt
5'b1_1110	chip_info_reg	Chip information
	rgmii_duplex	RGMII Half-Duplex Mode Configuration Register

2.1.1.1 work_mode_cfg

Register offset: 5' b0_0000

Register Description: Chip working mode configuration register

Bits	Name	R/W	Description 1'b0 :	Default
0	gephy0_off RW		gephy[0:3] is turned off 1'b1 : gephy[0:3] on 1'b0 :	Reset default value latch pin signal
1	gephy1_off RW		gephy[4:7] off 1'b1 : gephy[4:7] on 1'b0 : 10G	Reset default value latch pin signal
2:4	sdxg0_en RW		SerDes[0] off 1'b1 : 10G SerDes[0] enabled	Reset default value latch pin signal

5:7	sdxg1_en RW		1'b0 : 10G SerDes[1] disabled 1'b1: 10G SerDes[1] enables the	Reset default value latch pin signal
8	sync_en	R W	synchronous Ethernet function, and the reference clock of each PHY Selection condition, select 1'b1 reference_serdes_clk; 1'b0 selects reference_system_clk	1'b0
9	reuse_ind RW		Multiplexing mode selection of X_XMII_????? series PINs If the series of PINs is used for non-RGMII functions (Refer to xmii_state and xmii_mode registers) According to the reuse_ind signal, it is selected to be parallel LED is used as GPIO&QSPI. 1'b0 : GPIO&QSPI 1'b1 : parallel LED	1'b0
10:12	led_mode RW		LED Mode Select	Reset default value latch pin signal
13	led_active_low RW	blink_rate	LED Active Low or Active High	1'b1
14:16	RW burst_cycle RW		Blink Period	3'b000
17:18	clock_cycle RW		Serial LED Period	2'b00
19:20	serial_data_en RW		Clock	2'b00
twenty one	serial_clk_en RW	23	Period Serial LED Data	1'b1
twenty two	sdxg_led_mode RW		Enable Serial LED Clock Enable	1'b1
			10G serdes led configuration	1'b0

2.1.1.2 pcs_switch_mode_cfg

Register offset: 5' b0_0001

Register Description: PCS and Switch Subsystem Mode Configuration Register

Bits	Name	R/W	Description	Default
0:1	sd1g_en_0 RW		1'b0 : 1G SerDes[0] is disabled 1'b1 : 1G SerDes[0] on 1'b0 :	Reset default value latch pin signal
2:3	sd1g_en_1 RW		1G SerDes[1] off 1'b1 : 1G SerDes[1] on 1'b0 :	Reset default value latch pin signal
4:5	sd1g_en_2 RW		1G SerDes[2] off 1'b1 : 1G SerDes[2] on 1'b0 :	Reset default value latch pin signal
6:7	sd1g_en_3 RW		1G SerDes[3] off 1'b1: 1G SerDes[3] management	Reset default value latch pin signal
8	imp_en	R W	interface enable signal 1'b1 : Open 1'b0 : Close	Reset default value latch pin signal
9:10	imp_sel	R W	Management interface channel selection signal: 2'b00 : 10G SerDes[0] 2'b01: 10G SerDes[1] 2'b10 : giphy[0] 2'b11 : RGMII[0]	2'b00
13	flow_control_en RW		Flow control enable signal 1'b1 : Flow control on 1'b0 : Flow control off	1'b0

14	manage_mode RW		Management mode control 1'b1 : Management 1'b0: Unmanaged	Reset default value latch pin signal
15:17	buff_size_sel RW		Data Cache Size Control Register 3'd0 : 1.5M bytes 3'd1 : 1.25M bytes 3'd2 : 1M byte 3'd3 : 0.75M bytes 3'd4 : 0.5M byte 3'd5\6\7 : 0.25M bytes	3'd0
18:20	hub_mode RW		Chip swap working mode 3'd0: 8-port Gigabit electrical port mode 3'd1: 4-way Gigabit electrical port mode 3'd2: 12-way Gigabit electrical port mode 3'd3: 16-channel Gigabit electrical port mode 3'd4: 20-way Gigabit electrical port mode 3'd5: 24-channel Gigabit electrical port mode 3'd6: 8 Gigabit electrical ports + 4 Gigabit optical ports 3'd7: 8 Gigabit Ethernet ports + 2 10G optical ports	Reset default value latch pin signal

2.1.1.3 ti_mode_cfg

Register offset: 5' b0_0010

Register Description: TI Subsystem Configuration Register

Bits	Name	R/W	Description 2	Default
0:1	sdxg_2p5g_speed RW		10G SerDes in SGMII mode, The rate can be selected as 1.25Gbps or 2.5Gbps. Each bit controls: bit[0] : 10G SerDes[0] bit[1] : 10G SerDes[1] 1'b1 : 1.25Gbps 1'b0 : 2.5Gbps	2'h0
2:5	sd1g_2p5g_speed RW		4 1G SerDes in SGMII mode can Select the rate as 1.25Gbps or 2.5Gbps. Each bit controls: bit[0] : 1G SerDes[0] bit[1] : 1G SerDes[1] bit[2] : 1G SerDes[2] bit[3] : 1G SerDes[3] 1'b1 : 1.25Gbps 1'b0 : 2.5Gbps	4'h0
6:13	ephy_en	R W	Each bit corresponds to gephys[0:7] and is used for internal If you need to remap the channel through the register To configure the chip's operating mode, you may need to press 8 The enabling of gephys resets this register. 1'b1: indicates that the corresponding gephys is in the open state 1'b0: indicates that the corresponding gephys is in shutdown state	Reset default value latch pin signal
14:17	comb_en	R W	Each bit controls whether the 4 COMB modes are working. do	Reset default value latch pin signal

			1'b1: corresponding to COMB mode on 1'b0: corresponding to	
18:19	comb_mode_0 RW		COMB mode off When COMB mode [0] is on, select its specific working mode: 2'b00: combination mode, gephypriority 2'b01: combination mode, 1G SerDes priority 2'b10: fixed	Reset default value latch pin signal
20:21	comb_mode_1 RW		gephy 2'b11: fixed 1G SerDes When COMB mode [1] is on, select its specific working mode: 2'b00: combination mode, gephypriority 2'b01: combination mode, 1G SerDes priority 2'b10: fixed	Reset default value latch pin signal
22:23	comb_mode_2 RW		gephy 2'b11: fixed 1G SerDes When COMB mode [2] is on, select its specific working mode: 2'b00: combination mode, gephypriority 2'b01: combination mode, 1G SerDes priority 2'b10: fixed	Reset default value latch pin signal
24:25	comb_mode_3 RW		gephy 2'b11: Fixed 1G SerDes When COMB mode [3] is turned on, select its specific working mode: 2'b00: Combination mode, gephypriority 2'b01: Combination mode, 1G SerDes priority 2'b10: Fixed gephy 2'b11: Fixed 1G SerDes	Reset default value latch pin signal

2.1.1.4 sys_pll_divisor

Register offset: 5' b0_0011

Register Description: System PLL parameter configuration register

Bits	Name	R/W	Description	Default
0:3	sys_post_div1_2	RW	HUB_MODE=0/1: post_div1_2 = 4'd6 (125M) HUB_MODE=2: post_div1_2 = 4'd5 (150M) sys_post_div1_ HUB_MODE=3/4: post_div1_2 = 4'd6 (250M) 2_def HUB_MODE=5: post_div1_2 = 4'd5 (300M)	
4:6	sys_post_div2_2	RW	HUB_MODE=0/1: post_div2_2 = 4'd2 (125M) HUB_MODE=2: post_div2_2 = 4'd2 (150M) sys_post_div2_ HUB_MODE=3/4: post_div2_2 = 4'd1 (250M) 2_def HUB_MODE=5: post_div2_2 = 4'd1 (300M)	

2.1.1.5 sdxg_pll_divisor

Register offset: 5' b0_0100

Register Description: 10G SerDes PLL parameter configuration register

Bits	Name	R/W	Description	Default

0:5	sdxg_pll_refdiv RW		The refdiv parameter of sdxg_pll controls the PLL to generate two clocks Used as reference for 10G SerDes[0] and 10G SerDes[1] respectively clock	6'd1
6:17	sdxg_pll_fbddiv RW		The fbddiv parameter of sdxg_pll	12'd50
18:21 sdxg_post_div1_1 RW			controls the post_div1 parameter of the first clock of sdxg_pll. The value is determined by the rate mode of 10G SerDes[0]: Non-XSBI mode: post_div1_1 = 4'd5 (this clock defaults to 125MHz) XSBI mode: post_div1_1 = 4'd4 (this is the default red 156.25MHz)	Reset default latch Pin signal
22:24 sdxg_post_div2_1 RW			The post_div2 parameter of the first clock of sdxg_pll and	3'd2
25:28 sdxg_post_div1_2 RW			the post_div1 parameter of the second clock of sdxg_pll are set by default. The value is determined by the rate mode of 10G SerDes[1]: Non-XSBI mode: post_div1_1 = 4'd5 (this clock defaults to 125MHz) XSBI mode: post_div1_1 = 4'd4 (this clock defaults to 156.25MHz)	Reset default latch Pin signal
29:31 sdxg_post_div2_2 RW			post_div2 parameter for the second clock of sdxg_pll	3'd2

2.1.1.6 sd1g_pll_divisor

Register offset: 5' b0_0101

Register Description: 1G SerDes PLL parameter configuration register

Bits	Name	R/W	Description	Default
0:5	sd1g_pll_refdiv	RW	sd1g_pll The refdiv parameter controls the PLL to generate a clock Used as the reference clock for 1G SerDes[0], the default frequency is 125MHz	6'd1
6:17	sd1g_pll_fbddiv RW	18:21	The fbddiv parameter of sd1g_pll controls	12'd50
sd1g_post_div1_1 RW	22:24		the post_div1 parameter of sd1g_pll controls	4'd5
sd1g_post_div2_1 RW			the post_div2 parameter of sd1g_pll controls the	3'd2

2.1.1.7 ptp_pll_divisor

Register offset: 5' b0_0110

Register Description: PTP PLL parameter configuration register

Bits	Name	R/W	Description	Default
0:5	ptp_pll_refdiv RW	6:17	refdiv parameter of ptp_pll controls	6'd1
ptp_pll_fbddiv RW	18:21	ptp_post_div1_1	the fbddiv parameter of ptp_pll	12'd50
RW	22:24	ptp_post_div2_1 RW	controls the post_div1 parameter of ptp_pll	4'd5
			controls the post_div2 parameter of ptp_pll controls the	3'd2

2.1.1.8 rgmii_csr

Register offset: 5' b0_0111

Register Description: RGMII Module Control and Status Register

Bits	Name	R/W	Description	Default
0:1	xmii_mode_0	R W	determines the working mode of the first RMGII[0] interface: 2'b00 : RGMII 2'b01: GMII 2'b10 : MII-MAC 2'b11 : MII-PHY	Reset default latch pin Signal
2:3	xmii_mode_1	R W	Determines the operating mode of the second RMGII[1] interface: 2'b00 : RGMII 2'b01: GMII 2'b10 : MII-MAC 2'b11 : MII-PHY The default value of this register is consistent with xmii_mode_0	Reset default latch pin Signal
4:5	xmii_state	R W	Mode selection of RGMII module: 2'00: Indicates no RGMII operation 2'b01: Indicates that at most one of the two RGMII interfaces is GMII mode 2'b01: Indicates that at most two of the two RGMII interfaces GMII mode 2'b11: unknown	Reset default latch pin Signal
6:7	xmii_speed	R W	Each bit is used to indicate RGMII[0] and RGMII[1] rate: bit[0] -> RGMII rate 100Mbps bit[1] -> RGMII rate 10Mbps Only when the corresponding RMGII channel is MII-MAC or Valid in MII-PHY mode	Reset default latch pin Signal
8:9	xmii_txdelay	R W	Each bit controls RGMII[0] and RGMII[1] respectively. TX direction delay	Reset default latch pin Signal
10:11	xmii_rxdelay	R W	Each bit controls RGMII[0] and RGMII[1] respectively. RX direction delay	Reset default latch pin Signal
12:13 upi_rgmiiloopback_en	RW		Each bit controls RGMII[0] and RGMII[1] respectively. Whether loopback mode is enabled: 1'b0 : Close 1'b1 : Open	2'b00

2.1.1.9 pll_pd_ctrl

Register offset: 5' b0_1000

Register Description: Control Register

Bits	Name	R/W	Description	Default
0 upi_sdsg_pll_fout1_pd	RW		Controls the power down signal of the first clock of sdsg_pll 1'b1: corresponding pll power down signal is valid 1'b0: corresponding pll power down signal is invalid The default value is determined by the chip working mode	Reset default value latch pin signal
1 upi_sdsg_pll_fout2_pd	RW		Control the power down signal of the second clock of sdsg_pll 1'b1: corresponding pll power down signal is valid 1'b0: corresponding pll power down signal is invalid The default value is determined by the chip working mode	Reset default value latch pin signal

2	upi_sd1g_pll_pd RW		Control the power down signal of sd1g_pll 1'b1: corresponding pll power down signal is valid 1'b0: corresponding pll power down signal is invalid The default value is determined by the chip working mode	Reset default value latch pin signal
3	upi_cdr_pll_pd RW		Control the power down signal of cdr_pll 1'b1: corresponding pll power down signal is valid 1'b0: corresponding pll power down signal is invalid The default value is determined by the chip working mode	Reset default value latch pin signal
4	upi_sys_pll_pd RW		Control the power down signal of sys_pll 1'b1: corresponding pll power down signal is valid 1'b0: corresponding pll power down signal is invalid The default value is determined by the chip working mode	Reset default value latch pin signal
5	upi_ptp_pll_pd RW		Control the power down signal of ptp_pll 1'b1: corresponding pll power down signal is valid 1'b0: corresponding pll power down signal is invalid The default value is determined by the chip working mode	Reset default value latch pin signal
6	upi_soc_pll_pd RW		Control the power down signal of soc_pll 1'b1: corresponding pll power down signal is valid 1'b0: corresponding pll power down signal is invalid The default value is determined by the chip working mode	Reset default value latch pin signal

2.1.1.10 sync_eth_cfg

Register offset: 5' b0_1001

Register Description: Synchronous Ethernet Configuration Register

Bits	Name	R/W	Description:	Default
0:4	recov_clk_sel0	R W	Used for synchronous Ethernet function, select the clock of the first output clock Source. Generated only when recov_clk_sel0_ind is 1'b0 effect.	5'b00000
5	recov_clk_sel0_ind RW		Used for synchronous Ethernet function, controls the clock of the first output clock Select the source of the condition. 1'b1 : Selection condition is determined by pin 1'b0: The selection condition is determined by register recov_clk_sel0	1'b1
6:10	recov_clk_sel1	RW 5'b00000	For synchronous Ethernet function, select the clock of the second output clock Source. Only valid when recov_clk_sel1_ind is 1'b0. Used for synchronous	
11	recov_clk_sel1_ind RW		Ethernet function to control the clock of the first output clock. Select the source of the condition. 1'b1 : Selection condition is determined by pin 1'b0: The selection condition is determined by the register recov_clk_sel1	1'b1
12:13	sdxg_fx100_sync_eth_mode RW		When the corresponding SerDes-PCS is in FX100 mode, this register The register is used to select the output synchronous Ethernet recovered clock in this mode. When the clock comes from the PCS CDR or the SerDes CDR 1'b1 : Derived from PCS CDR 1'b0 : from SerDes Each bit corresponds to 10G SerDes[0] and 10G SerDes[1] respectively.	2'b00
14:17	sd1g_fx100_sync_eth_mode RW		When the corresponding SerDes-PCS is in FX100 mode, this register The register is used to select the output synchronous Ethernet recovered clock in this mode.	4'h0

		When the clock comes from the PCS CDR or the SerDes CDR 1'b1 : Derived from PCS CDR 1'b0 : from SerDes Each bit corresponds to 1G SerDes[0:3]	
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2.1.1.11 reset_global

Register offset: 5' b0_1010

Register Description: Reset register, global reset control

Bits	Name	R/W	Description	Default
0	upi_RST_GLB_UPI_N	R W	Description Global UPI	1'b1
1	upi_RST_GLB_LOGIC_N	RW	register soft resetGlobal logic register soft reset	1'b1

2.1.1.12 reset_serdes

Register offset: 5' b0_1011

Register Description: Reset register, SerDes module reset control

Bits	Name	R/W	Description	Default
0:1	upi_RST_UPI_SDXG_N	RW	10G SerDes module UPI register reset control, each bit corresponds to 10G SerDes[0], 10G SerDes[1]	2'b11
2:5	upi_RST_UPI_SD1G_N	RW	1G SerDes module UPI register reset control, each bit corresponds to 1G SerDes[0:3]	4'hf
6:7	upi_RST_LOGIC_SDXG_N	RW	10G SerDes module logic register reset control, each bit corresponds to 10G SerDes[0], 10G SerDes[1]	2'b11
8:11	upi_RST_LOGIC_SD1G_N	RW	1G SerDes module logic register reset control, each bit corresponds to 1G SerDes[0:3]	4'hf

2.1.1.13 reset_serdes_pcs

Register offset: 5' b0_1100

Register Description: Reset Register, PCS Subsystem Reset Control

Bits	Name	R/W	Description	Default
0:1	upi_RST_UPI_SDXG_PCS_N	RW	10G PCS module UPI register reset control, each bit corresponds to 10G PCS[0], 10G PCS[1] respectively	2'b11
2:3	upi_RST_LOGIC_SDXG_PCS_N	RW	10G PCS module logic register reset control, each bit corresponds to 10G PCS[0], 10G PCS[1] respectively	2'b11
4:7	upi_RST_UPI_SD1G_PCS_N	RW	1G PCS module UPI register reset control, each bit corresponds to 1G PCS[0:3]	4'hf
8:11	upi_RST_LOGIC_SD1G_PCS_N	RW	1G PCS module logic register reset control, each bit corresponds to 1G PCS[0:3] respectively	4'hf
12:17	upi_RST_UPI_FX100_PCS_N	RW	FX100 PCS module UPI register reset control, Each bit corresponds to FX100 PCS[0:5]	6'h3f

18:23	upi_rst_logic_fx100_pcs_n RW		FX100 PCS module logic register reset control, Each bit corresponds to FX100 PCS[0:5]	6'h3f
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2.1.1.14 reset_switch_ephy

Register offset: 5' b0_1101

Register Description: Reset register, Switch subsystem and gephy module reset control

Bits	Name	R/W	Description	Default
0	upi_rst_upi_dp_n	R W	DP module UPI register reset control	1'b1
1	upi_rst_logic_dp_n	R W	DP module logic register reset control	1'b1
2	upi_rst_upi_pp_n	R W	PP module UPI register reset control	1'b1
3	upi_rst_logic_pp_n	R W	PP module logic register reset control	1'b1
4	upi_rst_upi_mac_n	R W	MAC module UPI register reset control	1'b1
5	upi_rst_logic_mac_n RW		MAC module logic register reset control	1'b1
6:13	upi_rst_logic_sgl_ephy_n	RW	Logic reset control of a single GEPHY module, per bit Corresponding to GEPHY[0:7] respectively	8'hff
14:15	upi_rst_logic_all_ephy_n	RW	Logic reset control of two GEPHY groups, each bit corresponds to group[0] and group[1] respectively	2'b11
16:17	upi_rst_upi_ephy_n	RW	UPI reset control of two GEPHY groups, Each bit corresponds to group[0] and group[1] respectively.	2'b11

2.1.1.15 reset_pcs_adpt

Register offset: 5' b0_1110

Register Description: Reset register, PCS adapter module reset control

Bits	Name	R/W	Description	Default
0	upi_rst_logic_sdsg_a_adpt_n	RW	10G PCS[0] adapter logic reset control, each bit Corresponding to 8 adapters[0:7]	8'hff
1	upi_rst_logic_sdsg_b_adpt_n	RW	10G PCS[1] adapter logic reset control, each bit Corresponding to 8 adapters[0:7]	8'hff
2:4	upi_rst_logic_sd1g_adpt_n	RW	1G PCS[0:3] adapter logic reset control, each bit Adapters corresponding to 4 PCS	4'hf
5:7	upi_rst_logic_ephy_adpt_n	RW	1000BASE-T PCS[0:7] adapter logic reset control Each bit corresponds to 8 PCS adapters.	8'hff

2.1.1.16 reset_misc

Register offset: 5' b0_1111

Register description: reset register, reset control of LED and other modules

Bits	Name	R/W	Description	Default
0	upi_rst_logic_led_n	R W	Logic reset control of LED module	1'b1
1	upi_rst_logic_mdio_n	RW	Logic reset control of mdio initiator module	1'b1
2:3	upi_rst_logic_rgmii_tx_n	RW TX	direction logic reset for RGMII[0] and RGMII[1] control	2'b11

4:5	upi_rst_logic_rgmiirx_n	RW RX	direction logic reset for RGMII[0] and RGMII[1] control	2'b11
6	upi_rst_upi_dec_pcs_n	RW UPI register	reset control of pcs decode module 1'b1	
7	upi_rst_upi_dec_switch_n	RW	switch decode module UPI register reset control system	1'b1
8:9	control upi_rst_logic_rgmiiadpt_n	RW	RGMII[0] and RGMII[1] adapter module logic Reset	2'b11
10	upi_rst_logic_dma_n	RW DMA module	logic register reset control	1'b1
11	upi_rst_upi_dma_n	RW DMA	module UPI register reset control	1'b1

2.1.1.17 axi_cp_cfg

Register offset: 5'b1_0100:5'b1_0110

Register Description: axi_cp module configuration register

Offset 0	Bits	Name	R/W	Description	Default
	3:5	axi_cp_mask	R W	Interrupt mask of axi_cp	3'd0
0	0:2	axi_cp_alm	RC	module Alarm register of axi_cp	3'd0
1	0:31	module_rpkt_header_chk	RW	register packet Sending direction packet header 32'h0600_beef	
2	0:31	rpkt_sop_tag	RW	register packet return direction packet header 32'h0500_beef	

2.1.1.18 soc_pll_divisor

Register offset: 5' b1_1000

Register Description: soc PLL parameter configuration register

Bits	Name	R/W	Description	Default
0:5	soc_pll_refdiv	RW	The refdiv parameter of the soc	6'd1
6:17	soc_pll_fbdiv	RW	pll controls the fbdiv parameter	12'd64
18:21	of the soc pll. The post_div1 parameter of the first clock output by the soc pll controls the soc_post_div1_1	RW		
22:24	soc_post_div2_1	RW	The post_div2 parameter controls the first clock output of the soc pll	3'd1
25:28	soc_post_div1_2	RW	The post_div1 parameter controls the second clock output of the soc pll	
29:31	soc_post_div2_2	RW	The second clock post_div2 parameter controls the output of the soc pll	3'd5

2.1.1.19 efuse_csr

Register offset: 5' b1_1001

Register Description: Control and Status Registers of the efuse Module

Bits	Name	R/W	Description	Chip	Default
0:1	pkg_type	RW	package type	ptp	6'd1
2:2	ptp_enable	RW	module enable control, 1'b1 enable		12'd80

2.1.1.20 tdc_cfg

Register offset: 5' b1_0001

Register Description: TDC Module Configuration Register

Bits	Name	R/W	Description	Default
13:20	trim_reg	RW	Temperature calibration control register of TDC module, see TDC Module Description	Reset default latch Pin signal
12	xen_reg	R W	TDC module power down control 1'b1 : Normal working mode 1'b0 : power down working mode	1'b0
11	xreset_reg	R W	TDC module reset control: 1'b1: TDC internal digital circuit reset to 0 1'b0 : Normal working mode	1'b1
10	xchopctrl_reg	R W	TDC OP-AMP chop control: 1'b1 : fix the chopper clock at high level 1'b0 : Enter chopper function	1'b0
0:9	xb_reg	RO	TDC module data output	10'd0

2.1.1.21 chip_intr

Register offset: 5'b1_1010:5'b1_1011

Register description: chip interrupt information and its mask

Offset 0	Bits	Name	R/W	DescriptionChip	Default
	0:20	intr_data_read	RO	interrupt signal	21h0
1	0:20	intr_data_mask	R W	indicationChip interrupt signal mask	21h0

2.1.1.22 rgmii_alm_csr

Register offset: 5' b1_1100

Register Description: RGMII module warning information and interrupt

Bits	Name	R/W	Description	Default
0:1	upi_rgmii_idle_in_data_alm	RC	RGMII alarm information, idle alarm, each bit is Corresponding to RGMII[0] and RGMII[1]	2'b00
2:3	upi_rgmii_nibble_err_alm	RC	RGMII warning information, half-byte error warning, each bit corresponds to RGMII[0] and RGMII[1] respectively	2'b00
4:5	upi_rgmii_rx_fifo_full_alm	RC	RGMII warning information, RX direction fifo full warning Alarm, each bit corresponds to RGMII[0] and RGMII[1]	2'b00
6:7	upi_rgmii_rx_fifo_empty_alm	RC	RGMII warning information, RX direction fifo read empty warning Alarm, each bit corresponds to RGMII[0] and RGMII[1]	2'b00
8:9	upi_rgmii_tx_fifo_full_alm	RC	RGMII warning information, TX direction fifo full warning Alarm, each bit corresponds to RGMII[0] and RGMII[1]	2'b00
10:11	upi_rgmii_tx_fifo_empty_alm	RW	RGMII alarm information, TX direction fifo read empty alarm Alarm, each bit corresponds to RGMII[0] and RGMII[1]	2'b00

12:13	upi_rgmiidle_in_data_alm_mask	RW RGMII alarm mask, alarm is not generated when the value is 1'b1 Generate an interrupt	2'b00
14:15	upi_rgmi_nibble_err_alm_mask	RW RGMII alarm mask, alarm is not generated when the value is 1'b1 Generate an interrupt	2'b00
16:17	upi_rgmi_rx_fifo_full_alm_mask	RW RGMII alarm mask, alarm is not generated when the value is 1'b1 Generate an interrupt	2'b00
18:19	upi_rgmi_rx_fifo_empty_alm_mask	RW RGMII alarm mask, alarm is not generated when the value is 1'b1 Generate an interrupt	2'b00
20:21	upi_rgmi_tx_fifo_full_alm_mask	RW RGMII alarm mask, alarm is not generated when the value is 1'b1 Generate an interrupt	2'b00
22:23	upi_rgmi_tx_fifo_empty_alm_mask	RW RGMII alarm mask, alarm is not generated when the value is 1'b1 Generate an interrupt	2'b00

2.1.1.23 chip_info_reg

Register offset: 5' b1_1101

Register Description: Chip Information

Bits	Name	R/W	Description chip	Default
0:31	chip_info	RO	Production time and batch code	32'h0

2.1.1.24 rgmii_duplex

Register offset: 5' b1_1110

Register Description: RGMII Half-Duplex Mode Configuration Register

Bits	Name	R/W	Description	Default
0:1	upi_rgmi_duplex_mode	R W	Each bit controls RGMII[0] and RGMII[1] respectively Half-duplex mode: 1'b0 : Half-duplex mode 1'b1 : Full-duplex mode	2'b11
2:6	upi_rgmi_rateadpt_thrd_h_0	RW RGMII[0]	adapter module high watermark value 5'd9	
7:11	upi_rgmi_rateadpt_thrd_l_0	RW RGMII[0]	adapter module low watermark value 5'd4	
12:16	upi_rgmi_rateadpt_thrd_h_1	RW RGMII[1]	adapter module high watermark value 5'd9	
17:21	upi_rgmi_rateadpt_thrd_l_1	RW RGMII[1]	adapter module low watermark value 5'd4	
22:23	upi_rgmi_crscol_sel	R W	Each bit controls RGMII[0] and RGMII[1] respectively. The col/crs signal value.	2'b00

2.1.2 mdio_initiator_reg

The mdio_initiator_reg register module contains three 32-bit registers: mdio_frm_field register, mdio_frm_ctrl register and mdio_master_ctrl register; it also contains 1 storage register (mdio_cmd). The register list is as follows:

Register Offset	Register Name	Description
2'b00	mdio_frm_field	Contents of each field of the mdio frame
2'b01	mdio_frm_ctrl	Indicates the completion status of sending and receiving mdio frames
2'b11	mdio_master_ctrl	Control the mode of the mdio initiator module

The storage register list is as follows:

Register Offset	Register Memory	Description
2'b10	mdio_cmd	The data field information of the mdio frame, as well as the start of sending or Receiving frame

2.1.2.1 mdio_frm_field

Register offset: 2'b00

Register description: the contents of each field of the mdio frame

Bits	Name	R/W	Description	Default
0:4	prt_phy_ad RW		CL22 frame : PHY AD field CL45 frame : PRT AD field See 802.3 Clauses 22 and 45 for details.	5'd1
5:9	dev_reg_ad RW		CL22 frame: REG AD field CL45 frame: DEV AD field See 802.3 Clause22&45 op	5'd0
10:11	op_code	R W	code field for details See 802.3 Clause 22&45st code	2'b10
12:13	st_code	R W	field for details See 802.3 Clause22&45 for	2'b01
14:15	in_delay	R W	details. It is valid when reading an mdio frame and controls the ta field. How many MDC cycles does it take to start receiving read data	2'b00
16:20	cl22_pre	R W	after the CL22 MDIO frame preamble field length?	5'd31
21:25	cl45_pre	R W	CL45 The length of the preamble field of the mdio frame controls	5'd31
26	status_mode RW		whether it is necessary to wait for the end of the data field after starting the mdio frame. 1'b0 : Wait 1'b1 : No waiting	1'b0

2.1.2.2 mdio_frm_ctrl

Register offset: 2'b01

Register Description: Indicates the completion status of the sending and receiving of the mdio frame

Bits	Name	R/W	Description	Default
0	mdio_frm_done RO		indicates that the transmission of this mdio frame is completed. status_mode is 1'b0, then after the data field of the frame The signal is valid; if status_mode is 1'b0, then the It becomes effective after mdio frame	1'b0

2.1.2.3 mdio_master_ctrl

Register offset: 2'b11

Register Description: Control the mode of the mdio initiator module

Bits	Name	R/W	Description	Default

0	mdio_take_over RW		1'b1: The mdio_initiator module can access 8 gephys. The chip is still in MDIO PHY device mode, and the external MDIO STA is accessible Chip register	1'b0
1	cpu_sta_en RW		1'b1: The chip is in mdio STA mode and can access external MDIO During PHY.	1'b0
2	mdio_frm_idle RW	Controls whether the mdio frame is in the idle state, logic 1 or logic 0		1'b1

2.1.2.4 mdio_cmd

Storage register description: data field information of mdio frame, and start sending or receiving frame, NumOfEntries is 1, words is 1.

Bits	Name	R/W	Description
0:15	mdio_data	RW	If the initiated mdio frame is a write or address format frame, then the The register must be pre-written with write data or reg address. mdio frame is a read format frame, then this register is in the mdio frame After the transfer is completed, the read data information can be read.

2.2 PKT_DMA

The pkt_dma_reg register module contains 16 registers, the register list is as follows:

Register Offset	Register Name	Description
4'b0000	pkt_dma_rx_addr	CPU receive packet DMA address configuration
4'b0001	pkt_dma_rx_state	CPU receive packet DMA status indication
4'b0010	pkt_dma_rx_start	CPU starts receiving packet DMA instruction
4'b0011	pkt_dma_tx_addr	CPU send packet DMA address configuration
4'b0100	pkt_dma_tx_cfg	CPU sends packet DMA information configuration
4'b0101	pkt_dma_tx_start	CPU starts sending packet DMA instruction
4'b0110	pkt_dma_cfg	DMA Control Configuration
4'b0111	pkt_dma_axi_wr_cfg	DMA AXI interface write configuration
4'b1000	pkt_dma_axi_rd_cfg	DMA AXI interface read configuration
4'b1001	pkt_dma_bresp_wd_cfg	DMA Bresp watchdog configuration
4'b1010	pkt_dma_tx_wd_cfg	DMA packet watchdog configuration
4'b1011	pkt_dma_rx_ready_wd_cfg	DMA packet side ready watchdog configuration
4'b1100	pkt_dma_rx_wd_cfg	DMA packet receiving watchdog configuration
4'b1101	pkt_dma_status	DMA Status
4'b1110	pkt_dma_alarm	DMA Alerts
4'b1111	pkt_dma_int_mask	DMA interrupt mask

2.2.1 pkt_dma_rx_addr

Register offset: 4'b0000

Register Description: CPU receive packet DMA address configuration

Bits	Name	R/W	Description	Default
0:31	upi_dma_rx_addr	RW	CPU receive packet DMA buffer start address in DLM/DDR 32'h0	

2.2.2 pkt_dma_rx_state

Register offset: 4'b0001

Register Description: CPU receive packet DMA status indication

Bits	Name	R/W	Description	Default
0:11	upi_dma_rx_length	RO	CPU receives packet length information indication	12'h0
12	upi_dma_rx_port	RO	CPU receive packet port indication 0:PTP, 1:OAM	1'b0

2.2.3 pkt_dma_rx_start

Register offset: 4'b0010

Register Description: CPU starts receiving packet DMA instruction

Bits	Name	R/W	Description	Default
0	upi_dma_rx_start_en	WO/W1C	CPU receives packet DMA start enable, write 1 to trigger 1'b0	

2.2.4 pkt_dma_tx_addr

Register offset: 4'b0011

Register Description: CPU send packet DMA address configuration

Bits	Name	R/W	Description	Default
0:31	upi_dma_tx_addr	RW	CPU sends packet DMA buffered start address in DLM/DDR 32'h0	

2.2.5 pkt_dma_tx_cfg

Register offset: 4'b0100

Register Description: CPU sends packet DMA information configuration

Bits	Name	R/W	Description	Default
0:11	upi_dma_tx_length	RW	CPU send packet length configuration	12'h0
12	upi_dma_tx_port	R W	CPU send packet port configuration 0:PTP, 1:OAM	1'b0

2.2.6 pkt_dma_tx_start

Register offset: 4'b0101

Register Description: CPU starts sending packet DMA instruction

Bits	Name	R/W	Description	Default
0	upi_dma_tx_start_en	WO/W1C	Send packet DMA start enable, write 1 to trigger	1'b0

2.2.7 pkt_dma_cfg

Register offset: 4'b0110

Register Description: DMA Control Configuration

Bits	Name	R/W	Description	Default
0	upi_dma_byte_endian	R W	Byte size endian control (4 bytes per block) 0: big endian, 1: little	1'b0
1	upi_dma_block_endian	R W	Endian block size control 0: big endian, 1: little endian	1'b0
2	upi_dma_priority	R W	channel priority 0: PTP priority, 1: OAM priority	1'b0

2.2.8 pkt_dma_axi_wr_cfg

Register offset: 4'b0111

Register Description: DMA AXI Interface Write Configuration

Bits	Name	R/W	Description	Default
0:7	upi_axi4_wlen_max	R W	The maximum burst block length of a Write transaction on an AXI interface (i.e. Maximum value of AWLEN[7:0])	8'hff
8:15	upi_axi4_awid	RW	AXI interface Write awid/wid configuration	8'h0
16:17	upi_axi4_awburst RW		AXI interface Write awburst configuration	2'h1
	upi_axi4_awlock RW 18:19 20:23		AXI interface Write awlock configuration	2'h0
upi_axi4_awcache RW	upi_axi4_awprot RW		AXI interface Write awcache configuration	4'h0
24:26			AXI interface Write awprot configuration	3'h0

2.2.9 pkt_dma_axi_rd_cfg

Register offset: 4'b1000

Register Description: DMA AXI Interface Read Configuration

Bits	Name	R/W	Description	Default
0:7	upi_axi4_rlen_max	R W	The maximum burst block length of a Read transaction on an AXI interface (i.e. ARLEN[7:0] maximum value)	8'hff
8:15	upi_axi4_arid	R W	AXI Interface Read arid/rid Configuration	8'h0
16:17	upi_axi4_arburst RW		AXI Interface Read arbust Configuration	2'h1
18:19	upi_axi4_arlock RW		AXI Interface Read Arlock Configuration	2'h0
20:23	upi_axi4_arcache RW		AXI Interface Read Arcache Configuration	4'h0
24:26	upi_axi4_arprot RW		AXI interface Read arprot configuration	3'h0

2.2.10 pkt_dma_bresp_wd_cfg

Register offset: 4'b1001

Register Description: DMA Bresp Watchdog Configuration

Bits	Name	R/W	Description	Default
0:23	upi_dma_bresp_wd_th RW		AXI Bresp Watchdog Threshold	24'hffff
Twenty Four	upi_dma_bresp_wd_en RW		AXI Bresp watchdog enable	1'b1
25	upi_dma_bresp_id_en RW		AXI Bresp ID Enable	1'b0

2.2.11 pkt_dma_tx_wd_cfg

Register offset: 4'b1010

Register Description: DMA packet watchdog configuration

Bits	Name	R/W	Description	Default
0:23	upi_dma_tx_wd_th	R W	CPU send packet operation watchdog threshold	24'h00ffff
Twenty Four	upi_dma_tx_wd_en RW		CPU sends packet operation watchdog enable	1'b1

2.2.12 pkt_dma_rx_ready_wd_cfg

Register offset: 4'b1011

Register Description: DMA packet side ready watchdog configuration

Bits	Name	R/W	Description	Default
0:23	upi_dma_rx_ready_wd_th RW		CPU packet side ready back pressure watchdog threshold	24'h00ffff
Twenty Four	upi_dma_rx_ready_wd_en RW		CPU packet side ready back pressure watchdog enable	1'b1

2.2.13 pkt_dma_rx_wd_cfg

Register offset: 4'b1100

Register Description: DMA packet receiving watchdog configuration

Bits	Name	R/W	Description	Default
0:23	upi_dma_rx_wd_th	R W	CPU receive packet operation watchdog threshold	24'h00ffff
Twenty Four	upi_dma_rx_wd_en RW		CPU receive packet operation watchdog enable	1'b1

2.2.14 pkt_dma_status

Register offset: 4'b1101

Register Description: DMA Status

Bits	Name	R/W	Description	Default
0	upi_dma_rx_end RO	CPU receives packet DMA end indication, write upi_dma_rx_start_en to clear 1'b0		
1	upi_dma_rx_req RO	CPU receives the packet DMA start request, write upi_dma_rx_start_en to clear 1'b0		
2	upi_dma_tx_end RO	CPU sends packet DMA end indication, write upi_dma_tx_start_en clear 1'b0		
upi_dma_rresp_stat RO			AXI Rresp result, updated per DMA operation 4:5	2'b00
upi_dma_bresp_stat RO			AXI Bresp results, updated per DMA operation 6:7	2'b00

2.2.15 pkt_dma_alarm

Register offset: 4'b1110

Register Description: DMA Alarm

Bits	Name	R/W	Description	Default
0	upi_dma_rx_len_err_alm	RC	CPU receive packet DMA length error alarm (apply Burst and the amount of read data does not match)	1'b0
1	upi_dma_rx_len_err_int_mask RW	CPU receive packet DMA length error interrupt mask 1'b0		
2	upi_dma_tx_len_err_alm	RC	CPU sends packet DMA length error alarm (actual packet length and Length mismatch in SOP)	1'b0
3	upi_dma_tx_len_err_int_mask RW	CPU transmit packet DMA length error interrupt mask 1'b0		
4	upi_dma_rx_wd_alm	RC	CPU receiving packet operation timeout alarm 1'b0	
5	upi_dma_rx_wd_int_mask RW		CPU receive packet operation timeout alarm interrupt mask 1'b0	
6:7	upi_dma_rx_ready_wd_alm	RC	CPU packet side ready back pressure timeout alarm	1'b0
8:9	upi_dma_rx_ready_wd_int_mask RW	CPU packet side ready back pressure timeout alarm interrupt mask 1'b0		
10	upi_dma_tx_wd_alm	RC	CPU packet sending operation timeout alarm 1'b0	
11	upi_dma_tx_wd_int_mask RW		CPU send packet operation timeout alarm interrupt mask 1'b0	

2.2.16 pkt_dma_int_mask

Register offset: 4'b1111

Register Description: DMA Interrupt Mask

Bits	Name	R/W	Description	Default
0	upi_dma_rx_req_int_mask RW	CPU receive packet DMA end indication interrupt mask 1'b0		
1	upi_dma_rx_end_int_mask RW	CPU receives packet DMA to start requesting interrupt mask 1'b0		
2	upi_dma_tx_end_int_mask RW	CPU sends packet DMA to start requesting interrupt mask 1'b0		

2.3 DP2REG

The dp2reg_reg register module contains 2 registers, the register list is as follows:

Register Offset	Register Name	Description
2'b00	dp2reg_cfg	DP2REG module configuration register
2'b01	dp2reg_alm	DP2REG Alarm Register

2.3.1 dp2reg_cfg

Register offset: 2'b00

Register Description: DP2REG module configuration register.

Bits	Name	R/W	Description	Default
0:3	rpkt_header_len RW		Register packet invalid header length 4'd0...8 bytes 4'd1...16 bytes	4'd2

			4'd2..24 bytes ... 4'd7..64 bytes (maximum)	
4	add_crc_dummy RW		Whether to add CRC bytes to the register packet 1...Add null byte 0..do not add null bytes	1'b1
5	reverse_mac RW		Whether to swap DMAC and SMAC when register packet read register returns. 1...Swap 0...Do not swap	1'b1

2.3.2 dp2reg_alm

Register offset: 2'b01

Register Description: DP2REG alarm register.

Bits	Name	R/W	Description Read	Default
0	out_fifo_outflow	RC	direction FIFO read empty alarm	1'b0
1	out_fifo_overflow	RC	Write direction FIFO write full alarm	1'b0
2	in_fifo_outflow	RC	Write direction FIFO read empty	1'b0
3	in_fifo_overflow	RC	alarm Read direction FIFO write	1'b0
4	reg_error_end	RC	full alarm Internal register decoding	1'b0
5:9	alm_mask	R W	error warning Alarm mask register, corresponding to this register 0~4 bits 1: Alarm is invalid 0: Alarm is valid	5'b1_1110

2.4 CPU_CFG

The cpu_cfg_reg register module contains 4 registers, as shown in the following table:

Register Offset	Register Name	Description
4'b0000: 4'b0001	clk_cfg	CPU clock division configuration register
4'b0010	rst_cfg	CPU Reset Register
4'b1000: 4'b1001	rst_v_cfg	CPU reset start vector register
4'b1011	timer_cfg	CPU Timer Configuration Registers

2.4.1 clk_cfg

Register offset: 4'b0000: 4'b0001

Register Description: CPU clock division configuration register.

Offset	Bits	Name	R/W	DescriptionBus	Default
0	0:5	fab_div_value RW		frequency division configuration register, startup configuration register, other registers The register cannot be configured to be	6'b01
0	6:11	smaller than this register. sys_div_value RW		System frequency division configuration register, needs to be equal to fab_div_value 6'b01	6'b01
0	12:17 cg_udma_div_value RW	18:23		DMA module clock frequency division register	6'b01
0	uart0_div_value RW	uart1_div_value RW		UART0 module clock frequency division register	6'b01
0	24:29			UART1 module clock frequency division register	6'b01

1	0:5	i2c_div_value RW		I2C module clock divider register	6'b01
1	6:11	Qspi0_div_value RW		QSPI0 clock divider register	6'b01
1	12:17	Qspi1_div_value RW 18:23		QSPI1 clock divider register	6'b01
1	gpio_div_value RW 24:29	localbus_div_value		GPIO clock divider register	6'b01
1	RW 30:31	ddr_div_value RW		Internal configuration bus divider register	6'b01
1				DDR AXI interface divider register	2'b01

2.4.2 rst_cfg

Register offset: 4'b0010

Register Description: CPU reset register.

Bits	Name	R/W	Description	Default
0	core_reset_n	R W	CPU overall reset register	1'b1
1	rst_fab_n	R W	System bus reset register	1'b1
2	rst_sys_n	R W	System internal bus reset register	1'b1
3	rst_cg_udma_n	R W	DMA bus interface reset register	1'b1
4	rst_uart0_n	R W	UART0 peripheral reset register	1'b1
5	rst_uart1_n	R W	UART1 peripheral reset register	1'b1
6	rst_i2c_n	R W	I2C Peripheral Reset Register	1'b1
7	rst_qspi0_n	R W	QSPI0 peripheral reset register	1'b1
8	rst_qspi1_n	R W	QSPI1 Peripheral Reset Register	1'b1
9	rst_gpio_n	R W	GPIO peripheral reset register	1'b1

2.4.3 rst_v_cfg

Register offset: 4'b1000: 4'b1001

Register Description: CPU reset start vector register.

Offset 0	Bits	Name	R/W	Description	Default
	0:31	reset_vector_0 RW	reset_vector_1	CPU boot address lower 32 bits	32'h8000_0000
1	0:31	RW		CPU boot address high 32 bits	32'b0

2.4.4 timer_cfg

Register offset: 4'b1011

Register Description: CPU timer configuration register.

Bits	Name	R/W	Description	Default
0:3	wdt_toggle_divider RW		Watchdog flag divider register	4'd11
4:7	dbg_toggle_divider RW		Debug flag divider register	4'd13
8:11	mtime_toggle_divider RW		MTIME flag divider register	4'd13

2.5 DDR

The ddr_reg register module contains 5 registers, as shown in the following table:

Register Offset	Register Name	Description
4'b0000	ddr_all_cfg	DDR IP Configuration Registers
4'b0001	ddra_cfg	DDR Address IP Configuration Register
4'b0010	ddrd_cfg	DDR Data IP Configuration Register
4'b0100: 4'b0101	ddr_pll_cfg	DDR PLL Configuration Registers
4'b1000: 4'b1010	ddr_RST_seq_cfg	DDR Reset Configuration Register

2.5.1 ddr_all_cfg

Register offset: 4'b0000

Register Description: DDR IP Configuration Register.

Bits	Name	R/W	Description	Default
1:3	ddr_vref_select	R W	Description When ddr_selfbias = 1, the PHY output is used VREF Bias Voltage 000:0.55*VCC15O_DDR 001:0.525*VCC15O_DDR 010:0.475*VCC15O_DDR 011:0.45*VCC15O_DDR 100~111:0.5*VCC15O_DDR	3'h4
4	ddr_sio	R W	1: DQS is in standalone mode 0: DQS is in separate mode	1'b0
5	ddr_selfbias	R W	Enable Self-bias generation 1: Bias comes from inside 0: Bias comes from external (VREF)	1'b0
6	ddr_mddr1	R W	LPDDR mode is	1'b0
7	ddr_ddr3	R W	valid DDR3 mode	1'b1
8	ddr_conupdate	R W	is valid Continuous DDR DLL	1'b1
9	ddr_io15v	R W	is valid 1: 1.35V, 1.5V, 1.8V 0: 1.2V	1'b1
10	ddr_clock_en	R W	DDR PHY internal clock valid DLL	1'b1
11:13	ddr_dllrange	R W	reference frequency selection 000: 260Mbps~400Mbps 001: 400Mbps~600Mbps 010: 600Mbps~700Mbps 011: 700Mbps~800Mbps 100: 800Mbps~900Mbps 101: 900Mbps~1000Mbps 110: 1000Mbps~1200Mbps 111: 1200Mbps~1600Mbps	3'b100
14	ddr_byone	R W	1:1:1 mode 0: 1:2 mode	1'b0

2.5.2 ddra_cfg

Register offset: 4'b0001

Register Description: DDR Address IP Configuration Register.

Bits	Name	R/W	Description	Default
0	ddra_lpddr2	mode RW	Controls CKE and RESET_N_DRAM mode	1'b0
1	ddra_dsrnrb		1: Normal mode 0: CKE is all low, RESET_N_DRAM is high and effective.	1'b1
2:5	ddra_dutysel	RW	CK/CKB judgment bit, do not modify the	4'h8
6:8	ddra_cmd_cktree_skew	RW 3'h3	phase used to control the internal clock	
9:13	ddra_cmd_cktree_delay	RW	Used to balance the clock of DDR_PHY and controller	5'h1b

2.5.3 ddrd_cfg

Register offset: 4'b0010

Register Description: DDR Data IP Configuration Register.

Bits	Name	R/W	Description	Default
0:2	ddrd1_cktree_skew	RW	is used to control the phase of the internal clock	3'h3
3:7	ddrd1_cktree_delay	RW	is used to balance the timing between DDR_PHY and controller. bell	5'hf
8:10	ddrd0_cktree_skew	RW	Used to control the phase of the internal clock	3'h3
11:15	ddrd0_cktree_delay	RW	is used to balance the timing between DDR_PHY and controller. bell	5'hc

2.5.4 ddr_pll_cfg

Register offset: 4'b0100: 4'b0101

Register Description: DDR PLL Configuration Register

Offset 0	Bits	Name	R/W	Description	Default
	0:5	ddr_pll_refdiv	REF=25M;REFDIV=1;FBDIV=50; FVCO=1250M RW		6'd1
0	6:17	ddr_pll_fbdiv	REF=25M;REFDIV=1;FBDIV=50; FVCO=1250M RW SDXG PLL		12'd80
0	18:21	ddr_post_div1_1	fout1 for left SerDes: left SerDes not XSBI MODE : post_div1_1 = 4'd5 (125M) left SerDes is XSBI MODE : post_div1_1 = 4'd4 (156.25)		4'd5
0	22:24	ddr_post_div2_1	RW default always 3'd2 RW SDXG PLL		3'd1
0	25:28	ddr_post_div1_2	fout2 for right SerDes right SerDes not XSBI MODE : post_div1_2 = 4'd5 (125M) right SerDes is XSBI MODE : post_div1_2 = 4'd4 (156.25)		4'd5
0	29:31	ddr_post_div2_2	RW default always 3'd2 DDR		3'd2
1	0	ddr_pll_pdn	RW	PLL switch control ddr_pll_pdn_cfg	
1	1	ddr_reset_ready	RO	DDR reset completion signal	1'b0

2.5.5 ddr_rst_seq_cfg

Register offset: 4'b1000: 4'b1010

Register Description: DDR Reset Configuration Register

Offset	Bits	Name	R/W	Description	Default
0	0:19	ddr3a_pll_RST_n_max RW		DDR PLL reset wait time 20'd20100	
0	20:29	pllpdn_max	RW	PLLPDN Waiting Time	9'd450
1	0:19	ddr3a_RST_n_max	R W	DDR3A reset wait time	20'd40100
1	20:24	dllpdn_max	R W	DLLPDN reset wait time	5'd16
2	0:15	ddr3c_m_RST_n_max RW		DDR controller reset wait time 16'd2100	

3 Interface

3.1 IpBlock

3.1.1 sd1g_reg

The sd1g_reg register module contains 10 registers, as shown in the following table:

Register Offset	Register Name	Description
5'b00000	reset_ctrl	Reset
5'b00001	pd_ctrl	Power down configuration
5'b00010	width_ctrl	Bit width configuration
5'b00011	rate_ctrl	Rate Configuration
5'b00100	idle_ctrl	Idle Configuration
5'b00101	serdes_ctrl	serdes configuration
5'b00110	rx_ctrl	rx channel configuration
5'b01000: 5'b01001	rx_eq_ctrl	rx equalization correction configuration
5'b01010	eye_diag_ctrl	Eye diagram configuration
5'b01011	rd_status	serdes status

3.1.1.1 reset_ctrl

Register offset: 5'b00000

Register Description: Reset

Bits	Name	R/W	Description RW Used in Multi-Standard	Default
0	irst_multi_hard_synth_b_a	mode	Only. Used to Synthesizer Lane. Low Active.	1'b1
1	irst_multi_hard_txrx_l0_b_a	RW	Used in Multi-Standard mode Only. Used to tx/rx lane. Low Active.	1'b1

3.1.1.2 pd_ctrl

Register offset: 5'b00001

Register Description: Power down configuration

Bits	Name	R/W	Description Default	
0:1	ictl_multi_pstate_l0_	RW 00 : Wake Power State(P0), 01 : Doze Power State(P0s), 10 : Slumber Power State(P1), 11 : Coma Power State(P2), Individual Lane power down state. Config		2'b00
2	ipd_multi_synth_b	R W	Used in Multi-Standard mode Only. Individual Synthesizer Powerdown. Low Avtive. Config RW Used in Multi-	1'b1
3	ipd_multi_rx_l0_b	Standard	mode Only. Individual Receive Lane Powerdown. Low Active Config RW Used in Multi-Standard mode Only. Individual	1'b1
4	ipd_multi_tx_l0_b	Transmit	Lane Powerdown. Low Active. Config	1'b1

3.1.1.3 width_ctrl

Register offset: 5'b000010

Register Description: Bit Width Configuration

Bits	Name	R/W	Description	Default
0:2	ictl_multi_rxdatawidth_I0_	data word. Config	Defines the Receive 001...10 bits, 101...40 bits	pad_rx_width
3:5	ictl_multi_txdatawidth_I0_	RW	Defines the Transmit data word. Config 001...10bit, 101...40bit	pad_tx_width

3.1.1.4 rate_ctrl

Register offset: 5'b000011

Register Description: Rate Configuration

Bits	Name	R/W	Description	Default
0:2	ictl_multi_rxrate_I0_	receive	Selects the PMA data rate within a specific standard.	pad_rx_rate
3:5	ictl_multi_txrate_I0_	RW	Selects the PMA transmit data rate within a specific standard.	pad_tx_rate

3.1.1.5 idle_ctrl

Register offset: 5'b00100

Register Description: Idle Configuration

Bits	Name	R/W	Description	Default
0:3	idat_multi_txelecidle_I0_	TXWORD	Each bit controls 10 bits. 1..forced Idle.	4'h0

3.1.1.6 serdes_ctrl

Register offset: 5'b00101

Register Description: serdes configuration

Bits	Name	R/W	Description	Default
0	octl_multi_txdetectrxstat_I0_a	RO	Status, Transmit Receiver detection status signal. 1..detected. doc 2.6.6	1'b0
1	octl_multi_txdetectrxack_I0_a	RO	Status, Transmit Receiver detection acknowledge signal. doc 2.6.6	1'b0
2	ictl_multi_txdetectrxreq_I0_a	Transmit	Receiver detection request signal. doc 2.6.6 Beacon enable input	1'b0
	ictl_multi_txbeacon_I0_a	signal.		1'b0
3	ictl_multi_txamp_I0_	RW	Transmit Amplitude control signal.	3'b111
4:6 7	ictl_multi_txamp_en_I0	RW	Enables ICTL_MULTI_TxAMP_L0_ for transmit driver amplitude control.	1'b0
	ictl_multi_txswing_I0	RW	Used to PCIe gen1/gen2 only. 1'b0	
8 9:11	ictl_multi_txmargin_I0	RW	Select for transmitter driver swing voltage. 3'h0	

12:29	ictl_multi_txdeemph_l0_	RW	Select transmitter de-emphasis. Doc 2.6.9 to 2.6.13 for details.	18'h1
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3.1.1.7 rx_ctrl

Register offset: 5'b00110

Register Description: rx path configuration

Bits	Name	R/W	Description	Default
	octl_multi_rxcdrlck2data_l0_a RO		CDR Lock to Data Status indicator.	1'b0
	octl_multi_rxsignaldetect_l0_a RO		Data Detection Status Signal.	1'b0
0 1 2	ictl_multi_andme_en_l0_a	RW	Enables Differential Manchester Encoding mode in receiver for Ethernet link training. Config.	1'b0

3.1.1.8 rx_eq_ctrl

Register offset: 5'b01000: 5'b01001

Register Description: rx equalization correction configuration

Offset Bits	Name	R/W	Description	Default
0 0:2	ictl_multi_rxeq_precal_code_sel_l0_nt_RW	0 3	ictl_multi_rxeq_start_l0_a Cfg doc 2.2.11.1 Cfg	3'h0
		RW	doc 2.2.11.1 Status	1'b0
4:17	odat_multi_rxeq_best_eye_val_l0_a_RO	0	doc 2.2.11.1 Status doc	14'h0
0 octl_multi_rxeq_done_l0_a 0	ictl_multi_rxeq_en_l0	RO	2.2.11.1 Cfg doc 2.2.11.1	1'b0
19		RW	Cfg doc 2.2.11.1 Cfg	1'b0
0 ictl_multi_rxeq_0_l		RW	doc 2.2.11.1	1'b0
1 ictl_multi_rxeq_0_h		R W		32'h0

3.1.1.9 eye_diag_ctrl

Register offset: 5'b01010

Register Description: Eye Diagram Configuration

Bits	Name	R/W	Description	Default
	octl_multi_rxeyediag_err_l0_a	RO	Status doc 2.2.11.2	1'b0
0	octl_multi_rxeyediag_stat_l0_a_RO		Status doc 2.2.11.2	14'h0
	octl_multi_rxeyediag_done_l0_a RO		Status doc 2.2.11.2 Cfg	1'b0
1:14 15 16	ictl_multi_rxeyediag_start_l0_a RW		doc 2.2.11.2	1'b0

3.1.1.10 rd_status

Register offset: 5'b01011

Register Description: serdes status

Bits	Name	R/W	Description	Default
	octl_multi_synthstatus_a	RO	Synth state transition status.	1'b0
0 1	octl_multi_synthready_a	RO	Synth Ready Status Signal	1'b0

2	octl_multi_rxstatus_l0_a	RO	Receive Lane State Transition Status.	1'b0
3	octl_multi_rxready_l0_a	RO	Receive Lane Ready Status Signal.	1'b0
4	octl_pma_txstatus_l0_a	RO	Transmit Lane State Transition Status.	1'b0
5	octl_multi_txready_l0_a	RO	Transmit Lane Ready Status Signal.	1'b0

3.1.2 gphy_reg

The gphy_reg register module contains 6 registers, as shown in the following table:

Register Offset	Register Name	Description
5'b0_0000	mode_ctrl	Mode Configuration
5'b0_0001	fiber_en	Fiber mode enabled
5'b0_1010	pd_ctrl	Power down configuration
5'b0_1011	reset_ctrl	Reset Configuration
5'b0_1100	gphy_alm	Gephy alarm indication
5'b0_1101	adpt_alm	adapt alarm indication

3.1.2.1 mode_ctrl

Register offset: 5'b0_0000

Register Description: Mode Configuration

Bits	Name	R/W	Description	Default
0:3	pi_port_en		intended to be active.	4'b1111
4:5	pi_common_reg_sel RW		Common module register select signal. 00 : common register setting comes from port0, 01 : from port1, 10 : from port2, 11 :from port3.	2'b00
6	pi_turbo_sim	R W	1 : Speed up the timer, 0 : Normal operation.(Please tie low in ASIC). operation	1'b0
7:9	pi_opmode_p0 RW		control mode for port 0~3, and only for internal use. 3'b000 : 100BASE-TX mode with auto-negotiation. 3'b001 : force 100BASE-TX mode bypass auto-negotiation. 3'b010 : force 10BASE-Te mode bypass auto-negotiation. 3'b011 : force 100BASE-FX mode.	3'b000
10:12	pi_opmode_p1 RW		operation control mode for port 0~3, and only for internal use. 3'b000 : 100BASE-TX mode with auto-negotiation. 3'b001 : force 100BASE-TX mode bypass auto-negotiation. 3'b010 : force 10BASE-Te mode bypass auto-negotiation. 3'b011 : force 100BASE-FX mode.	3'b000
13:15	pi_opmode_p2 RW		operation control mode for port 0~3, and only for internal use. 3'b000 : 100BASE-TX mode with auto-negotiation. 3'b001 : force 100BASE-TX mode bypass auto-negotiation. 3'b010 : force 10BASE-Te mode bypass auto-negotiation. 3'b011 : force 100BASE-FX mode.	3'b000
16:18	pi_opmode_p3 RW		operation control mode for port 0~3, and only for internal use. 3'b000 : 100BASE-TX mode with auto-negotiation. 3'b001 : force 100BASE-TX mode bypass auto-negotiation. 3'b010 : force 10BASE-Te mode bypass auto-negotiation. 3'b011 : force 100BASE-FX mode.	3'b000
19	auto_enable	RW	1: power on sequence auto_mode, 0: register mode 1'b1	
20:23	upi_rx2tx_lb_en RW		ephy loopback enable 4'h0	

24:25	i_pll_oob_refs RW		select the input clock frequency of I_ASICIN from 25MHz to 100MHz.	2'b00
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3.1.2.2 fiber_en

Register offset: 5'b0_0001

Register Description: Fiber Mode Enable

Bits	Name	R/W	Description	Default
0	pi_fiber_en_p3	R W	1 : force fiber mode (100BASE-FX) operation. 0: Normal operation. 1:	1'b0
1	pi_fiber_en_p2	R W	force fiber mode(100BASE-FX) operation. 0: Normal operation. 1:	1'b0
2	pi_fiber_en_p1	R W	force fiber mode(100BASE-FX) operation. 0: Normal operation. 1:	1'b0
3	pi_fiber_en_p0	R W	force fiber mode(100BASE-FX) operation. 0 : Normal operation.	1'b0

3.1.2.3 pd_ctrl

Register offset: 5'b0_1010

Register Description: Power down configuration

Bits	Name	R/W	Description	Default
0	pi_pwrndn_p0	IP,	Power down for the common part and port 0 ~ 3, active high.	1'b0
1	pi_pwrndn_p1	RW	Power down for the IP, including common part and port 0 ~ 3, active high.	1'b0
2	pi_pwrndn_p2	RW	Power down for the IP, including common part and port 0 ~ 3, active high.	1'b0
3	pi_pwrndn_p3	RW	Power down for the IP, including common part and port 0 ~ 3, active high.	1'b0
4	pi_pwrndn_all	RW	Power down for the IP, including common part and port 0 ~ 3, active high.	1'b0

3.1.2.4 reset_ctrl

Register offset: 5'b0_1011

Register Description: Reset Configuration

Bits	Name	R/W	Description	Default
0	pi_sys_resetn_p0	low.	1: PHY system works normally. 0 : PHY system reset.	1'b0
1	pi_sys_resetn_p1	RW	System reset, active low. 1: PHY system works normally. 0: PHY system reset.	1'b0
2	pi_sys_resetn_p2	RW	System reset, active low. 1: PHY system works normally. 0: PHY system reset.	1'b0
3	pi_sys_resetn_p3	RW	System reset, active low. 1: PHY system works normally. 0: PHY system reset.	1'b0

4	pi_pwr_resetn	RW	power-on reset. 1: Power is ready for operation. 0: Power is not ready for operation.	1'b0
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3.1.2.5 gephys_alm

Register offset: 5'b0_1100

Register Description: gephys alarm indication

Bits	Name	R/W	Description	Default
0	gephys_lane0_alm	RC	lane0 alm	1'b0
	gephys_lane0_alm_mask RW		lane0 mask	1'b0
1	gephys_lane1_alm	RC	lane1 alm	1'b0
2	gephys_lane1_alm_mask RW		lane1 mask	1'b0
3	gephys_lane2_alm	RC	lane2 alm	1'b0
4	gephys_lane2_alm_mask RW		lane2 mask	1'b0
5	gephys_lane3_alm	RC	lane3 alm	1'b0
6:7	gephys_lane3_alm_mask RW		lane3 mask	1'b0

3.1.2.6 adpt_alm

Register offset: 5'b0_1101

Register Description: adapt alarm indication

Bits	Name	R/W	Description	Default
0:3 upi_tx_fifo_empty_alm		RC	Tx empty alm	4'h0
4:7 upi_tx_fifo_empty_alm_mask RW	8:11		Tx empty mask	4'h0
upi_tx_fifo_full_alm		RC	Tx full alm	4'h0
12:15 upi_tx_fifo_full_alm_mask RW	16:19		Tx full mask	4'h0
upi_rx_fifo_empty_alm		RC	Rx empty alm	4'h0
20:23 upi_rx_fifo_empty_alm_mask RW	24:27		rx_empty mask	4'h0
upi_rx_fifo_full_alm		RC	Rx full alm	4'h0
28:31 upi_rx_fifo_full_alm_mask RW			Rx full mask	4'h0

3.2 PcsBlock

3.2.1 eth_fx100_reg

The eth_fx100_reg register module contains 7 registers, as shown in the following table:

Register Offset	Register Name	Description
4'b0000	reset_ctrl	Reset Configuration
4'b0001	mode_ctrl	Mode Configuration
4'b0010	cdr_ctrl	cdr configuration
4'b0011	adpt_alm	adapt alarm indication
4'b0100: 4'b0111	cdr_state	cdr status indication
4'b1000	rx_state	rx path status
4'b1011	rxerr_cnt	rxerr status count

3.2.1.1 reset_ctrl

Register offset: 4' b0000

Register Description: Reset Configuration

Bits	Name	R/W	Description rx	Default
0	upi_rx_rst_n	R W	reset, low effective	1'b1
1	upi_tx_rst_n	R W	tx reset, low effective	1'b1
2	upi_rx_reset_by_link RW		TBD	1'b1
3	upi_tx_reset_by_link RW		TBD	1'b1

3.2.1.2 mode_ctrl

Register offset: 4' b0001

Register Description: Mode Configuration

Bits	Name	R/W	Description	Default
0	upi_rx2tx_lb_en RW 1		loopback enable eee	1'b0
1	upi_eee_mode_rx RW 2		rx mode enable eee tx	1'b0
2	upi_eee_mode_tx RW 3:4		mode enable	1'b0
3	upi_speed_mode RW 5:7		00:auto.01:force fx100.10:force sgmii sgmii	top_speed_mode
4	fx100_threshold	R W	threshold, 000->95%, 001->90%, 010->85%, 011->80%, 100->75%, 101->70%, 110->65%, 111->60%	3'b011
5	period_unit RW fx100_state		count period unit, 0->10us, 10->100us	1'b0
6	RW auto_switich module current_state=fx100 state sgmii_state RW auto_switich module			1'b0
7	current_state=sgmii_state			1'b0

3.2.1.3 cdr_ctrl

Register offset: 4' b0010

Register Description: cdr configuration

Bits	Name	R/W	Description	Default
0:2	upi_samp_offset_ctr	R W	upi_samp_offset_ctr	3'd4
3:5	upi_cdr_lock_ctr	R W	upi_cdr_lock_ctr	3'd3

3.2.1.4 adpt_alm

Register offset: 4' b0011

Register Description: adapt alarm indication

Bits	Name	R/W	Description	Default
0	upi_tx_fifo_empty_alm	RC	empty alm	1'b0
1	upi_tx_fifo_empty_alm_mask RW		empty alm mask full	1'b0
2	upi_tx_fifo_full_alm	RC	alm full	1'b0
3	upi_tx_fifo_full_alm_mask RW		alm mask empty	1'b0
4	upi_rx_fifo_empty_alm	RC	alm	1'b0

5	upi_rx_fifo_empty_alm_mask RW		empty alm mask full	1'b0
6	upi_rx_fifo_full_alm	RC	alm full	1'b0
7	upi_rx_fifo_full_alm_mask RW		alm mask	1'b0

3.2.1.5 cdr_state

Register offset: 4'b0100: 4'b0111

Register Description: cdr status indication

Offset 0	Bits	Name	R/W	Description	Default
0	0:7 upi_step_cnt		RO		8'h0
0	8:15 upi_skip_cnt		RO	TBD	8'h0
0	16:23 upi_fix_cnt		RO	TBD	8'h0
1	24:31 upi_serdes_unlock_cnt RO 0:9			TBD	8'h0
	upi_cha_point_rec RO 10:12			TBD	10'h0
	upi_max_samp_loc_step RO 13:20			TBD	3'h0
	upi_cdr_unlock_cnt RO 21 rx_cdr_lock			TBD	8'h0
			RO	rx cdr lock	1'b0
1 1 1 2	0:29	upi_serdes_data_buf0 RO		upi_serdes_data_buf = {upi_serdes_data_buf1, upi_serdes_data_buf0}	30'h0
3	0:19	upi_serdes_data_buf1 RO		upi_serdes_data_buf = {upi_serdes_data_buf1, upi_serdes_data_buf0}	20'h0

3.2.1.6 rx_state

Register offset: 4' b1000

Register Description: rx channel status

Bits	Name	R/W	Description	Default
0:4	upi_rx_cs_dt	RO	TBD	5'h0
5:7	upi_shift_dt	RO	TBD	3'h0
	upi_rx_err_alm	RC	TBD	1'b0
8 9	upi_rx_err_alm_mask	R W	TBD	1'b1

3.2.1.7 rxerr_cnt

Register offset: 4' b1011

Register Description: rxerr status count

Bits	Name	R/W	Description	Default
0:31	upi_rx_err_cnt	RO	TBD	32'h0

3.2.2 eth_xsgmii_reg

The eth_xsgmii_reg register module contains 51 registers, as shown in the following table:

Register Offset	Register Name	Description
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6'b00_0000 6'b00_0001	reset_ctrl	Reset Configuration
6'b00_0010 6'b00_0011	mode_ctrl	Mode Configuration
6'b00_0100 6'b00_0101	an_ctrl	Auto-negotiation configuration
6'b00_0110 6'b00_0111	en_ctrl	Output Configuration
6'b00_1000 6'b00_1001	loop_ctrl	Loopback Configuration
6'b00_1010 6'b00_1011	tp_ctrl	Test mode configuration
6'b00_1100 6'b00_1101	lpi_ctrl	Energy Efficient Ethernet Configuration
6'b00_1110 6'b00_1111	rd_ctrl	Polarity Reversal Configuration
6'b01_0000 6'b01_0001	los_ctrl	los Configuration
6'b01_0010 6'b01_0011	err_cnt_ctrl	Error count configuration
6'b01_0100 6'b01_0101	an_cfg_0	Auto-negotiation configuration channel 0
6'b01_0110 6'b01_0111	an_cfg_1	Auto-negotiation configuration channel 1
6'b01_1000 6'b01_1001	an_cfg_2	Auto-negotiation configuration channel 2
6'b01_1010 6'b01_1011	an_cfg_3	Auto-negotiation configuration channel 3
6'b01_1100 6'b01_1101	an_cfg_4	Auto-negotiation configuration channel 4
6'b01_1110	an_cfg_5	Auto-negotiation configuration channel 5
6'b01_1111 6'b10_0000	an_cfg_6	Auto-negotiation configuration channel 6
6'b10_0001 6'b10_0010	an_cfg_7	Auto-negotiation configuration channel 7
6'b10_0011 6'b10_0100	an_tim_cfg	Link timer configuration
6'b10_0101 6'b10_0110	eee_ctrl	eee Configuration
6'b10_0111 6'b10_1000	tx_res_reg	Sleep Timer Configuration
6'b10_1001 6'b10_1010	rx_res_reg	Twr Timer Configuration
6'b10_1011 6'b10_1100	an_restart	Auto-negotiation restart configuration
6'b10_1101	sync_restart	Synchronous restart configuration
	init_ctrl	Initial configuration
	wkerr_cnt	wake error status count
	xdr_err_cnt_0	rx error counting channel 0
	xdr_err_cnt_1	rx error counting channel 1
	xdr_err_cnt_2	rx error counting channel 2
	xdr_err_cnt_3	rx error counting channel 3
	xdr_err_cnt_4	rx error counting channel 4
	xdr_err_cnt_5	rx error counting channel 5
	xdr_err_cnt_6	rx error count channel 6
	xdr_err_cnt_7	rx error counting channel 7
	remote_fault_alm	Remote fault alarm
	rxfifo_ovf_alm	rxfifo full indication
	rxfifo_unf_alm	rxfifo empty indication
	an37_status	Auto-negotiation completion status
	an_sgmii_status	Auto-negotiation field status
	rx_status	rx status
	lpi_status	Energy Efficient Ethernet Status
	adpt_tx_alm	adapt tx alarm
	adpt_rx_alm	adapt rx alarm
	adpt_thrd0	adapt threshold configuration 0 channel
	adpt_thrd1	adapt Threshold configuration 1 channel
	adpt_thrd2	adapt threshold configuration 2 channels

6'b10_1110	adpt_thrd3	adapt threshold configuration 3 channels
6'b10_1111	adpt_thrd4	adapt threshold configuration 4 channels
6'b11_0000	adpt_thrd5	adapt threshold configuration 5 channels
6'b11_0001	adpt_thrd6	adapt Threshold configuration 6 channels
6'b11_0010	adpt_thrd7	adapt Threshold configuration 7 channels
6'b11_0100:6'b11_0101	adpt_ctrl	adapt configuration

3.2.2.1 reset_ctrl

Register offset: 6' b00_0000

Register Description: Reset Configuration

Bits	Name	R/W	Description	Default
0	upi_eee_RST_N RW		EEE submodule soft reset, low effective	1'b1
1	upi_tx_RST_N RW		TX submodule soft reset, low effective	1'b1
2	upi_rx_RST_N RW		RX submodule soft reset, low effective	1'b1
3	upi_an_RST_N RW		AN submodule soft reset, low effective	1'b1

3.2.2.2 mode_ctrl

Register offset: 6' b00_0001

Register Description: Mode Configuration

Bits	Name	R/W	Description	Default
0	upi_8lanes_en RW		Number of lanes is 8 Enable, applicable to O-USGMII mode top_8lanes_en	
1	upi_4lanes_en	RW	Channel quantity is 4 Enabled, applicable to QSGMII and Q-USGMII model	top_4lanes_en
2	upi_mask_rd_error	R W	Polarity error shutdown enable, must be configured as 1 under QSGMII/USGMII	top_mask_rd_error
4:5	upi_pcs_mode	R W	PCS Mode: 2'b00: 1000BaseX 2'b01: Reserved 2'b10: SGMII 2'b11: QSGMII/USGMII	top_pcs_mode
6:8	sgmii_threshold	RW	sgmii threshold, 000->95%, 001->90%, 010->85%, 011->80%, 100->75%, 101->70%, 110->65%, 111->60%	3'h0
9:10	upi_force_duplex_mode	RW	00-> duplex info from config, 01->force full duplex, 10->force half duplex	2'b00

3.2.2.3 an_ctrl

Register offset: 6' b00_0010

Register Description: Auto-negotiation Configuration

Bits	Name	R/W	Description	Default

0:7	upi_an_enable RW		Auto-negotiation is turned on, and the auto-negotiation class is automatically selected according to the current mode Type: Only bit 0 can be configured in SGMII mode Only bits 3:0 can be configured in QSGMII/Q-USGMII mode	8'hff
8:15	upi_mac_auto_sw RW		Whether the MAC side is controlled by the auto-negotiation sent by the other end is only upi_tx_config_ctrl=1'b0 and Valid when upi_phy_mode_ctrl=1'b0 Only bit 0 can be configured in SGMII mode Only bits 3:0 can be configured in QSGMII/Q-USGMII mode	top_mac_auto_sw
16:23	upi_phy_mode_ctrl RW		Only complete auto-negotiation transmission and MAC side control based on input pins Only bit 0 can be configured in SGMII mode Only bits 3:0 can be configured in QSGMII/Q-USGMII mode	top_phy_mode_ctrl
24	upi_tx_config_ctrl RW		Force the other party to respond to our self-negotiation control upi_phy_mode_ctrl=1'b1 Control according to input upi_phy_mode_ctrl=1'b0 Control according to UPI configuration Only bit 0 can be configured in SGMII mode Only bits 3:0 can be configured in QSGMII/Q-USGMII mode	top_tx_config_ctrl

3.2.2.4 en_ctrl

Register offset: 6' b00_0011

Register Description: Output Configuration

Bits	Name	R/W	Description	Default
0	upi_rx_en	R W	RX enable, affects the pcs_rx_en_o output pin	1'b1
1	upi_tx_en	R W	TX enable, affecting the auto-negotiation of the pcs_tx_en_o	1'b1
2	upi_an_usgmii RW		output pin. The TxConfigReg format follows the protocol format: 0: SGMII/QSGMII 1: USGMII	top_an_usgmii

3.2.2.5 loop_ctrl

Register offset: 6' b00_0100

Register Description: Loopback Configuration

Bits	Name	R/W	Description	Default
0:7	upi_rx2tx_lb_en	R W	GMII port RX to TX loopback enable Only bit 0 can be configured in SGMII mode Only bits 3:0 can be configured in QSGMII/Q-USGMII mode	8'h00
8	upi_loopback_en RW		SerDes external loopback	1'b0

3.2.2.6 tp_ctrl

Register offset: 6' b00_0101

Register Description: Test Mode Configuration

Bits	Name	R/W	DescriptionTest	Default
0	upi_tx_test_mode RW		mode is enabled	1'b0

1	upi_mftp	R W	Mixed frequency test pattern enable	1'b0
2	upi_hftp	R W	High frequency test pattern enable	1'b0
3	upi_lftp	R W	Low frequency test pattern enable	1'b0

3.2.2.7 lpi_ctrl

Register offset: 6' b00_0110

Register Description: Energy Efficient Ethernet Configuration

Bits	Name	R/W	Description	Default
0	upi_lrx_en	R W	LPI RX Enable	1'b0
1	upi_ltx_en	R W	LPI TX Enable	1'b0
2	upi_lrx_rx_en_ctl RW		LPI RX Enable Control	1'b0
3	upi_ltx_tx_en_ctl RW		LPI TX Enable Control	1'b0
4	upi_lrx_quiet_en RW		LPI RX Silent Enable	1'b0
5	upi_ltx_quiet_en RW		LPI TX Silent Enable	1'b0
6	upi_trans_lpi_mode RW	Disable TX EEE state machine to jump to TX QUIET	Enable fast emulation	1'b0
7	upi_fast_sim	R W	mode clock stop	1'b0
8:11	upi_clkstop_cnt RW		count value	4'h8

3.2.2.8 rd_ctrl

Register offset: 6' b00_0111

Register Description: Polarity Inversion Configuration

Bits	Name	R/W	Description	Default
0	upi_rx_polarity_inv RW		RX polarity inversion enable	1'b0
1	upi_tx_polarity_inv RW		TX polarity inversion enable	1'b0

3.2.2.9 los_ctrl

Register offset: 6' b00_1000

Register Description: los Configuration

Bits	Name	R/W	Description	Default
0	upi_supress_eee_los_det RW		EEE LOS detection shutdown enable	1'b0
1	upi_supress_los_det	RW	LOS detection shutdown enable	1'b0

3.2.2.10 err_cnt_ctrl

Register offset: 6' b00_1001

Register Description: Error count configuration

Bits	Name	R/W	Description	Default
0:7	upi_err_cnt_en	R W	Error count enable Only bit 0 can be configured in SGMII mode	8'hff

			Only bits 3:0 can be configured in QSGMII/Q-USGMII mode	
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3.2.2.11 an_cfg_0

Register offset: 6' b00_1010

Register Description: Auto-negotiation configuration channel

Bits	Name	R/W	Description	Default
	upi_mii_an_fd_0	RW/RC	AN37 ConfigReg Full Duplex	1'b1
0 1	upi_mii_an_hd_0	R W	AN37 ConfigReg Half Duplex	1'b0
2:3	upi_mii_an_rf_0	R W	AN37 ConfigReg remote fault 00:No error 01:Off line 10: Link failure 11:AN error	2'h0
4:5	upi_mii_an_ps_0	R W	AN37 pause 00:No pause 01:Asymmetric Pause toward link partner 10:Symmetric Pause 11:both	2'h0
	upi_sgmii_link_sts_0	R W	AN SGMII/QSGMII/USGMII link_sts	1'b1
	upi_duplex_mode_cfg_0 RW AN	SGMII/QSGMII/USGMII duplex_mode		1'b1
	upi_lrx_clkstop_en_0	RW AN	SGMII/QSGMII/USGMII clk_stop_en	1'b1
6 7 8 9:10	upi_sgmii_link_speed_0 RW AN	SGMII/QSGMII/USGMII link_speed		2'b10

3.2.2.12 an_cfg_1

Register offset: 6' b00_1011

Register Description: Auto-negotiation configuration channel

Bits	Name	R/W	Description	Default
0	upi_mii_an_fd_1	RW/RC	AN37 ConfigReg Full Duplex Invalid configuration in SGMII mode	1'b1
1	upi_mii_an_hd_1	R W	AN37 ConfigReg Half Duplex Invalid configuration in SGMII mode	1'b0
2:3	upi_mii_an_rf_1	R W	AN37 ConfigReg remote fault 00:No error 01:Off line 10: Link failure 11:AN error Invalid configuration in SGMII mode	2'h0
4:5	upi_mii_an_ps_1	R W	AN37 pause 00:No pause 01:Asymmetric Pause toward link partner 10:Symmetric Pause 11:both Invalid configuration in SGMII mode	2'h0
6	upi_sgmii_link_sts_1	R W	AN SGMII/QSGMII/USGMII link_sts Invalid configuration in SGMII mode	1'b1
7	upi_duplex_mode_cfg_1 RW		AN SGMII/QSGMII/USGMII duplex_mode Invalid configuration in SGMII mode	1'b1

	upi_lrx_clkstop_en_1	RW AN	SGMII/QSGMII/USGMII clk_stop_en	1'b1
8:9:10	upi_sgmii_link_speed_1	RW AN	SGMII/QSGMII/USGMII link_speed	2'b10

3.2.2.13 an_cfg_2

Register offset: 6' b00_1100

Register Description: Auto-negotiation configuration channel

Bits	Name	R/W	Description	Default
0	upi_mii_an_fd_2	RW/RC	AN37 ConfigReg Full Duplex Invalid configuration in SGMII mode	1'b1
1	upi_mii_an_hd_2	R W	AN37 ConfigReg Half Duplex Invalid configuration in SGMII mode	1'b0
2:3	upi_mii_an_rf_2	R W	AN37 ConfigReg remote fault 00:No error 01:Off line 10: Link failure 11:AN error Invalid configuration in SGMII mode	2'h0
4:5	upi_mii_an_ps_2	R W	AN37 pause 00:No pause 01:Asymmetric Pause toward link partner 10:Symmetric Pause 11:both Invalid configuration in SGMII mode	2'h0
6	upi_sgmii_link_sts_2	R W	AN SGMII/QSGMII/USGMII link_sts Invalid configuration in SGMII mode	1'b1
7	upi_duplex_mode_cfg_2	RW	AN SGMII/QSGMII/USGMII duplex_mode Invalid configuration in SGMII mode	1'b1
	upi_lrx_clkstop_en_2	RW AN	SGMII/QSGMII/USGMII clk_stop_en	1'b1
8:9:10	upi_sgmii_link_speed_2	RW AN	SGMII/QSGMII/USGMII link_speed	2'b10

3.2.2.14 an_cfg_3

Register offset: 6' b00_1101

Register Description: Auto-negotiation configuration channel

Bits	Name	R/W	Description	Default
0	upi_mii_an_fd_3	RW/RC	AN37 ConfigReg Full Duplex Invalid configuration in SGMII mode	1'b1
1	upi_mii_an_hd_3	R W	AN37 ConfigReg Half Duplex Invalid configuration in SGMII mode	1'b0
2:3	upi_mii_an_rf_3	R W	AN37 ConfigReg remote fault 00:No error 01:Off line 10: Link failure 11:AN error Invalid configuration in SGMII mode	2'h0
4:5	upi_mii_an_ps_3	R W	AN37 pause 00:No pause 01:Asymmetric Pause toward link partner	2'h0

			10:Symmetric Pause 11:both Invalid configuration in SGMII mode	
6	upi_sgmii_link_sts_3	R W	AN SGMII/QSGMII/USGMII link_sts Invalid configuration in SGMII mode	1'b1
7	upi_duplex_mode_cfg_3	R W	AN SGMII/QSGMII/USGMII duplex_mode Invalid configuration in SGMII mode	1'b1
	upi_lrx_clkstop_en_3	RW AN	SGMII/QSGMII/USGMII clk_stop_en	1'b1
8:9:10	upi_sgmii_link_speed_3	RW AN	SGMII/QSGMII/USGMII link_speed	2'b10

3.2.2.15 an_cfg_4

Register offset: 6' b00_1110

Register Description: Auto-negotiation configuration channel

Bits	Name	R/W	Description	Default
0	upi_mii_an_fd_4	RW/RC	AN37 ConfigReg Full Duplex Invalid configuration in SGMII mode	1'b1
1	upi_mii_an_hd_4	R W	AN37 ConfigReg Half Duplex Invalid configuration in SGMII mode	1'b0
2:3	upi_mii_an_rf_4	R W	AN37 ConfigReg remote fault 00:No error 01:Off line 10: Link failure 11:AN error Invalid configuration in SGMII mode	2'h0
4:5	upi_mii_an_ps_4	R W	AN37 pause 00:No pause 01:Asymmetric Pause toward link partner 10:Symmetric Pause 11:both Invalid configuration in SGMII mode	2'h0
6	upi_sgmii_link_sts_4	R W	AN SGMII/QSGMII/USGMII link_sts Invalid configuration in SGMII mode	1'b1
7	upi_duplex_mode_cfg_4	R W	AN SGMII/QSGMII/USGMII duplex_mode Invalid configuration in SGMII mode	1'b1
	upi_lrx_clkstop_en_4	RW AN	SGMII/QSGMII/USGMII clk_stop_en	1'b1
8:9:10	upi_sgmii_link_speed_4	RW AN	SGMII/QSGMII/USGMII link_speed	2'b10

3.2.2.16 an_cfg_5

Register offset: 6' b00_1111

Register Description: Auto-negotiation configuration channel

Bits	Name	R/W	Description	Default
0	upi_mii_an_fd_5	RW/RC	AN37 ConfigReg Full Duplex Invalid configuration in SGMII mode	1'b1
1	upi_mii_an_hd_5	R W	AN37 ConfigReg Half Duplex Invalid configuration in SGMII mode	1'b0
2:3	upi_mii_an_rf_5	R W	AN37 ConfigReg remote fault	2'h0

			00:No error 01:Off line 10: Link failure 11:AN error Invalid configuration in SGMII mode	
4:5	upi_mii_an_ps_5	R W	AN37 pause 00:No pause 01:Asymmetric Pause toward link partner 10:Symmetric Pause 11:both Invalid configuration in SGMII mode	2'h0
6	upi_sgmii_link_sts_5	R W	AN SGMII/QSGMII/USGMII link_sts Invalid configuration in SGMII mode	1'b1
7	upi_duplex_mode_cfg_5 RW		AN SGMII/QSGMII/USGMII duplex_mode Invalid configuration in SGMII mode	1'b1
8 9:10	upi_lrx_clkstop_en_5 upi_sgmii_link_speed_5 RW AN	RW AN	SGMII/QSGMII/USGMII clk_stop_en SGMII/QSGMII/USGMII link_speed	1'b1 2'b10

3.2.2.17 an_cfg_6

Register offset: 6' b01_0000

Register Description: Auto-negotiation configuration channel

Bits	Name	R/W	Description	Default
0	upi_mii_an_fd_6	RW/RC	AN37 ConfigReg Full Duplex Invalid configuration in SGMII mode	1'b1
1	upi_mii_an_hd_6	R W	AN37 ConfigReg Half Duplex Invalid configuration in SGMII mode	1'b0
2:3	upi_mii_an_rf_6	R W	AN37 ConfigReg remote fault 00:No error 01:Off line 10: Link failure 11:AN error Invalid configuration in SGMII mode	2'h0
4:5	upi_mii_an_ps_6	R W	AN37 pause 00:No pause 01:Asymmetric Pause toward link partner 10:Symmetric Pause 11:both Invalid configuration in SGMII mode	2'h0
6	upi_sgmii_link_sts_6	R W	AN SGMII/QSGMII/USGMII link_sts Invalid configuration in SGMII mode	1'b1
7	upi_duplex_mode_cfg_6 RW		AN SGMII/QSGMII/USGMII duplex_mode Invalid configuration in SGMII mode	1'b1
8 9:10	upi_lrx_clkstop_en_6 upi_sgmii_link_speed_6 RW AN	RW AN	SGMII/QSGMII/USGMII clk_stop_en SGMII/QSGMII/USGMII link_speed	1'b1 2'b10

3.2.2.18 an_cfg_7

Register offset: 6' b01_0001

Register Description: Auto-negotiation configuration channel

Bits	Name	R/W	Description	Default
0	upi_mii_an_fd_7	RW/RC	AN37 ConfigReg Full Duplex Invalid configuration in SGMII mode	1'b1
1	upi_mii_an_hd_7	R W	AN37 ConfigReg Half Duplex Invalid configuration in SGMII mode	1'b0
2:3	upi_mii_an_rf_7	R W	AN37 ConfigReg remote fault 00:No error 01:Off line 10: Link failure 11:AN error Invalid configuration in SGMII mode	2'h0
4:5	upi_mii_an_ps_7	R W	AN37 pause 00:No pause 01:Asymmetric Pause toward link partner 10:Symmetric Pause 11:both Invalid configuration in SGMII mode	2'h0
6	upi_sgmii_link_sts_7	R W	AN SGMII/QSGMII/USGMII link_sts Invalid configuration in SGMII mode	1'b1
7	upi_duplex_mode_cfg_7	R W	AN SGMII/QSGMII/USGMII duplex_mode Invalid configuration in SGMII mode	1'b1
8:9:10	upi_lrx_clkstop_en_7	RW AN	\$GMII/QSGMII/USGMII clk_stop_en	1'b1
8:9:10	upi_sgmii_link_speed_7	RW AN	SGMII/QSGMII/USGMII link_speed	2'b10

3.2.2.19 an_tim_cfg

Register offset: 6' b01_0010

Register Description: Link timer configuration

Bits	Name	R/W	Description	Default
0:15	upi_an37_link_tim	RW/RC 16	Link Timer Register Configuration Values	16'h0000
upi_an37_tmr_ovr_ride	Link Timer value is configured using upi_an37_link_tim register	RW	1'b0	

3.2.2.20 eee_ctrl

Register offset: 6' b01_0011

Register Description: eee Configuration

Bits	Name	R/W	Description	Default
0:3	upi_lct_res_regs	RW/RC	clk_eee_i Clock cycle, default 100	4'h9
4	upi_sign_bit_regs	R W	plus or minus counts	1'b0

3.2.2.21 tx_res_reg

Register offset: 6' b01_0100

Register Description: Sleep Timer Configuration

Bits	Name	R/W	Description	Default
0:5	upi tsl_res_regs	RW/RC	Sleep Timer	6'h00

3.2.2.22 rx_res_reg

Register offset: 6' b01_0101

Register Description: Twr Timer configuration

Bits	Name	R/W	Description	Default
0:5	upi_rwr_res_regs	RW/RC	Twr Timer	6'h00
8:15	upi_100us_res_regs	R W	generates 100us ideal	8'h00

3.2.2.23 an_restart

Register offset: 6' b01_0110

Register Description: Auto-negotiation restart configuration

Bits	Name	R/W	Description an	Default
0:7	upi_an_restart	WO/W1C	Restart, write 1 to take effect	8'h00

3.2.2.24 sync_restart

Register offset: 6' b01_0111

Register Description: Synchronous Restart Configuration

Bits	Name	R/W	Description	Default
0:7	upi_restart_sync	WO/W1C	The receiving side is restarted synchronously, and the write takes effect	8'h00

3.2.2.25 init_ctrl

Register offset: 6' b01_1000

Register Description: Initialization Configuration

Bits	Name	R/W	Description	Default
0	upi_init_pls	WO/W1C	Init generates pulses, write takes effect	1'b0
1	upi_init_done	RO	Init completion indication	1'b0

3.2.2.26 wkerr_cnt

Register offset: 6' b01_1001

Register description: wake error status count

Bits	Name	R/W	Description	Default
0	upi_wkerr_cnt_rd	WO/W1C	wkerr_cnt Read enable, write	1'b0
16:31	upi_lrx_wkerr_cnt	RO	latch wkerr_cnt	16'h0

3.2.2.27 xdr_err_cnt_0

Register offset: 6' b01_1010

Register Description: rx error counting channel

Bits	Name	R/W	Description	Default
0	upi_err_cnt_rd_0	WO/W1C	XDR err_cnt Read enable, write latch	1'b0
16:23	upi_xdr_err_cnt_0	RO	XDR err_cnt	8'h00

3.2.2.28 xdr_err_cnt_1

Register offset: 6' b01_1011

Register Description: rx error counting channel

Bits	Name	R/W	Description	Default
0	upi_err_cnt_rd_1	WO/W1C	XDR err_cnt Read enable, write latch Invalid configuration in SGMII mode	1'b0
16:23	upi_xdr_err_cnt_1	RO	XDR err_cnt	8'h00

3.2.2.29 xdr_err_cnt_2

Register offset: 6' b01_1100

Register Description: rx error counting channel

Bits	Name	R/W	Description	Default
0	upi_err_cnt_rd_2	WO/W1C	XDR err_cnt Read enable, write latch Invalid configuration in SGMII mode	1'b0
16:23	upi_xdr_err_cnt_2	RO	XDR err_cnt	8'h00

3.2.2.30 xdr_err_cnt_3

Register offset: 6' b01_1101

Register Description: rx error counting channel

Bits	Name	R/W	Description	Default
0	upi_err_cnt_rd_3	WO/W1C	XDR err_cnt Read enable, write latch Invalid configuration in SGMII mode	1'b0
16:23	upi_xdr_err_cnt_3	RO	XDR err_cnt	8'h00

3.2.2.31 xdr_err_cnt_4

Register offset: 6' b01_1110

Register Description: rx error counting channel

Bits	Name	R/W	Description	Default
0	upi_err_cnt_rd_4	WO/W1C	XDR err_cnt Read enable, write latch Invalid configuration in SGMII mode	1'b0
16:23	upi_xdr_err_cnt_4	RO	XDR err_cnt	8'h00

3.2.2.32 xdr_err_cnt_5

Register offset: 6' b011111

Register Description: rx error counting channel

Bits	Name	R/W	Description	Default
0	upi_err_cnt_rd_5	WO/W1C	XDR err_cnt Read enable, write latch Invalid configuration in SGMII mode	1'b0
16:23	upi_xdr_err_cnt_5	RO	XDR err_cnt	8'h00

3.2.2.33 xdr_err_cnt_6

Register Description: rx error counting channel

Register offset: 6' b10_0000

Bits	Name	R/W	Description	Default
0	upi_err_cnt_rd_6	WO/W1C	XDR err_cnt Read enable, write latch Invalid configuration in SGMII mode	1'b0
16:23	upi_xdr_err_cnt_6	RO	XDR err_cnt	8'h00

3.2.2.34 xdr_err_cnt_7

Register offset: 6' b10_0001

Register Description: rx error counting channel

Bits	Name	R/W	Description	Default
0	upi_err_cnt_rd_7	WO/W1C	XDR err_cnt Read enable, write latch Invalid configuration in SGMII mode	1'b0
16:23	upi_xdr_err_cnt_7	RO	XDR err_cnt	8'h00

3.2.2.35 remote_fault_alm

Register offset: 6' b10_0010

Register Description: Remote Fault Alarm

Bits	Name	R/W	Description	Default
0	upi_remote_fault_alm	RC	remote fault alarm signal	1'b0
1	upi_remote_fault_int_mask	RW	remote fault int mask	1'b0

3.2.2.36 rxfifo_ovf_alm

Register offset: 6' b10_0011

Register Description: rxfifo full indication

Bits	Name	R/W	Description	Default
0:7	upi_rxfifo_ovf_alm	RC	RX FIFO overflow warning signal	8'h00

8:15	upi_rxfifo_ovf_int_mask RW		RX FIFO overflow int mask	8'h00
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3.2.2.37 rxfifo_unf_alm

Register offset: 6' b10_0100

Register Description: rxfifo empty indication

Bits	Name	R/W	Description	Default
0:7	upi_rxfifo_unf_alm	RC	RX FIFO underflow warning signal	8'h00
8:15	upi_rxfifo_unf_int_mask RW		RX FIFO underflow int mask	8'h00

3.2.2.38 an37_status

Register offset: 6' b10_0101

Register Description: Auto-negotiation completion status

Bits	Name	R/W	Description	Default
0:7	upi_an_completed	RO	AN37 Auto-negotiation completion indication	8'h00
8:15	upi_mii_duplex_mode	RO	AN37 Auto-negotiation half-duplex state	8'h00

3.2.2.39 an_sgmii_status

Register offset: 6' b10_0110

Register Description: Auto-Negotiation Field Status

Bits	Name	R/W	Description	Default
0:31	upi_an_sgmii_status	RO	SGMII/QSGMII/USGMII auto-negotiation status, every 4 Bit per channel: [3]:link_status [2:1]:link_speed [0]:link_mode	8'h00

3.2.2.40 rx_status

Register offset: 6' b10_0111

Register Description: rx Status

Bits	Name	R/W	Description	Default
0:3	upi_cdt_shift_value	RO	common shift value	4'h0
4	upi_rx_aligned	RO	RX aligned state	1'b0
5	upi_los	RO	PHY los status	1'b0
6	upi_phy_rdy	RO	PHY ready state	1'b0

3.2.2.41 lpi_status

Register offset: 6' b10_1000

Register Description: Energy Efficient Ethernet Status

Bits	Name	R/W	Description LPI	Default
0	upi_rxlpi_rcvd	RO	pattern received on the receive	1'b0
1	upi_txlpi_rcvd	RO	pathLPI pattern received on the transmit path	1'b0
2:4	upi_lrx_state	RO	LPI RX FSM Status	3'h0
5:6	upi_ltx_state	RO	LPI TX FSM Status	2'h0

3.2.2.42 adpt_tx_alm

Register offset: 6' b10_1001

Register description: adapt tx alarm

Bits	Name	R/W	Description tx	Default
0:7 upi_tx_fifo_empty_alm		RC	empty alm tx	8'h00
8:15 upi_tx_fifo_empty_alm_mask RW 16:23			empty alm mask tx full	8'h00
upi_tx_fifo_full_alm		RC	alm tx full	8'h00
24:31 upi_tx_fifo_full_alm_mask		R W	alm mask	8'h00

3.2.2.43 adpt_rx_alm

Register offset: 6' b10_1010

Register Description: adapt rx alarm

Bits	Name	R/W	Description rx	Default
0:7 upi_rx_fifo_empty_alm		RC	empty alm rx	8'h00
8:15 upi_rx_fifo_empty_alm_mask RW upi_rx_fifo_full_alm			empty alm mask rx full	8'h00
16:23		RC	alm rx full	8'h00
upi_rx_fifo_full_alm_mask RW 24:31			alm mask	8'h00

3.2.2.44 adpt_thrd_0

Register offset: 6' b10_1011

Register Description: adapt threshold configuration channel

Bits	Name	R/W	Description	Default
0:4	upi_rateadpt_thrd_l_0	R W	TBD	5'd4
8:12	upi_rateadpt_thrd_h_0	R W	TBD	5'd9

3.2.2.45 adpt_thrd_1

Register offset: 6'b10_1100

Register Description: adapt threshold configuration channel

Bits	Name	R/W	Description	Default
0:4	upi_rateadpt_thrd_l_1	R W	TBD	5'd4
8:12	upi_rateadpt_thrd_h_1	R W	TBD	5'd9

3.2.2.46 adpt_thrd_2

Register offset: 6' b10_1101

Register Description: adapt threshold configuration channel

Bits	Name	R/W	Description	Default
0:4	upi_rateadpt_thrd_l_2	R W	TBD	5'd4
8:12	upi_rateadpt_thrd_h_2	R W	TBD	5'd9

3.2.2.47 adpt_thrd_3

Register offset: 6' b10_1110

Register Description: adapt threshold configuration channel

Bits	Name	R/W	Description	Default
0:4	upi_rateadpt_thrd_l_3	R W	TBD	5'd4
8:12	upi_rateadpt_thrd_h_3	R W	TBD	5'd9

3.2.2.48 adpt_thrd_4

Register offset: 6' b10_1111

Register Description: adapt threshold configuration channel

Bits	Name	R/W	Description	Default
0:4	upi_rateadpt_thrd_l_4	R W	TBD	5'd4
8:12	upi_rateadpt_thrd_h_4	R W	TBD	5'd9

3.2.2.49 adpt_thrd_5

Register offset: 6' b11_0000

Register Description: adapt threshold configuration channel

Bits	Name	R/W	Description	Default
0:4	upi_rateadpt_thrd_l_5	R W	TBD	5'd4
8:12	upi_rateadpt_thrd_h_5	R W	TBD	5'd9

3.2.2.50 adpt_thrd_6

Register offset: 6' b11_0001

Register Description: adapt threshold configuration channel

Bits	Name	R/W	Description	Default
0:4	upi_rateadpt_thrd_l_6	R W	TBD	5'd4
8:12	upi_rateadpt_thrd_h_6	R W	TBD	5'd9

3.2.2.51 adpt_ctrl

Register offset: 6' b11_0010:6' b11_0011

Register Description: adapt configuration

Offset 0	Bits	Name	R/W	Description	Default
0	0:7	upi_tx_reset_by_link RW		TBD	8'hff
0	8:15	upi_rx_reset_by_speed RW		TBD	8'hff
0	16:23	upi_rx_reset_by_link RW		TBD	8'hff
1	24:31	upi_tx_reset_by_speed RW upi_crscol_sel		TBD	8'hff
	0:7		R W	TBD	8'h00

3.2.3 eth_xsbi_reg

The eth_xsbi_reg register module contains 18 registers, as shown in the following table:

Register Offset	Register Name	Description
5'b0_0000	reset_ctrl	Reset Configuration
5'b0_0001	en_ctrl	Output Enable Configuration
5'b0_0010	tx_func_cfg	tx function configuration
5'b0_0011	tx_tp_cfg	tx test configuration
5'b0_0100:5'b0_0111	tx_tp_param_cfg	tx test parameter configuration
5'b0_1000	rx_func_cfg	rx function configuration
5'b0_1001	rx_tp_cfg	rx test configuration
5'b0_1010	lpi_ctrl	Energy-saving configuration
5'b0_1011	tx_res_reg	tx timer configuration
5'b0_1100	rx_res_reg	rx timer configuration
5'b0_1101	wkerr_cnt	wake error status
5'b0_1110	init_ctrl	Initial configuration
5'b0_1111	err_cnt	Error Configuration
5'b1_0000	tpc_err_cnt	Testing Error Status
5'b1_0001	lpi_status	Energy Efficient Ethernet Status
5'b1_0010	rx_status	rx status
5'b1_0011	tx_alm	tx alarm status
5'b1_0100	rx_alm	rx alarm status

3.2.3.1 reset_ctrl

Register offset: 5'b0_0000

Register Description: Reset Configuration

Bits	Name	R/W	Description	Default
0	upi_eee_rst_n	R W	EEE submodule soft reset, low effective	1'b1
1	upi_tx_rst_n	R W	TX submodule soft reset, low effective	1'b1
2	upi_rx_rst_n	R W	RX submodule soft reset, low effective	1'b1
3	upi_logicrst_by_rdy RW		TBD	1'b1

3.2.3.2 en_ctrl

Register offset: 5'b0_0001

Register Description: Output Enable Configuration

Bits	Name	R/W	Description	Default
0	upi_rx_en	RW	RX enable, affects the pcs_rx_en_o output pin	1'b1
1	upi_tx_en	RW	TX enable, affects the pcs_tx_en_o output pin	1'b1

3.2.3.3 tx_func_cfg

Register offset: 5'b0_0010

Register description: tx function configuration

Bits	Name	R/W	Description	Control	Default
0	upi_pcctx_byp_slr	RW	TX input via SLR		1'b0
1	upi_pcctx_polarity_inv	RW	TX input polarity inversion enable		1'b0
2	upi_rx2tx_lb_en	RW	GMII port RX to TX loopback enable		1'b0

3.2.3.4 tx_tp_cfg

Register offset: 5'b0_0011

Register Description: tx test configuration

Bits	Name	R/W	Description	Test	Default
0	upi_pcctx_tp_en	RW	mode enabled	Pseudo-random	1'b0
1	upi_pcctx_pr_tp_sel	RW		random test mode	1'b0
2	upi_pcctx_sw_tp_sel	RW		enabled	1'b0
3	upi_pcctx_prbs31_tp_sel	RW		Square wave test mode enabled	1'b0
4	upi_pcctx_prbs9_tp_sel	RW		PRBS31 test mode enable	1'b0
				PRBS9 test mode enable	1'b0

3.2.3.5 tx_tp_param_cfg

Register offset: 5'b0_0100: 5'b0_0111

Register Description: tx test parameter configuration

Offset	Bits	Name	R/W	Description	Data	Default
0	0:2	upi_pcctx_pr_pat_ctrl	RW	Pseudo-random test control		3'h1
0	3:5	upi_pcctx_nval	RW	Continuous 0 and 1 Test mode		3'h0
0	6:31	upi_seeda_lo	RW	Scramble code seeda lower 26 bytes		26'h0
1	0:31	upi_seeda_hi	RW	Scramble code seeda upper 32 bytes		32'h0
2	0:31	upi_seedb_lo	RW	Scramble code seedb lower 32 bytes		32'h0
3	0:25	upi_seedb_hi	RW	Scramble code seedb upper 26 bytes		26'h0

3.2.3.6 rx_func_cfg

Register offset: 5'b0_1000

Register Description: rx function configuration

Bits	Name	R/W	DescriptionScrambling	Default
0	upi_pcsrx_byp_slr	R W	code pass-through enable	1'b0
1	upi_pcsrx_polarity_inv RW		RX input polarity inversion enable	1'b0
2	upi_supress_los_det RW		LOS detection shutdown enable	1'b0

3.2.3.7 rx_tp_cfg

Register offset: 5'b0_1001

Register Description: rx test configuration

Bits	Name	R/W	DescriptionTest	Default
0	upi_pcsrx_tp_en	R W	mode enabledPseudo-	1'b0
1	upi_pcsrx_pr_tp_sel	R W	random test mode	1'b0
2	upi_pcsrx_sw_tp_sel	R W	enabledSquare wave test mode enabled	1'b0
3	upi_pcsrx_prbs31_tp_sel RW		PRBS31 test mode enable	1'b0
4	upi_pcsrx_prbs9_tp_sel RW		PRBS9 test mode enable	1'b0

3.2.3.8 lpi_ctrl

Register offset: 5'b0_1010

Register Description: Energy Saving Configuration

Bits	Name	R/W	Description	Default
0	upi_lrx_en	R W	LPI RX Enable	1'b0
1	upi_ltx_en	R W	LPI TX Enable	1'b0
2	upi_lrx_rx_en_ctl RW		LPI RX Enable Control	1'b0
3	upi_ltx_tx_en_ctl RW		LPI TX Enable Control	1'b0
4	upi_lrx_quiet_en RW		LPI RX Silent Enable	1'b0
5	upi_ltx_quiet_en RW		LPI TX silent enable	1'b0
6	upi_slr_byp_en RW		scramble pass-	1'b0
7	upi_sign_bit_regs RW		through enable	1'b0
	upi_lrx_clkstop_en RW		add/subtract	1'b1
8:9:12	upi_lct_res_regs RW 4'h9		counts clk_stop_en clk_eee_i clock cycle, default 100	
13	upi_trans_lpi_mode RW D		isable TX EEE state machine to jump to TX QUIET Enable 1'b0	
14	upi_fast_sim	R W	Fast simulation	1'b0
15:18	upi_clkstop_cnt RW		mode clock stop count value	4'h8

3.2.3.9 tx_res_reg

Register offset: 5'b0_1011

Register Description: tx timer configuration

Bits	Name	R/W	Description	Default
0:1	upi_t1u_res_regs	RW/RC	T1u Timer	2'h0
2:7	upi tsl res regs	R W	Sleep Timer	6'h00
8:12	upi_tw1_res_regs	R W	Tw1 Timer	5'h0

3.2.3.10 rx_res_reg

Register offset: 5'b0_1100

Register Description: rx timer configuration

Bits	Name	R/W	Description	Default
0:7	upi_100us_res_regs	RW/RC	generates 100us ideal	8'h00
8:13	upi_rwr_res_regs	R W	Twr Timer	6'h00

3.2.3.11 wkerr_cnt

Register offset: 5'b0_1101

Register description: wake error status

Bits	Name	R/W	Description	Default
0	upi_wkerr_cnt_rd	RW/RC	wkerr_cnt Read enable, write	1'b0
16:31	upi_lrx_wkerr_cnt	RO	latch wkerr_cnt	16'h0

3.2.3.12 init_ctrl

Register offset: 5'b0_1110

Register Description: Initialization Configuration

Bits	Name	R/W	Description	Default
0	upi_init_pls	RW/RC	Init generates pulses, write takes effect	1'b0

3.2.3.13 err_cnt

Register offset: 5'b0_1111

Register description: error configuration

Bits	Name	R/W	Description	Default
0:7	upi_rdec_err_cnt	RO	rdec_err_cnt	8'h00
8:13	upi_berm_err_cnt	RO	berm_err_cnt	6'h0
14	upi_err_cnt_rd_pls	RW/RC	Read enable, write latch	1'b0

3.2.3.14 tpc_err_cnt

Register offset: 5'b1_0000

Register Description: Test Error Status

Bits	Name	R/W	Description	Default
0	upi_tpc_err_cnt_rd_pls	RW/RC	upi_tpc_err_cnt tpc_err_cnt Read enable, write	1'b0
16:31		RO	latch tpc_err_cnt	16'h0

3.2.3.15 lpi_status

Register offset: 5'b1_0001

Register Description: Energy Efficient Ethernet Status

Bits	Name	R/W	DescriptionLPI	Default
0	upi_rxlpi_rcvd	RO	pattern received on the receive	1'b0
1	upi_txlpi_rcvd	RO	pathLPI pattern received on the transmit path	1'b0
2:4	upi_lrx_state	RO	LPI RX FSM Status	3'h0
5:7	upi_ltx_state	RO	LPI TX FSM Status	3'h0

3.2.3.16 rx_status

Register offset: 5'b1_0010

Register Description: rx Status

Bits	Name	R/W	DescriptionReceive	Default
0	upi_bklk_lock	RO	LPI pattern received on the receive	1'b0
1	upi_pcsrc_aligned	RO	pathAlignment	1'b0
2	upi_berm_hiber	RO	statusEncoding	1'b0
3	upi_berm_hiber_lh	RO	statusEncoding latch status	1'b0
4	upi_phy_rdy	RO	PHY ready state	1'b0

3.2.3.17 tx_alm

Register offset: 5'b1_0011

Register description: tx alarm status

Bits	Name	R/W	Description tx	Default
0	upi_pcctx_fault_alm	RC	fault alarm signal	1'b0
	upi_pcctx_fault_int_mask	RW	tx_fault_int_mask	1'b0
1 2	upi_xgmii_inv_char_alm	RC	xgmii inv char alarm signal	1'b0
3	upi_xgmii_inv_char_int_mask	RW	xgmii inv char int mask xgmii	1'b0
4	upi_xgmii_inv_sp_alm	RC	inv sp alarm signal xgmii	1'b0
5	upi_xgmii_inv_sp_int_mask	RW	inv sp int mask xgmii inv	1'b0
6	upi_xgmii_inv_term_alm	RC	term alarm signal xgmii inv	1'b0
7	upi_xgmii_inv_term_int_mask	RW	term int mask	1'b0

3.2.3.18 rx_alm

Register offset: 5'b1_0100

Register Description: rx alarm status

Bits	Name	R/W	Description tx	Default
0	upi_los_alm	RC	fault alarm signal los	1'b0
	upi_los_int_mask	R W	int mask rx	1'b0
1 2	upi_pcsrcx_fault_alm	RC	fault alarm signal rx	1'b0
3	upi_pcsrcx_fault_int_mask RW		fault int mask	1'b0
4	upi_rxfifo_ovf_alm	RC	RX FIFO overflow warning signal	1'b0
5	upi_rxfifo_ovf_int_mask RW upi_rxfifo_unf_alm		RX FIFO overflow int mask	1'b0
6		RC	RX FIFO underflow warning signal	1'b0
7	upi_rxfifo_unf_int_mask RW		RX FIFO underflow int mask	1'b0

3.3 MacBlock

3.3.1 eth_top_reg

The eth_top_reg register module contains 9 registers and 1 storage register.

The register list is as follows:

Register Offset	Register Name	Description
7'b000_0000	cmac_sys_loop_en_cfg	Mac system side loopback register
7'b000_0001	cmac_line_loop_en_cfg	mac line side loopback register
7'b000_0010	cmac_RST_N	mac reset register
7'b000_0101	glb_clr_pls_int	Global Statistics Clear Register
7'b000_0110		Interrupt Register
7'b000_0111	pause_quanta_cfg	pause quanta frequency configuration register
7'b000_1000	slot_num_cfg	Slot number configuration register
7'b000_1010	ptp_ctrl	PTP function control register
7'b000_1011	lpi_us_cfg	Power Saving Microseconds Configuration Register

The storage register list is as follows:

Register Offset	Register Name	Description
7'b100_0000:7'b111_1111	chan_slot_srm	TBD

3.3.1.1 cmac_sys_loop_en_cfg

Register offset: 7'b000_0000

Register Description: mac system side loopback register

Bits	Name	R/W	Description	Default
0:29	upi_cmac_sys_loop_en_cfg	RW	Mac system side loopback: loopback from mactx to macrx, Loopback under clk_core, statistics are valid	30'h0

3.3.1.2 cmac_line_loop_en_cfg

Register offset: 7'b000_0001 Register

Register Description: mac line side loopback

Bits	Name	R/W	Description	Default
0:29	upi_cmac_line_loop_en_cfg	RW	Mac line side loopback: loopback from macrx to mactx, Loopback under clk_core, statistics are valid	30'h0

3.3.1.3 cmac_rst_n

Register offset: 7'b000_0010

Register Description: mac reset register

Bits	Name	R/W	Description	Default
0	upi_cmactx_fuci_rst_n	RW	Mactx register reset, low effective	1'h1
1	upi_cmactx_logic_rst_n	RW	Mactx logic reset, low effective	1'h1
2	upi_cmacrx_fuci_rst_n	RW	Macrx register reset, low effective	1'h1
3	upi_cmacrx_logic_rst_n	RW	Logic reset of Macrx, low effective	1'h1

3.3.1.4 glb_clr_pls

Register offset: 7'b000_0101

Register Description: Global Statistics Clear Register

Bits	Name	R/W	Description	Default
0	upi_global_cnt_clr	WO/W1C	Global register clear signal	1'b0

3.3.1.5 int

Register offset: 7'b000_0110

Register Description: Interrupt Register

Bits	Name	R/W	Description	Default
0	upi_cmactx_int	RO	Mactx interrupt signal	1'b0
1	upi_cmactx_int_mask	R W	Mactx interrupt mask signal	1'b0
2	upi_cmacrx_int	RO	Macrx interrupt signal	1'b0
3	upi_cmacrx_int_mask	R W	Macrx interrupt mask signal	1'b0

3.3.1.6 pause_quanta_cfg

Register offset: 7'b000_0111

Register Description: Pause quanta frequency configuration register

Bits	Name	R/W	Description	Default
0:4	upi_pause_quanta_cfg	RW	Description Supports 51.2ns time; Calculation method upi_pause_quanta_cfg =51.2ns/(1000/frequency) For example, when the main frequency is 300M, 51.2ns(512bit)/(1000/300M) 16 The main frequency is 200M, 51.2ns/(1000/200), and so on	upi_pause_- = quanta_init

3.3.1.7 slot_num_cfg

Register offset: 7'b000_1000

Register Description: Slot Quantity Configuration Register

Bits	Name	R/W	Description	Default
0:5 upi_slot_num_cfg	RW		Slot quantity configuration signal, 1=1 slot, 2=2slot, ...63=63slot, 0=64slot	upi_slot_num_init

3.3.1.8 ptp_ctrl

Register offset: 7'b000_1010

Register Description: PTP function control register

Bits	Name	R/W	Description	Default
0	upi_ptp_en	R W	Ptp function global enable: 1 = enable 0 = disable	1'b0
1	upi_ptp_mode	R W	Ptp mode: 1 = tc mode, 0 = bc mode	1'b0
2	upi_ipv4_chksum_en	RW	IPv4 packet checksum recalculation enable: 1 = recalculate; 0 = do not recalculate When the checksum in the received ptp packet is 0, this configuration is 1 to reset Calculate checksum. If this configuration is 0, it will not be recalculated. When recalculating, if the recalculated value is 0, replace it with all 1s	1'b0
3	upi_ipv6_chksum_en	RW	IPv6 packet checksum recalculation enable: 1 = recalculate; 0 = do not recalculate When the checksum in the received ptp packet is 0, this configuration is 1 to reset Calculate checksum. If this configuration is 0, it will not be recalculated. When recalculating, if the recalculated value is 0, replace it with all 1s when configure 0 (doncare) : checksum of pkt of incomeing == 0 , the checksum don't recalculate when configure 1(care) : checksum of pkt of incomeing ==0 the checksum recal,if recal chusum=0,replace all 1	1'b0
4:16	upi_half_backpressure_cnt	RW	Half-duplex back pressure release parameter: When the back pressure is enabled, it is greater than this The parameter value is set to release the back pressure function every unit time, and no more blocking frames are sent.	13'd4103

3.3.1.9 lpi_us_cfg

Register offset: 7'b000_1011

Register Description: Power Saving Microsecond Configuration Register

Bits	Name	R/W	Description	Default
0:8	upi_lpi_us_cfg	RW	configuration value is only 1us time	upi_lpi_us_init

3.3.1.10 chan_slot_srm

Storage register description: Channel slot configuration storage register, NumOfEntries is 64, words is 1.

Bits	Name	R/W	Description
0:4	chan_slot	RW	Channel Number

3.3.2 eth_cmacrx_reg

The eth_cmacrx_reg register module contains 6 registers and 15 storage registers.

The register list is as follows:

Register Offset	Register Name	Description
12'b0000_0000_0000:12'b0000_0001_1101	rx_port_ctrl_cfg[30]	macrx control register
12'b0000_0010_0000	sta_channel_clr_num	Statistics registers clear channel by channel Number Register
12'b0000_0010_0001	sta_glb_clr_pls	Statistics register clear register
12'b0000_0010_0010	sta_clr_done	Statistics counter clearing completion status Memory
12'b0000_0010_0011	port_int	Port Interrupt Register
12'b0000_0100_0000:12'b0000_0101_1101 Note: Each	port_alm[30]	Port Alarm Register

register list contains 30 identical registers, that is, the register word value, register threshold, etc. are the same.

The storage register list is as follows:

Register Offset	Register Name	Description
12'b0000_1100_0000:12'b0000_1101_1101	undersize_cfg_srm	minimum frame length configuration register
12'b0000_1110_0000:12'b0000_1111_1101	mtu_frame_cfg_srm	Maximum frame length configuration register
12'b0001_0000_0000:12'b0001_0001_1101	vlan_tag_cfg_0_srm	vlan_tag domain configuration register
12'b0001_0010_0000:12'b0000_0011_1101	vlan_tag_cfg_1_srm	vlan_tag domain configuration register
12'b0001_0100_0000:12'b0001_0101_1101	vlan_tag_cfg_2_srm	vlan_tag domain configuration register
12'b0001_0110_0000:12'b0001_0111_1101	vlan_tag_cfg_3_srm	vlan_tag domain configuration register
12'b0001_1000_0000:12'b0001_1001_1101	vlan1_tag_cfg_0_srm	domain configuration register
12'b0001_1100_0000:12'b0001_1111_1101	total_frame_cnt_srm	Total frame statistics register
12'b0010_0000_0000:12'b0010_0011_1101	total_bytes_cnt_srm	Total bytes statistics register
12'b0010_1000_0000:12'b0010_1011_1011	control_frame_cnt_srm	Control frame number statistics register
12'b0011_0000_0000:12'b0011_0011_1011	pause_frame_cnt_srm	pause frame statistics register
12'b0100_0000_0000:12'b0100_1011_0011	good_frame_cnt_srm	Check the correct frame number statistics register
12'b0110_0000_0000:12'b0111_0010_1011	cast_frame_cnt_srm	cast frame number statistics register
	unusual_frame_cnt_srm	unusual frame count register
12'b1000_0000_0000:12'b1010_0101_0111	segment_frame_cnt_srm	Segment frame statistics storage Device

3.3.2.1 rx_port_ctrl_cfg[30]

Register offset: 12'b0000_0000_0000:12'b0000_0001_1101

Register Description: macrx control register

Note: Each register list contains 30 identical registers, that is, the register word value, register threshold, etc. are all the same.

Bits Name R/W			Description	Default
0	upi_rx_en_cfg	R W	Macrx receiving is enabled, statistics are closed when turned off, and cannot be turned off Generate any exception packet 1 = Enable 0 = Disable	1'b1

1	upi_err_flag_cfg	R W	The err flag at the end of the packet is enabled. When an overflow packet or an undershort packet is detected or When crc check error occurs, an err mark is displayed at the eop position, 1 = enable 0=Disable	1'b1
2	upi_crc_del_en_cfg RW		macrxcrc stripping enable	1'b0
3	upi_pause_en_cfg RW		pause enable, 1=enable 0=disable, configured as enable, macrx recognizes pause frames, otherwise it does not.	upi_pause_en_cfg_e_nable
4	upi_pause_del_cfg RW	macrx pause frame deletion enable, 1 = enable 0 = disable 1'b1		

3.3.2.2 sta_channel_clr_num

Register offset: 12'b0000_0010_0000

Register Description: Statistics register Clear channel number register by channel

Bits	Name	R/W	Description	Default
0:4	upi_sta_channel_clr_num RW		Statistics register by channel Clear channel number.	5'h0

3.3.2.3 sta_glb_clr_pls

Register offset: 12'b0000_0010_0001

Register Description: Statistics Register Clear Register

Bits	Name	R/W	Description	Default
0	upi_sta_glb_clr_pls	WO/W1C	Macrx All statistics counters are cleared	1'b0
1	upi_sta_channel_clr_pls	WO/W1C	Single channel clear indication: sta_channel_clr_num The corresponding statistics counter is cleared.	1'b0

3.3.2.4 sta_clr_done

Register offset: 12'b0000_0010_0010

Register Description: Statistics counter clearing completion status register

Bits	Name	R/W	Description	Default
0	upi_sta_clr_done RO		counter clearing completion indication, when reset or statistics clearing is enabled, The statistical counter starts to clear, and this signal is pulled high after the clearing is completed.	1'b0

3.3.2.5 port_int

Register offset: 12'b0000_0010_0011

Register Description: Port Interrupt Register

Bits	Name	R/W	Description	Default
0	upi_afifo_full_port_int	RO	Afifo full interrupt	1'h0
1	upi_afifo_full_port_int_mask RW		Afifo full interrupt mask	1'h0
2	upi_sop_mis_timer_port_int	RO	Sop_mis_timer interrupt	1'h0
3	upi_sop_mis_timer_port_int_mask RW		Sop_mis_timer interrupt mask	1'h0

3.3.2.6 port_alm[30]

Register offset: 12'b0000_0100_0000:12'b0000_0101_1101

Register Description: Port Alarm Register

Note: Each register list contains 30 identical registers, that is, the register word value, register threshold, etc. are all the same.

Bits	Name	R/W	Description	Default
0	upi_afifo_full_alm	RO	Asynchronous FIFO full warning signal across clock domains between PHY and MAC Number.	1'h0
1	upi_afifo_full_int_mask	RW	The interrupt	1'h0
2	upi_sop_mis_timer_alm	RO	mask header position is the interrupt mask of the time	1'h0
	upi_sop_mis_timer_int_mask	RW	stamp alarm signal	1'h0

3.3.2.7 undersize_cfg_srm

Storage register description: minimum frame length configuration register, NumOfEntries is 30, words is 1.

Bits	Name	R/W	Description
0:13	undersize_cfg	R W	Minimum frame length configuration, the default value is 0x40.

3.3.2.8 mtu_frame_cfg_srm

Storage register description: Maximum frame length configuration register, NumOfEntries is 30, words is 1.

Bits	Name	R/W	Description
0:13	mtu_frame_cfg	R W	The maximum frame length is configured, the default is 16000, when a single-layer VLAN is used, the maximum frame length =MTU+4, when double-layer VLAN, the maximum frame length = MTU+8, MTU+4/MTU+8 exceeds 16000, 16000 shall prevail, other frames are subject to the maximum frame Long = MTU, RAM depth is 30, each address corresponds to a mac channel.

3.3.2.9 vlan_tag_cfg_0_srm

Storage register description: vlan_tag domain configuration register, NumOfEntries is 30, words is 1.

Bits	Name	R/W	Description
0:15	vlan_tag_cfg_0	RW	vlan tag domain matches configuration item 0, each address represents a channel, the default value is 0x88a8.

3.3.2.10 vlan_tag_cfg_1_srm

Storage register description: vlan_tag domain configuration register, NumOfEntries is 30, words is 1.

Bits	Name	R/W	Description
0:15	vlan_tag_cfg_1	RW	The outer VLAN matches configuration item 1. Each address represents a channel. The default value is 0x88a8. When any one of vlan_tag_cfg_1/ vlan_tag_cfg_2/ vlan_tag_cfg_3/ vlan_tag_cfg_4 is matched, it is considered a match, and the same applies below.

3.3.2.11 vlan_tag_cfg_2_srm

Storage register description: vlan_tag domain configuration register, NumOfEntries is 30, words is 1.

Bits	Name	R/W	Description
0:15	vlan_tag_cfg_2	RW Outer VLAN	matching configuration item 2. Each address represents a channel. The default value is 0x88a8.

3.3.2.12 vlan_tag_cfg_3_srm

Storage register description: vlan_tag domain configuration register, NumOfEntries is 30, words is 1.

Bits	Name	R/W	Description
0:15	vlan_tag_cfg_3	RW Outer	vlan matches configuration item 3, each address represents a channel, the default value is 0x88a8.

3.3.2.13 vlan1_tag_cfg_0_srm

Storage register description: vlan_tag domain configuration register, NumOfEntries is 30, words is 1.

Bits	Name	R/W	Description
0:15	vlan1_tag_cfg_0	RW	Each address of memory vlan represents a channel, and the default value is 0x8100; when the received packet is Single-layer VLAN, any one of vlan_tag_cfg_1/ vlan_tag_cfg_2/ vlan_tag_cfg_3/ vlan_tag_cfg_4/ vlan1_tag_cfg_0 is considered a match; when receiving When the packet is a double-layer VLAN, the outer VLAN must match any one of vlan_tag_cfg_1/ vlan_tag_cfg_2/ vlan_tag_cfg_3/ vlan_tag_cfg_4, and the inner VLAN must match any one of vlan_tag_cfg_2/ vlan_tag_cfg_3/ vlan_tag_cfg_4. The layer vlan and vlan1_tag_cfg_0 must match to be considered a match.

3.3.2.14 total_frame_cnt_srm

Storage register description: Total frame count register, NumOfEntries is 30, words is 2.

Offset	Bits	Name	R/W	Description
0	0:31	total_frame_cnt0	RO	Total frame statistics, including control_frame and data_frame, total_frame_cnt[31:0], the default value is 0.
1	0:31	total_frame_cnt1	WO	total_frame_cnt[63:32]

3.3.2.15 total_bytes_cnt_srm

Storage register description: Total byte count register, NumOfEntries is 30, words is 2.

Offset	Bits	Name	R/W	Description
0	0:31	total_bytes_cnt0	RO	Total byte count, including control_frame and data_frame, total_bytes_cnt[31:0], the default value is 0x0.
1	0:31	total_bytes_cnt1	WO	total_bytes_cnt[63:32]

3.3.2.16 control_frame_cnt_srm

Storage register description: Control frame count register, NumOfEntries is 30, words is 2.

Offset	Bits	Name	R/W	Description
0	0:31	control_frame_cnt0	RO	Control frame statistics: frames with frame type 0x8808, control_frame_cnt[31:0], the default value is 0x0, including the pause frame.
1	0:31	control_frame_cnt1	WO	control_frame_cnt[64:32]

3.3.2.17 pause_frame_cnt_srm

Storage register description: Pause frame frame count register, NumOfEntries is 30, words is 2.

Offset Bits	0	Name	R/W	Description
	0:31	pause_frame_cnt0	RO	Pause frame statistics, pause_frame_cnt[31:0], the default value is 0x0.
1	0:31	pause_frame_cnt1 WO		pause_frame_cnt[63:32]

3.3.2.18 good_frame_cnt_srm

Storage register description: Check the correct frame count register, NumOfEntries is 30, words is 2.

Offset Bits		Name	R/W	Description
0	0:31	good_frame_cnt0 RO		Undersize <= packet length <= mtu and the CRC check is correct. good_frame_cnt[31:0], the default value is 0x0.
1	0:31	good_frame_cnt1 WO		good_frame_cnt[63:32]

3.3.2.19 cast_frame_cnt_srm

Storage register description: cast frame count register, NumOfEntries is 90, words is 2.

Offset Bits		Name	R/W	Description
0	0:31	cast_frame_cnt0 RO		0~29 Unicast packet statistics 30~59 Multicast packet statistics 60~89 Broadcast packet statistics Unicase + muticast + broadcast = good frame, excluding control frames cast_frame_cnt [31:0], the default value is 0x0.
1	0:31	cast_frame_cnt1 WO		cast_frame_cnt [63:32]

3.3.2.20 unusual_frame_cnt_srm

Storage register description: unusual frame number statistics register, NumOfEntries is 150, words is 2.

Offset Bits		Name	R/W	Description
0	0:31	unusual_frame_cnt0 RO		0~29 undersize frames (<undersize & crc_ok) 30~59 fragment frames (<undersize & crc_fail) 60~89oversize frames (>mtu & crc_ok) 90~119jabber frames (>mtu & crc_fail) 120~149 bad frames (undersize < <oversize & crc_fail) Contains data frames and control frames unusual_frame_cnt[31:0], the default value is 0x0
1	0:31	unusual_frame_cnt1 WO		unusual_frame_cnt[63:32]

3.3.2.21 segment_frame_cnt_srm

Storage register description: segment frame number statistics register, NumOfEntries is 300, words is 2.

Offset Bits		Name	R/W	Description
0	0:31	segment_frame_cnt0 RO		0~29: 64 bytes 30~59: 65-127 bytes

				60~89: 128-255 bytes 90~119: 256-511 bytes 120~149: 512-1023bytes 150~179 1024-1518bytes 180~209 1519-2047bytes 210~239 2048-4095bytes 240~269 4096-9215bytes 270-299: 9216-MTU bytes The sum of all the above = total frame segment_frame_cnt [31:0], the default value is 0x0
1	0:31 segment_frame_cnt1 WO			segment_frame_cnt [63:32]

3.3.3 eth_cmactx_reg

The eth_cmactx_reg register module contains 14 registers and 19 storage registers.

The register list is as follows:

Register Offset	Register Name	Description
12'b0000_0000_0000:12'b0000_0001_1101 tx_port_ctrl0_cfg[30] Note: 12'b0000_0010_0000		mactx control register
:12'b0000_0011_1101 tx_port_ctrl1_cfg[30] Note12'b0000_0100_0000 12'b0000_0100_0001		mactx control register
12'b0000_0100_0110	sta_channel_clr_num	Statistics counter clear configuration register per channel
12'b0000_0100_0111	fc_off_pls	pause Stop frame sending configuration register
	sta_clr_done	Statistics counter clearing completion register
	port_int	Port Interrupt Aggregation Register
12'b0000_0110_0000:12'b0000_0111_1101 12'b0000_0100_0010	port_alm[30] note	Port Alarm Interrupt Register
	sta_glb_clr_pls	Statistics counter clear register
12'b1100_1100_0000:12'b1100_1101_1101 timer_ts_ns_cmp[30] Note		ns Compensation Register
12'b1101_0000_0000:12'b1101_0001_1101 timer_cf_fns_cmp[30] Note		fns compensation register
12'b1101_1000_0000 sw_start_pls 12'b1101_1000_0001 sw_end_pls		Power saving start configuration register
lpi_time[30] Note 12'b1101_1010_0000:12'b1101_1011_1101		Power saving end configuration register
12'b1101_1100_0000:12'b1101_1100_0111 debug_status		Energy saving duration configuration register
		Debug Dedicated Registers
Note: Each register list contains 30 identical registers, that is, the register word value, register threshold, etc. are all the same.		

The storage register list is as follows:

Register Offset	Register Name	Description
12'b1101_0100_0000:12'b1101_0101_1101	undersize_cfg_srm	Minimum frame length configuration register
12'b0000_1000_0000:12'b0000_1001_1101 mtu_frame_cfg_srm		Maximum frame length configuration register
12'b0000_1010_0000:12'b0000_1011_1101 pause_time_srm 12'b0000_1100_0000:12'b0000_1101_1101		pause frame count configuration register
pause_time_vec_srm 12'b0001_0000_0000:12'b0001_0001_1101	vlan_tag_cfg_0_srm	pause Send time interval register
12'b0001_0010_0000:12'b0001_0011_1101 vlan_tag_cfg_1_srm		vlan tag domain match configuration item register
12'b0001_0100_0000:12'b0001_0101_1101 vlan_tag_cfg_2_srm		vlan tag domain match configuration item register
12'b0001_0110_0000:12'b0001_0111_1101 vlan_tag_cfg_3_srm		vlan tag domain match configuration item register
12'b0001_1000_0000:12'b0001_1001_1101 vlan1_tag_cfg_0_srm		vlan tag domain match configuration item register
12'b0001_1100_0000:12'b0001_1111_1011 total_frame_cnt_srm	12'b0010_0000_0000:12'b0010_0011_1011	total frame statistics register
total_bytes_cnt_srm		Total Bytes Statistics Register

12'b0010_0100_0000:12'b0010_0111_1011 control_frame_cnt_srm	Control frame number statistics register	
12'b0010_1000_0000:12'b0010_1011_1011 pause_frame_cnt_srm	good frame number statistics	pause frame frame count register
12'b0010_1100_0000:12'b0010_1111_1011 good_frame_cnt_srm	cast frame number statistics	register
12'b0011_0000_0000:12'b0011_1011_0011 cast_frame_cnt_srm	unusual Frame count statistics	register
12'b0100_0000_0000:12'b0100_1011_0011 unusual_frame_cnt_srm		register
12'b1000_0000_0000:12'b1010_0101_0111 segment_frame_cnt_srm	Segment frame statistics register	
12'b1100_0100_0000:12'b1100_0111_1011 ptp timestamp	pause_sa_srm	pause frame sa configuration register
12'b1100_1000_0000:12'b1100_1011_1011 register	ptp_int_time_ts_srm	

3.3.3.1 tx_port_ctrl0_cfg[30]

Register offset: 12'b0000_0000_0000:12'b0000_0001_1101

Register Description: mactx control register

Note: Each register list contains 30 identical registers, that is, the register word value, register threshold, etc. are all the same.

Bits	Name	R/W	Description	RW	Macrx Receive enable, statistics count is closed when turned	Default
0	upi_tx_en_cfg		off,		Cannot generate any abnormal packets, 1 = enable 0 = disable	1'b1
1	upi_err_flag_cfg		RW	The err flag is enabled at the end of the packet. When an overlong or undershort packet is detected	When the err flag is set at the eop position, 1 = enable 0 = disable	1'b0
2	upi_crc_ctrl_add	RW	crc enable add, add crc and recalculate, 1=enable, 0=Disable			1'b0
3	upi_crc_ctrl_recal	R W	CRC recalculation enable, 1 = enable, 0 = disable	1'b1		
4	upi_fc_cfg	RW	Send pause frame enable, 1 = enable, 0 = disable	1'b0		
5:6	upi_fc_ctrl_cfg	RW	Pause Control: 2'b00: Disable the pause function 2'b01: Whether to send pause is determined by the system side instruction 2'b11: Whether to send pause is determined by upi_fc_cfg		upi_fc_ctrl_cfg_enable	
7	upi_pad_ctrl_cfg	RW	Mactx fill enable: Packets less than 64 bytes are filled to 64 bytes Section, 1 = fill 0 = do not fill			1'b1
8:12	upi_port_fifo_threshold	RW	The read threshold of the fifo receiving system data. sop and the number of bytes cached is greater than or equal to this setting value, open Start reading data from the cache; the fifo depth is 32, this value is set The setting must be between 0 and upi_port_afull_gap			5'hc
13:17	upi_port_fifo_afull_gap	RW	The fifo receiving system data is almost full. The number of bytes cached in the buffer is greater than or equal to this setting value, giving the next level Back pressure signal, fifo depth is 32, this value setting range is 0~24			5'h18
18:21	upi_ipg_value	RW/ WC	xgmii mode: average ipg 'd1=8 'd2=9 ...'d7=14, the maximum is 'd7; if configure 'd0 or >'d7, equal to minimum ipg gmii_mode : only configure 4'd4~4'd13, configure 0~3 or >13, equal to 'd11			4'h0
twenty two	upi_egress_fifo_restart_en_cfg	RW	Receive system side data fifo restart enable. 1=fifo restart 0=Do not			1'b0
twenty three	upi_lpi_hw_en	restart	RW Energy Efficient Ethernet Hardware Enable 1=Enable 0=Disable			1'b0
twenty four	upi_lpi_sw_en	RW	Energy Efficient Ethernet software enable 1 = Enable 0 = Disable			1'b0

25	upi_half_duplex_drop_en	RW	is used for testing and debugging. Users cannot configure it at will. Half-duplex The discard enable, whether to discard when it is greater than the number of retransmissions 1 = discard Discard 0 = Do not discard	1'h0
26	upi_full_duplex_debug_cfg_en	RW	Test debug use, users cannot configure it at will, 1=full/ Half-duplex indication takes upi_full_duplex_debug_cfg 0= Full/half duplex indication to get PCS connection signal	1'b0
27	upi_full_duplex_debug_cfg	RW	is used for test and debug, and cannot be configured arbitrarily by the user. 1 = full double Mode 0 = half duplex	1'h0

3.3.3.2 tx_port_ctrl1_cfg[30]

Register offset: 12'b0000_0010_0000:12'b0000_0011_1101

Register Description: mactx control register

Note: Each register list contains 30 identical registers, that is, the register word value, register threshold, etc. are all the same.

Bits	R/W	Description	RW	Name	Value	Default
0:6		upi_bussw_afull_gap			Almost full threshold, RAM cache per channel is 128 deep Degree, 32bits bit width, this value setting range is 64~127	7'h40
8:14		upi_bussw_rd_threshold	RW		debug use, users cannot arbitrarily configure: ram array package The tail is written to the idle watermark. When it is less than this watermark, it is written to the cache. idle, to ensure that the packet tail can be read normally, this value cannot be set Too large. Too large will result in insufficient bandwidth.	7'd9
16:26		upi_port_ptp_en	RW/ WC		Timestamp Enable 1 = Enable 0 = Disable Corresponding to the following frame formats respectively [10:0] = {sync to follow up, management,signalling,announce,pdelay resp follow up,delay resp,follow up,pdelay resp, pdelay req, delay req, sync} sync to follow up: The timestamp of the follow up frame is replaced by the previous A sync timestamp replacement	11'h4ff
27	RW	upi_port_ptp_step_mode			1 = double step mode 0 = single step mode	1'h0
28:31		upi_max_retry	RW/ WC		Half-duplex collision retransmission times	4'hd

3.3.3.3 sta_channel_clr_num

Register offset: 12'b0000_0100_0000

Register Description: Statistics Counter Per Channel Clear Configuration Register

Bits	Name	R/W	Description	Default
0:4	upi_sta_channel_clr_num	RW	When clearing statistics counters by channel, the corresponding port channel number 5'h0	5'h0

3.3.3.4 fc_off_pls

Register offset: 12'b0000_0100_0001

Register Description: pause stop frame sending configuration register

Bits	Name	R/W	Description	Default
0:29	upi_fc_off_pls	WO/W1C pause	stop frame indication, 1 = send a pause Stop Frame	1'b0

3.3.3.5 sta_clr_done

Register offset: 12'b0000_0100_0110

Register Description: Statistics counter clearing completion register

Bits	Name	R/W	Description	Default
0	upi_sta_clr_done	RO	counter clearing completion indication	1'b0
1:30	upi_lpi_sleep_status	RO	Mac energy saving status indicator	1'b0

3.3.3.6 port_int

Register offset: 12'b0000_0100_0111

Register Description: Port Interrupt Aggregation Register

Bits	Name	R/W	Description	Default
0	upi_egress_fifo_full_port_int	RO	System-side cache fifo full alarm signal	1'b0
1	upi_egress_fifo_full_port_int_mask	RW	interrupt mask	1'b0
2	upi_frame_afifo_full_port_int	RO	Pcs side asynchronous FIFO full alarm signal	1'b0
3	upi_frame_afifo_full_port_int_mask	RW	interrupt mask 1'b0	
4	upi_tx_data_missop_port_int	RO	Phy clock receives no sop packet alarm signal 1'b0	
5	upi_tx_data_missop_port_int_mask	RW	Interrupt mask 1'b0	
6	upi_tx_data_miseop_port_int	RO	PHY clock receives no eop warning signal 1'b0	
7	upi_tx_data_miseop_port_int_mask	RW	Interrupt mask 1'b0	
8	upi_tx_bus_dic_port_int	RO	Traffic underload alarm signal	1'b0
9	upi_tx_bus_dic_port_int_mask	RW	interruption	1'b0
10	upi_singlecollision_port_int	RO	mask Single collision alarm	1'b0
11	upi_singlecollision_port_int_mask	RW	signal	1'b0
12	upi_excessivecollision_port_int	RO	interruption mask Collision to maximum	1'b0
upi_excessivecollision_port_int	mask		number of	1'b0
14	upi_multiplecollision_port_int	RO	alarm signal interruption mask	1'b0
15	upi_multiplecollision_port_int_mask	RW	Multiple collision alarm signal interruption mask	1'b0
16	upi_ptp_port_int	RO	Ptp sync frame warning alarm	1'b0
17	upi_ptp_port_int_mask	RW	signal	1'b0
18	upi_tx_data_ipg_port_int	RO	interrupt mask 10g mode: xgmii ipg less than 5 alarm 1 mode: SFIFO_FULL alarm signal	1'b0
19	upi_tx_data_ipg_port_int_mask	RW	interrupt mask	1'b0
20	upi_sop_mis_timer_port_int	RO	No timestamp alarm signal was collected at Sop	1'b0
upi_sop_mis_timer_port_int	mask		Interrupt Mask	1'b0
upi_half_fifo_full_port_int	RO		Half-duplex fallback fifo full alarm signal	1'b0
upi_half_fifo_full_port_int	mask		interrupt mask	1'b0

3.3.3.7 port_alm[30]

Register offset: 12'b0000_0110_0000:12'b0000_0111_1101

Register Description: Port Alarm Interrupt Register

Note: Each register list contains 30 identical registers, that is, the register word value, register threshold, etc. are all the same.

Bits	Name	R/W	DescriptionSystem	Default
0	upi_egress_fifo_full_alm	RO	-side cache fifo full alarm signal	1'b0
1	upi_egress_fifo_full_int_mask RW		interrupt mask	1'b0
2	upi_frame_afifo_full_alm	RO	Pcs side asynchronous FIFO full alarm signal	1'b0
3	upi_frame_afifo_full_int_mask RW		interrupt mask 1'b0	
4	upi_tx_data_missop_alm	RO	Phy clock receives no sop packet alarm signal 1'b0	
5	upi_tx_data_missop_int_mask RW		Interrupt mask 1'b0	
6	upi_tx_data_miseop_alm	RO	PHY clock receives no eop warning signal 1'b0	
7	upi_tx_data_miseop_int_mask RW		Interrupt mask 1'b0	
8	upi_tx_bus_dic_alm	RO	Traffic underload alarm signal	1'b0
9	upi_tx_bus_dic_int_mask	R W	interruption mask	1'b0
10	upi_tx_data_ipg_alm	RO	10g mode: xgmii ipg is less than 5 alarm signal 1 mode: SFIFO_FULL alarm signal	1'b0
11	upi_tx_data_ipg_int_mask	R W	interrupt mask 1'b0	
12	upi_sop_mis_timer_alm	NO	No timestamp alarm signal was collected at RO Sop 1'b0	
13	upi_sop_mis_timer_int_mask	RW	Interrupt Mask 1'b0	
14	upi_singlecollision_alm	RO	Single collision alarm signal	1'b0
15	upi_singlecollision_int_mask	R W	interrupt mask	1'b0
16	upi_excessivecollision_alm	RO	Collision to maximum number of alarm	1'b0
17	upi_excessivecollision_int_mask RW		signal interrupt	1'b0
18	upi_multiplecollision_alm	RO	mask Multiple collision alarm	1'b0
19	upi_multiplecollision_int_mask RW		signal interrupt	1'b0
20	upi_half_fifo_full_alm	RO	mask Half-duplex fallback fifo full alarm	1'b0
quarter one	upi_half_fifo_full_int_mask	R W	signal interrupt mask	1'b0
quarter two	upi_ptp_int	RO	Ptp sync frame warning alarm signal	1'b0
quarter three	upi_ptp_int_mask	R W	interrupt mask	1'b0

3.3.3.8 sta_glb_clr_pls

Register offset: 12'b0000_0100_0010

Register Description: Statistics Counter Clear Register

Bits	Name	R/W	Description	Default
0	upi_sta_glb_clr_pls	WO/W1C	statistics counter is cleared. This indication can clear all traffic in the tx direction. Clear the road counter	1'b0
1	upi_sta_channel_clr_pls	WO/W1C	channel_clr: Only used for single channel clearing, clearing upi_sta_channel_clr_num corresponds to the channel statistics count	1'b0

3.3.3.9 timer_ts_ns_cmp[30]

Register offset: 12'b1100_1100_0000:12'b1100_1101_1101

Register Description: ns Compensation Register

Note: Each register list contains 30 identical registers, that is, the register word value, register threshold, etc. are all the same.

Bits Name	R/W	Description	Default
0:16	upi_timer_ts	RW/WC mode, before sending the next packet, the first	17'h0
17:20	upi_half_crs_ipg	RW/WC check The window of crs is upi_ipg_value, the second and third Subsequent detection windows use this value.	4'h0
21:27	upi_half_fifo_threshold	RW/WC debug use, users cannot arbitrarily configure: rollback fifo Pressure threshold, this fifo 128 depth.	7'h1e

3.3.3.10 timer_cf_fns_cmp[30]

Register offset: 12'b1101_0000_0000:12'b1101_0001_1101

Register Description: fns compensation register

Note: Each register list contains 30 identical registers, that is, the register word value, register threshold, etc. are all the same.

Bits Name	R/W	Description	Default
0:16	upi_timer_cf_fns	RW/WC RW/WC For debug use, users cannot configure it at will: fallback byte	17'h0
17:23	upi_half_back_bytes	configuration The user cannot adjust it at will.	7'h40

3.3.3.11 sw_start_pls

Register offset: 12'b1101_1000_0000

Register Description: Energy Saving Start Configuration Register

Bits	Name	R/W	Description	Default
0:29	upi_lpi_sw_start_pls	WO/W1C	saving software configuration starts to enable	1'b0

3.3.3.12 sw_end_pls

Register offset: 12'b1101_1000_0001

Register Description: Power saving end configuration register

Bits	Name	R/W	Description	Default
0:29	upi_lpi_sw_end_pls	WO/W1C	saving software configuration end enable	1'b0

3.3.3.13 lpi_time[30]

Register offset: 12'b1101_1010_0000:12'b1101_1011_1101

Register Description: Energy saving duration configuration register

Note: Each register list contains 30 identical registers, that is, the register word value, register threshold, etc. are all the same.

Bits	Name	R/W	Description	Default
0:15	upi_lpi_sleep_time	RW/WC	After energy saving is enabled, wait for this time to enter sleep mode 1=1us 16'd100	
16:31	upi_lpi_wake_time	RW/WC	After energy saving is enabled, wait for this time to enter the wake-up mode 1=1us 16'd100	

3.3.3.14 debug_status

Register offset: 12'b1101_1100_0000:12'b1101_1100_0100

Register Description: Debug Dedicated Registers

Offset	Bits	0:29	Name	R/W	Description	Default
	0:29		upi_crs_status	RC	Crs	30'h0
1			upi_col_status	RC	Statuscol Status	30'h0
2	0:29		upi_crs_wait_status	RC	has a packet waiting to be sent but crs is high 30'h0	
3	0:29		upi_dp_fc_status	RC	system side send pause enable state 30'h0	
4	0:29		upi_tx_data_err_status		The data packet sent by RC to pcs has an err status indication 30'h0	
5	0:29		upi_gmii_speed0_status	RO	0-15 port speed indication	30'h0
6	0:29 16:32	port speed indication state RO				
7	0:29 upi_gmii_full_duplex_status	RO	Full/half duplex status indication of each port	30'h0		

3.3.3.15 undersize_cfg_srm

Storage register description: minimum frame length configuration register, NumOfEntries is 30, words is 1.

Bits	Name	R/W	Description
0:13	undersize_cfg	RW	Minimum frame length configuration, the default value is 0x40.

3.3.3.16 mtu_frame_cfg_srm

Storage register description: Maximum frame length configuration register, NumOfEntries is 30, words is 1.

Bits	Name	R/W	Description
0:13	mtu_frame_cfg	RW	The maximum frame length is configured, the default is 16000, when a single-layer VLAN is used, the maximum frame length =MTU+4, RAM depth is 26, each address corresponds to a mac channel.

3.3.3.17 pause_time_srm

Storage register description: pause frame count configuration register, NumOfEntries is 30, words is 1.

Bits	Name	R/W	Description
0:15	pause_time	RW	Normal pause frame pause time, the default value is 0xf000.

3.3.3.18 pause_time_vec_srm

Storage register description: pause sending time interval register, NumOfEntries is 30, words is 1.

Bits	Name	R/W	Description
0:15	pause_time_vec	RW	pause frame sending time interval configuration, the unit is time slot (sending 512bit time), RAM The depth is 26, each address corresponds to a mac channel. The total time is longer than pause_time. Small, the default value is 0x0800.

3.3.3.19 vlan_tag_cfg_0_srm

Storage register description: vlan tag domain match configuration item register, NumOfEntries is 30, words is 1.

Bits	Name	R/W	Description
0:15	vlan_tag_cfg_0	RW	The vlan tag domain matches configuration item 0. Each address represents a channel. The default value is 0x88a8.

3.3.3.20 vlan_tag_cfg_1_srm

Storage register description: vlan tag domain match configuration item register, NumOfEntries is 30, words is 1.

Bits	Name	R/W	Description
0:15	vlan_tag_cfg_1	RW	vlan tag domain matches configuration item 1, each address represents a channel, the default value is 0x88a8.

3.3.3.21 vlan_tag_cfg_2_srm

Storage register description: vlan tag domain match configuration item register, NumOfEntries is 30, words is 1.

Bits	Name	R/W	Description
0:15	vlan_tag_cfg_2	RW	The vlan tag domain matches configuration item 2. Each address represents a channel. The default value is 0x88a8.

3.3.3.22 vlan_tag_cfg_3_srm

Storage register description: vlan tag domain match configuration item register, NumOfEntries is 30, words is 1.

Bits	Name	R/W	Description
0:15	vlan_tag_cfg_3	RW	vlan tag domain matches configuration item 3, each address represents a channel, the default value is 0x88a8 vlan_tag_cfg_0~3 : external vlan tag; match any one

3.3.3.23 vlan1_tag_cfg_0_srm

Storage register description: vlan tag domain match configuration item register, NumOfEntries is 30, words is 1.

Bits	Name	R/W	Description
0:15	vlan1_tag_cfg_0	RW	The vlan1 tag domain matches configuration item 0. Each address represents a channel. The default value is 0x8100, vlan1_tag_cfg_0 : internal vlan tag; when pkt is single vlan, match one of vlan_tag_cfg0-3 or vlan1_tag_cfg_0

3.3.3.24 total_frame_cnt_srm

Storage register description: Total frame count register, NumOfEntries is 30, words is 2.

Offset	Bits	Name	R/W	Description
0	0:31	total_frame_cnt0	RO	Total frame statistics, including control_frame and data_frame, total_frame_cnt[31:0], the default value is 0
1	0:31	total_frame_cnt1	WO	total_frame_cnt[63:32]

3.3.3.25 total_bytes_cnt_srm

Storage register description: Total byte count register, NumOfEntries is 30, words is 2.

Offset	Bits	Name	R/W	Description
0	0:31	total_bytes_cnt0 RO		Total byte count, including control_frame and data_frame, total_bytes_cnt[31:0], the default value is 0x0
1	0:31	total_bytes_cnt1 WO		total_bytes_cnt[63:32]

3.3.3.26 control_frame_cnt_srm

Storage register description: Control frame count register, NumOfEntries is 30, words is 2.

Offset	Bits	Name	R/W	Description
0	0:31	control_frame_cnt0 RO		Control frame statistics: frames with frame type 0x8808, control_frame_cnt[31:0], default value is 0x0, including pause frame
1	0:31	control_frame_cnt1 WO		control_frame_cnt[64:32]

3.3.3.27 pause_frame_cnt_srm

Storage register description: pause frame frame number statistics register, NumOfEntries is 30, words is 2.

Offset	Bits	Name	R/W	Description
0	0:31	pause_frame_cnt0 RO		pause frame statistics, pause_frame_cnt[31:0], the default value is 0x0
1	0:31	pause_frame_cnt1 WO		pause_frame_cnt[63:32]

3.3.3.28 good_frame_cnt_srm

Storage register description: good frame frame count register, NumOfEntries is 30, words is 2.

Offset	Bits	Name	R/W	Description
0	0:31	good_frame_cnt0 RO		Undersize <= packet length <= mtu and the CRC check is correct. good_frame_cnt[31:0],, the default value is 0x0
1	0:31	good_frame_cnt1 WO		good_frame_cnt[63:32]

3.3.3.29 cast_frame_cnt_srm

Storage register description: cast frame count register, NumOfEntries is 90, words is 2.

Offset	Bits	Name	R/W	Description
0	0:31	cast_frame_cnt0 RO		0~29 Unicast packet statistics 30~59 Multicast packet statistics 60~89 Broadcast packet statistics Unicase + muticast + broadcast = good frame, does not include control frame cast_frame_cnt [31:0], default value is 0x0
1	0:31	cast_frame_cnt1 WO		cast_frame_cnt [63:32]

3.3.3.30 unusual_frame_cnt_srm

Storage register description: unusual frame number statistics register, NumOfEntries is 150, words is 2.

Offset	Bits	Name	R/W	Description
0	0:31	cast_frame_cnt0	RO	0~29 undersize frames (<undersize & crc_ok) 30~59 fragment frames (<undersize & crc_fail) 60~89 oversize frames (>mtu & crc_ok) 90~119 jabber frames (>mtu & crc_fail) 120~149 bad frames (undersize < oversize & crc_fail) Contains data frames and control frames unusual_frame_cnt[31:0], the default value is 0x0
1	0:31	unusual_frame_cnt1	WO	unusual_frame_cnt[63:32]

3.3.3.31 segment_frame_cnt_srm

Storage register description: segment frame number statistics register, NumOfEntries is 300, words is 2.

Offset	Bits	Name	R/W	Description
0	0:31	segment_frame_cnt0	RO	0~29: 64 bytes 30~59: 65-127 bytes 60~89: 128-255 bytes 90~119: 256-511 bytes 120~149: 512-1023bytes 150~179 1024-1518bytes 180~209 1519-2047bytes 210~239 2048-4095bytes 240~269 4096-9215bytes 270-299: 9216-MTU bytes The sum of all the above = total frame segment_frame_cnt [31:0], the default value is 0x0
1	0:31	segment_frame_cnt1	WO	segment_frame_cnt [63:32]

3.3.3.32 pause_sa_srm

Storage register description: pause frame sa configuration register, NumOfEntries is 30, words is 2.

Offset	Bits	0	Name	R/W	Description
0	31		pause_sa0	RO	pause sa [31:0], the default value is 0x0.
1	15	0:15	pause_sa1	WO	pause sa [47:32] sa=x010203040506 sa1=0x0102 sa0=0x03040506

3.3.3.33 ptp_int_time_ts_srm

Storage register description: ptp timestamp register, NumOfEntries is 30, words is 2.

Offset	Bits	0	Name	R/W	Description
0	31	0:31	ptp_int_time_ts0	RO	int_time_ts [31:0], the default value is 0x0.
1	31	0:31	ptp_int_time_ts1	WO	int_time_ts [63:32]

4 DP

4.1 dp_ctrl

The dp_reg register module contains 3 registers, as shown in the following table:

Register Offset	Register Name	Description
4'b0000	logical_rst_ctrl	Logic reset control register
4'b0001	upi_rst_ctrl	UPI reset control register
4'b0010	dp_int_ctrl	Interrupt Register

4.1.1 logical_rst_ctrl

Register offset: 4'b0000

Register Description: Logic reset control register.

Bits	Name	R/W	Description	Default
0	upi_rst_tw_n	R W	Traffic_write module reset register, low effective	1'b1
1	upi_rst_trep_n	R W	Traffic_rep module reset register, low effective	1'b1
2	upi_rst_td_n	R W	Traffic_drop module reset register, low effective	1'b1
3	upi_rst_tq_n	R W	Traffic_queue module reset register, low effective	1'b1
4	upi_rst_ts_n	R W	Traffic_schedule module reset register, low effective 1'b1	
5	upi_rst_trd_n	R W	Traffic_read module reset register, low effective	1'b1
6	upi_rst_ptp_ptp_n RW		Ptp module ptp clock domain reset register, low effective 1'b1	
7	upi_rst_ptp_core_n RW		Ptp module reset register in the system clock domain, low effective 1'b1	
8	upi_rst_dapt_core_n RW		The reset register of the Dma_adapter module in the system clock domain. Low effective	1'b1
9	upi_rst_dapt_dma_n RW		Dma_adapter module reset register in dma clock domain Device, low effective	1'b1
10	upi_rst_oamtx_n	R W	Reset register of Oam module, low effective	1'b1

4.1.2 upi_rst_ctrl

Register offset: 4'b0001

Register Description: Reset register of each DP module UPI.

Bits	Name	R/W	Description	Default
0	upi_rst_upi_tw_n RW		Traffic_write module UPI reset register, low effective 1'b1	
1	upi_rst_upi_trep_n RW		Traffic_rep module UPI reset register, low effective 1'b1	
2	upi_rst_upi_td_n RW		Traffic_drop module UPI reset register, low effective 1'b1	
3	upi_rst_upi_tq_n RW		Traffic_queue module UPI reset register, low effective 1'b1	
4	upi_rst_upi_ts_n RW		Traffic_schedule module UPI reset register, low effective 1'b1	
5	upi_rst_upi_trd_n RW		Traffic_drop module UPI reset register, low effective 1'b1	
6	upi_rst_upi_ptp_n RW	1'b1	PTP module UPI reset register, low effective	
7	upi_rst_upi_dapt_n RW		Dma_adapter module UPI reset register, low effective 1'b1	
8	upi_rst_upi_oamtx_n RW		OAM module UPI reset register, low effective	1'b1

4.1.3 dp_int_ctrl

Register offset: 4'b0010

Register description: DP interrupt signal.

Bits	Name	R/W	Description	Default
0	tw_linklist_ecc2_alm	RC	Data cache linked list ECC2 error interrupt indication, 1 means error 1'b0	
1	tw_linklist_ecc1_alm	RC	ECC1 error interrupt indication of data cache linked list, 1 indicates Error	1'b0
2	tw_ib_full_alm	RC	Traffic_write module input buffer full interrupt indication, 1 input buffer Full	1'b0
3	tw_len_err_alm	RC	Input data packet length error interrupt indication, 1 means error 1'b0	
4	tw_in_err_alm	RC	Input data frame indication err interrupt indication, 1 means error 1'b0	
5	tw_sop_err_alm	RC	Interrupt indication of SOP/EOP error in input data packet, 1 table The interrupt	1'b0
6	tw_portmap_err_alm	RC	indication of the port mapping configuration error of the wrong input data packet is shown in Table 1. The error	1'b0
7	trep_mcnum_ecc1_alm	RC	multicast replication statistics table shows the number of multicast errors in ECC1 interruption indicator 1 indicates the number of	1'b0
8	trep_mcnum_ecc2_alm	RC	multicast replication errors in the multicast replication statistics table ECC2 error interrupt indicator 1 indicates an interrupt indication of an error	1'b0
9	tq_rd_empty_alm	RC	queue buffer read empty, 1 indicates an interrupt indication of an error queue buffer read empty, and 1 indicates a queue buffer empty and power Road Read Indicator	1'b0
10	tq_quelink_ecc2_alm	RC	queue cache linked list ECC2 error interrupt indication, 1 means error 1'b0	
11	tq_quelink_ecc1_alm	RC	ECC1 error interrupt indication of the queue cache linked list, 1 means error	1'b0
12 tw_linklist_ecc2_alm_mask	RW		Data cache linked list ECC2 interrupt mask indication, if it is 1, it will not report the	1'b0
13 tw_linklist_ecc1_alm_mask	RW		Interrupt data cache linked list ECC1 interrupt mask indication, 1 means no interrupt Reports the	1'b0
14 tw_ib_full_alm_mask	RW		interrupt input buffer full interrupt mask indication, 1 means not reporting the interrupt Break	1'b0
15 tw_len_err_alm_mask	RW		Input data packet length error interrupt mask indication, 1 means no Report the interrupt	1'b0
16 tw_in_err_alm_mask	RW		Input packet error interrupt mask indication, 1 means do not report the interrupt	1'b0
17 tw_sop_err_alm_mask	RW		Input packet SOP/EOP error interrupt mask indication, 1 means no Report the	1'b0
18 tw_portmap_err_alm_mask	RW		interrupt input packet port mapping error interrupt mask indication, 1 means no Report the	1'b0
19 trep_mcnum_ecc1_alm_mask	RW		interrupt multicast count statistics entry ECC2 error interrupt mask, 1 means Do not report the	1'b0
20 trep_mcnum_ecc2_alm_mask	RW		interrupt multicast count statistics entry ECC1 error interrupt mask indication, which is 1 Indicates that the interrupt queue buffer read empty	1'b0
twenty one	tq_rd_empty_alm_mask	RW	interrupt mask indication is not reported. A value of 1 indicates that the interrupt queue buffer read empty interrupt mask indication is not reported. Break	1'b0
22 tq_quelink_ecc2_alm_mask	RW		Queue cache linked list ECC2 error interrupt mask indication, 1 means Do not report the interrupt	1'b0

23 tq_quelink_ecc1_alm_mask RW		Queue cache linked list ECC1 error interrupt mask indication, 1 means Do not report the interrupt	1'b0
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4.2 traffic_write

The traffic_write_reg register module contains 4 registers; as shown in the following table:

Register Offset	Register Name	Description
6'b00_0001	tw_state	Traffic_write module status indication register
6'b00_0010	tw_maxlen	Traffic_write module maximum packet length configuration register
6'b00_1000:6'b00_1110	tw_port_map	Traffic_write module physical port to logical port mapping configuration register
6'b10_0000:6'b11_0101	tw_cnt	Traffic_write Statistics counter of packets input by each port

4.2.1 tw_state

Register offset: 6'b00_0001

Register Description: Status register of the traffic_write module.

Bits	Name	R/W	Description	Default
0:3	freeptr_prefetch_num RO		number of data cache free list prefetches	4'd0
4:17	freeptr_num	RO	number of data cache free list prefetches	14'd0
18	freeptr_empty	RO	data cache free list empty indication, which means the data cache is full	1'b0
19	linklist_ready	RO	cache list initialization completed indication signal Input data	1'b0
20	tw_portmap_err_st RO	RO	packet port mapping error indication Input	1'b0
21	tw_b_full_st		cache full indication signal Input	1'b0
22	tw_len_err_st	RO	data packet length error indication	1'b0
23	tw_in_err_st	RO	Input data packet err error indication	1'b0
24	tw_sop_err_st	RO	Input data packet SOP/EOP error indication	1'b0

4.2.2 tw maxlen

Register offset: 6'b00_0010

Register Description: Input packet length configuration register.

Bits	Name	R/W	Description	Default
0:13	pkt_maxlen	RW	maximum packet length configuration, long A length exceeding this value indicates a length error	14'd16004
14	linklist_ecc_enable	RW	Data cache linked list ECC enable signal Number, 1 to start ECC check, 0 Disable ECC check function	1'b1
16:23	pkt_minlen	RW	minimum packet length configuration, small The packet length indicates the wrong length	8'd64

4.2.3 tw_port_map

Register offset: 6'b00_1000:6'b00_1110

Register Description: Input packet physical port to logical port mapping configuration register.

Offset 0	Bits	Name	R/W	Description	Default
	0:5	mac0_lg_port	RW MAC0	port mapping Logical port number	MAC0 maps the default configuration of the logical port. The setting is determined by hub_mode
0	6:11	mac1_lg_port	RW MAC1	port mapping Logical port number	MAC1 maps the default configuration of the logical port. The setting is determined by hub_mode
0	12:17	mac2_lg_port	RW MAC2	port mapping Logical port number	MAC2 mapping logical port default configuration The setting is determined by hub_mode
0	18:23	mac3_lg_port	RW MAC3	port mapping Logical port number	MAC3 mapping logical port default configuration The setting is determined by hub_mode
0	24:29	mac4_lg_port	RW MAC4	port mapping Logical port number	MAC4 Mapping Logical Port Default Configuration The setting is determined by hub_mode
1	0:5	mac5_lg_port	RW MAC5	port mapping Logical port number	MAC5 Mapping Logical Port Default Configuration The setting is determined by hub_mode
1	6:11	mac6_lg_port	RW MAC6	port mapping Logical port number	Default configuration of MAC6 mapped logical port The setting is determined by hub_mode
1	12:17	mac7_lg_port	RW MAC7	port mapping Logical port number	Default configuration of MAC7 mapped logical port The setting is determined by hub_mode
1	18:23	mac8_lg_port	RW MAC8	port mapping Logical port number	Default configuration of MAC8 mapped logical port The setting is determined by hub_mode
1	24:29	mac9_lg_port	RW MAC9	port mapping Logical port number	Default configuration of MAC9 mapped logical port The setting is determined by hub_mode
2	0:5	mac10_lg_port	RW MAC10	Port Mapping Logical port number	MAC10 Mapping logical port default Configuration is determined by hub_mode
2	6:11	mac11_lg_port	RW MAC11	Port Mapping Logical port number	MAC11 Mapping logical port default Configuration is determined by hub_mode
2	12:17	mac12_lg_port	RW MAC12	Port Mapping Logical port number	MAC12 Default mapping logical port Configuration is determined by hub_mode
2	18:23	mac13_lg_port	RW MAC13	Port Mapping Logical port number	MAC13 Default mapping logical port Configuration is determined by hub_mode
2	24:29	mac14_lg_port	RW MAC14	Port Mapping Logical port number	MAC14 Default mapping logical port Configuration is determined by hub_mode
3	0:5	mac15_lg_port	RW MAC15	Port Mapping Logical port number	MAC15 mapping logical port default Configuration is determined by hub_mode
3	6:11	mac16_lg_port	RW MAC16	Port Mapping Logical port number	MAC16 mapping logical port default Configuration is determined by hub_mode
3	12:17	mac17_lg_port	RW MAC17	Port Mapping Logical port number	MAC17 Default mapping logical port Configuration is determined by hub_mode
3	18:23	mac18_lg_port	RW MAC18	Port Mapping Logical port number	MAC18 Default mapping logical port Configuration is determined by hub_mode
3	24:29	mac19_lg_port	RW MAC19	Port Mapping Logical port number	MAC19 Mapping logical port default Configuration is determined by hub_mode
4	0:5	mac20_lg_port	RW MAC20	Port Mapping Logical port number	MAC20 Mapping logical port default Configuration is determined by hub_mode
4	6:11	mac21_lg_port	RW MAC21	Port Mapping Logical port number	MAC21 Mapping logical port default Configuration is determined by hub_mode
4	12:17	mac22_lg_port	RW MAC22	Port Mapping Logical port number	MAC22 Default mapping logical port Configuration is determined by hub_mode

4	18:23	mac 23_lg_port	RW MAC23 Port Mapping Logical port number	MAC23 Mapping logical port default Configuration is determined by hub_mode
4	24:29	mac 24_lg_port	RW MAC24 Port Mapping Logical port number	MAC24 Mapping logical port default Configuration is determined by hub_mode
5	0:5	mac25_lg_port	RW MAC25 Port Mapping Logical port number	MAC25 Default mapping logical port Configuration is determined by hub_mode
5	6:11	mac26_lg_port	RW MAC26 Port Mapping Logical port number	MAC26 Mapping logical port default Configuration is determined by hub_mode
5	12:17	mac27_lg_port	RW MAC27 Port Mapping Logical port number	MAC27 Default mapping logical port Configuration is determined by hub_mode
5	18:23	mac28_lg_port	RW MAC28 Port Mapping Logical port number	MAC28 Default mapping logical port Configuration is determined by hub_mode
5	24:29	mac29_lg_port	RW MAC29 Port Mapping Logical port number	MAC29 Mapping Default Logical Port Configuration is determined by hub_mode
6	0:5	ptp_lg_port	RW PTP input port mapping Logical port number	6'd33
6	6:11	oam_lg_port	RW OAM input port mapping The logical port number of the target	6'd34
6	12:17	dma0_lg_port	RW DMA0 port mapped Logical port number	6'd30
6	18:23	dma1_lg_port	RW DMA1 port mapped Logical port number	6'd31
6	24:29	cprx_lg_port	RW CP Configuration Packet Port Mapping The logical port number of the target	6'd32

4.2.4 tw_cnt

Register offset: 6'b10_0000:6'b11_0101

Register Description: Statistics of the number of input data packets on each port.

Offset 0	Bits	Name	R/W	Description	Default
	0:15	mac0_pkt_cnt	RO	Packet statistics of MAC0 input packets	16'h0
0	16:31	mac1_pkt_cnt	RO	Packet statistics for MAC1 input packets	16'h0
1	0:15	mac2_pkt_cnt	RO	Packet statistics for MAC2 input packets	16'h0
1	16:31	mac3_pkt_cnt	RO	Packet statistics for MAC3 input packets	16'h0
2	0:15	mac4_pkt_cnt	RO	Packet statistics for MAC4 input packets	16'h0
2	16:31	mac5_pkt_cnt	RO	Packet statistics for MAC5 input packets	16'h0
3	0:15	mac6_pkt_cnt	RO	Packet statistics of MAC6 input packets	16'h0
3	16:31	mac7_pkt_cnt	RO	Packet statistics for MAC7 input packets	16'h0
4	0:15	mac8_pkt_cnt	RO	Packet statistics for MAC8 input packets	16'h0
4	16:31	mac9_pkt_cnt	RO	Packet statistics for MAC9 input packets	16'h0
5	0:15	mac10_pkt_cnt	RO	Packet statistics of MAC10 input packets	16'h0
5	16:31	mac11_pkt_cnt	RO	Packet statistics for MAC11 input packets	16'h0
6	0:15	mac12_pkt_cnt	RO	Packet statistics for MAC12 input packets	16'h0
6	16:31	mac13_pkt_cnt	RO	Packet statistics for MAC13 input packets	16'h0
7	0:15	mac14_pkt_cnt	RO	Packet statistics for MAC14 input packets	16'h0
7	16:31	mac15_pkt_cnt	RO	Packet statistics for MAC15 input packets	16'h0
8	0:15	mac16_pkt_cnt	RO	Packet statistics for MAC16 input packets	16'h0

8	16:31	mac17_pkt_cnt	RO	Packet statistics for MAC17 input packets	16'h0
9	0:15	mac18_pkt_cnt	RO	Packet statistics of MAC18 input packets	16'h0
9	16:31	mac19_pkt_cnt	RO	Packet statistics for MAC19 input packets	16'h0
10	0:15	mac20_pkt_cnt	RO	Packet statistics of MAC20 input packets	16'h0
10	16:31	mac21_pkt_cnt	RO	Packet statistics of MAC21 input packets	16'h0
11	0:15	mac22_pkt_cnt RO		Packet statistics for MAC22 input packets	16'h0
11	16:31	mac23_pkt_cnt	RO	Packet statistics for MAC23 input packets	16'h0
12	0:15	mac24_pkt_cnt RO		Packet statistics for MAC24 input packets	16'h0
12	16:31	mac25_pkt_cnt	RO	Packet statistics for MAC25 input packets	16'h0
13	0:15	mac26_pkt_cnt RO		Packet statistics of MAC26 input packets	16'h0
13	16:31	mac27_pkt_cnt	RO	Packet statistics for MAC27 input packets	16'h0
14	0:15	mac28_pkt_cnt RO		Packet statistics for MAC28 input packets	16'h0
14	16:31	mac29_pkt_cnt	RO	Packet statistics for MAC29 input packets	16'h0
15	0:15	cprx_pkt_cnt	RO	Packet statistics for CP input packets	16'h0
15	16:31	ptp_pkt_cnt	RO	Packet statistics for PTP input packets	16'h0
16	0:15	oam_pkt_cnt	RO	Packet statistics of OAM input packets	16'h0
16	16:31	dma0rx_pkt_cnt RO 0:15		Packet statistics of DMA0 input packets	16'h0
17		dma1rx_pkt_cnt RO		DMA1 Packet statistics of input	16'h0
17	16:31	tw2pp_pkt_cnt	RO	packets Output to PP module Packet statistics 16'h0	
18	0:15	tw_rls_cnt	RO	Traffic_write module discards packets and releases cache statistics	16'h0
18	16:31	trep_rls_cnt	RO	Traffic_rep module outputs packet release statistics 16'h0	
19	0:15	tw_ptrused_cnt	RO	Data statistics of linked lists used by data cache	16'h0
20	0:31	mac_rxbyte_cnt RO		Byte statistics input to MAC	32'h0
20	0:31	tw2pp_byte_cnt RO		Byte statistics output to PP module	32'h0

4.3 traffic_rep

The traffic_rep_reg register module contains 5 registers; as shown in the following table:

Register Offset	Register Name	Description
5'b0_0000	trep_ctrl	Traffic_rep Module Control Registers
5'b0_0001	trep_st	Traffic_rep Module Status Register
5'b0_0010:5'b0_0011	trep_map_port	Port Configuration Registers
5'b0_0100	trep_mir_port	Mirror Port Configuration Register
5'b0_1000:5'b0_1011	trep_cnt	Traffic_rep module statistics counters

4.3.1 trep_ctrl

Register offset: 5'b0_0000

Register Description: traffic_rep module control register.

Bits	Name	R/W	Description	Default
0	mnum_ecc_enable	RW Multi	cast statistics table ECC enable, 1 turns on the ECC check circuit; 0 turns off the ECC check circuit	1'b1
1	cp_tx_disable	RW Output	packet to CP Configuration packet close indication, 1 does not occur to CP, 0 allows sending to CP	1'b0

2	trap_enable	RW Trap	port transmission enable, 1 allows the trap of the sending packet, 0 Not allowed.	1'b1
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4.3.2 trep_st

Register offset: 5'b0_0001

Register Description: Status register of the traffic_rep module.

Bits	Name	R/W	Description	Default
0	trep_ini_ready	RO	Traffic_rep module initialization completed Indication signal.	1'b0
1	mc_fifo_afull	RO	Multicast cache is almost full indication signal	1'b0

4.3.3 trep_map_port

Register offset: 5'b0_0010:5'b0_0011

Register Description: trap and trunk logical port configuration.

Offset 0	Bits	Name	R/W	Description	Default
	0:5	trap_port	R W	Trap logical port configuration 6'd0	
0	6:11	trunk0_port	R W	Trunk0 logical port configuration 6'd1	
0	12:17	trunk1_port	R W	Trunk1 logical port configuration 6'd2	
0	18:23	trunk2_port	R W	Trunk2 logical port configuration 6'd3	
0	24:29	trunk3_port	R W	Trunk3 logical port configuration 6'd4	
1	0:5	trunk4_port	R W	Trunk4 logical port configuration 6'd5	
1	6:11	trunk5_port	R W	Trunk5 logical port configuration 6'd6	
1	12:17	trunk6_port	R W	Trunk6 logical port configuration 6'd7	
1	18:23	trunk7_port	R W	Trunk7 logical port configuration 6'd8	

4.3.4 trep_mir_port

Register offset: 5'b0_0100

Register Description: Mirror port configuration.

Bits	Name	R/W	Description	Default
0:5	outmir_port	R W	mirroring logical port	6'd2
6:11	inmir_port	R W	configurationInbound mirroring logical port configuration	6'd1

4.3.5 trep_cnt

Register offset: 5'b0_1000:5'b0_1011

Register Description: traffic_rep module statistics count.

Offset 0	Bits	Name	R/W	Description	Default
	0:15	pp2rep_pkt_cnt	RO	PP module input packet statistics	16'h0
0	16:31	pp2rep_droppkt_cnt	RO	PP module input indicator bit dropped packet statistics	16'h0

1	0:15	pp2trep_lbpkt_cnt RO		PP module input indicator bit loopback packet statistics 16'h0	
1	16:31	trep_lbpkt_cnt	RO	Traffic_rep module multicast loopback packet statistics 16'h0	
2	0:31	trep_llbyte_cnt	RO	Traffic_rep module multicast loopback byte statistics 32'h0	
3	0:31	pp2trep_byte_cnt RO		PP module input byte statistics 32'h0	

4.4 traffic_drop

The traffic_drop_reg register block contains 5 registers and 1 storage register.

The register list is as follows:

Register Offset	Register Name	Description
12'b0000_0000_0000:12'b0000_0000_0001	gbl_adm_ctrl	Cache threshold configuration based on global admission control register
12'b0000_0000_0010:12'b0000_0000_0011	td_cnt	Traffic_drop module statistics registers
12'b0000_0000_1000:12'b0000_0000_1110	adm_ctrl	Admission Control Register
12'b0000_0100_0000:12'b0000_01111_1110	sport_adm_ctrl	Cache threshold allocation based on source port admission control Set Register
12'b0000_1000_0000:12'b0000_1100_0001	dport_adm_ctrl	Cache gate for admission control based on destination port Configuration register only

The storage registers are as follows:

Register Offset	Register Name	Description
12'b1000_0000_0000:12'b1100_0001_1111	qwred	Queue WRED parameter configuration register

4.4.1 gbl_adm_ctrl

Register offset: 12'b0000_0000_0000:12'b0000_0000_0001

Register Description: Cache threshold configuration register based on global admission control.

Offset	Bits	Name	R/W	Description	Default
0	0:13	gbl_thd_red	RW	Discard threshold configuration based on global red packets	The default value is configured by the top level buff_sise_sel OK
0	16:29	gbl_thd_yellow	RW	Global yellow packet discard threshold configuration	The default value is configured by the top level buff_sise_sel OK
1	0:13	gbl_thd_green	RW	Global green packet discard threshold configuration	The default value is configured by the top level buff_sise_sel OK

4.4.2 td_cnt

Register offset: 12'b0000_0000_0010:12'b0000_0000_0011

Register Description: Traffic_drop module statistics register.

Offset 0	Bits	Name	R/W	Description	Default
	0:15	trep2td_pkt_cnt	RW	Traffic_rep module input packet statistics 16'h0	

0	16:31	trep2td_droppkt_cnt	RW Traffic_rep module input indicates discarded data Package Statistics	16'h0
1	0:15	td_droppkt_cnt	RW Traffic_drop Module admission control determines that the traffic is discarded Packet Statistics	16'h0
1	16:31	td2tq_pkt_cnt	The RW Traffic_drop module outputs to the queue through admission control Packet statistics for columns	16'h0

4.4.3 adm_ctrl

Register offset: 12'b0000_0000_1000:12'b0000_0000_1110

Register Description: Admission control register.

Offset	Bits	Name	R/W	Description	Default
0	0:31 dport_adm_color_aware_31to0 RW			Based on the color of the destination port 0~31 Other indication bitmap, 1 bit indication Indicates that the corresponding destination port is enabled for color identification. Otherwise, the color is not recognized.	32'h0
1	0	dport_adm_color_aware_32 RW		The color identification indicator for the destination port is 32 1 indicates color identification.	1'b0
2	0:31	dport_adm_enable_31to0 RW		Admission control based on destination ports 0 to 31 Enable bitmap, a bit of 1 indicates Enable admission control for the corresponding port.	32'hffffffff
3	0	dport_adm_enable_32	R W	The admission control with destination port 32 enables 1 means enable, 0 means disable able.	1'b1
4	0:31	sport_adm_enable_31to0 RW		Admission control based on source port 0~31 Enable bitmap, a bit of 1 indicates Enable admission control for the corresponding source port.	32'h0
5	0:2	sport_adm_enable_34to32 RW		The access control for source ports 32 to 34 is Enable bitmap, corresponding bit is 1 Admission control is enabled on this port.	3'h0
6	0	gbl_adm_color_aware	R W	Based on the global admission control enablement, 1 Start based on global admission control, no It is not enabled.	1'b0
6	1	que_adm_enable	R W	Enable queue-based admission control. 0 means admission control is enabled for all queues system.	1'b0
6	2	adm_mode	R W	Admission control mode, 0 based on data Block (128B), 0 means packet-based Perform admission control	1'b0
6	3	pkt_red_drop_ind	R W	Enter the red discard indication. The red packet byte is discarded; if it is 0, it passes Admission control determines whether to discard the packet.	1'b1

4.4.4 sport_adm_ctrl

Register offset: 12'b0000_0100_0000:12'b0000_01111_1110

Register Description: Source port-based admission cache threshold configuration.

Offset	Bits	Name	R/W	DescriptionLogical	Default
0	0:13	sport0_pause_on_thd	R W	port 0 corresponds to the flow control of the source port The buffer threshold indicating the signal is turned on.	14'd600
0	16:29	sport0_pause_off_thd	R W	The flow of the source port corresponding to logical port 0. The buffer threshold of the control indication signal is	14'd500
1	0:13	sport0_drop_thd	R W	closed. Logical port 0 corresponds to the discard of the source port Cache threshold.	14'd800
2	0:13	sport1_pause_on_thd	R W	Logical port 1 corresponds to the flow control of the source port Indicates the buffer threshold for the signal to be turned	14'd600
2	16:29	sport1_pause_off_thd	R W	on. Logical port 1 corresponds to the flow control of the source port Indicates the buffer threshold for signal closure.	14'd500
3	0:13	sport1_drop_thd	R W	Logical port 1 corresponding to the source port discard Cache threshold.	14'd800
4	0:13	sport2_pause_on_thd	R W	Logical port 2 corresponds to the flow control of the source port Indicates the buffer threshold for the signal to be turned	14'd600
4	16:29	sport2_pause_off_thd	R W	on. Logical port 2 corresponds to the flow control of the source port Indicates the buffer threshold for signal closure.	14'd500
5	0:13	sport2_drop_thd	R W	Logical port 2 corresponding to the source port discard Cache threshold.	14'd800
6	0:13	sport3_pause_on_thd	R W	Logical port 3 corresponds to the flow control of the source port Indicates the buffer threshold for the signal to be turned	14'd600
6	16:29	sport3_pause_off_thd	R W	on. Logical port 3 corresponds to the flow control of the source port Indicates the buffer threshold for signal closure.	14'd500
7	0:13	sport3_drop_thd	R W	Logical port 3 corresponding to the source port discard Cache threshold.	14'd800
8	0:13	sport4_pause_on_thd	R W	Logical port 4 corresponds to the flow control of the source port Indicates the buffer threshold for the signal to be turned	14'd600
8	16:29	sport4_pause_off_thd	R W	on. Logical port 4 corresponds to the flow control of the source port Indicates the buffer threshold for signal closure.	14'd500
9	0:13	sport4_drop_thd	R W	Logical port 4 corresponding to the source port discard Cache threshold.	14'd800
10	0:13	sport5_pause_on_thd	R W	Logical port 5 corresponds to the flow control of the source port Indicates the buffer threshold for the signal to be turned	14'd600
10	16:29	sport5_pause_off_thd	R W	on. Logical port 5 corresponds to the flow control of the source port Indicates the buffer threshold for signal closure.	14'd500
11	0:13	sport5_drop_thd	R W	Logical port 5 corresponding to the source port discard Cache threshold.	14'd800
12	0:13	sport6_pause_on_thd	R W	Logical port 6 corresponds to the flow control of the source port Indicates the buffer threshold for signal opening.	14'd600
12	16:29	sport6_pause_off_thd	R W	Logical port 6 corresponds to the flow control of the source port Indicates the buffer threshold for signal closure.	14'd500
13	0:13	sport6_drop_thd	R W	Logical port 6 corresponding to the source port discard Cache threshold.	14'd800
14	0:13	sport7_pause_on_thd	R W	Logical port 7 corresponds to the flow control of the source port Indicates the buffer threshold for signal opening.	14'd600
14	16:29	sport7_pause_off_thd	R W	Logical port 7 corresponds to the flow control of the source port Buffer threshold indicating signal off.	14'd500

15	0:13	sport7_drop_thd	R W	Logical port 7 corresponding to the source port discard Cache threshold.	14'd800
16	0:13	sport8_pause_on_thd	R W	Logical port 8 corresponds to the flow control of the source port Indicates the buffer threshold for signal opening.	14'd600
16	16:29	sport8_pause_off_thd	R W	Logical port 8 corresponds to the flow control of the source port Indicates the buffer threshold for signal closure.	14'd500
17	0:13	sport8_drop_thd	R W	Logical port 8 corresponding to the source port discard Cache threshold.	14'd800
18	0:13	sport9_pause_on_thd	R W	Logical port 9 corresponds to the flow control of the source port Indicates the buffer threshold for the signal to be turned on.	14'd600
18	16:29	sport9_pause_off_thd	R W	on. Logical port 9 corresponds to the flow control of the source port Indicates the buffer threshold for signal closure.	14'd500
19	0:13	sport9_drop_thd	R W	Logical port 9 corresponding to the source port discard Cache threshold.	14'd800
20	0:13	sport10_pause_on_thd	R W	Logical port 10 corresponds to the flow of the source port The buffer threshold for the control indication signal to be turned on.	14'd600
20	16:29	sport10_pause_off_thd	R W	turned on. Logical port 10 corresponds to the flow of the source port The buffer threshold of the control indication signal is	14'd500
twenty one	0:13	sport10_drop_thd	R W	closed. Logical port 10 corresponds to the source port loss The discard cache	14'd800
twenty two	0:13	sport11_pause_on_thd	R W	threshold. Logical port 11 corresponds to the source port of the flow The buffer threshold for the control indication signal to be turned on.	14'd600
twenty two	16:29	sport11_pause_off_thd	R W	turned on. Logical port 11 corresponds to the flow of the source port The buffer threshold of the control indication signal is	14'd500
twenty three	0:13	sport11_drop_thd	R W	closed. Logical port 11 corresponds to the source port loss The discard cache	14'd800
twenty four	0:13	sport12_pause_on_thd	R W	threshold. Logical port 12 corresponds to the flow of the source port The buffer threshold for the control indication signal to be turned on.	14'd600
twenty four	16:29	sport12_pause_off_thd	R W	turned on. Logical port 12 corresponds to the flow of the source port The buffer threshold of the control indication signal is	14'd500
25	0:13	sport12_drop_thd	R W	closed. Logical port 12 corresponds to the source port loss The discard cache	14'd800
26	0:13	sport13_pause_on_thd	R W	threshold. Logical port 13 corresponds to the source port of the flow The buffer threshold for the control indication signal to be turned on.	14'd600
26	16:29	sport13_pause_off_thd	R W	turned on. Logical port 13 corresponds to the flow of the source port The buffer threshold of the control indication signal is	14'd500
27	0:13	sport13_drop_thd	R W	closed. Logical port 13 corresponds to the source port loss The discard cache	14'd800
28	0:13	sport14_pause_on_thd	R W	threshold. Logical port 14 corresponds to the flow of the source port The buffer threshold for the control indication signal to be turned on.	14'd600
28	16:29	sport14_pause_off_thd	R W	turned on. Logical port 14 corresponds to the flow of the source port The buffer threshold of the control indication signal is	14'd500
29	0:13	sport14_drop_thd	R W	closed. Logical port 14 corresponds to the source port loss The discard cache	14'd800
30	0:13	sport15_pause_on_thd	R W	threshold. Logical port 15 corresponds to the flow of the source port The buffer threshold for the control indication signal to be turned on.	14'd600
30	16:29	sport15_pause_off_thd	R W	turned on. Logical port 15 corresponds to the flow of the source port The buffer threshold that controls the indication signal to be closed.	14'd500

31	0:13	sport15_drop_thd	R W	Logical port 15 corresponding to the source port loss The discard cache	14'd800
32	0:13	sport16_pause_on_thd	R W	threshold. Logical port 16 corresponds to the flow of the source port The buffer threshold for the control indication signal to be	14'd600
32	16:29	sport16_pause_off_thd	R W	turned on. Logical port 16 corresponds to the flow of the source port The buffer threshold for controlling the indication signal to	14'd500
33	0:13	sport16_drop_thd	R W	be closed. Logical port 16 corresponds to the source port loss. The discard cache	14'd800
34	0:13	sport17_pause_on_thd	R W	threshold. Logical port 17 corresponds to the source port of the flow The buffer threshold for the control indication signal to be	14'd600
34	16:29	sport17_pause_off_thd	R W	turned on. Logical port 17 corresponds to the flow of the source port The buffer threshold of the control indication signal is	14'd500
35	0:13	sport17_drop_thd	R W	closed. Logical port 17 corresponds to the source port loss The discard cache	14'd800
36	0:13	sport18_pause_on_thd	R W	threshold. Logical port 18 corresponds to the source port of the flow The buffer threshold for the control indication signal to be	14'd600
36	16:29	sport18_pause_off_thd	R W	turned on. Logical port 18 corresponds to the flow of the source port The buffer threshold of the control indication signal is	14'd500
37	0:13	sport18_drop_thd	R W	closed. Logical port 18 corresponds to the source port loss The discard cache	14'd800
38	0:13	sport19_pause_on_thd	R W	threshold. Logical port 19 corresponds to the source port of the flow The buffer threshold for the control indication signal to be	14'd600
38	16:29	sport19_pause_off_thd	R W	turned on. Logical port 19 corresponds to the flow of the source port The buffer threshold of the control indication signal is	14'd500
39	0:13	sport19_drop_thd	R W	closed. Logical port 19 corresponds to the source port loss The discard cache	14'd800
40	0:13	sport20_pause_on_thd	R W	threshold. Logical port 20 corresponds to the source port of the flow The buffer threshold for the control indication signal to be	14'd600
40	16:29	sport20_pause_off_thd	R W	turned on. The source port corresponding to logical port 20 Flow control indicator signal closes the buffer gate limit.	14'd500
41	0:13	sport20_drop_thd	R W	Logical port 20 corresponding to the source port loss The discard cache	14'd800
42	0:13	sport21_pause_on_thd	R W	threshold. Logical port 21 corresponds to the source port of the flow The buffer threshold for the control indication signal to be	14'd600
42	16:29	sport21_pause_off_thd	R W	turned on. Logical port 21 corresponds to the flow of the source port The buffer threshold of the control indication signal is	14'd500
43	0:13	sport21_drop_thd	R W	closed. Logical port 21 corresponds to the source port loss The discard cache	14'd800
44	0:13	sport22_pause_on_thd	R W	threshold. Logical port 22 corresponds to the flow of the source port The buffer threshold for the control indication signal to be	14'd600
44	16:29	sport22_pause_off_thd	R W	turned on. Logical port 22 corresponds to the flow of the source port The buffer threshold of the control indication signal is	14'd500
45	0:13	sport22_drop_thd	R W	closed. Logical port 22 corresponds to the source port loss The discard cache	14'd800
46	0:13	sport23_pause_on_thd	R W	threshold. Logical port 23 corresponds to the flow of the source port The buffer threshold for the control indication signal to be	14'd600
46	16:29	sport23_pause_off_thd	R W	turned on. Logical port 23 corresponds to the flow of the source port The buffer threshold that controls the indication signal to be closed.	14'd500

47	0:13	sport23_drop_thd	R W	Logical port 23 corresponding to the source port loss The discard cache	14'd800
48	0:13	sport24_pause_on_thd	R W	threshold. Logical port 24 corresponds to the flow of the source port. The buffer threshold for the control indication signal to be	14'd600
48	16:29	sport24_pause_off_thd	R W	turned on. Logical port 24 corresponds to the flow of the source port. The buffer threshold of the control indication signal is	14'd500
49	0:13	sport24_drop_thd	R W	closed. Logical port 24 corresponds to the source port loss The discard cache	14'd800
50	0:13	sport25_pause_on_thd	R W	threshold. Logical port 25 corresponds to the source port of the flow. The buffer threshold for the control indication signal to be	14'd600
50	16:29	sport25_pause_off_thd	R W	turned on. Logical port 25 corresponds to the flow of the source port. The buffer threshold of the control indication signal is	14'd500
51	0:13	sport25_drop_thd	R W	closed. Logical port 25 corresponds to the source port loss The discard cache	14'd800
52	0:13	sport26_pause_on_thd	R W	threshold. Logical port 26 corresponds to the source port of the flow. The buffer threshold for the control indication signal to be	14'd600
52	16:29	sport26_pause_off_thd	R W	turned on. Logical port 26 corresponds to the flow of the source port. The buffer threshold of the control indication signal is	14'd500
53	0:13	sport26_drop_thd	R W	closed. Logical port 26 corresponding to the port discard Cache threshold.	14'd800
54	0:13	sport27_pause_on_thd	R W	Logical port 27 corresponds to the flow of the source port The buffer threshold for the control indication signal to be	14'd600
54	16:29	sport27_pause_off_thd	R W	turned on. Logical port 27 corresponds to the flow of the source port. The buffer threshold of the control indication signal is	14'd500
55	0:13	sport27_drop_thd	R W	closed. Logical port 27 corresponds to the source port loss The discard cache	14'd800
56	0:13	sport28_pause_on_thd	R W	threshold. Logical port 28 corresponds to the source port of the flow. The buffer threshold for the control indication signal to be	14'd600
56	16:29	sport28_pause_off_thd	R W	turned on. Logical port 28 corresponds to the flow of the source port. The buffer threshold of the control indication signal is	14'd500
57	0:13	sport28_drop_thd	R W	closed. Logical port 28 corresponds to the source port loss The discard cache	14'd800
58	0:13	sport29_pause_on_thd	R W	threshold. Logical port 29 corresponds to the source port of the flow. The buffer threshold for the control indication signal to be	14'd600
58	16:29	sport29_pause_off_thd	R W	turned on. Logical port 29 corresponds to the flow of the source port. The buffer threshold of the control indication signal is	14'd500
59	0:13	sport29_drop_thd	R W	closed. Logical port 29 corresponds to the source port loss The discard cache threshold.	14'd800
60	0:13	sport30_drop_thd	R W	The discard cache threshold of logical port 30 corresponds to the source port. The discard cache threshold.	14'd800
60	16:29	sport31_drop_thd	R W	Logical port 31 corresponds to the discard cache threshold of the source port. The discard cache threshold.	14'd800
61	0:13	sport32_drop_thd	R W	Logical port 32 corresponds to the discard cache threshold of the source port. The discard cache threshold.	14'd800
61	16:29	sport33_drop_thd	R W	Logical port 33 corresponds to the discard cache threshold of the source port. The discard cache threshold.	14'd800
62	0:13	sport34_drop_thd	R W	Logical port 34 corresponds to the discard cache threshold of the source port. Cache discard threshold.	14'd800

4.4.5 dport_adm_ctrl

Register offset: 12'b0000_0100_0000:12'b0000_01111_1110

Register Description: Cache gate configuration based on destination port admission control.

Offset	Bits	Name	R/W	DescriptionLogical	Default
0	0:13	dport0_droptd_green	R W	port 0 corresponds to the destination port Green packet cache discard threshold	14'd800
0	16:29	dport0_droptd_yellow	R W	logical port 0 corresponds to the destination port The cache discard threshold logic port 0 of	14'd700
1	0:13	dport0_droptd_red	R W	the yellow packet corresponds to the destination port The cache discard threshold of red packets.	14'd600
2	0:13	dport1_droptd_green	R W	Logical port 1 corresponds to the destination port Green packet cache discard threshold	14'd800
2	16:29	dport1_droptd_yellow	R W	logical port 1 corresponds to the destination port The cache discard threshold logic port 1 of	14'd700
3	0:13	dport1_droptd_red	R W	the yellow packet corresponds to the destination port Red packet cache discard threshold.	14'd600
4	0:13	dport2_droptd_green	R W	Logical port 2 corresponds to the destination port Green packet cache discard threshold	14'd800
4	16:29	dport2_droptd_yellow	R W	logical port 2 corresponds to the destination port The cache discard threshold logic port 2 of	14'd700
5	0:13	dport2_droptd_red	R W	the yellow packet corresponds to the destination port Red packet cache discard threshold.	14'd600
6	0:13	dport3_droptd_green	R W	Logical port 3 corresponds to the destination port Green packet cache discard threshold	14'd800
6	16:29	dport3_droptd_yellow	R W	logical port 3 corresponds to the destination port The cache discard threshold logic port 3 of	14'd700
7	0:13	dport3_droptd_red	R W	the yellow packet corresponds to the destination port The cache discard threshold for red packets.	14'd600
8	0:13	dport4_droptd_green	R W	Logical port 4 corresponds to the destination port Green packet cache discard threshold	14'd800
8	16:29	dport4_droptd_yellow	R W	logic port 4 corresponds to the destination port The cache discard threshold logic port 4 of	14'd700
9	0:13	dport4_droptd_red	R W	the yellow packet corresponds to the destination port The cache discard threshold for red packets.	14'd600
10	0:13	dport5_droptd_green	R W	Logical port 5 corresponds to the destination port Green packet cache discard threshold	14'd800
10	16:29	dport5_droptd_yellow	R W	logical port 5 corresponds to the destination port The cache discard threshold logic port 5 of	14'd700
11	0:13	dport5_droptd_red	R W	the yellow packet corresponds to the destination port The cache discard threshold for red packets.	14'd600
12	0:13	dport6_droptd_green	R W	Logical port 6 corresponds to the destination port Green packet cache discard threshold	14'd800
12	16:29	dport6_droptd_yellow	R W	logical port 6 corresponds to the destination port The cache discard threshold logic port 6 of	14'd700
13	0:13	dport6_droptd_red	R W	the yellow packet corresponds to the destination port Cache discard threshold for red packets.	14'd600

14	0:13	dport7_droptd_green	R W	Logical port 7 corresponds to the destination port Green packet cache discard threshold	14'd800
14	16:29	dport7_droptd_yellow	R W	logical port 7 corresponds to the destination port The cache discard threshold logic port 7 of	14'd700
15	0:13	dport7_droptd_red	R W	the yellow packet corresponds to the destination port Red packet cache discard threshold.	14'd600
16	0:13	dport8_droptd_green	R W	Logical port 8 corresponds to the destination port Green packet cache discard threshold	14'd800
16	16:29	dport8_droptd_yellow	R W	logical port 8 corresponds to the destination port The cache discard threshold logic port 8 of	14'd700
17	0:13	dport8_droptd_red	R W	the yellow packet corresponds to the destination port Red packet cache discard threshold.	14'd600
18	0:13	dport9_droptd_green	R W	Logical port 9 corresponds to the destination port Green packet cache discard threshold	14'd800
18	16:29	dport9_droptd_yellow	R W	logic port 9 corresponds to the destination port The cache discard threshold logic port 9 of	14'd700
19	0:13	dport9_droptd_red	R W	the yellow packet corresponds to the destination port The cache discard threshold for red	14'd600
20	0:13	dport10_droptd_green	R W	packets. Logical port 10 corresponds to the destination port Green packet cache discard threshold	14'd800
20	16:29	dport10_droptd_yellow	R W	logical port 10 corresponds to the destination port The cache discard threshold logic port 10	14'd700
twenty one	0:13	dport10_droptd_red	R W	of the yellow packet corresponds to the destination por The cache discard threshold for red	14'd600
twenty two	0:13	dport11_droptd_green	R W	packets. Logical port 11 corresponds to the destination port Green packet cache discard threshold	14'd800
twenty two	16:29	dport11_droptd_yellow	R W	logical port 11 corresponds to the destination port The cache discard threshold logic port 11	14'd700
twenty three	0:13	dport11_droptd_red	R W	of the yellow packet corresponds to the destination por The cache discard threshold for red	14'd600
twenty four	0:13	dport12_droptd_green	R W	packets. Logical port 12 corresponds to the destination port Green packet cache discard threshold	14'd800
twenty four	16:29	dport12_droptd_yellow	R W	logical port 12 corresponds to the destination port The cache discard threshold logic port 12	14'd700
25	0:13	dport12_droptd_red	R W	of the yellow packet corresponds to the destination por The cache discard threshold for red	14'd600
26	0:13	dport13_droptd_green	R W	packets. Logical port 13 corresponds to the destination port Green packet cache discard threshold	14'd800
26	16:29	dport13_droptd_yellow	R W	logical port 13 corresponds to the destination port The cache discard threshold logic port 13	14'd700
27	0:13	dport13_droptd_red	R W	of the yellow packet corresponds to the destination por The cache discard threshold for red	14'd600
28	0:13	dport14_droptd_green	R W	packets. Logical port 14 corresponds to the destination port Green packet cache discard threshold	14'd800
28	16:29	dport14_droptd_yellow	R W	logical port 14 corresponds to the destination port The cache discard threshold logic port 14	14'd700
29	0:13	dport14_droptd_red	R W	of the yellow packet corresponds to the destination por Cache discard threshold for red packets.	14'd600

30	0:13	dport15_droptd_green	R W	Logical port 15 corresponds to the destination port Green packet cache discard threshold	14'd800
30	16:29	dport15_droptd_yellow	R W	logical port 15 corresponds to the destination port The cache discard threshold logic port 15	14'd700
31	0:13	dport15_droptd_red	R W	of the yellow packet corresponds to the destination port The cache discard threshold for red	14'd600
32	0:13	dport16_droptd_green	R W	packets. Logical port 16 corresponds to the destination port Green packet cache discard threshold	14'd800
32	16:29	dport16_droptd_yellow	R W	logical port 16 corresponds to the destination port The cache discard threshold logic port 16	14'd700
33	0:13	dport16_droptd_red	R W	of the yellow packet corresponds to the destination port The cache discard threshold for red	14'd600
34	0:13	dport17_droptd_green	R W	packets. Logical port 17 corresponds to the destination port Green packet cache discard threshold	14'd800
34	16:29	dport17_droptd_yellow	R W	logical port 17 corresponds to the destination port The cache discard threshold logic port 17	14'd700
35	0:13	dport17_droptd_red	R W	of the yellow packet corresponds to the destination port The cache discard threshold for red	14'd600
36	0:13	dport18_droptd_green	R W	packets. Logical port 18 corresponds to the destination port Green packet cache discard threshold	14'd800
36	16:29	dport18_droptd_yellow	R W	logical port 18 corresponds to the destination port The cache discard threshold logic port 18	14'd700
37	0:13	dport18_droptd_red	R W	of the yellow packet corresponds to the destination port The cache discard threshold for red	14'd600
38	0:13	dport19_droptd_green	R W	packets. Logical port 19 corresponds to the destination port Green packet cache discard threshold	14'd800
38	16:29	dport19_droptd_yellow	R W	logical port 19 corresponds to the destination port The cache discard threshold logic port 19	14'd700
39	0:13	dport19_droptd_red	R W	of the yellow packet corresponds to the destination port The cache discard threshold for red	14'd600
40	0:13	dport20_droptd_green	R W	packets. Logical port 20 corresponds to the destination port Green packet cache discard threshold	14'd800
40	16:29	dport20_droptd_yellow	R W	logical port 20 corresponds to the destination port The cache discard threshold logical port 20	14'd700
41	0:13	dport20_droptd_red	R W	of the yellow packet corresponds to the destination port The cache discard threshold for red	14'd600
42	0:13	dport21_droptd_green	R W	packets. Logical port 21 corresponds to the destination port Green packet cache discard threshold	14'd800
42	16:29	dport21_droptd_yellow	R W	logical port 21 corresponds to the destination port The cache discard threshold logical port 21	14'd700
43	0:13	dport21_droptd_red	R W	of the yellow packet corresponds to the destination port The cache discard threshold for red	14'd600
44	0:13	dport22_droptd_green	R W	packets. Logical port 22 corresponds to the destination port Green packet cache discard threshold	14'd800
44	16:29	dport22_droptd_yellow	R W	logical port 22 corresponds to the destination port The cache discard threshold logical port 22	14'd700
45	0:13	dport22_droptd_red	R W	of the yellow packet corresponds to the destination port Cache discard threshold for red packets.	14'd600

46	0:13	dport23_droptd_green	R W	Logical port 23 corresponds to the destination port Green packet cache discard threshold	14'd800
46	16:29	dport23_droptd_yellow	R W	logical port 23 corresponds to the destination port The cache discard threshold logical port 23	14'd700
47	0:13	dport23_droptd_red	R W	of the yellow packet corresponds to the destination port The cache discard threshold for red	14'd600
48	0:13	dport24_droptd_green	R W	packets. Logical port 24 corresponds to the destination port Green packet cache discard threshold	14'd800
48	16:29	dport24_droptd_yellow	R W	logical port 24 corresponds to the destination port The cache discard threshold logical port 24	14'd700
49	0:13	dport24_droptd_red	R W	of the yellow packet corresponds to the destination port The cache discard threshold for red	14'd600
50	0:13	dport25_droptd_green	R W	packets. Logical port 25 corresponds to the destination port Green packet cache discard threshold	14'd800
50	16:29	dport25_droptd_yellow	R W	logical port 25 corresponds to the destination port The cache discard threshold logical port 25	14'd700
51	0:13	dport25_droptd_red	R W	of the yellow packet corresponds to the destination port The cache discard threshold for red	14'd600
52	0:13	dport26_droptd_green	R W	packets. Logical port 26 corresponds to the destination port Green packet cache discard threshold	14'd800
52	16:29	dport26_droptd_yellow	R W	logical port 26 corresponds to the destination port The cache discard threshold logical port 26	14'd700
53	0:13	dport26_droptd_red	R W	of the yellow packet corresponds to the destination port The cache discard threshold for red	14'd600
54	0:13	dport27_droptd_green	R W	packets. Logical port 27 corresponds to the destination port Green packet cache discard threshold	14'd800
54	16:29	dport27_droptd_yellow	R W	logical port 27 corresponds to the destination port The cache discard threshold logical port 27	14'd700
55	0:13	dport27_droptd_red	R W	of the yellow packet corresponds to the destination port The cache discard threshold for red	14'd600
56	0:13	dport28_droptd_green	R W	packets. Logical port 28 corresponds to the destination port Green packet cache discard threshold	14'd800
56	16:29	dport28_droptd_yellow	R W	logical port 28 corresponds to the destination port The cache discard threshold logical port 28	14'd700
57	0:13	dport28_droptd_red	R W	of the yellow packet corresponds to the destination port The cache discard threshold for red	14'd600
58	0:13	dport29_droptd_green	R W	packets. Logical port 29 corresponds to the destination port Green packet cache discard threshold	14'd800
58	16:29	dport29_droptd_yellow	R W	logical port 29 corresponds to the destination port The cache discard threshold logical port 29	14'd700
59	0:13	dport29_droptd_red	R W	of the yellow packet corresponds to the destination port The cache discard threshold for red	14'd600
60	0:13	dport30_droptd_green	R W	packets. Logical port 30 corresponds to the destination port Green packet cache discard threshold	14'd800
60	16:29	dport30_droptd_yellow	R W	logical port 30 corresponds to the destination port The cache discard threshold logical port 30	14'd700
61	0:13	dport30_droptd_red	R W	of the yellow packet corresponds to the destination port Cache discard threshold for red packets.	14'd600

62	0:13	dport31_droptd_green	R W	Logical port 31 corresponds to the destination port Green packet cache discard threshold	14'd800
62	16:29	dport31_droptd_yellow	R W	logical port 31 corresponds to the destination port The cache discard threshold logical port 31	14'd700
63	0:13	dport31_droptd_red	R W	of the yellow packet corresponds to the destination port The cache discard threshold for red	14'd600
64	0:13	dport32_droptd_green	R W	packets. Logical port 32 corresponds to the destination port Green packet cache discard threshold	14'd800
64	16:29	dport32_droptd_yellow	R W	logical port 32 corresponds to the destination port The cache discard threshold logical port 32	14'd700
65	0:13	dport32_droptd_red	R W	of the yellow packet corresponds to the destination port Cache discard threshold for red packets.	14'd600

4.4.6 qwred

Storage register description: Queue WRED parameter configuration, a total of 264 entries, corresponding to the configuration of 264 queues.

Offset	Bits	Name	R/W	Description
0	0:13	wred_start_red	R W	WRED start discard threshold for red packets.
0	14:27	wred_end_red	R W	WRED end discard threshold for red packets
0	28:31	wred_mdrp_red	R W	WRED maximum drop probability for red packets
1	0:13	wred_start_yellow RW		WRED start discard threshold for yellow packets
1	14:27	wred_end_yellow RW		WRED end discard threshold for yellow packets
1	28:31	wred_mdrp_yellow RW		Maximum drop probability of WRED for yellow packets
2	0:13	wred_start_green RW	wred_end_green	WRED start discard threshold for green packets
2	14:27	RW wred_mdrp_green RW		WRED end discard threshold for green packets
2	28:31	wred_weight		WRED maximum drop probability for green packets
3	0:3		R W	WRED average queue length calculation weight
3	4	color_aware	R W	Color recognition enable for queue admission control, 1 to identify the color; 0, access control is performed according to the green packet threshold.
3	5	wred_ind	R W	Queue drop mode, 0 means tail drop, configured with end threshold Used as the drop threshold for tail drop. When it is 1, wred drop is used.
3	6	adm_en	WO	Enable the queue admission control. 1 enables discarding; 0 does not discard. abandoned.

4.5 traffic_queue

The traffic_queue_reg register module contains 3 registers and 1 storage register.

The register list is as follows:

Register Offset	Register Name	Description
10'b00_0000_0000	que_ctrl	Traffic_queue module control registers
10'b00_0000_0001	que_st	Traffic_queue module status register
10'b00_0001_0000:10'b00_0001_1000	tq_port_cnt	specifies the number of scheduled packet descriptions for the queue.

The storage registers are as follows:

Register Offset	Register Name	Description
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10'b10_0000_0000:10'b11_0000_0111	que_count Statistics on the number of packet descriptions stored in each queue in the queue cache.
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4.5.1 que_ctrl

Register offset: 10'b00_0000_0000

Register Description: Traffic_queue module control register

Bits	Name	R/W	Description	Default
0:5	port0_cnt_cfg	R W	number configured for this signal is 0. It specifies the queue to which it belongs for the scheduled packet description. The port number	6'd0
8:13	port1_cnt_cfg	R W	configured by this signal specifies the queue to which the scheduled packets are to be reported. The queue	6'd1
16	qualink_ecc_enable	RW	cache list ECC enable signal.	1'b1

4.5.2 que_st

Register offset: 10'b00_0000_0001

Register Description: Traffic_queue module status register

Bits	Name	R/W	Description	Default
0:13	freetr_ptr_cnt	RO	the number of free lists in the queue cache. Indication	14'd0
16	tq_ini_ready	RO	that the queue module has completed initialization configuration.	1'b0

4.5.3 tq_port_cnt

Register offset: 10'b00_0001_0000:10'b00_0001_1000

Register description: Specifies the number of scheduled packets for the queue.

Offset	Bits	Name	R/W	Description	Default
0	0:15	port0_que0_cnt	RO	The priority of the port configured in port0_cnt_cfg Output packet statistics for queue 0.	16'h0
0	16:31	port0_que1_cnt	RO	The priority of the configured port port0_cnt_cfg Output packet description statistics of the queue	16'h0
1	0:15	port0_que2_cnt	RO	with value 1. The priority of the configured port port0_cnt_cfg Output packet statistics for queue 2.	16'h0
1	16:31	port0_que3_cnt	RO	The priority of the configured port port0_cnt_cfg Output packet statistics for queue 3.	16'h0
2	0:15	port0_que4_cnt	RO	The priority of the configured port port0_cnt_cfg Output packet statistics for queue 4.	16'h0
2	16:31	port0_que5_cnt	RO	The priority of the configured port port0_cnt_cfg Output packet statistics for queue 5.	16'h0
3	0:15	port0_que6_cnt	RO	The priority of the configured port port0_cnt_cfg Output packet statistics for queue 6.	16'h0
3	16:31	port0_que7_cnt	RO	The priority of the configured port port0_cnt_cfg Output packet statistics for queue 7.	16'h0

4	0:15	port1_que0_cnt RO		The priority of the configured port port1_cnt_cfg Output packet description statistics of the queue	16'h0
4	16:31	port1_que1_cnt RO		with value 0. The priority of the configured port port1_cnt_cfg Output packet description statistics of	16'h0
5	0:15	port1_que2_cnt	RO	queue 1. The priority of the configured port port1_cnt_cfg Output packet description statistics for	16'h0
5	16:31	port1_que3_cnt RO		queue 2. The priority of the configured port port1_cnt_cfg Output packet statistics for queue 3.	16'h0
6	0:15	port1_que4_cnt RO		The priority of the configured port port1_cnt_cfg Output packet statistics for queue 4.	16'h0
6	16:31	port1_que5_cnt RO		The priority of the configured port port1_cnt_cfg Output packet statistics for queue 5.	16'h0
7	0:15	port1_que6_cnt RO		The priority of the configured port port1_cnt_cfg Output packet statistics for queue 6.	16'h0
7	16:31	port1_que7_cnt RO		The priority of the configured port port1_cnt_cfg Output packet statistics for queue 7.	16'h0
8	0:15	ts2tq_req_cnt	RO	Scheduler module input scheduling request count. 16'h0	
8	16:31	tq2ts_pkt_cnt	RO	outputs the number of packet descriptions to the scheduling module. 16'h0	

4.5.4 que_count

Storage register description: Statistics of the number of storage packets for each queue in the queue cache, a total of 264 entries, storing each queue separately
The number of package descriptions.

Offset	Bits	Name	R/W	Description
0	0:13	que_cnt RW		The number of packet descriptions stored in each queue in the queue cache

4.6 traffic_schedule

The traffic_schedule_reg register module contains 3 registers and 3 storage registers.

The register list is as follows:

Register Offset	Register Name	Description
12'b0000_0000_0000	tsch_ctrl	Control registers for the traffic_schedule module.
12'b0000_0000_0010:12'b0000_0000_0011	shpupd_ctrl	Token filling interval configuration of the shaped token bucket Set.
12'b0000_0001_0000:12'b0000_0001_1000	ifg_ctrl	Port-based frame interval configuration.

The storage registers are as follows:

Register Offset	Register Name	Description
12'b0000_1000_0000:12'b0000_1100_0001	port_shp	Port shaping configuration
12'b0001_0000_0000:12'b0001_0110_0010	que_sch	Queue Scheduling Configuration
12'b1000_0000_0000:12'b1100_0001_1111	que_shp	Queue Shaping Configuration

4.6.1 tsch_ctrl

Register offset: 12'b0000_0000_0000

Register Description: Traffic_schedule module configuration class register

Bits	Name	R/W	DescriptionWhether	Default
0	shp_ifg_en RW		the shaping module considers the frame interval indication signal when performing shaping token deduction. Indicates that when the shaping token is deducted, the IPG configuration length of the port will be deducted at the same time.	1'b1
1	shp_adjust_en RW		time. When the shaping token is deducted, the correction indication of the packet modification resulting in the length change. The token will calculate the packet modification resulting in length changes; if it is 0, it will only calculate based on the original	1'b1
2	wrr_ifg_en RW	3	packet length. dwrr token calculation frame interval	1'b0
wrr_adjust_en RW			indication dwrr token calculation packet modification length indication	1'b0

4.6.2 shpupd_ctrl

Register offset: 12'b0000_0000_0010:12'b0000_0000_0011

Register Description: The filling interval configuration of the shaping token bucket is in clock cycles. The calculated filling interval is calculated according to the configuration:
 $\text{token_upd_intev} = (\text{shp_intev1_num} * \text{shp_intev1} + \text{shp_intev0_num} * \text{shp_intev0}) / (\text{shp_intev1} + \text{shp_intev0})$. Usually the configuration requires that shp_intev1 is equal to shp_intev0 or separated by 1.

Offset	Bits	Name	R/W	Description	Default
0	0:15	shp_intev1_num RW	The number of times shp_intev1 is used as the filling cycle. shpitv1num_def		
0	16:31	shp_intev1	RW Fill	time interval, in clock cycles. shpitv1_def	
1	0:15	shp_intev0_num RW	The number of times shp_intev0 is used as the filling cycle. shpitv0num_def		
1	16:31	shp_intev0	RW Fill	time interval in clock cycles shpitv0_def	

4.6.3 ifg_ctrl

Register offset: 12'b0000_0001_0000:12'b0000_0001_1000

Register Description: Port-based frame interval configuration, used for shaping token calculation, should include IPG interval and preamble.

Offset	Bits	Name	R/W	Default	Description
0	0:5	port0_ifg_bytes RW	Frame interval configuration of logical port 0, in bytes. 6'd20		
0	8:13	port1_ifg_bytes RW	Frame interval configuration of logical port 1, in bytes. 6'd20		
0	16:21	port2_ifg_bytes RW	Frame interval configuration of logical port 2, in bytes. 6'd20		
0	24:29	port3_ifg_bytes RW	Frame interval configuration of logical port 3, in bytes. 6'd20		
1	0:5	port4_ifg_bytes RW	Frame interval configuration of logical port 4, in bytes. 6'd20		
1	8:13	port5_ifg_bytes RW	Frame interval configuration of logical port 5, in bytes. 6'd20		
1	16:21	port6_ifg_bytes RW	Frame interval configuration of logical port 6, in bytes. 6'd20		
1	24:29	port7_ifg_bytes RW	Frame interval configuration of logical port 7, in bytes. 6'd20		
2	0:5	port8_ifg_bytes RW	Frame interval configuration of logical port 8, in bytes. 6'd20		
2	8:13	port9_ifg_bytes RW	Frame interval configuration of logical port 9, in bytes. 6'd20		
2	16:21	port10_ifg_bytes RW	Frame interval configuration of logical port 10, in bytes. 6'd20		
2	24:29	port11_ifg_bytes RW	Frame interval configuration of logical port 11, in bytes. 6'd20		
3	0:5	port12_ifg_bytes RW	Frame interval configuration of logical port 12, in bytes. 6'd20		
3	8:13	port13_ifg_bytes RW	Frame interval configuration of logical port 13, in bytes. 6'd20		
3	16:21	port14_ifg_bytes RW	Frame interval configuration of logical port 14, in bytes. 6'd20		
3	24:29	port15_ifg_bytes RW	Frame interval configuration of logical port 15, in bytes. 6'd20		
4	0:5	port16_ifg_bytes RW	Frame interval configuration of logical port 16, in bytes. 6'd20		
4	8:13	port17_ifg_bytes RW	Frame interval configuration of logical port 17, in bytes. 6'd20		

4	16:21	port18_ifg_bytes RW	Frame interval configuration of logical port 18, in bytes. 6'd20	
4	24:29	port19_ifg_bytes RW	Frame interval configuration of logical port 19, in bytes. 6'd20	
5	0: 5	port20_ifg_bytes RW	Frame interval configuration of logical port 20, in bytes. 6'd20	
5	8:13	port21_ifg_bytes RW	Frame interval configuration of logical port 21, in bytes. 6'd20	
5	16:21	port22_ifg_bytes RW	Frame interval configuration of logical port 22, in bytes. 6'd20	
5	24:29	port23_ifg_bytes RW	Frame interval configuration of logical port 23, in bytes. 6'd20	
6	0: 5	port24_ifg_bytes RW	Frame interval configuration of logical port 24, in bytes. 6'd20	
6	8:13	port25_ifg_bytes RW	Frame interval configuration of logical port 25, in bytes. 6'd20	
6	16:21	port26_ifg_bytes RW	Frame interval configuration of logical port 26, in bytes. 6'd20	
6	24:29	port27_ifg_bytes RW	Frame interval configuration of logical port 27, in bytes. 6'd20	
7	0: 5	port28_ifg_bytes RW	Frame interval configuration of logical port 28, in bytes. 6'd20	
7	8:13	port29_ifg_bytes RW	Frame interval configuration of logical port 29, in bytes. 6'd20	
7	16:21	port30_ifg_bytes RW	Frame interval configuration of logical port 30, in bytes. 6'd20	
7	24:29	port31_ifg_bytes RW	Frame interval configuration of logical port 31, in bytes. 6'd20	
8	0: 5	port32_ifg_bytes RW	Frame interval configuration of logical port 32, in bytes. 6'd20	

4.6.4 port_shp

Storage register description: Port shaping configuration, including shaping configurations of 33 ports in total.

Offset	Bits	Name	R/W	Description
0	0:20	port_fillrate	R W	The fill rate of port shaping is 8kbps per unit in byte mode. In packet mode, the unit is 16pps.
1	0:15	port_maxsize	R W	Maximum bucket depth for port shaping.
1	16:17	port_shp_quantum RW		The maximum depth of the token bucket is configured in granularity. 00=512B;01=1KB;10=2KB;11=4KB.
1	18	port_shp_mode	R W	Integer mode, 0=byte mode; 1=packet mode.

4.6.5 que_sch

Storage register description: Queue scheduling configuration based on output logical ports, a total of 33 ports.

Offset 0	Bits	Name	R/W	Description
	0:6	qpri0_wrr_weight RW	W	WRR/DWRR scheduling weight for priority 0 queues.
0	8:14	qpri1_wrr_weight RW	W	WRR/DWRR scheduling weight for priority 1 queues.
0	16:22	qpri2_wrr_weight RW	W	WRR/DWRR scheduling weight of the priority 2 queue.
0	24:30	qpri3_wrr_weight RW	W	WRR/DWRR scheduling weight for priority 3 queues.
1	0:6	qpri4_wrr_weight RW	W	WRR/DWRR scheduling weight for priority 4 queues.
1	8:14	qpri5_wrr_weight RW	W	WRR/DWRR scheduling weight for priority 5 queues.
1	16:22	qpri6_wrr_weight RW	W	WRR/DWRR scheduling weight of the priority 6 queue.
1	24:30	qpri7_wrr_weight RW	W	WRR/DWRR scheduling weight for priority 7 queues.
2	0:1	wrr_quantum	R W	The unit of DWRR scheduling weight, that is, the granularity of token filling. 00=512B,01=1KB,10=2KB,11=4KB
2	4:7	wrr_pri	RW W	WRR/DWRR scheduling priority, if the same as SP scheduling priority, SP Scheduling takes priority.
2	8	sch_mode	RW	DWRR/WRR scheduling mode selection, 0=WRR, 1=DWRR.
2	16:23	sch_bmp	RW Q	Queue indication of the 8 queues using WRR/DWRR. A bit of 1 indicates The queue adopts WRR/DWRR scheduling mode. 0 means SP scheduling mode. Mode.

4.6.6 que_shp

Storage register description: Queue shaping parameter configuration, queue shaping token bucket uses dual token bucket shaping, including C bucket and P bucket.
 Each entry in the table includes four queue shaping configurations, of which the eight queues of port 0 use two configurations of entries 0 to 1;
 Use 2~3 item configuration, and so on.

Offset	Bits	Name	R/W	Description
0	0:20	c_fillrate_q0 RW	The fill rate configuration of the C bucket of queue 0, with a granularity of 8kbps.	
1	0:20	p_fillrate_q0 RW	The fill rate of the P bucket of queue 0, with a granularity of 8kbps.	
2	0:15	c_maxsize_q0 RW	Maximum	Maximum bucket depth configuration for bucket C of queue 0
2	16:31	p_maxsize_q0 RW	The maximum bucket depth configuration of the P bucket of queue 0	
3	0:1	shp_quantum_q0 RW		simultaneous configuration unit of queue 0, 00=256KB, 01=1KB, 10=2KB,11=4KB
3	2	shp_mode_q0 RW	c_fillrate_q1	Shaping mode for queue 0, 0=byte mode; 1=packet mode.
4	0:20	RW	The fill rate configuration of the C bucket of queue 1, with a granularity of 8kbps.	
5	0:20	p_fillrate_q1 RW	The fill rate configuration of the P bucket of queue 1, with a granularity of 8kbps.	
6	0:15	c_maxsize_q1 RW		Maximum bucket depth configuration for bucket C of queue 1
6	16:31	p_maxsize_q1 RW		The maximum depth configuration of the P bucket of queue 1.
7	0:1	shp_quantum_q1 RW		The maximum simultaneous configuration unit of queue 1, 00=256KB, 01=1KB, 10=2KB,11=4KB
7	2	shp_mode_q1 RW	c_fillrate_q2	Shaping mode for queue 1, 0 = byte mode; 1 = packet mode.
8	0:20	RW	The fill rate configuration of the C bucket of queue 2, with a granularity of 8kbps.	
9	0:20	p_fillrate_q2 RW	The fill rate configuration of the P bucket of queue 2, with a granularity of 8kbps.	
10	0:15	c_maxsize_q2 RW	Maximum	Maximum bucket depth configuration for bucket C of queue 2
10	16:31	p_maxsize_q2 RW	The maximum configuration of the P bucket of queue 2.	
11	0:1	shp_quantum_q2 RW		simultaneous configuration unit of queue 2, 00=256KB, 01=1KB, 10=2KB,11=4KB
11	2	shp_mode_q2 RW	c_fillrate_q3	Shaping mode for queue 2, 0 = byte mode; 1 = packet mode.
12	0:20	RW	The fill rate configuration of the C bucket of queue 3, with a granularity of 8kbps.	
13	0:20	p_fillrate_q3 RW	The fill rate configuration of the P bucket of queue 3, with a granularity of 8kbps.	
14	0:15	c_maxsize_q3 RW	16:31	Maximum bucket depth configuration for bucket C of queue 3
14	p_maxsize_q3 RW			The maximum depth configuration of the P bucket of queue 3.
15	0:1	shp_quantum_q3 RW		The maximum simultaneous configuration unit of queue 3, 00=256KB, 01=1KB, 10=2KB,11=4KB
15	2	shp_mode_q3 RW		Shaping mode for queue 3, 0 = byte mode; 1 = packet mode.

4.7 traffic_read

The traffic_read_reg register module contains 5 registers and 2 storage registers.

The register list is as follows:

Register Offset	Register Name	Description
8'b0000_0000	slot_ctl	Timing slot control configuration
8'b0000_0010:8'b0000_0011	tx_ctrl	Port Output Control Register
8'b0000_0100:8'b0000_0110	tx_stall	Status register
8'b0000_1000:8'b0000_1100	tag_cfg	Packet modifies the configuration parameters of the vian tag class
8'b0010_0000:8'b0011_0001	trd_cnt	Output Statistics Register

The storage registers are as follows:

Register Offset	Register Name	Description
8'b0100_0000:8'b0111_1111	slot_cfg	Slot configuration register based on port timing arrangement
8'b1000_0000:8'b1010_0000	port_map	Logical port to physical port mapping configuration

4.7.1 slot_ctl

Register offset: 8'b0000_0000

Register Description: Timing slot control configuration.

Bits	Name R/W	Description	Default
0:5	slot_num	The total number of RW Slots is usually configured based on the total port rate, with 1G as the unit. Bit.	slot_num_def

4.7.2 tx_ctrl

Register offset: 8'b0000_0010:8'b0000_0011

Register Description: Output enable based on output logic port.

Offset	Bits	Name	R/W	Description	Default
0	0:5	port_tx_enable_31to0	RW	Output logical port 0~31 transmit enable. 32'hffffffff	
1	0	port_tx_enable_32	RW	Output Transmit enable for logical port 32.	1'b1

4.7.3 tx_stall

Register offset: 8'b0000_0100:8'b0000_0110

Register Description: Port-based status register.

Offset	Bits	Name	R/W	Description	Default
0	0:29	cmactx_stall RO		CMAC input back pressure indication for each physical port, Indicates back pressure, stop sending data to this MAC.	1 30'h0
1	0	dma0_tx_stall RO		DMA0 channel input back pressure indication, 1 stops sending data Back	1'h0
1	1	dma1_tx_stall RO		pressure indication to DMA0 DMA1 channel input, 1 stops sending data Back	1'h0
1	2	cptx_stall RO		pressure indication to DMA1 CP channel input, 1 stops sending data to CP module	1'h0
2	0:29	cmacrx_fc RO		is based on MAC flow control indication. If it is 1, the current data packet is sent. Sending completed, stop sending subsequent packets to this MAC	30'h0

4.7.4 tag_cfg

Register offset: 8'b0000_1000:8'b0000_1100

Register Description: Configuration register for vlan label modification.

Offset	Bits	Name	R/W	Description	Vlan	Default
0	0:15	ctag_type	R W	is modified when ctag type is configured.	16'h8100	
1	0:15	stag_type0	R W	When modifying Vlan, configure stag type	16'h88a8	
1	16:31	stag_type1	R W	0 When modifying Vlan, configure stag	16'h88a8	
2	0:15	stag_type2	R W	type 1 When modifying Vlan, configure	16'h88a8	
2	16:31	stag_type3	R W	stag type 2 When modifying Vlan, configure	16'h88a8	
3	0:31	port_stag_sel_31to0 RW		stag type 3 Select and configure stag based on output ports 0~16. 2 bits per port select, 00 = select stag_type0,01=Select stag_type1,10=Select stag_type2,11=Select stag_type3.	32'h0	
4	0:27	port_stag_sel_59to32 RW		Select stag type based on output ports 17~29 Select configuration, each port has 2 bits for selection indication, 00= select stag_type0;01=select stag_type1;10= Select stag_type2;11=Select stag_type3.	18'h0	

4.7.5 trd_cnt

Register offset: 8'b0010_0000:8'b0011_0001

Register Description: Port-based statistics register for sending packets.

Offset	Bits	Name	R/W	Description	RO Statistics of packets	Default
0	0:15	tm2mac0_pkt_cnt	sent to MAC0.	16'h0		
0	16:31	tm2mac1_pkt_cnt	Statistics	of packets sent by RO to MAC1.	16'h0	
1	0:15	tm2mac2_pkt_cnt	Statistics	of packets sent by RO to MAC2.	16'h0	
1	16:31	tm2mac3_pkt_cnt	Statistics	of packets sent by RO to MAC3.	16'h0	
2	0:15	tm2mac4_pkt_cnt	Statistics	of packets sent by RO to MAC4.	16'h0	
2	16:31	tm2mac5_pkt_cnt	Statistics	of packets sent by RO to MAC5.	16'h0	
3	0:15	tm2mac6_pkt_cnt	Statistics	of packets sent by RO to MAC6	16'h0	
3	16:31	tm2mac7_pkt_cnt	RO	Statistics of packets sent to MAC7	16'h0	
4	0:15	tm2mac8_pkt_cnt	RO	Statistics of packets sent to MAC8	16'h0	
4	16:31	tm2mac9_pkt_cnt	RO	Statistics of packets sent to MAC9	16'h0	
5	0:15	tm2mac10_pkt_cnt	Statistics	of packets sent by RO to MAC10	16'h0	
5	16:31	tm2mac11_pkt_cnt	Statistics	of packets sent by RO to MAC11	16'h0	
6	0:15	tm2mac12_pkt_cnt	Statistics	of packets sent by RO to MAC12	16'h0	
6	16:31	tm2mac13_pkt_cnt	Statistics	of packets sent by RO to MAC13	16'h0	
7	0:15	tm2mac14_pkt_cnt	Statistics	of packets sent by RO to MAC14	16'h0	
7	16:31	tm2mac15_pkt_cnt	Statistics	of packets sent by RO to MAC15	16'h0	
8	0:15	tm2mac16_pkt_cnt	Statistics	of packets sent by RO to MAC16	16'h0	
8	16:31	tm2mac17_pkt_cnt	Statistics	of packets sent by RO to MAC17	16'h0	
9	0:15	tm2mac18_pkt_cnt	Statistics	of packets sent by RO to MAC18	16'h0	
9	16:31	tm2mac19_pkt_cnt	Statistics	of packets sent by RO to MAC19	16'h0	
10	0:15	tm2mac20_pkt_cnt	Statistics	of packets sent by RO to MAC20	16'h0	
10	16:31	tm2mac21_pkt_cnt	Statistics	of packets sent by RO to MAC21	16'h0	
11	0:15	tm2mac22_pkt_cnt	Statistics	of packets sent by RO to MAC22	16'h0	
11	16:31	tm2mac23_pkt_cnt	Statistics	of packets sent by RO to MAC23	16'h0	
12	0:15	tm2mac24_pkt_cnt	Statistics	of packets sent by RO to MAC24	16'h0	
12	16:31	tm2mac25_pkt_cnt	Statistics	of packets sent by RO to MAC25	16'h0	

13	0:15	tm2mac26_pkt_cnt	Statistics of packets sent by RO to MAC26	16'h0	
13	16:31	tm2mac27_pkt_cnt	Statistics of packets sent by RO to MAC27	16'h0	
14	0:15	tm2mac28_pkt_cnt	Statistics of packets sent by RO to MAC28	16'h0	
14	16:31	tm2mac29_pkt_cnt	Statistics of packets sent by RO to MAC29	16'h0	
15	0:15	tm2cptx_pkt_cnt	Statistics of packets sent by RO to CP	16'h0	
15	16:31	tm2dma0_pkt_cnt	RO	Statistics of packets sent to DMA0	16'h0
16	0:15	tm2dma1_pkt_cnt	RO	Statistics of packets sent to DMA1	16'h0
17	0:31	tm2mac_byte_cnt	RO	Total byte statistics sent to MAC	32'h0

4.7.6 slot_cfg

Storage register description: The transmission timing configuration of each port, a maximum of 64, including only the logical ports mapped by the MAC port.

Bits	Name	R/W	Description
0:5	slot_lg_port		logical port configuration

4.7.7 port_map

Storage register description: Mapping from logical ports to output physical ports, including MAC interface, CPTX, DMA0 and DMA1.

Bits	Name	R/W	Description
0:5	phy_port	R W	Physical port configuration

4.8 ptp

The ptp_reg register block contains 26 registers; it also contains 3 storage registers.

The register list is as follows:

Register Offset	Register Name	Description
13'b0_0000_0000_0000:13'b0_0000_0000_0001	ptp_pkt_gen_ctl	PTP automatic packet sending function delay information configuration Place
13'b0_0000_0000_0010	ptp_sync_en_ctl	PTP module enables time synchronization
13'b0_0000_0000_0011	ptp_offset_trig_ctl	Timestamp modification configuration trigger register
13'b0_0000_0000_0100	ptp_cm_tod_rx_ctl0	Rx direction PPS/TOD control register
13'b0_0000_0000_0101	ptp_cm_tod_rx_ctl4	Rx direction Ptp time capture control Memory
13'b0_0000_0000_0110	ptp_cm_tod_tx_ctl0	Time parameter setting
13'b0_0000_0000_0111	ptp_cm_tod_tx_ctl1	PPS/TOD control register
13'b0_0000_0000_1000	ptp_cm_tod_tx_ctl2	PPS/TOD control register
13'b0_0000_0000_1001	ptp_cm_tod_tx_ctl3	PPS/TOD control register
13'b0_0000_0000_1010	ptp_cm_tod_tx_ctl4	PPS/TOD control register
13'b0_0000_0000_1011	ptp_cm_tod_tx_ctl5	PPS/TOD control register
13'b0_0000_0000_1100	ptp_cm_tod_tx_ctl6	PTP module nanosecond carry configuration
13'b0_0000_0000_1101	ptp_cm_tod_tx_ctl7	PPS/TOD control register
13'b0_0000_0000_1110	ptp_time_rate_ctl	PTP time unit configuration
13'b0_0000_0001_0000:13'b0_0000_0001_0001	ptp_time_drift	PTP clock adjustment function
13'b0_0000_0001_0100:13'b0_0000_0001_0110	ptp_time_offset_ctl	PTP module time adjustment function

13'b0_0000_0001_1000	ptp_time_comp_ctl	PTP time compensation complete indication
13'b0_0000_0001_1001	ptp_cm_rx_tod	Record the internal timestamp status of the capture moment Memory
13'b0_0000_0001_1010	ptp_cm_cap_tod	Record the internal timestamp status of the capture moment Memory
13'b0_0000_0001_1011	ptp_cm_tod_rx_ctl1b	Rx direction PPS/TOD receiving status Memory
13'b0_0000_0001_1100	ptp_cm_tod_rx_ctl2b	Rx direction PPS/TOD receiving status Memory
13'b0_0000_0001_1101	ptp_cm_tod_rx_ctl3b	Rx direction PPS/TOD receiving status Memory
13'b0_0000_0001_1110	ptp_cm_tod_rx_ctl4b	Rx direction Ptp time capture control Memory
13'b0_0000_0001_1111	ptp_cm_tod_rx_ctl5b	Sync cap capture time TOD frame UTC time
13'b0_0000_0010_0000	ptp_ram_init_done	Initialization completion indication
13'b0_0000_0010_0100:13'b0_0000_0010_0101	ptp_time_ctl	Ptp module real time

The storage register list is as follows:

Register Offset	Register Memory	Description
13'b1_0000_0000_0000:13'b1_1111_1111_1111	ptp_pkt_srm	PTP automatic packet sending function data packet content
13'b0_0010_0000_0000: 13'b0_0011_1111_1111	ptp_pktinfo_srm	PTP automatic packet sending function data packet information
13'b0_0011_0000_0000: 13'b0_0011_1111_1111	ptp_seqid_srm	Send PTP packet seqid configuration

4.8.1 ptp_pkt_gen_ctl

Register offset: 13'b0_0000_0000_0000:13'b0_0000_0000_0001

Register description: PTP automatic packet sending function delay information setting.

Offset	Bits	Name	R/W	Description	Default
0	0:31	cf_entry_delay	RW	The global delay time is the configured value x8ns	32'd100
1	0:31	cf_global_delay	RW	The delay time of each entry is the configured value x8ns	32'd1000

4.8.2 ptp_sync_en_ctl

Register offset: 13'b0_0000_0000_0010

Register Description: Ptp module enables time synchronization.

Bits	Name	R/W	Description	Default
0	cf_sync_time_en	RW	packet sending function enabled	1'b0
1	ptp_auto_send_en	RW	Time synchronization enabled	1'b0

4.8.3 ptp_offset_trig_ctl

Register offset: 13'b0_0000_0000_0011

Register Description: Timestamp modification configuration trigger register.

Bits	Name	R/W	Description	Default
0	cf_time_offset_trig	RW	modification configuration trigger register, configure this register The modified value is then written to the hardware counter.	1'b0

4.8.4 ptp_cm_tod_rx_ctl0

Register offset: 13'b0_0000_0000_0100

Register Description: Rx direction PPS/TOD control register.

Bits	Name	R/W	Description	Default
0	cf_pps_tod_rx_en	RW	Receive direction Pps time enable	1'b1

4.8.5 ptp_cm_tod_rx_ctl4

Register offset: 13'b0_0000_0000_0101

Register Description: Rx direction Ptp time capture control register.

Bits	Name	R/W	Description	Default
0	cf_rx_time_cap_en	RW/WC	capture enable	1'b0

4.8.6 ptp_cm_tod_tx_ctl0

Register offset: 13'b0_0000_0000_0110

Register Description: Time parameter setting.

Bits	Name	R/W	Description	Default
0	cf_cm_tod_tx_en	RW PPS	TOD Tx direction time transmission able	1'b1
1	cf_send_state_frame_en	R W	Time status frame sending enable, with The body code is as follows: "1" sends the time status frame; "0" does not send the time status frame. Sending time information frame;	1'b1
2:17	cf_baud_rate_tx_ctl	R W	Baud rate setting	16'h32dc

4.8.7 ptp_cm_tod_tx_ctl1

Register offset: 13'b0_0000_0000_0111

Register Description: Tx direction PPS/TOD control register.

Bits	Name	R/W	Description	Default
0:31	cf_tx_gps_diff	RW GPS	time and UTC time offset 32'h12d53d93	

4.8.8 ptp_cm_tod_tx_ctl2

Register offset: 13'b0_0000_0000_1000

Register Description: Tx direction PPS/TOD control register.

Bits	Name	R/W	Description	Default
0:7	cf_leaps	R W	Leap Seconds (GPS-UTC) The offset between GPS time and UTC time, default The default value is 33 seconds	8'h0
8:15	cf_sec_status	R W	Pulse-second status 0x00 = Normal 0x01 = Degraded 0x02 = Not available Other reservations	8'h0
16:23	cf_tacc	R W	PPS jitter magnitude (0-255): 0-0ns 1-15ns 2-30ns ... 255-meaningless Note: Transmission and base station equipment are fixed settings is 255	8'h1
24:31	cf_src_type	R W	Clock source type: 0x00: Beidou 0x01: GPS 0x02: 1588	8'h2

			0x03: Other	
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4.8.9 ptp_cm_tod_tx_ctl3

Register offset: 13'b0_0000_0000_1001

Register Description: Tx direction PPS/TOD control register.

Bits	Name	R/W	Description	Default
0:15	cf_src_status	R W	<p>Clock source working status:</p> <p>GPSfix Type, range 0..3</p> <p>0x00 = no fix</p> <p>0x01 = dead reckoning only</p> <p>0x02 = 2D-fix</p> <p>0x03 = 3D-fix</p> <p>0x04 = GPS + dead reckoning combined</p> <p>0x05 = Time only fix</p> <p>0x06..0xff = reserved</p>	16'h5
16:31	cf_src_alm	R W	<p>Clock source status alarm:</p> <p>Bit 0: not used</p> <p>Bit 1: Antenna open</p> <p>Bit 2: Antenna shorted</p> <p>Bit 3: Not tracking satellites</p> <p>Bit 4: not used</p> <p>Bit 5: Survey-in progress</p> <p>Bit 6: no stored position</p>	16'h11fe

			Bit 7: Leap second pending Bit 8: In test mode Bit 9: Position is questionable Bit 10: not used Bit 11: Almanac not complete Bit 12: PPS was generated	
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4.8.10 ptp_cm_tod_tx_ctl4

Register offset: 13'b0_0000_0000_1010

Register Description: Tx direction PPS/TOD control register.

Bits	Name	R/W	Description	Default
0	cf_time_comp_sign	R W	Sign of the PPS signal compensation value	1'b0
1:30	cf_time_comp_data	RW	PPS signal compensation value (CLK is single Bit)	30'h0

4.8.11 ptp_cm_tod_tx_ctl5

Register offset: 13'b0_0000_0000_1011

Register Description: Tx direction PPS/TOD control register.

Bits	Name	R/W	Description	Default
0:31	cf_duty_cycle	R W	PPS signal pulse width	32'h4c4b40

4.8.12 ptp_cm_tod_tx_ctl6

Register offset: 13'b0_0000_0000_1100

Register Description: PTP module nanosecond carry configuration.

Bits	Name	R/W	Description	Default
0:29	cf_ns_carry_length	R W	Nanosecond carry length	30'h3b9aca00

4.8.13 ptp_cm_tod_tx_ctl7

Register offset: 13'b0_0000_0000_1101

Register Description: Tx direction PPS/TOD control register.

Bits	Name	R/W	Description	Default
0:19	cf_send_time	RW PPS	signal and TOD signal transmission time interval	20'h2dc6c
20:27	cf_resv_mask	R W	Masked fields sent by TOD	8'h0

4.8.14 ptp_time_rate_ctl

Register offset: 13'b0_0000_0000_1110

Register Description: PTP time unit configuration.

Bits	Name	R/W	Description	Default
0:29	time_rate	R W	PTP time unit configuration	30'd8

4.8.15 ptp_time_drift

Register offset: 13'b0_0000_0001_0000:13'b0_0000_0001_0001

Register Description: PTP clock adjustment function.

Offset 0	Bits	Name	R/W	Description	Default
	0:29	cf_nor_add_frac_ns	RW/WC	Fractional part of nanosecond count	30'h0
1	0:29	cf_nor_add_ns	RW/WC	Nanosecond count	30'd8

4.8.16 ptp_time_offset_ctl

Register offset: 13'b0_0000_0001_0100:13'b0_0000_0001_0110

Register description: PTP module time adjustment function.

Offset 0	Bits	Name	R/W	Description	Default
	0	cf_add_ns_sign	RW/WC	Nanosecond count sign	1'h0
0	1:30	cf_add_ns	RW/WC	Nanosecond count	30'h0
0	31	cf_add_sec_sign	RW/WC	Second count sign	1'h0
1	0:30	cf_add_sec	RW/WC	Second count	31'h60011250
1	31	cf_add_frac_ns_sign	RW/WC	Fractional part of cf_add_frac_ns	1'h0
2	0:29		RW/WC	Nanosecond count fractional part	30'd0

4.8.17 ptp_time_comp_ctl

Register offset: 13'b0_0000_0001_1000

Register Description: PTP time compensation completion indication.

Bits	Name	R/W	Description/Indicates	Default
0	cf_compensate_complete	RO	that time compensation is complete	1'b0

4.8.18 ptp_cm_rx_tod

Register offset: 13'b0_0000_0001_1001

Register Description: Records the internal timestamp status register of the capture moment.

Bits	Name	R/W	Description	Default
0	cm_rx_tod_sec	RO Sync cap	captures the seconds portion of the moment storage Content	32'h0

4.8.19 ptp_cm_cap_tod

Register offset: 13'b0_0000_0001_1010

Register Description: Records the internal timestamp status register of the capture moment.

Bits	Name	R/W	Description	Default
0	cm_int_cap_sec	RO Sync cap	captures the nanoseconds stored at the moment Part	32'h0

4.8.20 ptp_cm_tod_rx_ctl1b

Register offset: 13'b0_0000_0001_1011

Register Description: Rx direction PPS/TOD receive status register.

Bits	Name	R/W	Description	Default
0:7	cf_rx_src_type	RO	Clock source type: 0x00: Beidou 0x01: GPS 0x02:1588 0x03: Other	8'h0
8:15	cf_rx_tacc	RO	PPS jitter magnitude (0-255): 0-0ns 1-15ns 2-30ns ... 255-meaningless Note: Transmission and base station equipment Set to	8'h0

			255	
16:23	cf_rx_sec_status	RO	<p>Pulse-second status</p> <p>0x00 = Normal</p> <p>0x01 = Degraded</p> <p>0x02 = Not available</p> <p>Other reservations</p>	8'h0
24:31	cf_rx_leaps	RO	<p>Leap Seconds (GPS-UTC)</p> <p>The offset between GPS time and UTC time, default</p> <p>The default value is 33 seconds</p>	8'h0

4.8.21 ptp_cm_tod_rx_ctl2b

Register offset: 13'b0_0000_0001_1100

Register Description: Rx direction PPS/TOD receive status register.

Bits	Name	R/W	Description	Default
0:15	cf_rx_src_status	RO	<p>Clock source working status:</p> <p>GPSfix Type, range 0..3</p> <p>0x00 = no fix</p> <p>0x01 = dead reckoning only</p> <p>0x02 = 2D-fix</p> <p>0x03 = 3D-fix</p> <p>0x04 = GPS + dead reckoning combined</p> <p>0x05 = Time only fix</p> <p>0x06..0xff = reserved</p>	16'h0
16:31	cf_rx_src_alm	RO	<p>Clock source status alarm:</p> <p>Bit 0: not used</p>	16'h0

			Bit 1: Antenna open Bit 2: Antenna shorted Bit 3: Not tracking satellites Bit 4: not used Bit 5: Survey-in progress Bit 6: no stored position Bit 7: Leap second pending Bit 8: In test mode Bit 9: Position is questionable Bit 10: not used Bit 11: Almanac not complete Bit 12: PPS was generated	
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4.8.22 ptp_cm_tod_rx_ctl3b

Register offset: 13'b0_0000_0001_1101

Register Description: Rx direction PPS/TOD receive status register.

Bits	Name	R/W	Description	Default
0	cf_rx_crc_err	RO	RO receives TOD frame CRC error alarm	1'b0
1	cf_rx_posedge_pps	RO	Pps rising edge, can be used for statistics	1'b0
2	cf_rx_rcv_inf_finish	RO	RX receives TOD information frame indication, can For statistics	1'b0
3	cf_rx_rcv_sta_finish	RO	RX receives TOD status frame indication, can For statistics	1'b0
4	cf_rx_pps_los	RO	PPS signal LOS alarm	1'b0
5	cf_rx_tod_los	RO	TOD signal LOS alarm	1'b0

4.8.23 ptp_cm_tod_rx_ctl4b

Register offset: 13'b0_0000_0001_1110

Register Description: Rx direction Ptp time capture control register.

Bits	Name	R/W	Description	Default
0	cf_rx_time_cap_complete	RO	Capture time action completion indication	1'b0

4.8.24 ptp_cm_tod_rx_ctl5b

Register offset: 13'b0_0000_0001_1111

Register Description: Rx direction TOD Received UTC register.

Bits	Name	R/W	Description	Default
0	cf_rx_time_sync_cap_utc	RO	Sync cap capture time TOD frame UTC time	32'h0

4.8.25 ptp_ram_init_done

Register offset: 13'b0_0000_0010_0000

Register Description: Initialization completion indication.

Bits	Name	R/W	Description	Default
0	ptp_ram_init_done	RO	RAM initialization completed indication	1'b0

4.8.26 ptp_time_ctl

Register offset: 13'b0_0000_0010_0100:13'b0_0000_0010_0101

Register description: Ptp module real time.

Offset	Bits	Name	R/W	Description	Default
0	0:31	cf_ns	RO	valueSeconds	32'h0
1	0:31	cf_sec	RO	value	32'h0

4.8.27 ptp_pkt_srm

Storage register description: The content of this table entry is the data packet content of the PTP automatic packet sending function.

Offset	Bits	Name	R/W	Description
0	0:31	pkt_data0	R W	Packet Contents
1	0:31	pkt_data1	R W	Packet Contents
2	0:31	pkt_data2	R W	Packet Contents
3	0:31	pkt_data3	R W	Packet Contents
4	0:31	pkt_data4	R W	Packet Contents
5	0:31	pkt_data5	R W	Packet Contents
6	0:31	pkt_data6	R W	Packet Contents
7	0:31	pkt_data7	R W	Packet Contents

4.8.28 ptp_pktinfo_srm

Storage register description: PTP automatic packet sending function data packet information.

Bits	Name	R/W	Description
0	chk_sum_en	R W	chkSum checksum enable
1:8	seq_id_offset	R W	SeqId offset
9:16	valid_bytes	R W	Data packet effective length
17:22	pkt_dport	R W	Destination port indication
23:25	pkt_priority	R W	Send priority indication
26	ppbypass	R W	Indicates PP straight through
27	enable_entry	R W	Ingress Enable

4.8.29 ptp_seqid_srm

Storage register description: The content of this entry is the seqId value.

Bits	Name	R/W	Description
0:15	seq_id	R W	SeqId value

4.9 oam_transmit

The oam_transmit_reg register module contains one 32-bit register: flow_tx_enable register; and three storage

Registers: flow_pkt register, flow_payload_ctrl register, flow_statis register, and flow_tx_ctrl register.

The register list is as follows:

Register Offset	Register Name	Description
13'b0_0000_0000_0000:13'b0_0000_0000_0010	flow_tx_enable	Transmit enable configuration for each flow

The storage register list is as follows:

Register Offset	Register Memory	Description
13'b1_0000_0000_0000:13'b1_1011_1111_1111	flow_pkt	Send data packet header content configuration
13'b0_0001_0000_0000: 13'b0_0001_1011_1111	flow_payload_ctrl	Send data packet payload configuration
13'b0_0000_1000_0000: 13'b0_0000_1101_1111	flow_statis	Statistics of sent packets
13'b0_0100_0000_0000: 13'b0_0111_1101_1111	flow_tx_ctrl	packet sending control

4.9.1 flow_tx_enable

Register offset: 13'b0_0000_0000_0000:13'b0_0000_0000_0010

Register Description: OAM sends the send enable based on each flow. Set the corresponding bit to 1 to start sending and set it to 0 to stop sending. There are 96 bits in total.

Enable the sending configuration of the stream.

Offset	Bits	Name	R/W	Description	Default
0	0:31	flow_tx_en_31to0	RW Stream	0-31 send enable configuration Set.	32'h0

1	0:31	flow_tx_en_63to32	RW Stream	32~63 send enable Configuration	32'h0
2	0:31	flow_tx_en_95to64	RW Stream	64~95 send enable Configuration.	32'h0

4.9.2 flow_pkt

Storage register description: Packet header data configuration of the sending stream, 96 streams share 1536 depth, 64-bit wide packet header configuration.

Offset 0	Bits	Name	R/W	Description
	0:31	pktdata_lo	RW	Packet header data lower 32bit configuration
1	0:31	pktdata_hi	RW	Packet header data high 32bit configuration

4.9.3 flow_payload_ctrl

Storage register description: Transmit data packet configuration for each stream, 96 streams in total.

Offset	Bits	Name	R/W	Description
0	0:10	endaddr		The send packet header of the RO flow is at the end address of the flow_pkt table entry Configuration
0	16:26	iniaddr		The send packet header of the RW flow is at the starting address of the flow_pkt table entry Configuration
1	0:15	pktload_byte	RO	The payload bytes of the flow's packets are configured.
1	16:26	pktload_mode	R W	Payload mode configuration 00/01=fixed, continuous sending pktload_byte; 10=increment; 11=decrement;

4.9.4 flow_statis

Storage register description: Send statistics for each stream, a total of 96 streams.

Bits	Name	R/W	Description
0:27	flow_cnt	R W	Statistics of packets sent by the flow

4.9.5 flow_tx_ctrl

Storage register description: Stream sending configuration register, a total of 96 streams.

Offset 0	Bits	Name R/W Description	
	0:31	flow_tx_intev1_lo	RO The high-order portion of the packet sending interval 1 for each flow.
1	0:3	flow_tx_intev1_hi	RW The lower part of the configuration of the transmission interval 1 of each flow
1	4:31	flow_tx_num1	R W Number of packets sent based on interval 1
2	0:31	flow_tx_intev0_lo	RW The lower part of the packet transmission interval 0 of each flow
3	0:3	flow_tx_intev0_hi	RW The high part of the packet transmission interval 0 of each flow
3	4:31	flow_tx_num0	R W Number of packets sent based on interval 0
4	0:5	flow_tx_dport	R W Destination logical port indicator for the flow
4	6:8	flow_tx_priority	R W Stream sending priority configuration
4	9	flow_tx_ppbypass	RW Ppbypass indication, 1 means PP does not process, Then configure
4	10	flow_crc_ind	R W 0=without crc, 1=withcrc

4	11:12	flow_tx_mode	R W	0 = continue to send packets at intev1 intervals; 1=send tx_num1 packets at intev1 intervals; 2 = tx_num0 packets occur at intervals of intev0, then continue at intervals of intev1 sends packets at intervals; 3 = tx_num0 packets occur at intervals of intev0, then intev1 sends tx_num1 packets at intervals.
4	16:29	flow_tx_len	WO	Length configuration of the data packet sent by the stream

4.10 dma_adapter

The dma_adapter_reg register module contains 2 registers, as shown in the following table:

Register Offset	Register Name	Description
6'b00_0000: 6'b00_0001	delimiter	Delimiter flag configuration field
6'b00_0010	timeout	DMA transmit direction timeout configuration

4.10.1 delimiter

Register offset: 6'b00_0000: 6'b00_0001

Register Description: Delimiter flag configuration field.

Offset 0	Bits	Name	R/W	Description	Default
	0:31	start_ind_cfg	RW packet	header delimiter flag configuration	32'hc704dd7b
1	0:31	end_ind_cfg	RW Packet	end delimiter flag configuration	32'h004c1db7

4.10.2 timeout

Register offset: 6'b00_0010

Register Description: DMA transmit direction timeout configuration.

Bits	Name	R/W	Description	Default
0:23	timeout_thd	R W	DMA send timeout configuration, in clock The unit is cycle. The configuration is 256 clock cycle, 1.28us	24'd200

5 PP

5.1 pptop_reg

The pptop_reg register module contains 2 registers, the register list is as follows:

Register Offset 1'b0	Register Name	Description
1'b1	pt_init_done_sta	top init state configuration
	pt_module_init_done_sta	Module init state configuration

5.1.1 pt_init_done_sta

Register offset: 1'b0

Register Description: PP initialization completion indication

Bits	Name	R/W	Description	Default
0	pt_init_done_sta_init_done_state	RO	pp top init done indication signal	1'd0

5.1.2 pt_module_init_done_sta

Register offset: 1'b1

Register Description: pp module ram initialization completion indication

Bits	Name	R/W	Description	Default
0	pt_module_init_done_sta_edst_init_done_state	RO	edst module ram init done indication signal	1'd0
1	pt_module_init_done_sta_epol_init_done_state	RO	epol module ram init done indication signal	1'd0
2	pt_module_init_done_sta_eacl_init_done_state	RO	eacl module ram init done indication signal	1'd0
3	pt_module_init_done_sta_epf_init_done_state	RO	epf module ram init done indication signal	1'd0
4	pt_module_init_done_sta_eee_init_done_state	RO	eee module ram init done indication signal	1'd0
5	pt_module_init_done_sta_idest_init_done_state	RO	idst module ram init done indication signal	1'd0
6	pt_module_init_done_sta_ipol_init_done_state	RO	ipol module ram init done indication signal	1'd0
7	pt_module_init_done_sta_iacl_init_done_state	RO	iacl module ram init done indication signal	1'd0
8	pt_module_init_done_sta_ifwd_init_done_state	RO	ifwd module ram init done indication signal	1'd0
9	pt_module_init_done_sta_inet_init_done_state	RO	inet module ram init done indication signal	1'd0
10	pt_module_init_done_sta_ivt_init_done_state	RO	ivt module ram init done indication signal	1'd0

5.2 ipr0_reg

The ipr0_reg register module contains 8 registers, listed as follows:

Register Offset	Register Name	Description
5'b0_0000		Global Configuration
5'b0_0100:5'b0_0110	chksum_ctl	IPv4 packet checksum configuration
5'b0_1000	loop_ctl	Loopback processing configuration information
5'b1_0000:5'b1_0100	stag bmp_ctl	stag port configuration
5'b1_1000:5'b1_1001	stag_tpid_ctl	stag TPID

5'b1_1010	ctag_tpid_ctl	ctag TPID udf
5'b1_1011	offset_ctl	configuration
5'b1_1100	out_cnt_ctl	Packet Counter

5.2.1 ctl

Register offset: 5'b0_0000

Register Description: Packet Parsing Configuration

Bits	Name	R/W	Description	Default
0	ctl_pr_exclude_crc	RW	frame parsing content does not include the crc field enable	1'd0
1	ctl_l2_pr_err_drop_en	RW	L2 header parsing error discard enable	1'd0
2	ctl_l3_pr_err_drop_en	RW	L3 header parsing error discard enable	1'd0
3	ctl_l4_pr_err_drop_en	RW	L4 header parsing error discard enable	1'd0
4	ctl_l5_pr_err_drop_en	RW	L4 header parsing error discard Enable	1'd0
5	ctl_pr_err_trap_en	RW	packet parsing error trap to CPU Enable ipv6	1'd0
6:13	ctl_ipv6_ext_hop_proto_id	RW	hop-by-hop extension header protocol	8'd0
14	ctl_alw_none_zero_ip_flag	RW	number Allow ipv4 frag[2] to be non-zero Enable	1'd0
15	ctl_alw_df_mf	RW	Allow DF and MF of IPv4 to be 1 Enable	1'd0

5.2.2 cksum_ctl

Register offset: 5'b0_0100:5'b0_0110

Register description: cksum configuration of ipv4 packets

Offset	Bits	Name	R/W	Description	Default
0	0:31	chksum_ctl_l3_cksum_en_0	RW 0:2	ipv4 checksum check enable	32'd0
1		chksum_ctl_l3_cksum_en_1	RW 3:31	ipv4 checksum check enable	3'd0
1		chksum_ctl_l3_chk_strict_0	RW	ipv4 strict check checkSum enable 29'd0	
2	0:5	chksum_ctl_l3_chk_strict_1	RW	ipv4 strict check checkSum enable 6'd0	
2	6:21	chksum_ctl_l3_cksum	RW	ipv4 checkSum value	16'd0

5.2.3 loop_ctl

Register offset: 5'b0_1000

Register Description: Loopback Packet Control

Bits	Name	R/W	Description	Default
0:7	loop_ctl_loop_bypass	RW	Loopback packet bypass indication, 0: no bypass; 1: bypass	8'd0

5.2.4 stag bmp_ctl

Register offset: 5'b1_0000: 5'b1_0100

Register Description: stag port configuration

Offset	Bits 0	Name	R/W	Description	Default
	0:31	stag_bmp_ctl_stag_bmp_0	R W	Stag bmp of each port, 4 bits per port	32'd286 331153
1	0:31	stag_bmp_ctl_stag_bmp_1	R W	Stag bmp of each port, 4 bits per port	32'd286 331153
2	0:31	stag_bmp_ctl_stag_bmp_2	R W	Stag bmp of each port, 4 bits per port	32'd286 331153
3	0:31	stag_bmp_ctl_stag_bmp_3	R W	Stag bmp of each port, 4 bits per port	32'd286 331153
4	0:11	stag_bmp_ctl_stag_bmp_4	R W	stag bmp of each port, 4 bits per port	12'd273

5.2.5 stag_tpid_ctl

Register offset: 5'b1_1000: 5'b1_1001

Register Description: stag TPID

Offset	Bits 0	Name	R/W	Description	Default
0:15	0 16:31	stag_tpid_ctl_stag_tpid0	RW	stagTpid0	16'd34984
1 0:15	1 16:31	stag_tpid_ctl_stag_tpid1	RW	stagTpid1	16'd0
		stag_tpid_ctl_stag_tpid2	RW	stagTpid2	16'd0
		stag_tpid_ctl_stag_tpid3	RW	stagTpid3	16'd0

5.2.6 ctag_tpid_ctl

Register offset: 5'b1_1010

Register Description: ctag TPID

Bits	Name	R/W	Description	Default
0:15	ctag_tpid_ctl_ctag_tpid	R W	ctagTpid	16'd33024

5.2.7 offset_ctl

Register offset: 5'b1_1011

Register Description: udf Configuration

Bits	Name	R/W	Description	Default
0: 5	offset_ctl_l3_udf0_offset	RW L3	custom field 0 offset, 0 means L3 header The first byte, and so on	6'd0
6:11	offset_ctl_l3_udf1_offset	RW L3	custom field 1 offset, 0 means L3 header The first byte, and so on	6'd0
12:17	offset_ctl_l4_udf0_offset	RW L4	custom field 0 offset, 0 means L4 header The first byte, and so on	6'd0
18:23	offset_ctl_l4_udf1_offset	RW L4	custom field 1 offset, 0 means L4 header The first byte, and so on	6'd0

5.2.8 out_cnt_ctl

Register offset: 5'b1_1010

Register Description: Packet Counter

Bits	Name	R/W	Description	Default
0:15	out_cnt_ctl_pkt_cnt	RW/WC	Module output statistics	16'd0

5.3 ivt_reg

The ivt_reg register block contains 18 registers and 14 storage registers.

The register list is as follows:

Register Offset	Register Name	Description
14'b00_0000_0000_0000	loop_ctl	Loopback processing configuration information
14'b00_0000_0000_0001	ctl	Global Configuration Registers
14'b00_0000_0000_0010	cp_ctl	L2PDU Identification
14'b00_0000_0000_0100:14'b00_0000_0000_0101	pdu_smac_ctl	L2PDU Identification
14'b00_0000_0000_0110:14'b00_0000_0000_0111	pdu_op_ctl	L2PDU Identification
14'b00_0000_0000_1000:14'b00_0000_0000_1011	pdu_ctl0	L2PDU Identification
14'b00_0000_0000_1100:14'b00_0000_0000_1111	pdu_ctl1	L2PDU Identification
14'b00_0000_0001_0000:14'b00_0000_1000_0111	pdu_ctl[2:31] Note	L2PDU Identification
14'b00_0000_1000_1000:14'b00_0000_1001_0111 proto_vlan_ctl[16]		vlan protocol configuration entry srm_reg
14'b00_0000_1001_1000:14'b00_0000_1001_1001	flow_vlan_ctl	vlan flow configuration entries
14'b00_0000_1001_1010:14'b00_0000_1010_0001 sipv4_range_ctl[4]		ipv4 sip range srm_reg
14'b00_0000_1010_0010:14'b00_0000_1010_1001 dipv4_range_ctl[4]		IPv4 dip range
14'b00_0000_1011_0000:14'b00_0000_1011_1111 sipv6_range_ctl[2]		ipv6 sip range
14'b00_0000_1100_0000:14'b00_0000_1100_0011 src_port_range_ctl[4]		L4 source port range srm_reg
14'b00_0000_1100_0100:14'b00_0000_1100_0111 dst_port_range_ctl[4]		L4 destination port range srm_reg
14'b00_0000_1100_1000:14'b00_0000_1101_0111 dipv6_range_ctl[2]		IPv6 dip range
14'b00_0000_1101_1000:14'b00_0000_1101_1111	xlate_key_ctl[8]	VLAN conversion table key selection configuration
14'b00_0000_1110_0000	out_cnt_ctl	loopback processing configuration information srm_reg

Note: Each register list contains multiple (such as 30/16/4/2/8) identical registers, that is, the register word value, register threshold, etc. are the same.

The storage register list is as follows:

Register Offset	Register Name	Description
14'b00_0001_0000_0000:14'b00_0001_0010_0010	l_port_srm	iVt module lport configuration information
14'b00_0010_0000_0000:14'b00_0010_1010_1110	port_srm	iVt module port configuration information
14'b00_0100_0000_0000:14'b00_0100_0010_1111	svlan_range_srm	svlan range check
14'b00_0100_0100_0000:14'b00_0100_0110_1111	cvlan_range_srm	cvlan range check
14'b00_0100_0100_0000:14'b00_0100_1000_0111	scos_map_srm	scos mapping table
14'b00_0100_1000_1000:14'b00_0100_1000_1111	ccos_map_srm	ccos mapping table
14'b00_0101_0000_0000:14'b00_1000_1111_1111 xlate_key_left_srm[4]		vlan xlate table keytype is key(vlan) for VLAN

14'b00_1001_0000_0000: 14'b00_1100_1111_1111 xlate_key_right_srm[4]		vlan xlate table keytype is key(vlan) for VLAN
14'b00_1101_0000_0000: 14'b01_0000_1111_1111	xlate_left_srm[4]	vlan xlate in keytype VLAN or Mac behavior configuration Set (vlan)
14'b01_0001_0000_0000: 14'b01_0100_1111_1111 xlate_right_srm[4] flow_vlan_tcm		vlan xlate in keytype VLAN or Mac behavior configuration Set (vlan)
14'b01_1000_0000_0000: 14'b01_1111_1111_1111		flow vlan lookup table
14'b10_0000_0000_0000: 14'b10_0000_1111_1111 flow_vlan_tcm_srm		flow vlan behavior configuration information
14'b10_0001_0000_0000: 14'b10_0001_0001_1111	proto_vlan_srm	vlan protocal behavior configuration information
14'b10_0001_0010_0000: 14'b10_0001_0011_1111	vlan_op_srm Note:	Vlan conversion behavior configuration information

Each register list contains multiple (such as 4) identical registers, that is, the register word value, register threshold, etc. are the same.

5.3.1 loop_ctl

Register offset: 14'b00_0000_0000_0000

Register Description: Loopback processing configuration information

Bits	Name	R/W	Description	Default
0:7	loop_ctl_loop_bypass0	RW	Bypass indication of loopback packet, 0: no bypass; 1: bypass 8'd62	
8:15	loop_ctl_loop_bypass1	RW	Bypass indication of loopback packet, 0: no bypass; 1: bypass 8'd62	

5.3.2 ctl

Register offset: 14'b00_0000_0000_0001

Register Description: Global Configuration Register srm_reg

Bits	Name	R/W	Description	Default
0	ctl_smac_is_mc_drop_to_cpu	RW	Source mac is multicast mac address trap to cpu enable 1'd0	
1	ctl_smac_is_mc_drop	RW	Source mac is multicast mac address discard enable 1'd0	
2		RW	Use lport for flow vlan lookup ctl_flow_use_lport	1'd0
3	ctl_mac_ip_bind_miss_drop_en	RW	Mac ip binding lookup failure whether	1'd0
4	to_discard_ctl_mac_ip_bind_trap_en	RW	Mac ip binding search failed to trap	1'd0
5	ctl_mac_ip_bind_miss_bypass_en	RW	Mac ip binding search failed whether to bypass the subsequent module 1'd0	
6	ctl_pass_lport_lkp	RW	Whether to bypass lport table lookup	1'd1
7	ctl_same_mac_trap	RW	Is the same package of Smac and Dmac trapped?	1'd0
8	ctl_same_mac_drop	RW	Whether to drop the same package of Smac and dmac	1'd0

5.3.3 cp_ctl

Register offset: 14'b00_0000_0000_0010

Register Description: L2PDU Identification

Bits	Name	R/W	Description	Default
0:15	cp_ctl_eth_type	RW	Special ethertype sent to cp	16'd34952

16:21	cp_ctl_ctl_port	R W	The default port number that allows input of special control packets Default value: According to std_meta.impSel Value, 0:0; 1:8; 2:16; 3:24	def_std_meta_impsel
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5.3.4 pdu_smac_ctl

Register offset: 14'b00_0000_0000_0100:14'b00_0000_0000_0101

Register Description: L2PDU Identification

Offset	Bits	Name	R/W	Description	Default
	0:31	pdu_smac_ctl_smac_0	RW	Field Mask	32'd0
1	0:15	pdu_smac_ctl_smac_1	RW	Field Mask	16'd0

5.3.5 pdu_op_ctl

Register offset: 14'b00_0000_0000_0110:14'b00_0000_0000_0111

Register Description: L2PDU Identification

Offset	Bits	Name	R/W	Description	Default
0	0:31	pdu_op_ctl_pdu_op_0		behavior, where bits [1:0] are The other protocol messages are The specific coding is as follows: 0x0: NOP; 0x1: discard; 0x2: copy to CPU; 0x3: discard + copy to CPU	32'd4
1	0:31	pdu_op_ctl_pdu_op_1	R W	L2PDU processing behavior, where bit [1:0] is The other protocol messages are The specific coding is as follows: 0x0: NOP; 0x1: discard; 0x2: copy to CPU; 0x3: discard + copy to CPU	32'd0

5.3.6 pdu_ctl0

Register offset: 14'b00_0000_0000_1000:14'b00_0000_0000_1011

Register Description: L2PDU Identification

Offset	Bits	Name	R/W	The Description entry	Default
0	0	pdu_ctl0_valid	R W	effectively indicates the	1'd1
0	1:2	pdu_ctl0_l2_tp	R W	type of the Layer 2 message, and the specific encoding is as follows: 0x0: ETH_II; 0x1: JUMBO; 0x2: SNAP; 0x3: LLC cvid	2'd0
0	3:14	pdu_ctl0_cvld	R W	ctag	12'd0
0	15:0	pdu_ctl0_ctag_vld	R W	valid indication svld	1'd0
16:27	28	pdu_ctl0_svld	R W	stag	12'd0
0		pdu_ctl0_stag_vld	R W	valid indication	1'd0
0	29:31	pdu_ctl0_eth_type_0	R W	ethtype domain	3'd0
1		pdu_ctl0_eth_type_1	R W	ethtype domain	13'd0
1	13:31	pdu_ctl0_dmac	R W	destination MAC address	19'd0

2	0:28	pdu_ctl0_mask_dmac_1 RW		Destination MAC	29'd3151936
2	29	pdu_ctl0_mask_l2_tp RW 30		Address	1'd0
2	pdu_ctl0_mask_cvvid RW 31			Field Mask	1'd0
2	pdu_ctl0_mask_ctag_vld RW			Field Mask	1'd0
3	0	pdu_ctl0_mask_svid RW		Field Mask	1'd0
3	1	pdu_ctl0_mask_stag_vld RW 2		Field Mask	1'd0
3	pdu_ctl0_mask_eth_type RW 3:19			Field Mask	1'd0
3	pdu_ctl0_mask_dmac RW	pdu_ctl0_mask_smac		Field Mask	17'd131070
3	20	RW		Field Mask Field Mask	1'd0

5.3.7 pdu_ctl1

Register offset: 14'b00_0000_0000_1100:14'b00_0000_0000_1111

Register Description: L2PDU Identification

Offset	Bits	Name	R/W	The Description entry	Default	
0	0	pdu_ctl1_valid	R W	effectively indicates the	1'd1	
0	1:2	pdu_ctl1_l2_tp	R W	type of the Layer 2 message, and the specific encoding is as follows: 0x0: ETH_II; 0x1: JUMBO; 0x2: SNAP; 0x3: LLC	2'd0	
0	3:14	pdu_ctl1_cvvid	R W	cvvid	12'd0	
	15	pdu_ctl1_ctag_vld	R W	ctag valid indication	1'd0	
0 0 16:27 28	29:31 0:12	pdu_ctl1_pdu_ctl1_svid	R W	svid	12'd0	
0	29:31 0:12	pdu_ctl1_stag_vld RW		stag Valid indication	1'd0	
1	0:12	pdu_ctl1_eth_type_0 RW		ethtype field	3'd0	
1	13:31	pdu_ctl1_eth_type_1 RW		ethtype field	13'd0	
2	0:28	pdu_ctl1_dmac_0 RW		destination MAC	19'd0	
2	29	pdu_ctl1_dmac_1 RW		address destination	29'd3151936	
2	29	pdu_ctl1_mask_l2_tp RW 30		MAC	1'd0	
2	0	pdu_ctl1_mask_cvvid RW 31		address	1'd0	
2	0	pdu_ctl1_mask_ctag_vld	R W	pdu_ctl1_mask_svid	field mask	1'd0
3	0	RW	pdu_ctl1_mask_stag_vld RW 2		field mask	1'd0
3	1	pdu_ctl1_mask_eth_type RW 3:19			field mask	1'd0
3	0	pdu_ctl1_mask_dmac RW	pdu_ctl1_mask_smac		field mask	1'd0
3	20	RW			field mask	17'd131056
3	20				field mask field mask field mask	1'd0

5.3.8 pdu_ctl[2:31]

Register offset: 14'b00_0000_0001_0000:14'b00_0000_1000_0111

Register Description: L2PDU Identification

Note: Each register list contains multiple (eg 30) identical registers, that is, the register word values, register thresholds, etc. are all the same.

Offset	Bits	Name	R/W	Description	Default
0	0	pdu_ctl_valid	R W	entry valid indication	1'd0

0	1:2	pdu_ctl_l2_tp	R W	Layer 2 message type, specifically coded as follows: 0x0: ETH_II; 0x1: JUMBO; 0x2: SNAP; 0x3: LLC	2'd0
0	3:14	pdu_ctl_cvid	R W	cvid	12'd0
0 15:0	pdu_ctl_ctag_vld	RW	pdu_ctl_svid	ctag valid indication	1'd0
16:27 28	pdu_ctl_stag_vld	RW	RW	svid	12'd0
0 0 29:31	pdu_ctl_eth_type	0	RW	stag valid indication	1'd0
1 0:12	pdu_ctl_eth_type	1	RW	ethtype	3'd0
1 13:31	pdu_ctl_dmac	0	RW	domain	13'd0
2 0:28	pdu_ctl_dmac	1	R W	ethtype domain	19'd0
2 29	pdu_ctl_mask_l2_tp	RW	RW	destination MAC	29'd0
2 30	pdu_ctl_mask_cvid	RW	RW	address	1'd0
2 31	pdu_ctl_mask_ctag_vld	RW	RW	destination	1'd0
3 0	pdu_ctl_mask_svid	RW	RW	MAC	1'd0
3 1	pdu_ctl_mask_stag_vld	RW	RW	address field	1'd0
3 2	pdu_ctl_mask_eth_type	RW	3:19	mask field	1'd0
3 3	pdu_ctl_mask_dmac	RW	pdu_ctl_mask_smac	mask field	17'd0
3 20	RW			mask field mask field mask field mask field mask	1'd0

5.3.9 proto_vlan_ctl[16]

Register offset: 14'b00_0000_1000_1000:14'b00_0000_1001_0111

Register Description: vlan protocol configuration entry srm_reg

Note: Each register list contains multiple (eg 16) identical registers, that is, the register word value, register threshold, etc. are all the same.

Bits	Name	R/W	RW	Description	Default
proto	vlan_ctl_eth_type	RW		entry valid	1'd0
1:16				indication	16'd0
17:22	proto_vlan_ctl_in_lport		Ethernet type RW input internal logical port number, when inLag is valid	Indicates whether the input internal	6'd0
proto_vlan_ctl_in_is_lag		R W	logical port number is a LAG port.	Mouth, high effective	1'd0

5.3.10 flow_vlan_ctl

Register offset: 14'b00_0000_1001_1000:14'b00_0000_1001_1001

Register Description: vlan flow configuration entry

Offset	Bits	Name	R/W	Description	Default
0	0:15	flow_vlan_ctl_mac_key_RST_CTL	R W	{indexBase[6:0],keySize[1:0],table_eBase[6:0]}	16'd0
0 16:31	flow_vlan_ctl_vlan_key_RST_CTL	RW	{indexBase[6:0],keySize[1:0],table_eBase[6:0]}		16'd0
1	0:15	flow_vlan_ctl_ipv4_key_RST_CTL	RW	Same as macKeyRstCtl	16'd0
1	16:31	flow_vlan_ctl_ipv6_key_RST_CTL	RW	Same as macKeyRstCtl	16'd0

5.3.11 sipv4_range_ctl[4]

Register offset: 14'b00_0000_1001_1010:14'b00_0000_1010_0001

Register description: ipv4 sip range interval srm_reg

Note: Each register list contains multiple (eg 4) identical registers, that is, the register word value, register threshold, etc. are all the same.

Offset	Bits	Description	Name	R/W	Default
0	0:31	sipv4_range_ctl_sip_range_l	32'd0	RW	The lower limit of the IPv4 SIP domain range
1	0:31	sipv4_range_ctl_sip_range_h	32'd0	RW	The upper limit of the IPv4 SIP domain range

5.3.12 dipv4_range_ctl[4]

Register offset: 14'b00_0000_1010_0010:14'b00_0000_1010_1001

Register description: IPv4 dip range

Note: Each register list contains multiple (eg 4) identical registers, that is, the register word value, register threshold, etc. are all the same.

Offset	Bits	Description	Name	R/W	Default
0	0:31	dipv4_range_ctl_dip_range_l	32'd0	RW	The lower limit of the IPv4 DIP domain range
1	0:31	dipv4_range_ctl_dip_range_h	32'd0	RW	The upper limit of the IPv4 DIP domain range

5.3.13 sipv6_range_ctl[2]

Register offset: 14'b00_0000_1011_0000:14'b00_0000_1011_1111

Register description: ipv6 sip range

Note: Each register list contains multiple (eg, 2) identical registers, that is, the register word value, register threshold, etc. are all the same.

Offset	Bits	Description	Name	R/W	Default
0	0:31	sipv6_range_ctl_sip_range_l_0	IPv6 32'd0	RW	The lower limit of the SIP domain range of IPv6
1	0:31	sipv6_range_ctl_sip_range_l_1	32'd0	RW	The lower limit of the SIP domain range of IPv6 32'd0
2	0:31	sipv6_range_ctl_sip_range_l_2	32'd0	RW	The lower limit of the SIP domain range of IPv6 32'd0
3	0:31	sipv6_range_ctl_sip_range_l_3	32'd0	RW	The lower limit of the SIP domain range of IPv6 32'd0
4	0:31	sipv6_range_ctl_sip_range_h_0	32'd0	RW	The upper limit of the SIP domain range of IPv6 32'd0
5	0:31	sipv6_range_ctl_sip_range_h_1	32'd0	RW	The upper limit of the SIP domain range of IPv6 32'd0
6	0:31	sipv6_range_ctl_sip_range_h_2	32'd0	RW	The upper limit of the SIP domain range of IPv6 32'd0
7	0:31	sipv6_range_ctl_sip_range_h_3	32'd0	RW	The upper limit of the SIP domain range of IPv6 32'd0

5.3.14 src_port_range_ctl[4]

Register offset: 14'b00_0000_1100_0000:14'b00_0000_1100_0011

Register Description: L4 source port range interval srm_reg

Note: Each register list contains multiple (eg 4) identical registers, that is, the register word value, register threshold, etc. are all the same.

Bits	Name	R/W	Description	Default
0:15	src_port_range_ctl_src_port_range_l	RW	The lower limit of the srcPort domain range of L4	16'd0
16:31	src_port_range_ctl_src_port_range_h	RW	The upper limit of the srcPort domain range of L4	16'd0

5.3.15 dst_port_range_ctl[4]

Register offset: 14'b00_0000_1100_0100:14'b00_0000_1100_0111

Register description: L4 destination port range interval srm_reg

Note: Each register list contains multiple (eg 4) identical registers, that is, the register word value, register threshold, etc. are all the same.

Bits	Name	R/W	Description	Default
0:15	dst_port_range_ctl_dst_port_range_l	RW	The lower limit of the dstPort domain range of L4 16'd0	
16:31	dst_port_range_ctl_dst_port_range_h	RW	Upper limit of the dstPort domain range of L4 16'd0	

5.3.16 dipv6_range_ctl[2]

Register offset: 14'b00_0000_1100_1000:14'b00_0000_1101_0111

Register description: IPv6 dip range

Note: Each register list contains multiple (eg, 2) identical registers, that is, the register word value, register threshold, etc. are all the same.

Offset	Bits	Description	Name	R/W	Description	Default
0	0:31	dipv6_range_ctl_dip_range_l	0	RW	The lower limit of the dip range of IPv6 32'd0	
1	0:31	dipv6_range_ctl_dip_range_l	1	RW	The lower limit of the dip range of IPv6 32'd0	
2	0:31	dipv6_range_ctl_dip_range_l	2	RW	The lower limit of the dip range of IPv6 32'd0	
3	0:31	dipv6_range_ctl_dip_range_l	3	RW	The lower limit of the dip range of IPv6 32'd0	
4	0:31	dipv6_range_ctl_dip_range_h	0	RW	The upper limit of the dip range of IPv6 32'd0	
5	0:31	dipv6_range_ctl_dip_range_h	1	RW	The upper limit of the dip range of IPv6 32'd0	
6	0:31	dipv6_range_ctl_dip_range_h	2	RW	The upper limit of the dip range of IPv6 32'd0	
7	0:31	dipv6_range_ctl_dip_range_h	3	RW	The upper limit of the dip range of IPv6 32'd0	

5.3.17 xlate_key_ctl[8]

Register offset: 14'b00_0000_1101_1000:14'b00_0000_1101_1111

Register Description: VLAN conversion table key selection configuration

Note: Each register list contains multiple (eg 8) identical registers, that is, the register word value, register threshold, etc. are all the same.

Bits	Name	R/W	Description	Default
0	xlate_key_ctl_use_ccfi0	RW	xlate0 checks whether ccfi is used as key. 1: Use	1'd0
1	xlate_key_ctl_use_ccos0	RW	xlate0 checks whether ccos is used as key. 1: Use	1'd0
2	xlate_key_ctl_use_cvid0	RW	xlate0 checks whether cvid is used as key. 1: Use xlate_key_ctl_use_scfi0	1'd0
3	RW	xlate0 checks whether scfi is used as key. 1: Use xlate_key_ctl_use_scos0	RW xlate0 checks whether scfi is used as key. 1: Use	1'd0
4	whether scos is used as key. 1: Use xlate_key_ctl_use_svid0	RW	xlate0 checks whether scos is used as key. 1: Use xlate_key_ctl_use_svid0	1'd0
5	1'd0 as key. 1: Use			
6	xlate_key_ctl_use_sranging0	RW	Whether to use the value processed by svid range when searching xlate0. 1: Use	1'd0
7	xlate_key_ctl_use_cranging0	RW	Whether to use the value processed by cvid range when searching xlate0. 1: Use	1'd0
8	xlate_key_ctl_use_port0	RW	xlate0 checks whether to use port as key. 1: Use xlate_key_ctl_use_ccfi1	1'd0
9	RW	xlate1 checks whether to use ccfi as key. 1: Use xlate_key_ctl_use_ccos1	RW xlate1 checks whether to use ccfi as key. 1: Use	1'd0
10	whether to use ccos as key. 1: Use xlate_key_ctl_use_cvid1	RW	xlate1 checks whether to use ccos as key. 1: Use xlate_key_ctl_use_cvid1	1'd0
11	xlate_key_ctl_use_scfi1	RW	xlate1 checks whether to use scfi as key. 1: Use xlate_key_ctl_use_scos1	1'd0
	RW	xlate1 checks whether to use scos as key. 1: Use		1'd0

14	xlate_key_ctl_use_svid1	RW	xlate1 Checks whether svid is used as key. 1: Use	1'd0
15	xlate_key_ctl_use_srange1	RW	Whether to use the value processed by svid range when searching xlate1. 1: Use 1'd0	
16	xlate_key_ctl_use_crange1	RW	Whether to use the value processed by cvid range when searching xlate1. 1: Use 1'd0	
17	1'd0 xlate_key_ctl_use_port1	RW	xlate1 Checks whether to use the port as a key. 1: Use	

5.3.18 out_cnt_ctl

Register offset: 14'b00_0000_1110_0000

Register Description: Loopback processing configuration information srm_reg

Bits	Name	R/W	Description	Module	Default
0:15	out_cnt_ctl_pkt_cnt	RW/WC		output statistics	16'd0

5.3.19 l_port_srm

Storage register description: iVt module port configuration information (the default value of inLport is equal to inPort), NumOfEntries is 35, words is 1.

Bits	Name	R/W	Description
0:5	in_lport	RO	The internal logical port number entered. When inLag is valid, it indicates a LAG port. Otherwise, it indicates a normal port.
6	in_is_lag	WO	Indicates whether the input internal logical port number is a LAG port, high effective

5.3.20 port_srm

Storage register description: iVt module port configuration information, NumOfEntries is 35, words is 5.

Offset	Bits 0	Name	R/W	Description
0		bypass_en	RO	Bypass Enable
0	1	trap_en	RW	CPU enable
0	2	drop_en	RW	enable
0	3:4	color	RW	Color, the specific encoding is as follows: 0x0: RED 0x1: YELLOW 0x2: GREEN
0	5:7	priority	RW	Priority
0	8	pri_vld	RW	Do not priority and color valid indication
0	9	lrn	RW	Internal VLAN learn instruction
0	10:21	vlan_id	RW	vlan processing ID
0	22:25	vlan_tp_idx	RW	Replaced behavior index
0	26:31	cvid_0	RW	cvid value to replace
1	0:5	cvid_1	RW	Replace or add
1	6:8	ccos_ccos_val	RW	Replace or add
1	9	ccfi	RW	Replace or add ccfi value
	10:21	svid	RW	Replace or add svid value
1	22:24	scos	RW	Replace or add scos value
1	25	scfi	RW	Replace or add scfi value
	26	i_vt_edit_en	RW	Ingress vlan edit enable
	27:29	ccos_map_idx	RW	ccos The index of the mapping
	30:31	scos_map_idx_0	RW	Index of scos mapping
2cos	map_idx_1		RW	Index of scos mapping

2	1	ccos_map_en RW scbs		ccos mapping enable. 1: Enable
2	2	scbs_map_en RW cvlan range		mapping enable. 1: Enable
2	3:6	cvlan_range_idx RW svlan_range_idx		
2	7:10	svlan_range_idx RW cvlan_range_idx		
	11	cvlan_range_en RW 2 svlan_range_idx		enable. 1: Enable
Range enable	2	svlan_range_Enable en RW Protocol		
2	13	proto_vlan_en RW xlate0_enable		MLAN enable. 1: Enable
2		vxlate0_en RW 14 xlate1		1: Enable
2	16	xlate1_enable. 1: Enable en RW 2 16:17		
		xlate0_key_tp RW xlate0_search_type: 0: vlan_xlate; 1: Vlan Mac; 2: macip bind		
	2 18:19	xlate1_key_tp RW xlate1_search_type: 0: vlan_xlate; 1: Vlan Mac; 2: macip bind		
	2 20:22	xlate0_key_mode RW xlate1_key		xlate0 key composition
	2 23:25	xlate1_key_mode RW Left hash table		composition
2	26:27	left_alg_tp0	R W	algorithm, the specific encoding is as follows: 0x0: use the low bit of the crc32 operation result; 0x1: Use the low bit of the crc16-BISYNC operation result; 0x2: use the crc16-CCITT operation result Low; 0x3: use the low bit of the key value
2	28:29	right_alg_tp0	R W	Right hash table algorithm, the specific encoding is as follows: 0x0: use the low bit of the crc32 operation result; 0x1: Use the low bit of the crc16-BISYNC operation result; 0x2: use the crc16-CCITT operation result Low; 0x3: use the low bit of the key value
2	30:31	left_alg_tp1	R W	The left hash table algorithm is specifically coded as follows: 0x0: use the low bit of the crc32 operation result; 0x1: Use the high bit of the crc32 operation result; 0x2: use the crc16 operation result; 0x3: use key value
3	0:1	right_alg_tp1	R W	Right hash table algorithm, the specific encoding is as follows: 0x0: use the low bit of the crc32 operation result; 0x1: Use the high bit of the crc32 operation result; 0x2: use the crc16 operation result; 0x3: use key value
3	2	flow_vlan0_en RW		flowvlan0 enable. 1: Enable.
3	3	ipv4_force_mac_key	RW	IPv4 packets use MAC key
3	4	mac_force_ipv4_key	RW	Mac package uses ipv4 key
3	5	use_logic_port RW		/
3	6	ipv6_low_use_mac	R W	/
3	7	ipv6_force_mac_key	RW	/
3	8	ipv6_force_ipv4_key	RW	/
3	9	mac_force_ipv6_key	RW	/
3 10		ipv4_force_ipv6_key	RW	/
3 11	mac_key	use_llc RW 3 12		/
	use_vlan_key	RW 3 13 vlan_key_use_ip		/
	RW 3 14:25	def_cvid RW 3 26:31		/
	def_svid_0	RW def_svid_1 RW def_cos		Port default cvid
	RW def_cfi	RW dot1x_en RW		Port default svid
4	0:5			Port default svid
4	6:8			Port default cos
4	9			Port default cfi
4	10			1x authentication enabled, high effective

4	11	dot1x_drop RW		1x authentication fails and discards the enabled state, high validity
4 12:15		aft	R W	AFT filtering behavior, specifically coded as follows: 0x0: no operation; 0x1: discard all frames; 0x2: discard all untagged frames; 0x3: discard all tagged frames and only allow Untagged frames are passed; 0x4: all ctagged frames are discarded; 0x5: all tagged frames; 0x6: discard all double tagged frames; 0x7: discard all single tagged frame; 0x8: discard all single ctagged frames; 0x9: discard all single tagged frame; 0xa: only allow double tagged frames to pass; 0xb: only allow 0xc: only allow single ctagged frames to pass; 0xd: only tagged frames are allowed to pass; 0xe: only single-tagged frames are allowed to pass; 0xf: Only ctagged frames are allowed to pass
4	16	prib_ctag_is_tag RW	17	Priority CTAG is identified as a valid VLAN TAG
4	prio_stag_is_tag RW	18	fwd vld	Priority STAG is recognized as a valid VLAN TAG
4	RW out_lport RW	out_is_lag	WO	Forwarding Enable
4 19:24	4			Logical port number for forwarding
	25			Logical port indication for forwarding

5.3.21 svlan_range_srm

Storage register description: svlan range check, NumOfEntries is 16, words is 3.

Offset	Bits	Name	R/W	Description
0	0:11	svlan_range_I3	RO	svid range search interval 3 lower limit value
0	12:23	svlan_range_h3	R W	svid range search interval 3 upper limit value
0	24:31	svlan_range_I2_0 RW		svid range search interval 2 lower limit value
1	0:3	svlan_range_I2_1 RW		svid range search interval 2 lower limit value
1	4:15	svlan_range_h2	RW	svid range search interval 2 upper limit value
1	16:27	svlan_range_I1	R W	svid range search interval 1 lower limit value
1	28:31	svlan_range_h1_0 RW		svid range search interval 1 upper limit value
2	0:7	svlan_range_h1_1 RW	svlan_range_I0	svid range search interval 1 upper limit value
2	8:19	svlan_range_h0 WO	R W	svid range search interval 0 lower limit value
2	20:31			svid range search interval 0 upper limit value

5.3.22 cvlan_range_srm

Storage register description: cvlan range check, NumOfEntries is 16, words is 3.

Offset	Bits	Name	R/W	Description
0	0:11	cvlan_range_I3	RO	cvid range search interval 3 lower limit value
0	12:23	cvlan_range_h3	R W	cvid range search interval 3 upper limit value
0	24:31	cvlan_range_I2_0 RW		cvid range search interval 2 lower limit value
1	0:3	cvlan_range_I2_1	RW	cvid range search interval 2 lower limit value
1	4:15	cvlan_range_h2	R W	cvid range search interval 2 upper limit value
1	16:27	cvlan_range_I1	R W	cvid range search interval 1 lower limit value
1	28:31	cvlan_range_h1_0 RW		cvid range search interval 1 upper limit value
2	0:7	cvlan_range_h1_1 RW	cvlan_range_I0	cvid range search interval 1 upper limit value
2	8:19		RW	cvid range search interval 0 lower limit value
2	20:31	cvlan_range_h0 WO		cvid range search interval 0 upper limit value

5.3.23 scos_map_srm

Storage register description: scos mapping table, NumOfEntries is 8, words is 1.

Bits	Name	R/W	Description
0:2	cos0	RO	cos0 mapped value
3:5	cos1	R W	cos1 mapped value
6:8	cos2	R W	cos2 mapped value
9:11	cos3	R W	cos3 mapped value
12:14	cos4	R W	cos4 mapped value
15:17	cos5	R W	cos5 mapped value
18:20	cos6	R W	cos6 mapped value
21:23	cos7	R W	cos7 mapped value
Iserty four	cfi0	R W	cfi0 mapped value
25	cfi1	WO	cfi1 mapped value

5.3.24 ccos_map_srm

Storage register description: ccos mapping table, NumOfEntries is 8, words is 1.

Bits	Name	R/W	Description
0:2	cos0	RO	cos0 mapped value
3:5	cos1	R W	cos1 mapped value
6:8	cos2	R W	cos2 mapped value
9:11	cos3	R W	cos3 mapped value
12:14	cos4	R W	cos4 mapped value
15:17	cos5	R W	cos5 mapped value
18:20	cos6	R W	cos6 mapped value
21:23	cos7	R W	cos7 mapped value
Iserty four	cfi0	R W	cfi0 mapped value
25	cfi1	WO	cfi1 mapped value

5.3.25 xlate_key_left_srm[4]

Storage register description: vlan xlate table keytype is VLAN when key(vlan), NumOfEntries is 128, words is 2.

Note: Each register list contains multiple (eg 4) identical registers, that is, the register word value, register threshold, etc. are all the same.

Offset	R/W	Description	Name		
0	0	valid	RO		Effective instructions
0	1:12	svid	R W	svid	value
0	13	scfi	R W		scfi value
0	14:16	scos	R W		scos value
0	17:28	cvid	R W		cvid value
0	29	ccfi	R W		ccfi value
0	30:31	ccos_0	R W	ccos_1	R W
1	0				ccos value
1	1:6	in_lport	R W		The internal logical port number entered. When inLag is valid, it indicates that the LAG port Otherwise, it indicates a common port.

1	7	in_is_lag RW		Indicates whether the input internal logic port number is a LAG port, high effective
1	8:23	res	R W	Reserve
1	24:26	key_mode RW		key component type
1	27:28	key_tp	WO	xlate0 search type: 0: vlan xlate; 1: Vlan Mac; 2: macip bind

5.3.26 xlate_key_right_srm[4]

Storage register description: vlan xlate table keytype is VLAN when key(vlan), NumOfEntries is 128, words is 2.

Note: Each register list contains multiple (eg 4) identical registers, that is, the register word value, register threshold, etc. are all the same.

Offset	R/W	Description	Name	
0	0	bypass_en RO	trap_en	Bypass Enable
0	1	RW drop_en	RW	Trap to CPU enable
0	2			Discard Enable
0	3:4	color	R W	Color, the specific codes are as follows: 0x0: RED 0x1: YELLOW 0x2: GREEN
0	5:7	priority	RW	Internal Priority
0	8	pri_vld	RW	Internal priority and color indication
0	9	lrn_disable	RW	vlan_id
0	10:21	RW	vlan_op_idx	RW
0	22:25	cvid_0	RW	vlan processing behavior index
0	26:31			Replace or add cvid value
1	0:5	cvid_1	RW	Replace or add cvid value
1	6:8	ccos	R W	Replace or add ccos value
1	9	ccfi	R W	Replace or add ccfi value
1	10:21	svid	R W	Replace or add svid value
1	22:24	scos	R W	Replace or add scos value
1	25	scfi	WO	Replace or add scfi value

5.3.27 xlate_left_srm[4]

Storage register description: vlan xlate behavior configuration when keytype is VLAN or Mac (vlan), NumOfEntries is 128, words is 2.

Note: Each register list contains multiple (eg 4) identical registers, that is, the register word value, register threshold, etc. are all the same.

Offset	Name	R/W	Description	
0	0	bypass_en	RO	Bypass Enable
0	1	trap_en	RW	Trap to CPU enable
0	2	drop_en	RW	Discard Enable
0	3:4	color	R W	specific encoding is as follows: 0x0: RED 0x1: YELLOW 0x2: GREEN
0	5:7	priority	RW	Internal Priority
0	8	pri_vld	RW	Internal priority and color indication
0	9	lrn_disable	RW	vlan_id
0	10:21	RW	vlan_op_idx	RW
0	22:25			vlan processing behavior index
0	26:31	cvid_0	RW	Replace or add cvid value

1	0:5	cvid_1	R W	Replace or add cvid value
1	6:8	ccos	R W	Replace or add ccos value
1	9	ccfi	R W	Replace or add ccfi value
1	10:21	svid	R W	Replace or add svid value
1	22:24	scos	R W	Replace or add scos value
1	25	scfi	WO	Replace or add scfi value

5.3.28 xlate_right_srm[4]

Storage register description: vlan xlate behavior configuration when keytype is VLAN or Mac (vlan), NumOfEntries is 128, words is 2.

Note: Each register list contains multiple (eg 4) identical registers, that is, the register word value, register threshold, etc. are all the same.

Offset	Name	R/W	Description
0	bypass_en	RO	Bypass enable
0	trap_en	RW	Trap enable
0	drop_en	RW	Drop enable
0	color	R W	specific encoding is as follows: 0x0: RED 0x1: YELLOW 0x2: GREEN
0	priority	RW	Internal Priority
0	pri_vld	RW	Internal priority and color indication
0	lrn_disable	RW	Not learning instructions
0	vlan_id	RW	Internal vlanId value
0	vlan_op_idx	RW	vlan processing behavior index
0	cvid_0	RW	Replace or add cvid value
1	cvid_1	R W	Replace or add cvid value
1	ccos	R W	Replace or add ccos value
1	ccfi	R W	Replace or add ccfi value
1	svid	R W	Replace or add svid value
1	scos	R W	Replace or add scos value
1	scfi	WO	Replace or add scfi value

5.3.29 flow_vlan_tcm

Storage register description: flow vlan lookup table, NumOfEntries is 128, words is 9.

Offset	Bits	Name	R/W	Description
0	0:31	key_0	RO	Find key
1	0:31	key_1	R W	Find key
2	0:31	key_2	R W	Find key
3	0:31	key_3	R W	Find key
4	0:11	key_4	R W	Find key
4	12	valid	R W	Effective instructions
4	13:31	key_mask_0	RW	Find key mask
5	0:31	key_mask_1	RW	Find key mask
6	0:31	key_mask_2	RW	Find key mask
7	0:31	key_mask_3	RW	Find key mask
8	0:24	key_mask_4	RW	Find key mask
8	25	valid_mask	WO	Valid indication mask

5.3.30 flow_vlan_tcm_srm

Storage register description: flow vlan behavior configuration information, NumOfEntries is 128, words is 2.

Offset	Bits	Name	R/W	Description
0	0	bypass_en RO trap_en		Bypass Enable
0	1	RW drop_en RW		Trap to CPU enable
0	2			Discard Enable
0	3:4	color	R W	Color, the specific codes are as follows: 0x0: RED 0x1: YELLOW 0x2: GREEN
0	5:7	priority RW		Internal Priority
0	8	pri_vld	RW	Internal priority and color indication
0	9	lrn_disable RW vlan_id		Not learning instructions
0	10:21	RW vlan_op_idx RW		Internal vlanId value
0	22:25			vlan processing behavior index
0	26:31	cvid_0	RW	Replace or add cvid value
1	0:5	cvid_1	R W	Replace or add cvid value
1	6:8	ccos	R W	Replace or add ccos value
1	9	ccfi	R W	Replace or add ccfi value
1	10:21	svid	R W	Replace or add svid value
1	22:24	scos	R W	Replace or add scos value
1	25	scfi	R W	Replace or add scfi value
1	26:28	queue_num RW queue_vld WO		Queue Number
1	29			queueNum valid indication

5.3.31 proto_vlan_srm

Storage register description: vlan protocol behavior configuration information, NumOfEntries is 16, words is 2.

Offset	Bits	Name	R/W	Description
0	0	bypass_en RO trap_en		Bypass Enable
0	1	RW drop_en RW		Trap to CPU enable
0	2			Discard Enable
0	3:4	color	R W	Color, the specific codes are as follows: 0x0: RED 0x1: YELLOW 0x2: GREEN
0	5:7	priority RW		Internal Priority
0	8	pri_vld	RW	Internal priority and color indication
0	9	lrn_disable RW vlan_id		Not learning instructions
0	10:21	RW vlan_op_idx RW		Internal vlanId value
0	22:25			vlan processing behavior index
0	26:31	cvid_0	RW	Replace or add cvid value
1	0:5	cvid_1	R W	Replace or add cvid value
1	6:8	ccos	R W	Replace or add ccos value
1	9	ccfi	R W	Replace or add ccfi value
1	10:21	svid	R W	Replace or add svid value
1	22:24	scos	R W	Replace or add scos value
1	25	scfi	WO	Replace or add scfi value

5.3.32 vlan_op_srm

Storage register description: Vlan conversion behavior configuration information, NumOfEntries is 16, words is 2.

Offset	Bits	Name	R/W	Description
	0	ut_ivid	RO	0:noop; 1:add
		ut_ipri	RW	0:noop; 1:add
	1	ut_ovid RW ut_opri		0:noop; 1:add
0 0 0 0	2:3	RW sot_ivid RW		0:noop; 1:add
0	4:5	sot_ipri RW sot_ovid		0:noop; 1:add 2:copy
0	6:7	RW sot_opri RW		0:noop; 1:add 2:copy
0	8:9	sot_povid RW sit_ivid		0:noop; 2:replace 3:delete 0:noop;
0	10:11	RW		2:replace 3:delete 0:noop; 2:replace
0	12:13			3:delete 0:noop; 2:replace 3:delete
0	14:15			0:noop; 2:replace 3:delete 0:noop;
0	16:17	sit_ipri	RW	2:replace 3:delete 0:noop; 1:add 2:copy
0	18:19	sit_p_ivid RW sit_ovid		3:delete
0	20:21	RW sit_opri RW		
0	22:23			0:noop; 1:add 2:copy
0	24:25	dt_ivid	RW	0:noop; 1:copy 2:replace 3:delete
0	26:27	dt_ipri	RW	0:noop; 1:copy 2:replace 3:delete
0	28:29	dt_p_ivid RW dt_ovid		0:noop; 1:copy 2:replace 3:delete
0	30:31	RW dt_opri RW		0:noop; 1:copy 2:replace 3:delete
1	0:1	dt_povid WO		0:noop; 1:copy 2:replace 3:delete 0:noop; 1:copy
1	2:3			2:replace 3:delete

5.4 inet_reg

The inet_reg register module contains 13 registers and 5 storage registers.

The register list is as follows:

Register Offset	Register Name	Description
17'b0_0000_0000_0000_0000: 17'b0_0000_0000_0000_0010	ctl	Exception handling configuration information
17'b0_0000_0000_0000_0100	loop_ctl	Loopback processing configuration information
17'b0_0000_0000_0000_0101	pdu_ctl	PDU Global Configuration
17'b0_0000_0000_0000_1000: 17'b0_0000_0000_0000_1101	def_vlan_ctl	Default VLAN Attribute Table
17'b0_0000_0000_0001_0000: 17'b0_0000_0000_0101_1111	v4_addr_chk_ctl[16] Note	IPv4 address check configuration
17'b0_0000_0000_1001_0000: 17'b0_0000_0001_0001_1111	v6_addr_chk_ctl[16] Note	IPv6 address check configuration
17'b0_0000_0001_1001_0000: 17'b0_0000_0010_0000_1111	v6_addr_chk_mask_ctl[16] Note	IPv6 address check mask configuration
17'b0_0000_0010_0001_0000: 17'b0_0000_0010_1010_1111	tcp_dos_chk_ctl[32] Note	TCP DoS attack check configuration
17'b0_0000_0011_0001_0000: 17'b0_0000_0011_0010_1111	icmp_dos_chk_ctl[16] Note	ICMP DoS attack check configuration
17'b0_0000_0011_0011_0000: 17'b0_0000_0011_0011_0010	dos_trap_ctl	DoS attack trap configuration

17'b0_0000_0011_0011_0100: 17'b0_0000_0011_0011_0101	prot_ctl	Protection status
17'b0_0000_0011_0011_1000: 17'b0_0000_0011_0011_1011	cnt	Abnormal Statistics
17'b0_0000_0011_0011_1100 Note: Each	out_cnt_ctl	Package Statistics
register list contains multiple (such as 16/32) identical registers, that is, the register word value, register threshold, etc. are the same.		

The storage register list is as follows:

Register Offset	Register Name	Description
17'b0_0000_0100_0000_0000: 17'b0_0000_0100_1000_1011	port_srm	Port configuration information
17'b0_1000_0000_0000_0000: 17'b0_1101_1111_1111_1111	vlan_srm	vlan attribute table
17'b1_0000_0000_0000_0000: 17'b1_0010_1111_1111_1111	in_vlan_cnt_srm	vlan statistics
17'b1_0100_0000_0000_0000: 17'b1_0100_0101_1111_1111	stp_srm	stp state table
17'b1_0100_1000_0000_0000: 17'b1_0100_1000_0111_1111	erps_srm	erps status table

5.4.1 ctl

Register offset: 17'b0_0000_0000_0000_0000:17'b0_0000_0000_0000_0010

Register description: exception handling configuration information srm_reg

Offset	Bits	Name	R/W	Description	Default
0	0	ctl_stp_disable_chk_en	RW	Spanning tree disable status check enable	1'd0
0	1	ctl_stp_disable_drop_en	RW	The spanning tree state is in the Disable state. able	1'd0
0	2	ctl_stp_chk_en	RW	Spanning tree status check enable, default value: 0: std_meta.manageMode = 0; 1: std_meta.manageMode = 1	def_std_meta_manageMode
0	3	ctl_prot_drop_oam	RW	Drop oam packets during protection	1'd0
0	4	ctl_l3_dos_attack_chk_en	RW	Layer 3 packet dos attack check enable	1'd0
0	5	ctl_l4_dos_attack_chk_en	RW	Layer 4 packet dos attack check enable 6:13	1'd0
0	6:29	ctl_ipv6_ext_frag_proto_id	RW	IPv6 extension header fragmentation protocol number	8'd0
0	30:31	ctl_tcp_hdr_min_size	RW	TCP header minimum length, in bytes 0:14:19 6'd0	
1	0:1	ctl_ipv4_max_size_0	RW	The maximum length of the ipv4 message in bytes 12'd0	
1	2:15	ctl_ipv4_max_size_1	RW	The maximum length of the ipv4 message in bytes 2'd0	
1	16:29	ctl_ipv6_max_size	RW	The maximum length of the ipv6 message in bytes 14'd0	
1	30:31	ctl_ipv6_min_size_0	RW	The minimum length of the ipv6 message, in bytes 2'd0	
2	0:11	ctl_ipv6_min_size_1	RW	The minimum length of the ipv6 message, in bytes 12'd0	
2	12:16	ctl_port_bmp_hi	RW	Port mask	5'd31
2	17:2	ctl_lrn_upd_disable	RW	not	1'd0
18:19		ctl_erps_num	RW	learned 0:16; 1:32; 2:64; 3:128	2'd0

5.4.2 loop_ctl

Register offset: 17'b0_0000_0000_0000_0100

Register Description: Loopback processing configuration information

Bits	Name	R/W	Description	Default
0:7	loop_ctl_loop_bypass0	RW	Bypass indication of loopback packet, 0: no bypass; 1: bypass	8'd62
8:15	loop_ctl_loop_bypass1	RW	Bypass indication of loopback packet, 0: no bypass; 1: bypass	8'd62

5.4.3 pdu_ctl

Register offset: 17'b0_0000_0000_0000_0101

Register Description: PDU Global Configuration srm_reg

Bits	Name	R/W	Description:	Default
0:31	pdu_ctl_drop bmp	R W	Reports L2PDUs when the spanning tree is in DISABLE state. Discard	32'd0

5.4.4 def_vlan_ctl

Register offset: 17'b0_0000_0000_0000_1000:17'b0_0000_0000_0000_1101

Register Description: Default VLAN Attribute Table

Offset	Bits	Name	R/W	Description	Default
0	0	def_vlan_ctl_bypass_en	RW	EnabledDiscard	1'd0
0	1	def_vlan_ctl_drop_en	RW	EnabledTrap	1'd0
0	2	def_vlan_ctl_trap_en	RW	to CPU Enabled1x	1'd0
0	3	def_vlan_ctl_dot1x_en	RW	Authentication Enabled, High Effective	1'd0
0	4	def_vlan_ctl_dot1x_drop	RW	1x authentication fails to discard enable, high effective	1'd0
0	5	def_vlan_ctl_in_fpol_vld	RW	Ingress hierarchical meter small pipe valid indication	1'd0
0	index 6:12	def_vlan_ctl_qos_profile_idx	RW	7'd0 qos template	
0	indication 13	def_vlan_ctl_qos_profile_vld	RW	Color, qos template valid	1'd0
0	14:15	def_vlan_ctl_color	R W	the specific encoding is as follows: 0x0: RED; 0x1: YELLOW; 0x2: GREEN Internal	2'd0
0	16:18	def_vlan_ctl_priority	RW	priority	3'd0
0	19	def_vlan_ctl_pri_vld	RW	Internal priority and color valid indication	1'd0
0	20:28	def_vlan_ctl_stp_id	RW	spanning tree ID	9'd0
0	29:30	def_vlan_ctl_l2_key_tp	RW	Layer 2 forwarding type: 0x0: BRIDGE; 0x1: SCC; 0x2: DCC Disable	2'd0
0	31	enable_def_vlan_ctl_lrn_disable	RW	address learning	1'd0
1	def_vlan_ctl_lrn_upd_disable	RW	1'd0	Disable address learning update enable 0	
1	def_vlan_ctl_pdu_bypass_stp	RW	Identify PDU bypass	spanning tree check enable 1'd0	
1	2:31	def_vlan_ctl_port bmp	RW	Port member, bit 0 represents port 0, and so on push Default value: case odc (std_meta.padHubMode)	def_std_meta_padHubMode

				3'd0: 0x300000ff // 8port, corresponding to the logical port 0~7,24,25; 3'd1: 0x3000000f // 4port, corresponding to the logical port 0~3,24,25; 3'd2: 0x30000fff // 12port, corresponding to the logical port 0~11,24,25; 3'd3: 0x3000ffff // 16port, corresponding to the logical port 0~15,24,25; 3'd4: 0x300fffff // 20port, corresponding to the logical port 0~19,24,25; 3'd5: 0x30fffff // 24port, corresponding to the logical port 0~23,24,25; 3'd6: 0x30003fff // 14port, corresponding to the logical port 0~13,24,25; 3'd7: 0x30000fff // 12port, corresponding to the logical port 0~11,24,25.	
2	0:7	def_vlan_ctl_lag_bmp RW		lag member, bit 0 represents LAG port 0, The	8'd0
2	8	def_vlan_ctl_vlan_isot_en RW 9:12		following analogy enables port isolation	1'd0
2	def_vlan_ctl_vlan_isot_idx RW 13	def_vlan_ctl_in_vlan_mirror_en		based on VLANs. Enables mirroring of port	4'd0
2	RW	def_vlan_ctl_in_vlan_cnt_idx		isolation pointer entry based on VLANs.	1'd0
2	14	vid	R W	vlan statistics enable	1'd0
2	15	def_vlan_ctl_drop_ukw_uc RW		Unknown unicast message discard Enable	1'd0
2 16:17		def_vlan_ctl_pfm	R W	multicast pfm parameter to control the forwarding of multicast messages The specific encoding is as follows: 0x0: Do not start searching, directly flood to all ports 0x1: Start the search, and find the results based on the search results Forward to a specific port, discard if no search results are found 0x2: Do not start searching and directly discard all messages 0x3: Start the search, and find the results based on the search results Forward to a specific port, flood without search results	2'd0
2 18:31		def_vlan_ctl_pdu_op_0 RW		L2PDU processing behavior, where bits [1:0] correspond to a The same applies to other protocol messages. The specific encoding is as follows: 0x0: NOP; 0x1: discard; 0x2: copy to CPU; 0x3: discard + copy to CPU	14'd0
3	0:31	def_vlan_ctl_pdu_op_1 RW		L2PDU processing behavior, where bits [1:0] correspond to a The same applies to other protocol messages. The specific encoding is as follows: 0x0: NOP; 0x1: discard; 0x2: copy to CPU; 0x3: discard + copy to CPU	32'd0
4	0:17	def_vlan_ctl_pdu_op_2 RW		L2PDU processing behavior, where bits [1:0] correspond to a The same applies to other protocol messages. The specific encoding is as follows: 0x0: NOP; 0x1: discard; 0x2: copy to CPU; 0x3: discard + copy to CPU	18'd0
4 18:19		def_vlan_ctl_mac_list_tp RW		MAC address blacklist and whitelist mode: 0x1 means Blacklist, 0x2 means whitelist 0	2'd0
4 20:31		def_vlan_ctl_fid	R W		12'd0

5	0	def_vlan_ctl_fid_stm_ctl_vld RW		FID-based storm control enablement	1'd0
5	1:2	def_vlan_ctl_erps_id RW		Erps ID number	2'd0

5.4.5 v4_addr_chk_ctl[16]

Register offset: 17'b0_0000_0000_0001_0000:17'b0_0000_0000_0101_1111

Register Description: IPv4 address check configuration srm_reg

Note: Each register list contains multiple (eg 16) identical registers, that is, the register word value, register threshold, etc. are all the same.

Offset	Bits	Description	Name	R/W	IPv4 Source IP Address	IPv4 Destination IP Address	Default
0	0	v4_addr_chk_ctl_valid	v4_addr_chk_ctl_valid	RW 1:31		Destination IP	1'd0
0		v4_addr_chk_ctl_key_sip_0	v4_addr_chk_ctl_key_sip_0	RW		Address IPv4	31'd0
1	0	v4_addr_chk_ctl_key_sip_1	v4_addr_chk_ctl_key_sip_1	RW 1:31		Destination IP Address	1'd0
1		v4_addr_chk_ctl_key_dip_0	v4_addr_chk_ctl_key_dip_0	RW		Field Mask Field Mask	31'd0
2	0	v4_addr_chk_ctl_key_dip_1	v4_addr_chk_ctl_key_dip_1	RW 1:31		Field Mask Field Mask	1'd0
2		v4_addr_chk_ctl_mask_sip_0	v4_addr_chk_ctl_mask_sip_0	RW			31'd0
3		v4_addr_chk_ctl_mask_sip_1	v4_addr_chk_ctl_mask_sip_1	RW 1:31			1'd0
3		v4_addr_chk_ctl_mask_dip_0	v4_addr_chk_ctl_mask_dip_0	RW			31'd0
4		v4_addr_chk_ctl_mask_dip_1	v4_addr_chk_ctl_mask_dip_1	RW			1'd0

5.4.6 v6_addr_chk_ctl[16]

Register offset: 17'b0_0000_0000_1001_0000:17'b0_0000_0001_0001_1111

Register Description: IPv6 address check configuration srm_reg

Note: Each register list contains multiple (eg 16) identical registers, that is, the register word value, register threshold, etc. are all the same.

Offset	Bits	Description	Name	R/W	IPv6 source IP Address	IPv6 destination IP Address	Default
0	0	v6_addr_chk_ctl_valid	v6_addr_chk_ctl_valid	RW 1:31		source IP address	1'd0
0		v6_addr_chk_ctl_key_sip_0	v6_addr_chk_ctl_key_sip_0	RW 0:31		IPv6 source IP	31'd0
1		v6_addr_chk_ctl_key_sip_1	v6_addr_chk_ctl_key_sip_1	RW 0:31		address IPv6	32'd0
2		v6_addr_chk_ctl_key_sip_2	v6_addr_chk_ctl_key_sip_2	RW 0:31		destination IP address	32'd0
3		v6_addr_chk_ctl_key_sip_3	v6_addr_chk_ctl_key_sip_3	RW		IPv6 destination IP	32'd0
4	0	v6_addr_chk_ctl_key_sip_4	v6_addr_chk_ctl_key_sip_4	RW 1:31		address IPv6	1'd0
4		v6_addr_chk_ctl_key_dip_0	v6_addr_chk_ctl_key_dip_0	RW 0:31		destination IP address	31'd0
5		v6_addr_chk_ctl_key_dip_1	v6_addr_chk_ctl_key_dip_1	RW 0:31		IPv6 destination IP	32'd0
6		v6_addr_chk_ctl_key_dip_2	v6_addr_chk_ctl_key_dip_2	RW 0:31		address IPv6 destination	32'd0
7		v6_addr_chk_ctl_key_dip_3	v6_addr_chk_ctl_key_dip_3	RW		IP address	32'd0
8	0	v6_addr_chk_ctl_key_dip_4	v6_addr_chk_ctl_key_dip_4	RW			1'd0

5.4.7 v6_addr_chk_mask_ctl[16]

Register offset: 17'b0_0000_0001_1001_0000:17'b0_0000_0010_0000_1111

Register Description: IPv6 address check configuration srm_reg

Note: Each register list contains multiple (eg 16) identical registers, that is, the register word value, register threshold, etc. are all the same.

Offset	Bits	R/W	Name	Description	Default
0		31	v6_addr_chk_mask_sip_0	field mask	32'd0

1	0:31	v6_addr_chk_mask_ctl_mask_sip_1 RW		field mask	32'd0
2	0:31	v6_addr_chk_mask_ctl_mask_sip_2 RW		field mask	32'd0
3	0:31	v6_addr_chk_mask_ctl_mask_sip_3 RW		field mask	32'd0
4	0:31	v6_addr_chk_mask_ctl_mask_dip_0 RW		field mask	32'd0
5	0:31	v6_addr_chk_mask_ctl_mask_dip_1 RW		field mask	32'd0
6	0:31	v6_addr_chk_mask_ctl_mask_dip_2 RW		field mask	32'd0
7	0:31	v6_addr_chk_mask_ctl_mask_dip_3 RW		field mask	32'd0

5.4.8 tcp_dos_chk_ctl[32]

Register offset: 17'b0_0000_0010_0001_0000:17'b0_0000_0010_1010_1111

Register Description: TCP DoS attack check configuration srm_reg

Note: Each register list contains multiple (eg 32) identical registers, that is, the register word value, register threshold, etc. are all the same.

Offset	Bits R/W	Description	Item valid indication		Default
0	0	tcp_dos_chk_ctl_valid	RW		1'd0
0	1	tcp_dos_chk_ctl_key_is_tcp	RW	TCP message indication UDP message	1'd0
0	2	tcp_dos_chk_ctl_key_is_udp	RW	indication	1'd0
0	3	tcp_dos_chk_ctl_key_l4_hdr_vld	RW	L4 header valid indication ip	1'd0
0	4	tcp_dos_chk_ctl_key_ip_frag	RW	fragment message indication	1'd0
0	5	tcp_dos_chk_ctl_key_ip_frag_mf	RW	IP fragment message MF indication	1'd0
0:6:18	0	tcp_dos_chk_ctl_key_ip_frag_offset RW		IP fragment message offset value	13'd0
19:31	0:18	tcp_dos_chk_ctl_key_tcp_seq_0	RW	TCP message sequence number	13'd0
1		tcp_dos_chk_ctl_key_tcp_seq_1	RW	TCP message sequence number	19'd0
1	19:26	tcp_dos_chk_ctl_key_tcp_flag	RW	TCP message identification field	8'd0
1	27	tcp_dos_chk_ctl_key_tcp_offset_les_thrd RW	TCP header offset is less than the minimum threshold indication	1'd0	
1	28	tcp_dos_chk_ctl_key_l4_src_equal_dst RW	The Layer 4 source port number is equal to the destination port number. Show		1'd0
1	29	tcp_dos_chk_ctl_key_ipv4_len_exd_thrd RW	ipv4 length greater than threshold indication	1'd0	
1	30	tcp_dos_chk_ctl_key_ipv6_len_exd_thrd RW	ipv6 length greater than threshold indication	1'd0	
1	31	tcp_dos_chk_ctl_key_ipv4_len_les_thrd RW	ipv4 length is less than the threshold indication	1'd0	
2	0	tcp_dos_chk_ctl_key_ipv6_len_les_thrd RW	ipv6 length is less than the threshold indication	1'd0	
2	1	tcp_dos_chk_ctl_mask_is_tcp	RW	field mask	1'd0
2	2	tcp_dos_chk_ctl_mask_is_udp	RW	field mask	1'd0
2	3	tcp_dos_chk_ctl_mask_l4_hdr_vld	RW	field mask	1'd0
2	4	tcp_dos_chk_ctl_mask_ip_frag	RW	field mask	1'd0
2	5	tcp_dos_chk_ctl_mask_ip_frag_mf RW		field mask	1'd0
2:6:18	2	tcp_dos_chk_ctl_mask_ip_frag_offset RW		field mask	13'd0
19:31	0:18	tcp_dos_chk_ctl_mask_tcp_seq_0 RW		field mask	13'd0
3	tcp_dos_chk_ctl_mask_tcp_seq_1 19:26		RW	field mask	19'd0
tcp_dos_chk_ctl_mask_tcp_flag_27			RW	field mask	8'd0
3	tcp_dos_chk_ctl_mask_tcp_offset_les_thrd RW	28		field mask	1'd0
3	tcp_dos_chk_ctl_mask_l4_src_equal_dst RW	29		field mask	1'd0
3	tcp_dos_chk_ctl_mask_ipv4_len_exd_thrd RW	30		field mask	1'd0
3	tcp_dos_chk_ctl_mask_ipv6_len_exd_thrd RW	31		field mask	1'd0
3	tcp_dos_chk_ctl_mask_ipv4_len_les_thrd RW	0		field mask	1'd0
4	tcp_dos_chk_ctl_mask_ipv6_len_les_thrd RW			field mask	1'd0

5.4.9 icmp_dos_chk_ctl[16]

Register offset: 17'b0_0000_0011_0001_0000:17'b0_0000_0011_0010_1111

Register Description: ICMP DoS attack check configuration srm_reg

Note: Each register list contains multiple (eg 16) identical registers, that is, the register word value, register threshold, etc. are all the same.

Offset	Bits	Name	Description	Entry valid indication	icmp_dos_chk_ctl_valid	R/W			Default
0	0								
0	1	icmp_dos_chk_ctl_key_is_icmp_v4				RW	ipv4 format icmp message indication	1'd0	
0	2	icmp_dos_chk_ctl_key_is_icmp_v6	RW icmp message indication				in ipv6 format	1'd0	
0	3	icmp_dos_chk_ctl_key_ip_frag	RW ip			R W	IP fragment message indication	1'd0	
0	4	icmp_dos_chk_ctl_key_ip_frag_mf					MF indication	1'd0	
0	5:17	icmp_dos_chk_ctl_key_ip_frag_offset	RW IP fragment message offset value				13'd0		
0	18	icmp_dos_chk_ctl_key_ipv4_len_exd_thrd	RW ipv4 length greater than threshold				indication	1'd0	
0	19	icmp_dos_chk_ctl_key_ipv6_len_exd_thrd	RW ipv6 length greater than threshold				indication	1'd0	
0	20	icmp_dos_chk_ctl_key_ipv4_len_les_thrd	RW ipv4 length is less than the threshold				indication	1'd0	
0	21	icmp_dos_chk_ctl_key_ipv6_len_les_thrd	RW ipv6 length is less than the threshold				indication	1'd0	
0	22:29	icmp_dos_chk_ctl_key_icmp_type				RW	icmp message type field	8'd0	
0	30	icmp_dos_chk_ctl_mask_is_icmp_v4	RW icmp message indication				in ipv4 format	1'd0	
0	31	icmp_dos_chk_ctl_mask_is_icmp_v6	RW icmp message indication				in ipv6 format	1'd0	
1	0	icmp_dos_chk_ctl_mask_ip_frag				R W	IP fragment message indication	1'd0	
1	1	icmp_dos_chk_ctl_mask_ip_frag_mf	RW IP fragment message				MF indication	1'd0	
1	2:14	icmp_dos_chk_ctl_mask_ip_frag_offset	RW IP fragment message offset value				13'd0		
1	15	icmp_dos_chk_ctl_mask_ipv4_len_exd_thrd	RW ipv4 length greater than threshold				indication	1'd0	
1	16	icmp_dos_chk_ctl_mask_ipv6_len_exd_thrd	RW ipv6 length greater than threshold				indication	1'd0	
1	17	icmp_dos_chk_ctl_mask_ipv4_len_les_thrd	RW ipv4 length is less than the threshold				indication	1'd0	
1	18	icmp_dos_chk_ctl_mask_ipv6_len_les_thrd	RW ipv6 length is less than the threshold				indication	1'd0	
1	19:26	icmp_dos_chk_ctl_mask_icmp_type	RW icmp message type				field	8'd0	

5.4.10 dos_trap_ctl

Register offset: 17'b0_0000_0011_0011_0000:17'b0_0000_0011_0011_0010

Register Description: ICMP DoS attack check configuration srm_reg

Offset	Bits	Name	R/W	Description	Default
0	0:18	dos_trap_ctl_v4_hdr_chk_trap	RW	IPv4 header error trap configuration	1'd0
0	19:31	dos_trap_ctl_v6_hdr_chk_trap_0	RW	IPv6 header error trap configuration	13'd0
1	0:5	dos_trap_ctl_v6_hdr_chk_trap_1	RW	IPv6 header error trap configuration	6'd0
1	6:31	dos_trap_ctl_tcp_dos_chk_trap_0	RW	Tcp dos attack trap configuration	26'd0
2	0:5	dos_trap_ctl_tcp_dos_chk_trap_1	RW	Tcp dos attack trap configuration	6'd0
2	6:21	dos_trap_ctl_icmp_dos_chk_trap	RW	icmp dos attack trap configuration	16'd0

5.4.11 prot_ctl

Register offset: 17'b0_0000_0011_0011_0100:17'b0_0000_0011_0011_0101

Register Description: ICMP DoS attack check configuration srm_reg

Offset	Bits	Name	R/W	Description	Default
0	0:31	prot_ctl_prot_sta_0	R W		32'd0
1	0:2	prot_ctl_prot_sta_1	R W	DescriptionProtection Status	ProtStat0

5.4.12 cnt

Register offset: 17'b0_0000_0011_0011_1000:17'b0_0000_0011_0011_1011

Register Description: Exception Statistics

Offset	Bits	Name	R/W	Description	Default
0	0:31	cnt_ip_hdr_chk_fail_cnt_0	RW ip header check failure statistics count	32'd0	
1	0:3	cnt_ip_hdr_chk_fail_cnt_1	RW ip header check failure statistics count	4'd0	
1	4:31	cnt_ip_hdr_err_cnt_0	RW ip header error statistics count	28'd0	
2	0:7	cnt_ip_hdr_err_cnt_1	RW ip header error statistics count	8'd0	
2	8:31	cnt_ip_option_cnt_0	RW ipOption statistics count	24'd0	
3	0:11	cnt_ip_option_cnt_1	RW ipOption Statistics Count	12'd0	

5.4.13 out_cnt_ctl

Register offset: 17'b0_0000_0011_0011_1000:17'b0_0000_0011_0011_1011

Register Description: Loopback processing configuration information srm_reg

Bits	Name	R/W	Description	Default
0:15	out_cnt_ctl_pkt_cnt	RW/WC	DescriptionModule output statistics	16'd0

5.4.14 port_srm

Storage register description: port configuration information, NumOfEntries is 35, words is 4.

Offset	Bits	Name	R/W	Description
0	0	use_upd_svid	RO	Use the modified svid as the internal vlanId
0	1	use_pkt_svid	R W	Use the SVID of the original message as the internal VLANId
0	2	stp_chk_en	R W	Spanning tree checking is enabled. Default value: 0: std_meta.manageMode = 0; 1: std_meta.manageMode = 1
0	3	vlan_filter_en	R W	vlan filter enable
0	4	brg_en	R W	Layer 2 bridge search enable, high effective
0	5	alw_same_cls_smv_rw_hm	RW hm class	Allows ports with the same priority to perform site shift operations
0	6:7		R W	Port priority in case of site relocation
0	8:10	smv_flag	RW Site	shift control enable, the meaning of each bit is described as follows: [0]: Discard enable; [1]: trap to CPU enable; [2]: site shift enable
0	11	lrn_upd_disable	R W	Disable address learning update enable
0	12:18	qos_profile_idx	R W	qos template index
0	19	qos_profile_vld	R W	qos template valid indication
0	20	in_port_mir_en	R W	Mirror enable of input port
0	21:22	ip_option_op	R W	Ip option packet processing behavior
0	23:24	ip_hdr_err_op	R W	IP header error packet processing behavior

0	25	v4_hdr_chk_trap	RW	IPv4 header check trap enable
0	26:31	v4_hdr_chk_drop_0	RW	IPv4 header check discard enable
1	0:12	v4_hdr_chk_drop_1	RW	IPv4 header check discard enable
1	13	v6_hdr_chk_trap	RW	IPv6 header check trap enable
1	14:31	v6_hdr_chk_drop_0	RW	IPv6 header check discard enable
2	0	v6_hdr_chk_drop_1	RW	IPv6 header check discard enable
2	1	tcp_dos_chk_trap	RW	TCP dos attack trap enable
2	2:31	tcp_dos_chk_drop_0	RW	TCP dos attack drop enable
3	0:1	tcp_dos_chk_drop_1	RW	TCP dos attack drop enable
3	2	icmp_dos_chk_trap	RW	ICMP DOS attack trap enable
3	3:18	icmp_dos_chk_drop	RW	icmp dos attack drop enable
3	19	erps_lkp_en	WO	Erps search enable

5.4.15 vlan_srm

Storage register description: vlan attribute table, NumOfEntries is 4096, words is 6.

Offset Bits		Name	R/W	Description
0	0	valid	RO	Effectively enable
0	1	bypass_en	RW	Bypass Enable
0	2	drop_en	RW	Discard Enable
0	3	trap_en	RW	Trap to CPU enable
0	4	dot1x_en	RW	1x authentication enabled, high effective
0	5	dot1x_drop	RW	1x authentication fails and discards the enabled state, high validity
0	6	in_fpol_vld	RW	Inlet hierarchical metering, effective indication of small and medium pipelines
0	7:13	qos_profile_idx	RW	qos profile_vld
0	14	RW		qos template valid indication
0	15:16	color	RW	Color, the specific codes are as follows: 0x0: RED 0x1: YELLOW 0x2: GREEN
0	17:19	priority	RW	Internal Priority
0	20	pri_vld	RW	Internal priority and color indication
0	21:29	stp_id	RW	Spanning Tree ID
0	30:31	l2_key_tp	RW	Layer 2 forwarding type: 0x0: BRIDGE; 0x1: SCC; 0x2: DCC
1	0	lrn_disable	RW	Disable address learning
1	1	lrn_upd_disable	RW	Disable address learning update enable
1	2	RW		Identify PDU bypass spanning tree check enable
1	3:31	port_bmp_0	RW	Port member, bit 0 represents port 0, and so on
2	0	port_bmp_1	RW	Port member, bit 0 represents port 0, and so on
2	1:8	lag_bmp	RW	lag member, bit 0 represents LAG port 0, and so on
2	9	vlan_isot_en	RW	Enable VLAN-based port isolation
2	10:13	vlan_isot_idx	RW	VLAN-based port isolation pointer
2	14	in_vlan_mir_en	RW	Ingress mirroring enabled
2	15	in_vlan_cnt_idx_vld	RW	vlan statistics enable
2	16	drop_ukw_uc	RW	Unknown unicast packet discard enable
2	17:18	pfm		RW multicast pfm parameter, controls the forwarding behavior of multicast messages, the specific coding is as follows Next: 0x0: Do not start searching, directly flood to all ports; 0x1: Start searching Search, forward the found ones to a specific port according to the search results, and forward the found ones to a specific port according to the search results.

				Discard; 0x2: Do not start searching, directly discard all messages; 0x3: Start Search, forward the found items to a specific port based on the search results, no search results Flood
2	19:31	pdu_op_0	RW L2PDU/L3PDU processing behavior, where bits [1:0] correspond to a protocol message The specific encoding is as follows: 0x0: NOP; 0x1: discard; 0x2: copy to CPU; 0x3: discard + copy To CPU	
3	0:31	pdu_op_1	RW L2PDU/L3PDU processing behavior, where bits [1:0] correspond to a protocol message The specific encoding is as follows: 0x0: NOP; 0x1: discard; 0x2: copy to CPU; 0x3: discard + copy To CPU	
4	0:18	pdu_op_2	RW L2PDU/L3PDU processing behavior, where bits [1:0] correspond to a protocol message The specific encoding is as follows: 0x0: NOP; 0x1: discard; 0x2: copy to CPU; 0x3: discard + copy To CPU	
4	19:20	mac_list_tp	RW mac address blacklist and whitelist mode: 0x1 indicates blacklist, 0x2 indicates whitelist	
4	21:31	fid_0	RW fid	
5		fid_1	RW fid	
5	0:1	fid_stm_ctl_vld	RW erps_id	FID-based storm control enablement
5	2:3		WO	Erps id

5.4.16 in_vlan_cnt_srm

Storage register description: vlan statistics, NumOfEntries is 4096, words is 3.

Offset Bits		Name	R/W	Description
0	0:31	pkt_cnt_0	RO	Frame Statistics
1	0:3	pkt_cnt_1	R W	Frame Statistics
1	4:31	byte_cnt_0	R W	Byte Statistics
2	0:13	byte_cnt_1	WO	Byte Statistics

5.4.17 stp_srm

Storage register description: stp state table, NumOfEntries is 512, words is 3.

Offset Bits		Name	R/W	Description
0	0:31	stp_status_0	RO	The spanning tree status of the port, where bits [1:0] correspond to port 0 and other ports And so on. The specific encoding is as follows: 0x0: STP_DISABLE; 0x1: STP_BLOCKING; 0x2: STP_LEARNING; 0x3: STP_FORWARDING;
1	0:31	stp_status_1	R W	The spanning tree status of the port, where bits [1:0] correspond to port 0 and other ports And so on. The specific encoding is as follows: 0x0: STP_DISABLE; 0x1: STP_BLOCKING; 0x2: STP_LEARNING; 0x3: STP_FORWARDING;
2	0:21	stp_status_2	WO	The spanning tree status of the port, where bits [1:0] correspond to port 0 and other ports And so on. The specific encoding is as follows: 0x0: STP_DISABLE; 0x1: STP_BLOCKING; 0x2: STP_LEARNING; 0x3: STP_FORWARDING;

5.4.18 erps_srm

Storage register description: stp state table, NumOfEntries is 128, words is 1.

Bits	Name	R/W	Description
0:29	port_bmp	R W	Erps port bmp

5.5 ifwd_reg

The ifwd_reg register block contains 28 registers and 15 storage registers.

The register list is as follows:

Register Offset	Register Name	Description
17'b0_0000_0000_0000_0000	storm_alm	Storm Control Alert
17'b0_0000_0000_0000_0001	lrn_int	Learning interruption
17'b0_0000_0000_0000_0100:	lrn_sta_ctl	Learning Status
17'b0_0000_0000_0000_0110	loop_ctl	Loopback processing configuration information
17'b0_0000_0000_0000_1000	mac_hash_alg_ctl brg_ctl	Mac table hash algorithm configuration
17'b0_0000_0000_0000_1001	lrn_ctl	L2 Bridge Global Configuration
17'b0_0000_0000_0000_1010:	brg_cnt	L2 Bridge Statistics Count
17'b0_0000_0000_0001_0010:	lrn_lmt_ctl	L2 Learning Global Configuration
17'b0_0000_0000_0001_1000	lrn_lmt_ctl	Global address learning threshold configuration
17'b0_0000_0000_0001_1001:	lrn_cnt	L2 Learning Statistics
17'b0_0000_0000_0010_0000:	aging_ctl	L2 Aging Global Configuration
17'b0_0000_0000_0010_0100:	aging_port_ctl	L2 Aging port enable
17'b0_0000_0000_0010_1100:	aging_range_ctl[2] Note	L2 Aging Range Configuration
17'b0_0000_0000_0011_0000	aging_timer_ctl	Normal aging time configuration
17'b0_0000_0000_0011_0001	fast_aging_ctl	Fast aging global configuration
17'b0_0000_0000_0011_0010	fast_aging_rule_ctl	Fast aging matching update rule configuration
17'b0_0000_0000_0011_0011 fast_aging_new	umac_ctl	Fast aging UMAC update domain segment configuration
17'b0_0000_0000_0011_0100:	umac_ctl	Configuration of fast aging UMAC matching domain
17'b0_0000_0000_0011_1000 storm_ctl	17'b0_0000_0000_0011_1010:	Storm Control Configuration
17'b0_0000_0000_0011_1011	storm_sys_ctl	Global Storm Control Configuration
17'b0_0000_0000_0011_1100:	storm_port_ctl	Port-based storm control configuration
17'b0_0000_0000_0011_1101	storm_fid_ctl	Fid-based storm control configuration
17'b0_0000_0000_0100_0000:	port_lrn_num_ctl[47] Note	Port-based address learning statistics
17'b0_0000_0000_0110_1110	port_lrn_lmt_ctl[47] Note	Port-based address learning threshold configuration
17'b0_0000_0000_1001_1110	sys_lrn_num_ctl	Global address learning threshold statistics

17'b0_0000_0000_1010_0000: 17'b0_0000_0000_1101_1111	mac_cam_ctl[32] Note	mac table supplement cam
17'b0_0000_0000_1110_0000: 17'b0_0000_0001_0001_1111	mac_cam_act_ctl[32] Note	The mac table adds the corresponding behavior of cam
17'b0_0000_0001_0010_0000	out_cnt_ctl Note:	Loopback processing configuration information
Each register list contains multiple (such as 2/47/32) identical registers, that is, the register word value, register threshold, etc. are the same.		

The storage register list is as follows:

Register Offset	Register Name	Description
17'b0_0000_0001_1000_0000: 17'b0_0000_0001_1100_0101	port_srm	Port configuration information
17'b0_0001_0000_0000_0000: 17'b0_0100_1111_1111_1111	mac_key_left_srm[4] Note: Look up the Key table (I2) based on the BRIGE mac address	
17'b0_0101_0000_0000_0000: 17'b0_1000_1111_1111_1111	mac_key_right_srm[4] Note: Look up the Key table based on BRIGE's mac address (I2)	
17'b0_1001_0000_0000_0000: 17'b0_1100_1111_1111_1111	mac_left_srm[4] Note	Port-based mac address behavior table (port)
17'b0_1101_0000_0000_0000: 17'b1_0000_1111_1111_1111	mac_right_srm[4] Note	Port-based mac address behavior table (port)
17'b1_0001_0000_0000_0000: 17'b1_0001_1111_1111_1111	fid_lrn_lmt_srm	FID-based address learning threshold configuration
17'b1_0010_0000_0000_0000: 17'b1_0010_1111_1111_1111	fid_lrn_num_srm	FID-based address learning threshold configuration
17'b1_0011_0000_0000_0000: 17'b1_0011_0000_0000_0111	storm_sys_srm	Global Storm Control Table
17'b1_0011_0000_0000_1000: 17'b1_0011_0000_0000_1011	storm_sys_cnt_srm	Global Storm Control Count Table
17'b1_0011_0010_0000_0000: 17'b1_0011_0011_0111_0111	storm_port_srm	Port-based storm control table
17'b1_0011_0100_0000_0000: 17'b1_0011_0100_1011_1011	storm_port_en_srm	Port-based storm control enable table
17'b1_0011_0101_0000_0000: 17'b1_0011_0101_1011_1011	storm_port_cnt_srm	Port-based storm control counter table
17'b1_0011_1000_0000_0000: 17'b1_1011_0111_1111_1111	storm_fid_srm[32]	The storm control table based on fid is divided into 32 Table with a depth of 8k
17'b1_1011_1000_0000_0000: 17'b1_1011_1001_1111_1111	storm_fid_en_srm	FID-based storm control enable table
17'b1_1011_1010_0000_0000: 17'b1_1011_1011_1111_1111 Note: Each	storm_fid_cnt_srm[32]	The storm control token count table based on fid is split into 32 tables with a depth of 128
register list contains multiple (such as 2/47/32) identical registers, that is, the register word value, register threshold, etc. are the same.		

5.5.1 storm_alm

Register offset: 17'b0_0000_0000_0000_0000

Register Description: Loopback processing configuration information srm_reg

Bits	Name	R/W	Description	Default
0	storm_alm_fid_storm_alm	RC	Storm Control Alarm Based on FID	1'd0
1	storm_alm_port_storm_alm	RC	Port-based storm control alarm	1'd0
2	storm_alm_sys_storm_alm	RC	Global Storm Control Alarm	1'd0

5.5.2 lrn_int

Register offset: 17'b0_0000_0000_0000_0001

Register Description: Loopback processing configuration information srm_reg

Bits	Name	R/W	Description	Default
0	lrn_int_lrn_int	RC	New mac address is learned	1'd0
1	lrn_int_lrn_int_mask RW		indicating mask	1'd1

5.5.3 lrn_sta_ctl

Register offset: 17'b0_0000_0000_0000_0100:17'b0_0000_0000_0000_0110

Register Description: Loopback processing configuration information srm_reg

Offset	Bits	Name	R/W	Description	Default
0	0	lrn_sta_ctl_valid	RO	DescriptionLearned	1'd0
0	1:31	lrn_sta_ctl_mac_0	RO	valid	31'd0
1	0:16	lrn_sta_ctl_mac_1	RO	indicationLearned	17'd0
1	17:28	lrn_sta_ctl_fid	RO	mac	12'd0
1	29:30	lrn_sta_ctl_key_tp	RO	valueLearned mac	2'd0
1	31	lrn_sta_ctl_src_path_in_lport_0 RO		valueLearned fid	1'd0
2	0:4	lrn_sta_ctl_src_path_in_lport_1 RO		valueLearned	5'd0
2	5	lrn_sta_ctl_src_path_in_is_lag RO		key_tp valueLearned_lport valueLearned_lport indication value	10'd0

5.5.4 loop_ctl

Register offset: 17'b0_0000_0000_0000_1000

Register Description: Loopback processing configuration information srm_reg

Bits	Name	R/W	Description	Default
0:7	loop_ctl_loop_bypass0	RW	Bypass indication of loopback packet, 0: no bypass; 1: bypass	8'd62
8:15	loop_ctl_loop_bypass1	RW	Bypass indication of loopback packet, 0: no bypass; 1: bypass	8'd62
16:23	loop_ctl_loop_bypass2	RW	Loopback packet bypass indication, 0: no bypass; 1: bypass	8'd62

5.5.5 mac_hash_alg_ctl

Register offset: 17'b0_0000_0000_0000_1001

Register Description: Mac table Hash algorithm configuration srm_reg

Bits	Name	R/W	Description Left	Default
0:1	mac_hash_alg_ctl_left_alg_tp RW		hash table algorithm, the specific encoding is as follows: 0x0: use the low bit of crc32 operation result; 0x1: Use crc16-BISYNC operation Result low; 0x2: use crc16-CCITT The low bit of the operation result; 0x3: use the key value Low	2'd0

2:3	mac_hash_alg_ctl_right_alg_tp RW		Right hash table algorithm, the specific encoding is as follows: 0x0: use the low bit of crc32 operation result; 0x1: Use crc16-BISYNC operation Result low; 0x2: use crc16-CCITT The low bit of the operation result; 0x3: use the key value Low	2'd0
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5.5.6 brg_ctl

Register offset: 17'b0_0000_0000_0000_1010

Register Description: L2 Bridge Global Configuration

Bits	Name	R/W	Description	Default
0	brg_ctl_stp_chk_en	R W	Spanning tree status check enable	1'd0
1	brg_ctl_cc_src_path_chk_port RW SCC/DCC source path check port enable	1'd0		
2	brg_ctl_cc_port_no_match_drop RW SCC/DCC search port mismatch drop enable	1'd0		
3	brg_ctl_cc_port_no_match_drop_to_cpu RW		SCC/DCC find port mismatch trap to CPU Enable	1'd0
4	brg_ctl_cc_no_match_drop	RW	SCC/DCC search failure discard enable	1'd0
5	brg_ctl_cc_no_match_drop_to_cpu	R W	SCC/DCC search failure trap to CPU Can	1'd0
6	brg_ctl_bc_obey_mc_pfm	RW	broadcast message follows multicast pfm rule	1'd0
7	brg_ctl_drop_bc	RW	1'd0 Broadcast message discard enable	
8	brg_ctl_brg_cam_en	R W	L2 Table Cam Enable	1'd1

5.5.7 brg_cnt

Register offset: 17'b0_0000_0000_0001_0000:17'b0_0000_0000_0001_0110

Register Description: L2 Bridge Statistics Count

Offset	Bits	Name	R/W	Description	Default
0	0:31	l2_brg_drop_cnt_0:3	RW/RC	Statistics of the number of packets discarded by Layer 2 processing in normal mode	32'd0
1	brg_cnt_l2_brg_drop_cnt_1	RW/RC Statistics of		The number of packets dropped by Layer 2 processing in normal mode	4'd0
1	4:31	brg_cnt_l2_brg_cnt_0	RW/RC	The number of packets forwarded normally by Layer 2 processing in normal mode statistics	28'd0
2	0:7	brg_cnt_l2_brg_cnt_1	RW/RC	The number of packets forwarded normally by Layer 2 processing in normal mode Statistics	8'd0
2	8:31	brg_cnt_scc_brg_drop_cnt_0	RW/RC Statistics of	packets dropped by Layer 2 processing in SCC mode	24'd0
3	0:11	brg_cnt_scc_brg_drop_cnt_1	RW/RC Statistics of	the number of packets dropped by Layer 2 processing in SCC mode	12'd0
3	12:31	brg_cnt_scc_brg_cnt_0		Number of packets forwarded normally by Layer 2 processing in RW/RC SCC mode statistics	20'd0
Statistics	4:0	15 brg_cnt_scc_brg_cnt_1		Number of packets forwarded normally by Layer 2 processing in RW/RC SCC mode	16'd0
4	16:31	brg_cnt_dcc_brg_drop_cnt_0	RW/RC Statistics of	the number of packets dropped by Layer 2 processing in DCC mode	16'd0
5	0:19	brg_cnt_dcc_brg_drop_cnt_1	RW/RC Statistics of	the number of packets dropped by Layer 2 processing in DCC mode	20'd0

5:20:31	brg_cnt_dcc_brg_cnt_0	Number of packets forwarded normally by Layer 2 processing in RW/RC DCC mode statistics	12'd0
6:0:23	brg_cnt_dcc_brg_cnt_1	Number of packets forwarded normally by Layer 2 processing in RW/RC DCC mode statistics	24'd0

5.5.8 lrn_ctl

Register offset: 17'b0_0000_0000_0001_1000

Register Description: L2 Learning Global Configuration

Bits	Name	R/W	Description	Default
0	learning Enable	R W	Disable address	1'd0
1	lrn_ctl_lrn_disable_lrn_ctl_port_chk_fail_to_cpu	RW	Port binding failure trap to CPU Enable	1'd0
2	lrn_ctl_cbhm_en	R W	Priority-based site shifting	1'd0
3	lrn_ctl_src_list_upd_en	R W	enables updates of whitelist entries in non-whitelist mode, Yes, indicating that the SMAC replacement of the message is enabled	1'd0
4	lrn_ctl_smv_cls_fail_drop	RW	Priority-based site shift failure discard enable	1'd0
5	lrn_ctl_smv_cls_fail_to_cpu	RW	Priority-based site shift failure trap to CPU	1'd0
6	overflow discard enable lrn_ctl_lrn_num_exd_drop	RW	Address learning threshold	1'd0
7	RW lrn_ctl_lrn_num_exd_to_cpu	RW	Address learning threshold overflow trap to CPU enable	1'd0
8	lrn_ctl_upd_num_exd_drop	RW	Site shift learning threshold overflow drop enable	1'd0
9	lrn_ctl_upd_num_exd_to_cpu	RW	Site shift threshold overflow trap to CPU enable	1'd0
10	lrn_ctl_lrn_umac_bkt_ovfw_trap	RW	Learning overflow trap to CPU enable	1'd0

5.5.9 lrn_lmt_ctl

Register offset: 17'b0_0000_0000_0001_1001

Register Description: Global address learning threshold configuration

Bits	Name	R/W	Description Aging	Default
0	lrn_lmt_ctl_age_num_lmt_en	RW	threshold control Enable	1'd0
1	lrn_lmt_ctl_lrn_num_lmt_en	RW	address learning threshold control	1'd0
2:16	lrn_lmt_ctl_lrn_num_thrd	RW	Enable address learning threshold	15'd0

5.5.10 lrn_cnt

Register offset: 17'b0_0000_0000_0010_0000:17'b0_0000_0000_0010_0100

Register Description: L2 Learning Statistics Count

Offset	Bits	Name	R/W	Description 0	Default
0:31	lrn_cnt_fid_lrn_num_exd_cnt_0	RW/WC	Address learning threshold overflow message statistics based on fid	32'd0	
	0:3	lrn_cnt_fid_lrn_num_exd_cnt_1	RW/WC	Statistics of address learning threshold overflow messages based on fid	4'd0
1:4:31	lrn_cnt_port_lrn_num_exd_cnt_0	RW/WC	Port-based address learning threshold overflow message statistics	28'd0	
	0:7	lrn_cnt_port_lrn_num_exd_cnt_1	RW/WC	Port-based address learning threshold overflow message statistics	8'd0
2:2:8:31	lrn_cnt_sys_lrn_num_exd_cnt_0	RW/WC	Statistics of packets with global address learning threshold overflow	24'd0	

3:0:11	lrn_cnt_syst_lrn_num_exd_cnt_1	RW/WC	Statistics of packets with global address learning threshold overflow	12'd0
3:12:31	lrn_cnt_lrn_bkt_ovfw_cnt_0	RW/WC	Address table overflow message statistics	20'd0
4:0:15	lrn_cnt_lrn_bkt_ovfw_cnt_1	RW/WC	Address table overflow message statistics	16'd0

5.5.11 aging_ctl

Register offset: 17'b0_0000_0000_0010_1000:17'b0_0000_0000_0010_1001

Register Description: L2 Aging Global Configuration

Offset	Bits	Name	R/W	Description	Default
0:0:31		aging_ctl_s_counter_thrd	R W	Seconds timing threshold	s_counter_thrd
1	0	aging_ctl_aging_en	R W	Address aging Enable	1'd1
1	1	aging_ctl_disable_lrn_num_exd_del	RW	aging Replace operation Disable learning threshold overflow Delete original entry enable	1'd0
1		aging_ctl_disable_nrm_age_sid	RW	Normal aging prohibition of deletion of black and white list indication entry enable	1'd0
1	2:3	aging_ctl_disable_nrm_age_udm	RW	Normal aging prohibits deletion of pending entries to enable	1'd0
1	4	aging_ctl_nrm_age_clr_udm	RW	Normal aging clear pending confirmation entry status enable	1'd0
1	5	Fast aging_SCC_entry_enable	RW	Fast aging DCC entry enable	1'd0
1	6		R W		
1	7	aging_ctl_fast_aging_sid_umac	RW	Fast aging black and white list UMAC indication entry enable	1'd0
1	8	aging_ctl_fast_aging_slt_umac	RW	Fast aging black and white list UMAC status entry enable	1'd0
1	9	aging_ctl_fast_aging_udm_umac	RW	Fast aging pending confirmation UMAC entry enable	1'd0
1	10	aging_ctl_fast_aging_stc_umac	RW	Fast aging static UMAC entry enable	1'd0
1	11	aging_ctl_fast_aging_mode	RW	Fast aging mode, the specific coding is as follows: 0x0: FAST_AGING_DEL; 0x1:FAST_AGING REP	1'd0
1	12	aging_ctl_fast_aging_by_half	RW	Fast aging two-stage mode enable	1'd0
1	13	aging_ctl_fast_aging_all	R W	Fast aging clear enable	1'd0

5.5.12 aging_port_ctl

Register offset: 17'b0_0000_0000_0010_1010: 17'b0_0000_0000_0010_1011

Register Description: L2 Aging Port Enable

Offset	Bits	Name	R/W	Description	Port	Default
0:31		aging_port_ctl_en_0	RW	aging enable	Port	32'd4294967295
1	0:13	aging_port_ctl_en_1	RW	aging enable		14'd16383

5.5.13 aging_range_ctl[2]

Register offset: 17'b0_0000_0000_0010_1100: 17'b0_0000_0000_0010_1111

Register Description: L2 Aging Range Configuration srm_reg

Note: Each register list contains multiple (eg. 2) identical registers, that is, the register word value, register threshold, etc. are all the same.

Offset	Bits	Description	Default	Name	R/W	
0	0:10	aging_range_ctl_left_start_ptr	RW	Address aging operation left hash table starting index	11'd0	

0	11:21	aging_range_ctl_left_end_ptr RW Address	aging operation left hash table end index 11'd2047	
0	22:31	aging_range_ctl_right_start_ptr_0 RW Address	aging operation right hash table start index 10'd0	
1	0	aging_range_ctl_right_start_ptr_1 RW Address	aging operation right hash table starting index 1'd0	
1	1:11	aging_range_ctl_right_end_ptr RW Address	aging operation right hash table end index 11'd2047	

5.5.14 aging_timer_ctl

Register offset: 17'b0_0000_0000_0011_0000

Register Description: Normal Aging Time Configuration

Bits	Name	R/W	Description	Default
0:31	aging_timer_ctl_counter_thrd RW		Normal aging time threshold	old32'd300

5.5.15 fast_aging_ctl

Register offset: 17'b0_0000_0000_0011_0001

Register Description: Rapid Aging Global Configuration

Bits	Name	R/W	Description	Default
0	fast_aging_ctl_fast_aging_en RW/RC		Address fast aging enable	1'd0

5.5.16 fast_aging_rule_ctl

Register offset: 17'b0_0000_0000_0011_0010

Register Description: Fast Aging Match Update Rule Configuration

Bits	Name	R/W	Description	Default
0:9	fast_aging_rule_ctl_umac_aging_rule RW		on UMAC address fast matching rules, The body is described as follows: [9]: Based on inlsLag and inLport; [8]: based on srcInd; [7]: based on srcList; [6]: Based on fecIdTp and fecId; [5]: Based on hmClass; [4]: Based on static; [3]: Based on Based on aging; [2]: Based on FID; [1]: Based on MAC; [0]: Based on I2KeyTp,	10'd0
10:16	fast_aging_rule_ctl_umac_aging_upd RW		the address fast update rule based on UMAC has The body is described as follows: [6]: Based on srcInd; [5]: Based on srcList; [4]: based on inlsLag and inLport; [3]: Based on fecPathTp and fecPath; [2]: Based on Based on hmClass; [1]: Based on static; [0]: Based on aging	7'd0

5.5.17 fast_aging_new_umac_ctl

Register offset: 17'b0_0000_0000_0011_0011

Register Description: Configuration of the fast aging UMAC update field

Bits	Name	R/W	Description	Default
0	fast_aging_new_umac_ctl_aging	RW	Aging status bit, 1 indicates semi-aging status 1'd0	
1	fast_aging_new_umac_ctl_static	R W	Static indication 1'd0	
3	fast_aging_new_umac_ctl_hm_class	RW Port priority	In case of site shift 2'd0	
4	fast_aging_new_umac_ctl_src_list	R W	Source MAC blacklist and whitelist status	
5	fast_aging_new_umac_ctl_src_ind	RW Source	MAC blacklist and whitelist indication	1'd0
6:8	fast_aging_new_umac_ctl_fec_path_tp	RW	Forwarding FEC type, the specific encoding is as follows: 0x0: NOP; 0x1: PORT; 0x2: L2FLD; 0x3: MC; 0x4: PROTO; 0x5: PROT1	3'd0
9:20	fast_aging_new_umac_ctl_fec_path	RW	Forward FEC ID	12'd0
21:22	fast_aging_new_umac_ctl_in_is_lag	RW	Indicates whether the input internal logical port number is LAG Port, high effective	1'd0
22:27	fast_aging_new_umac_ctl_in_lport	RW	Internal logical port number of input, when inlsLag has If it is valid, it indicates a LAG port; otherwise, it indicates a normal port. mouth.	6'd0

5.5.18 fast_aging_old_umac_ctl

Register offset: 17'b0_0000_0000_0011_0100:17'b0_0000_0000_0011_0111

Register Description: Fast aging UMAC match domain configuration srm_reg

Offset	Bits	Name	R/W	Description	Default
0	0:1	fast_aging_old_umac_ctl_l2_key_tp	R W	Layer 2 forwarding type: 0x0: BRIDGE; 0x1: SCC; 0x2: DCC mac	2'd0
	2:31				
	fast_aging_old_umac_ctl_mac_0	RW	0:17	fast_aging_old_umac_ctl_mac_1 address mac	30'd0
	18:29	fast_aging_old_umac_ctl_fid	RW	1 12'd0 address	18'd0
	30	fast_aging_old_umac_ctl_aging	RW	Aging status bit, 1 indicates half aging status 1'd0	
1		fast_aging_old_umac_ctl_static	RW	Static indication 31 1'd0	
2	0:1	fast_aging_old_umac_ctl_hm_class	RW	Port priority In case of site shift 2'd0	
	2:4	fast_aging_old_umac_ctl_fec_path_tp	RW	Forwarding FEC type, the specific encoding is as follows: 0x0: NOP; 0x1: PORT; 0x2: L2FLD; 0x3: MC; 0x4: PROTO; 0x5: PROT1 3'd0	3'd0
2:5	16	fast_aging_old_umac_ctl_fec_path	RW	Forward FEC ID	12'd0
2:17	22	fast_aging_old_umac_ctl_in_lport	RW	Internal logical port number of the input. If it is valid, it indicates a LAG port; otherwise, it indicates a normal port. mouth.	6'd0
2	23	fast_aging_old_umac_ctl_in_is_lag	RW	Indicates whether the input internal logical port number is LAG Port, high effective	1'd0
24		fast_aging_old_umac_ctl_src_list	RW	source MAC black and white list status	1'd0
25		fast_aging_old_umac_ctl_src_ind	RW	source MAC black and white list indication	1'd0

5.5.19 storm_ctl

Register offset: 17'b0_0000_0000_0011_1000

Register Description: Storm Control Configuration

Bits	Name	R/W	Description	Default
0:5	storm_ctl_preamble_len	RW	Preamble and frame gap equivalent packet length	6'd0
6:9	storm_ctl_meter_gran	RW	Control granularity 4'd0	
10:13	storm_ctl_sys_en	RW	Storm control enable	4'd0

5.5.20 storm_sys_ctl

Register offset: 17'b0_0000_0000_0011_1010:17'b0_0000_0000_0011_1011

Register Description: Global Storm Control Configuration

Offset	Bits	Name	R/W	Description	Default
0:0:31		period_storm_sys_ctl_delay_interval	RW	Fill token bucket	32'd0
1	0:1	storm_sys_ctl_max_upd_idx	RW	token bucket maximum address	2'd0
1	2	storm_sys_ctl_upd_en	RW	Fill token bucket enable	1'd0
1	3:16	storm_sys_ctl_pkt_len_use_pkt	RW	Equivalent packet length when metering based on packets	14'd0

5.5.21 storm_port_ctl

Register offset: 17'b0_0000_0000_0011_1100:17'b0_0000_0000_0011_1101

Register Description: Port-based Storm Control Configuration

Offset	Bits	Name	R/W	Description	Default
0:0:31		storm_port_ctl_delay_interval	RW	token bucket cycle Fill	32'd0
1	0:9	storm_port_ctl_max_upd_idx	RW	token bucket maximum address	10'd0
enable	11:10	storm_port_ctl_upd_en	RW	Fill token bucket	
1	11:24	storm_port_ctl_pkt_len_use_pkt	RW	Equivalent packet length when metering based on packets	14'd0

5.5.22 storm_fid_ctl

Register offset: 17'b0_0000_0000_0011_1110:17'b0_0000_0000_0011_1111

Register Description: Fid-based storm control configuration

Offset	Bits	Name	R/W	Description	Default
0:0:31		period_storm_fid_ctl_delay_interval	RW	Fill token bucket	32'd0
1	0:12	storm_fid_ctl_max_upd_idx	RW	token bucket maximum address	13'd0
1	13	storm_fid_ctl_upd_en	RW	Fill token bucket enable	1'd0
1	14:27	storm_fid_ctl_pkt_len_use_pkt	RW	Equivalent packet length when metering based on packets	14'd0

5.5.23 port_lrn_num_ctl[47]

Register offset: 17'b0_0000_0000_0100_0000:17'b0_0000_0000_0110_1110

Register Description: Port-based address learning statistics

Note: Each register list contains multiple (eg 47) identical registers, that is, the register word values, register thresholds, etc. are all the same.

Bits	Description	Name	R/W		Default
0:14	Address learning statistics	port_lrn_num_ctl_lrn_num	RW/RC		15'd0

5.5.24 port_lrn_lmt_ctl[47]

Register offset: 17'b0_0000_0000_0110_1111: 17'b0_0000_0000_1001_1101

Register Description: Port-based address learning threshold configuration

Note: Each register list contains multiple (eg 47) identical registers, that is, the register word values, register thresholds, etc. are all the same.

Bits	Description	Name	R/W	Enable Address Learning Threshold	Default
0	port_lrn_lmt_ctl_age_num_lmt_en	RW			1'd0
1	port_lrn_lmt_ctl_lrn_num_lmt_en	RW			1'd0
2:16	port_lrn_lmt_ctl_lrn_num_thrd	R W			15'd0

5.5.25 sys_lrn_num_ctl

Register offset: 17'b0_0000_0000_1001_1110

Register Description: Global address learning threshold statistics

Bits	Name	R/W	Description	Default
0:14	sys_lrn_num_ctl_lrn_num	RW/RC	Address learning statistics	5'd0

5.5.26 mac_cam_ctl[32]

Register offset: 17'b0_0000_0000_1010_0000:17'b0_0000_0000_1101_1111

Register Description: mac table supplement cam

Note: Each register list contains multiple (eg 32) identical registers, that is, the register word value, register threshold, etc. are all the same.

Offset	Bits	Description	Name	R/W	Default
0	0	valid 0:1	1:30 key	R/W	
		mac_cam_ctl_valid		RW/RC	1'd0
		mac_cam_ctl_key_0		RW/RC	31'd0
		mac_cam_ctl_key_1		RW/RC	31'd0

5.5.27 mac_cam_act_ctl[32]

Register offset: 17'b0_0000_0000_1110_0000:17'b0_0000_0001_0001_1111

Register Description: mac table supplements cam corresponding behavior

Note: Each register list contains multiple (eg 32) identical registers, that is, the register word value, register threshold, etc. are all the same.

Offset	Bits	Name	R/W	Description	Default
0	0	mac_cam_act_ctl_aging_static	RW/RC	Aging status bit, 1 indicates half-aging status	1'd0
0	1	mac_cam_act_ctl_static_1'd0	indication	RW/RC	
0	2	mac_cam_act_ctl_dst_trap	RW/RC	Destination MAC address trap to CPU	Enable 1'd0
0	3	mac_cam_act_ctl_dst_drop	RW/RC	Destination MAC address filter indication	1'd0
0	4	mac_cam_act_ctl_src_trap	RW/RC	Source MAC address trap to CPU	Enable 1'd0
0	5	mac_cam_act_ctl_src_drop	RW/RC	Source MAC address filter indication	1'd0
0	6	status_mac_cam_act_ctl_src_list	RW/RC	source MAC black and white list	
0	7	mac_cam_act_ctl_src_ind	RW/RC	Source MAC blacklist and whitelist	1'd0
0	8	mac_cam_act_ctl_in_dmac_mir_en	RW/RC		1'd0
0	9	mac_cam_act_ctl_in_smac_mir_en	RW/RC		1'd0

0 10:11		mac_cam_act_ctl_color	RW/RC	Color, the specific encoding is as follows: 0x0: RED; 0x1: YELLOW; 0x2: GREEN	2'd0
0 12:14		priority mac_cam_act_ctl_priority	RW/RC	Internal	3'd0
0 15	mac_cam_act_ctl_pri_vld 16	RW/RC	Internal priority and color valid indication 1'd0		
0	mac_cam_act_ctl_smv_port_chk_en	RW/RC	Port-based station shift check enable 1'd0		
0 17:18	Forward	mac_cam_act_ctl_hm_class	RW/RC	Port priority in case of site shift 2'd0	
0 19:21		FEC type, the specific encoding is as follows: mac_cam_act_ctl_fec_path_tp	RW/RC	0x0: NOP; 0x1: PORT; 0x2: L2FLD; 0x3: MC; 0x4: PROTO; 0x5: PROT1	3'd0
0 22:31		ID mac_cam_act_ctl_fec_path_0	RW/RC	Forward FEC	10'd0
1	0:1	mac_cam_act_ctl_fec_path_1	RW/RC	FEC ID	2'd0
1	2:7	mac_cam_act_ctl_src_path_in_lport	RW/RC	internal logical port number. If valid, it indicates a LAG port; otherwise, it indicates a normal port. Pass port.	6'd0
1	8	mac_cam_act_ctl_src_path_in_is_la	RW/RC	Indicates whether the input internal logical port number is LAG port, high	1'd0
1	effective 9	mac_cam_act_ctl_src_path_chk_en	RW/RC	Source path information check enable	1'd0

5.5.28 out_cnt_ctl

Register offset: 17'b0_0000_0001_0010_0000

Register Description: Loopback processing configuration information srm_reg

Bits	Name	R/W	Description	Default
0:15	out_cnt_ctl_pkt_cnt	RW/RC	Module output statistics	16'd0

5.5.29 port_srm

Storage register description: port configuration information, NumOfEntries is 35, words is 2.

Offset	Bits	Name	R/W	Description
0	0:4	port_isot_en_bmp	RO	Port isolation is enabled. The specific description of each bit is as follows: [0]: known unicast; [1]: unknown [2]: known unicast; [3]: known multicast; [4]: broadcast
0	5:6	allow_port_to_src	RW	Loopback enable, the meaning of each bit is described as follows: [0]: L2 Bridge mode Allow loopback on the same port; [1]: Allow loopback on the same port in SCC/DCC mode
0	7	cc_svid_use_upd	RW	SCC/DCC looks up the svid in key from the updated svid value
0	8	cc_svid_use_vlan_id	RW	The svid in the SCC/DCC lookup key comes from the internal vlanid
0	9	cc_cvid_use_upd	RW	SCC/DCC looks up the cvid in the key from the updated cvid value
0	10 cc	cvid_use_vlan_id	RW	The cvid in the SCC/DCC lookup key comes from the internal vlanid
0	11:13	fec_id_tp	R W	Forward FEC type, the specific encoding is as follows: 0x0: NOP; 0x1: PORT 0x2: L2FLD; 0x3: MC; 0x4: PROTO; 0x5: PROT1
0	14:25	fec_id	R W	Forward FEC ID
0	26:27	pro_group	R W	
0	28	prot_sta	R W	Protection port indication
0	29	lrn_miss_to_cpu	RW	Source address lookup failure trap to CPU enable

0	30	lrn_miss_drop RW		Source address lookup failure discard enable
0	31	prot_ind_0	R W	Protection port indication, 2'b00: non-protection group; 2'b10: 1:1 protection group; 2'b11: 1+1 protection group
1	0	prot_ind_1	R W	Protection port indication, 2'b00: non-protection group; 2'b10: 1:1 protection group; 2'b11: 1+1 protection group
	1:2	prot_id	RW	Protection group id
11	3	drop_ukw_uc WO		

5.5.30 mac_key_left_srm[4]

Storage register description: Look up the Key table (I2) based on the mac address of BRIDGE, NumOfEntries is 2048, and words is 2.

Note: Each register list contains multiple (eg 4) identical registers, that is, the register word value, register threshold, etc. are all the same.

Offset	Bits	Name	R/W	Description
0	0	valid	RO	Effective instructions
0	1:31	mac_0	R W	mac address
	0:16	mac_1	R W	mac address
11	17:28	fid	R W	
1	29:30	key_tp	WO Layer 2 forwarding type: 0x0: BRIDGE; 0x1: SCC; 0x2: DCC	

5.5.31 mac_key_right_srm[4]

Storage register description: Look up the Key table (I2) based on the mac address of BRIDGE, NumOfEntries is 2048, and words is 2.

Note: Each register list contains multiple (eg 4) identical registers, that is, the register word value, register threshold, etc. are all the same.

Offset	R/W	Description	Name	
0	0	valid	RO	Effective instructions
0	1:31	mac_0	R W	mac address
1	0:16	mac_1	R W	mac address
1	17:28	fid	R W	Forwarding instance ID
1	29:30	key_tp	WO Layer 2 forwarding type: 0x0: BRIDGE; 0x1: SCC; 0x2: DCC	

5.5.32 mac_left_srm[4]

Storage register description: Port-based mac address behavior table (port), NumOfEntries is 2048, words is 2.

Note: Each register list contains multiple (eg 4) identical registers, that is, the register word value, register threshold, etc. are all the same.

Offset	Bits	Name	R/W	
0	0	aging	RO	Aging status bit, 1 indicates semi-aging status
0	1:1	static	R W	
0	2	dst_trap	R W	Destination MAC address trap to CPU enable
0	3	dst_drop	R W	Destination MAC address filtering indication
0	4	src_trap	R W	Source MAC address trap to CPU enable
0	5	src_drop	R W	Source MAC address filtering indication
0	6	src_list	R W	Source MAC blacklist and whitelist status
0	7	src_ind	RW	Source MAC blacklist and whitelist indication
0	8	in_dmac_mir_en	RW	
0	9	in_smac_mir_en	RW	
0	10:11	color	R W	Color, the specific codes are as follows:

				0x0: RED 0x1: YELLOW 0x2: GREEN
0	12:14	priority	R W	Internal Priority
0	15	pri_vld	R W	Internal priority and color indication
0	16	smv_port_chk_en RW hm_class		Port-based site shift check enable
0	17:18		R W	Port priority in case of site relocation
0	19:21	fec_path_tp	R W	Forward FEC type, the specific encoding is as follows: 0x0: NOP; 0x1: PORT 0x2: L2FLD; 0x3: MC; 0x4: PROT0; 0x5: PROT1
0	22:31	fec_path_0	R W	Forward FEC ID
1	0:1	fec_path_1	R W	Forward FEC ID
1	2:7	src_path_in_lport RW		The internal logical port number of the input. When inlsLag is valid, it indicates LAG port, otherwise it indicates a normal port.
1	8	src_path_in_is_lag RW		Indicates whether the input internal logical port number is a LAG port, high effective
1	9	src_path_chk_en WO		Source path information check enable

5.5.33 mac_right_srm[4]

Storage register description: Port-based mac address behavior table (port), NumOfEntries is 2048, words is 2.

Note: Each register list contains multiple (eg 4) identical registers, that is, the register word value, register threshold, etc. are all the same.

Offset	Bit/Field	Name	R/W	
0	0	aging	RO	
0		static	R W	
0	1	dst_trap	R W	
0	2	dst_drop	R W	
0	3	src_trap	R W	
0	4	src_drop	R W	
0	5:6	src_list	R W	Source MAC blacklist and whitelist status
0	7	src_ind	RW	Source MAC blacklist and whitelist indication
0	8	in_dmac_mir_en RW		
0	9	in_smac_mir_en RW		
0	10:11	color	R W	Color, the specific codes are as follows: 0x0: RED 0x1: YELLOW 0x2: GREEN
0	12:14	priority	R W	Internal Priority
0	15	pri_vld	R W	Internal priority and color indication
0	16	smv_port_chk_en RW		
0	17:18	hm_class	R W	
0	19:21	fec_path_tp	R W	
0	22:31	fec_path_0	R W	
1	0:1	fec_path_1	R W	
1	2:7	src_path_in_lport RW		The internal logical port number entered. When inlsLag is valid, it indicates that the LAG port Otherwise, it indicates a common port.
1	8	src_path_in_is_lag RW		Indicates whether the input internal logical port number is a LAG port, high effective
1	9	src_path_chk_en WO		

5.5.34 fid_lrn_lmt_srm

Storage register description: fid-based address learning threshold configuration, NumOfEntries is 4096, words is 1.

Bits	Name	R/W	Description
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0	age_num_lmt_en	RO	Aging threshold control enable
1	lrn_num_lmt_en	R/W	Address learning threshold control enable
2:15	lrn_num_thrd	WO	Address learning threshold

5.5.35 fid_lrn_num_srm

Storage register description: fid-based address learning threshold configuration, NumOfEntries is 4096, words is 1.

Bits	Name	R/W	Description
0:13	age_num_lmt_en RW		Address learning statistics

5.5.36 storm_sys_srm

Storage register description: Based on the global storm control table, NumOfEntries is 4 and words is 2.

Offset	Bits	Name	R/W	Description
0	0:3	bucket_thrd_shift RO		bucket size parameter: bucketSize = bucketThrd << bucketThrdShift
0	4:17	bucket_thrd RW		Bucket size parameter: bucketSize = bucketThrd << bucketThrdShift
0	18:31	bucket_rate_0 RW		Bucket token fill rate
1	0:3	bucket_rate_1 RW		Bucket token fill rate
1	4	pkt_bytes WO	0x0: policing based on bytes; 0x1: policing based on packets	

5.5.37 storm_sys_cnt_srm

Storage register description: Based on the global storm control count table, NumOfEntries is 4, words is 1.

Bits	Name	R/W	Description
0:23	bucket_cnt	R/W	Bucket token counter.

5.5.38 storm_port_srm

Storage register description: port-based storm control table, NumOfEntries is 188, words is 2.

Offset	Bits	Name	R/W	Description
0	0:3	bucket_thrd_shift RO		bucket size parameter: bucketSize = bucketThrd << bucketThrdShift
0	4:17	bucket_thrd RW		Bucket size parameter: bucketSize = bucketThrd << bucketThrdShift
0	18:31	bucket_rate_0 RW		Bucket token fill rate
1	0:3	bucket_rate_1 RW		Bucket token fill rate
1	4	pkt_bytes WO	0x0: policing based on bytes; 0x1: policing based on packets	

5.5.39 storm_port_en_srm

Storage register description: Port-based storm control enable table, NumOfEntries is 188, words is 1.

Bits	Name	R/W	Description
0	en	R/W	Storm control enabled.

5.5.40 storm_port_cnt_srm

Storage register description: Port-based storm control counter table, NumOfEntries is 188, words is 1.

Bits	Name	R/W	Description
0:23	bucket_cnt	R W	Bucket token counter.

5.5.41 storm_fid_srm[32]

Storage register description: Storm control table based on fid, the table is split into 32 tables with a depth of 8k, NumOfEntries is 512, words is 2.

Note: Each register list contains multiple (eg 32) identical registers, that is, the register word value, register threshold, etc. are all the same.			
Offset	Name	R/W	Description
0	bucket_threashold	RO /	
0	bucket_fid	RW /	
0	bucket_rate	RW /	
1	bucket_rate	RW /	
1	pkt_bytes	WO /	

5.5.42 storm_fid_en_srm

Storage register description: FID-based storm control enable table, NumOfEntries is 512, words is 1.

Bits	Name	R/W	Description
0:31	en	R W	Storm control enabled.

5.5.43 storm_fid_cnt_srm[32]

Storage register description: FID-based storm control token count table, which is split into 32 tables with a depth of 128, NumOfEntries is 512, and words is 1.

Note: Each register list contains multiple (eg 32) identical registers, that is, the register word value, register threshold, etc. are all the same.			
Bits	Name	Description	R/W
0:23	bucket_cnt	Bucket token counter.	R W

5.6 iacl_reg

The iacl_reg register module contains 6 registers and 4 storage registers.

The register list is as follows:

Register Offset	Register Name	Description
15'b000_0000_0000_0000	loop_ctl	Loopback processing configuration information
15'b000_0000_0000_0010:15'b000_0000_0000_0011	lkp_ctl	discards the lookup configuration information srm_reg
15'b000_0000_0000_0100:15'b000_0000_0000_0110	ctl	Configuration Entries
15'b000_0000_0000_1000	rst_sample_ctl	Sampling statistics configuration
15'b000_0000_0001_0000:15'b000_0000_0001_0111	rst_ctl	acl search result configuration information
15'b000_0000_0001_1000	out_cnt_ctl	loopback processing configuration information srm_reg

The storage register list is as follows:

Register Offset	Register Name	Description
15'b000_0000_0100_0000:15'b000_0000_0110_0010	port_srm	Port configuration information

15'b010_0000_0000_0000:15'b010_0101_1111_1111	tcm	Find Key Table
15'b100_0000_0000_0000:15'b100_0111_1111_1111	tcm_srm	Lookup behavior table
15'b100_1000_0000_0000:15'b100_1101_1111_1111	in_flow_srm	Flow Statistics

5.6.1 loop_ctl

Register offset: 15'b000_0000_0000_0000

Register Description: Loopback processing configuration information

Bits	Name	R/W	Description	Default
0:7	loop_ctl_loop_bypass	RW	Loopback packet bypass indication, 0: no bypass; 1: bypass	8'd62

5.6.2 lkp_ctl

Register offset: 15'b000_0000_0000_0010:15'b000_0000_0000_0011

Register Description: Discard search configuration information srm_reg

Offset	Bits	Name	R/W	Description Enables	Default
0	0:31	lkp_ctl_drop bmp 0	RW	the search for various packet loss reasons	32'd0
1	0:31	lkp_ctl_drop bmp 1	RW	Enables the search for various packet loss reasons	32'd0

5.6.3 ctl

Register offset: 15'b000_0000_0000_0100:15'b000_0000_0000_0110

Register Description: Configuration Entries

Offset	Bits	Name	R/W	Description	Default
0:19	ctl_mac_key_rst_ctl	RW	{indexBase[8:0],keySize[1:0]}	tableBase[8:0] 20'd0	
0	20:31	ctl_ipv4_key_rst_ctl	0	RW Same as macKeyRstCtl 12'd0	
1	0:7	ctl_ipv4_key_rst_ctl_1	RW	Same as macKeyRstCtl ctl_ipv6_key_rst_ctl	8'd0
1	8:27	RW	Same as macKeyRstCtl 28:31	ctl_mix_key_rst_ctl_0 RW Same as macKeyRstCtl 0:15	20'd0
1	as macKeyRstCtl 0:15	ctl_mix_key_rst_ctl_1	RW	Same as macKeyRstCtl	4'd0
2					16'd0

5.6.4 rst_sample_ctl

Register offset: 15'b000_0000_0000_1000

Register Description: Sampling Statistics Configuration

Bits	Name	R/W	Description	Default
0:15	rst_sample_ctl_sample_cnt_en	RW/RC	Sampling statistics enable	6'd0

5.6.5 rst_ctl

Register offset: 15'b000_0000_0001_0000:15'b000_0000_0001_0111

Register Description: acl search result configuration information

Offset Bits		Name	R/W	Description Maximum	Default
0	0:14	rst_ctl_sample_cnt0 RW	rst_ctl_res0	value of sampling statistics	15'd0
0	15		R W	res	1'd0
0	16:30	rst_ctl_sample_cnt1 RW	rst_ctl_res1	Sampling statistics maximum value	15'd0
0	31		R W	res	1'd0
	0:14	rst_ctl_sample_cnt2 RW	rst_ctl_res2	Sampling statistics maximum value	15'd0
11	15		R W	res	1'd0
	16:30	rst_ctl_sample_cnt3 RW	rst_ctl_res3	Sampling statistics maximum value	15'd0
11	31		R W	res	1'd0
	0:14	rst_ctl_sample_cnt4 RW	rst_ctl_res4	Sampling statistics maximum value	15'd0
twenty two	15		R W	res	1'd0
	16:30	rst_ctl_sample_cnt5 RW	rst_ctl_res5	Sampling statistics maximum value	15'd0
twenty two	31		R W	res	1'd0
3	0:14	rst_ctl_sample_cnt6 RW	rst_ctl_res6	Sampling statistics maximum value	15'd0
3	15		R W	res	1'd0
3	16:30	rst_ctl_sample_cnt7 RW	rst_ctl_res7	Sampling statistics maximum value	15'd0
3	31		R W	res	1'd0
4	0:14	rst_ctl_sample_cnt8 RW	rst_ctl_res8	Sampling statistics maximum value	15'd0
4	15		R W	res	1'd0
4	16:30	rst_ctl_sample_cnt9 RW	rst_ctl_res9	Sampling statistics maximum value	15'd0
4	31		R W	res	1'd0
5	0:14	rst_ctl_sample_cnt10 RW	rst_ctl_res10	Sampling statistics maximum value	15'd0
5	15		R W	res	1'd0
5	16:30	rst_ctl_sample_cnt11 RW	rst_ctl_res11	Sampling statistics maximum value	15'd0
5	31		R W	res	1'd0
6	0:14	rst_ctl_sample_cnt12 RW	rst_ctl_res12	Sampling statistics maximum value	15'd0
6	15		R W	res	1'd0
6	16:30	rst_ctl_sample_cnt13 RW	rst_ctl_res13	Sampling statistics maximum value	15'd0
6	31		R W	res	1'd0
7	0:14	rst_ctl_sample_cnt14 RW	rst_ctl_res14	Sampling statistics maximum value	15'd0
7	15		R W	res	1'd0
7	16:30	rst_ctl_sample_cnt15 RW		Sampling statistics maximum value	15'd0

5.6.6 out_cnt_ctl

Register offset: 15'b000_0000_0001_1000

Register Description: Loopback processing configuration information srm_reg

Bits	Name	R/W	DescriptionModule	Default
0:15	out_cnt_ctl_pkt_cnt	RW/RC	output statistics	16'd0

5.6.7 port_srm

Storage register description: port configuration information, NumOfEntries is 35, words is 1.

Bits	Name	R/W	Description
0	acl0_lkp_vld	WO	Acl0 search enable

1	acl1_lkp_vld	R W	Acl1 search enable
2	mac_key_use_llc	R W	Using LLC Domains
3	ipv4_force_mix_key0	R W	Acl0 lookup, IPv4 packets use mix key
4	ipv4_force_mac_key0	R W	Acl0 search, IPv4 packets use mac key
5	ipv4_force_ipv6_key0	R W	Acl0 search, IPv4 packets use IPv6 key
6	ipv6_force_mix_key0	R W	Acl0 lookup, IPv6 packets use mix key
7	ipv6_force_mac_key0	R W	Acl0 search, IPv6 packet uses mac key
8	ipv6_force_ipv4_key0	R W	Acl0 lookup, IPv6 packets use IPv4 key
9	mac_force_mix_key0	R W	Acl0 search, Ethernet packets use mix key
10	mac_force_ipv6_key0	R W	Acl0 search, Ethernet packets use ipv6 key
11	mac_force_ipv4_key0	R W	Acl0 search, Ethernet packets use ipv4 key
12	ipv4_force_mix_key1	R W	Acl1 lookup, IPv4 packets use mix key
13	ipv4_force_mac_key1	R W	Acl1 search, IPv4 packets use mac key
14	ipv4_force_ipv6_key1	R W	Acl1 search, IPv4 packet uses IPv6 key
15	ipv6_force_mix_key1	R W	Acl1 lookup, IPv6 packets use mix key
16	ipv6_force_mac_key1	R W	Acl1 search, IPv6 packet uses mac key
17	ipv6_force_ipv4_key1	R W	Acl1 lookup, IPv6 packets use IPv4 key
18	mac_force_mix_key1	R W	Acl1 search, Ethernet packets use mix key
19	mac_force_ipv6_key1	R W	Acl1 search, Ethernet packets use ipv6 key
20	mac_force_ipv4_key1	RO	Acl1 search, Ethernet packets use ipv4 key

5.6.8 tcm

Storage register description: Look up the Key table, NumOfEntries is 512, words is 11.

Offset	Bits	Name	R/W	Description
0	0:31	acl0_lkp_vld	WO	Find key
1	0:31	acl1_lkp_vld	R W	Find key
2	0:31	mac_key_use_llc	R W	Find key
3	0:31	ipv4_force_mix_key0	R W	Find key
4	0:31	ipv4_force_mac_key0	R W	Find key
5	0	ipv4_force_ipv6_key0	R W	Effective instructions
5	1:31	ipv6_force_mix_key0	R W	Find key mask
6	0:31	ipv6_force_mac_key0	R W	Find key mask
7	0:31	ipv6_force_ipv4_key0	R W	Find key mask
8	0:31	mac_force_mix_key0	R W	Find key mask
9	0:31	mac_force_ipv6_key0	R W	Find key mask
10	0	mac_force_ipv4_key0	R W	Find key mask
10	1	ipv4_force_mix_key1	RO	Valid indication mask

5.6.9 tcm_srm

Storage register description: Lookup behavior table, NumOfEntries is 512, words is 4.

Offset	Bits	Name	R/W	Description
0	0:11	fec_id	WO	Forward FEC ID
0	12:14	fec_id_tp	RW	Forward FEC type, the specific encoding is as follows: 0x0: NOP; 0x1: PORT; 0x2: L2FLD; 0x3: MC; 0x4: PROT0; 0x5: PROT1

			RW	Service forwarding type, the specific encoding is as follows: 0x0: NOP; 0x1: PORT; 0x2: L2; 0x3: SCC; 0x4: DCC; other values are preset
0	15:17	fwd_tp		Keep
0	18	fwd_tp_vld	R W	Service forwarding type enable
0	19	redir_en	RW	Redirection Enable
0	20:23	sample_thrd_shift	RW	Control ipfix random stream sampling rate (1/2, 1/4, ...)
0	empty four	ipfix_en	RW	ipfix enable
0	25:31	in_fpol_idx_0	R W	Hierarchical entry meter small and medium pipeline index
1	0:4	in_fpol_idx_1	R W	Hierarchical entry meter small and medium pipeline index
1	5	in_fpol_vld	R W	Inlet hierarchical metering, effective indication of small and medium pipelines
1	6:8	queue_num	R W	Queue Number
1	9	queue_vld	R W	queueNum valid indication
1	10:18	in_flow_cnt_idx	R W	Ingress flow statistics index
1	19	in_flow_cnt_idx_vld	RW	Ingress flow statistics enable
1	20:26	qos_profile_idx	RW	qos template index
1	27	qos_profile_vld	R W	qos template valid indication
			R W	Color, the specific encoding is as follows: 0x0: RED; 0x1: YELLOW; 0x2: GREEN
1	28:29	color	R W	Internal Priority
1	30:31	priority_0	R W	Internal Priority
2	0	priority_1	R W	Internal priority and color indication
2	1	pri_vld	R W	Redirect to CPU Enable
2	2	trap_en	R W	Discard Enable
2	4	bypass	R W	Bypass indication, 0 means invalid, 15 is the highest weight
	5	bypass_en	R W	Bypass Enable
empty two	6	permit	R W	permit
2	7:11	pdu_idx	R W	Protocol PDU Type
2	12	pdu_idx_en	R W	Protocol PDU type enable
2	13	upd_stag_vld	R W	Update stag valid indication
2	14:16	upd_scos	R W	Update scos value
2	17	upd_scfi	R W	Update scfi value
2	18:29	upd_svid	R W	Update svid value
2	30	upd_ctag_vld	R W	Update ctag valid instructions
2	31	upd_ccos_0	R W	Update ccos value
3	1	upd_ccos_1	R W	Update ccos value
3	2	upd_ccfi	R W	Update ccfi value
3	3:14	upd_cvrid	R W	Update cvrid value
			R W	Update information enable, each bit corresponds to a different updInfo, specific description As follows: [0]:{updStagVld,updScos,updScfi,updSvid}; [1]:{updCtagVld,updCcoss,updCcfsi,updCvrid}; [2]:{pduldxEn,pduldx}
3	15:17	upd_bmp	RW	Sampling mode, 1 means fixed sampling, 0 means random sampling
3	18	sample_mode	RW	Sampling mode, 1 means fixed sampling, 0 means random sampling
3	19:22	sample_profile	RO	Fixed sampling template

5.6.10 in_flow_srm

Storage register description: flow statistics, NumOfEntries is 512, words is 3.

Offset Bits	Name	R/W	Description
0	0:31	WO	Frame Statistics
1	0:3	R W	Frame Statistics
1	4:31	R W	Byte Statistics
2	0:13	RO	Byte Statistics

5.7 ipol_reg

The ipol_reg register module contains 7 registers and 7 storage registers.

The register list is as follows:

Register Offset	Register Name	Description
17'b0_0000_0000_0000_0000	loop_ctl	Loopback processing configuration information
17'b0_0000_0000_0000_0001	ctl	iPol configuration information
17'b0_0000_0000_0000_0010: 17'b0_0000_0000_0011	mpol_ctl	mpol enable
17'b0_0000_0000_0000_0100: 17'b0_0000_0000_0101	flow_upd_ctl	Update configuration of policing srm_reg
17'b0_0000_0000_0000_0110: 17'b0_0000_0000_0111	macro_upd_ctl_alm	Update configuration of policing srm_reg
17'b0_0000_0000_0000_1000		Policing alarm register
17'b0_0000_0000_0000_1001	out_cnt_ctl	Loopback processing configuration information srm_reg

The storage register list is as follows:

Register Offset	Register Name	Description
17'b0_0000_0000_1000_0000: 17'b0_0000_0000_1111_1111	qos_pro_srm	Priority Mapping Template Configuration
17'b0_0000_0001_0000_0000: 17'b0_0000_0001_1111_1111	cos_pri_map_srm_priority	mapping configuration based on vlan cos
17'b0_0001_0000_0000_0000: 17'b0_0001_1111_1111_1111	dscp_pri_map_srm_ip_dscp	based priority mapping configuration
17'b0_1000_0000_0000_0000: 17'b0_1100_1111_1111_1111	flow_meter_srm	Meter parameter table
17'b1_0000_0000_0000_0000: 17'b1_0001_1111_1111_1111	flow_meter_cnt_srm	Token Bucket Counter
17'b1_0010_0000_0000_0000: 17'b1_0010_0000_1010_1110	macro_meter_srm	Meter parameter table
17'b1_0010_0010_0000_0000: 17'b1_0010_0010_0100_0101	macro_meter_cnt_srm	Token Bucket Counter

5.7.1 loop_ctl

Register offset: 17'b0_0000_0000_0000_0000

Register Description: Loopback processing configuration information

Bits	Name	R/W	Description	Default
0:7	loop_ctl_loop_bypass0	RW	Loopback packet bypass indication, 0: no bypass; 1: bypass 8'd62	
8:15	loop_ctl_loop_bypass1	RW	Bypass indication of loopback packet, 0: no bypass; 1: bypass 8'd62	

5.7.2 ctl

Register offset: 17'b0_0000_0000_0000_0001

Register Description: iPol Configuration Information

Bits	Name	R/W	DescriptionPreamble	Default
0:5	ctl_preamble_len	R W	and interframe gap equivalent packet length	6'd0
6:9	ctl_meter_gran	R W	control granularity	4'd0
10	ctl_flow_pkt_bytes	RW	mode, 0x0: byte-based policing; 0x1: packet-based policing	1'd0
11	ctl_macro_pkt_bytes	R W	macro mode, 0x0: byte-based policing; 0x1: packet-based policing	1'd0
12:25	ctl_pkt_len_use_pkt	RW	When policing is based on packets, the equivalent packet length is 14'd0	

5.7.3 mpol_ctl

Register offset: 17'b0_0000_0000_0000_0010:17'b0_0000_0000_0000_0011

Register Description: mpol enable

Offset Bits	Name	R/W	Description	Default
0	0:31 mpol_ctl_m_pol_en_0	RW 0:2	mpol enable, one bit per port mpol	32'd0
1	mpol_ctl_m_pol_en_1	RW	enable, one bit per port	3'd0

5.7.4 flow_upd_ctl

Register offset: 17'b0_0000_0000_0000_0100:17'b0_0000_0000_0000_0101

Register Description: policing update configuration srm_reg

Offset Bits	Name	R/W	DescriptionToken	Default
0	0:14	R W	refresh cycle parameter	15'd0
0	15:29	R W	Token bucket refresh flow_upd_ctl_timer1 reserved flow_upd_ctl_timer0	2'd0
0	30:31	R W	flow_upd_ctl_timer1 num_cycle parameter flow_upd_ctl_reserved	4'd0
1	0:3	R W	Token bucket refresh cycle parameter flow_upd_ctl_timer0_num RW Maximum	4'd0
1	4:7	R W	address of each physical table filling token bucket 9'd0	
1	8:16	R W	flow_upd_ctl_max_upd_idx RW Fill token bucket to enable token bucket refresh cycle	1'd0
1	17	R W	parameter	15'd0

5.7.5 macro_upd_ctl

Register offset: 17'b0_0000_0000_0000_0110: 17'b0_0000_0000_0000_0111

Register Description: policing update configuration srm_reg

Offset Bits	Name	R/W	DescriptionToken	Default
0	0:14	R W	bucket refresh cycle parameter	15'd0
0	15:29	R W	reserved	15'd0

0	30:31	macro_upd_ctl_reserved RW Token bucket refresh cycle parameter		2'd0
1	0:3	macro_upd_ctl_timer1_num RW Token bucket refresh cycle parameter 4'd0		
1	4:7	macro_upd_ctl_timer0_num RW Maximum address of the token bucket filled in each physical table 4'd0		
1	8:13	macro_upd_ctl_max_upd_idx RW		Fill token bucket enable 6'd0
1	14	macro_upd_ctl_upd_en	RW	Token bucket refresh cycle parameters 1'd0

5.7.6 alm

Register offset: 17'b0_0000_0000_0000_1000

Register Description: Policing alarm register

Bits	Name	R/W	Description	Default
0	alm_rate_exd	RW/RC	Speeding warning	1'd0

5.7.7 out_cnt_ctl

Register offset: 17'b0_0000_0000_0000_1001

Register Description: Loopback processing configuration information srm_reg

Bits	Name	R/W	Description	Default
0:15	out_cnt_ctl_pkt_cnt	RW/RC	Module output statistics	16'd0

5.7.8 qos_pro_srm

Storage register description: Priority mapping template configuration, NumOfEntries is 128, words is 1.

Bits	Name	R/W	Description
0:5	phb_ptr	RO	PHB table index pointer high 6 bits
6	trust_ctag	R W	0x0: Use STAG first; 0x1: Use CTAG
7	use_l2_info	R W	0x0: Use L3 header information first; 0x1: Use L2 header information
8	use_default	WO	1: Use default priority; 0: Other

5.7.9 cos_pri_map_srm

Storage register description: priority mapping configuration based on vlan cos, NumOfEntries is 256, words is 1.

Bits	Name	R/W	Description
0:1	color0	RO	color
2:4	priority0	R W	priority
5:6	color1	R W	color
7:9	priority1	R W	priority
10:11	color2	R W	color
12:14	priority2	R W	priority
15:16	color3	R W	color
17:19	priority3	WO	priority

5.7.10 dscp_pri_map_srm

Storage register description: priority mapping configuration based on ip dscp, NumOfEntries is 4096, words is 1.

Bits	Name	R/W	Description
0:1	color0	RO	color
2:4	priority0	R W	priority
5:6	color1	R W	color
7:9	priority1	R W	priority
10:11	color2	R W	color
12:14	priority2	R W	priority
15:16	color3	R W	color
17:19	priority3	WO	priority

5.7.11 flow_meter_srm

Storage register description: Meter parameter table, NumOfEntries is 4096, words is 5.

Offset Bits	Name	R/W	Description
0	0:3 excess_thrd_shift RO e Bucket size parameter: ebs = excessThrd << excessThrdShift		
0	4:19 excess_thrd_e Maximum number of tokens added to a bucket	RW e	Bucket size parameter: ebs = excessThrd << excessThrdShift
0	20:31 excess_rate_max_0 RW tokens added to a bucket		
1	excess_rate_max_1 RW e Maximum number of tokens added to a bucket		
1	6:23 excess_rate RW e Bucket token fill rate	RW e	Bucket token fill rate
1	24:27 commit_thrd_shift RW c Bucket size parameter: cbs = commitThrd << commitThrdShift		
1	28:31 commit_thrd_0 RW c Bucket size parameter: cbs = commitThrd << commitThrdShift		
2	0:11 commit_thrd_1 RW c Bucket size parameter: cbs = commitThrd << commitThrdShift		
2	12:29 commit_rate_max RW commit_rate_0		c The maximum number of tokens added to bucket
2	RW 30:31 commit_rate_1 RW		c Bucket token fill rate
3	0:15		c Bucket token fill rate
3	16:17 meter_sharing_mode RW		0x0: Not SharingMode; 0x1: MIN_ONLY; 0x2: MAX_ONLY; 0x3: MIN_MAX
3	18 rfc4115_mode RW 0x1: ffc4115 mode; 0x0: dual rate three color marking mode;		
3	19 sr_tcm_mode RW	RW 0x1	single rate three-color marking mode; 0x0: non-single rate three-color marking mode
3	20 global_c_flag Global C bucket to E bucket coupling flag		
3	color_blind_0x0: color aware mode; 0x1: color-blind mode.	RW	
3	g_change_drop RW Green message update drop enable		
3	y_change_drop RW yellow message update drop enable		Yellow message update drop enable
3	RW Red message update drop enable		
3	g_change_pri R W		Green message update pri enable
3	y_change_pri Yellow message update pri enable	RW	
3	r_change_pri Themessage R W update pri enable		
3	28:30 g_pri new pri value of the green message (color == 2'b10)	RW	
3	31 y_pri_0 The new pri value of the yellow message (color == 2'b01)	RW	
4	0:1 y_pri_1 New pri value for yellow message (color == 2'b01)	RW	
4	2:4 r_pri The new pri value of the red message (color == 2'b00)	WO	

5.7.12 flow_meter_cnt_srm

Storage register description: Token bucket counter, NumOfEntries is 4096, words is 2.

Offset Bits		Name	R/W	Description
0	0:31	excess_cnt	RO	E Bucket token counter.
1	0:31	commit_cnt	WO	C Bucket token counter.

5.7.13 macro_meter_srm

Storage register description: Meter parameter table, NumOfEntries is 35, words is 5.

Offset Bits		Name	R/W	Description
0	0:3	excess_thrd_shift	RO	e Bucket size parameter: ebs = excessThrd << excessThrdShift
0	4:19	excess_thrd	e	Maximum number of tokens added to a bucket
0	20:31	excess_rate_max_0	RW	0x5: Maximum number of tokens added to a bucket
1		excess_rate_max_1	RW	e Maximum number of tokens added to a bucket
1	6:23	excess_rate	RW	e Bucket token fill rate
1	24:27	commit_thrd_shift	RW	c Bucket size parameter: cbs = commitThrd << commitThrdShift
1	28:31	commit_thrd_0	RW	c Bucket size parameter: cbs = commitThrd << commitThrdShift
2	0:11	commit_thrd_1	RW	c Bucket size parameter: cbs = commitThrd << commitThrdShift
2	12:29	commit_rate_max	RW	commit_rate_0
2				c The maximum number of tokens added to bucket
2		RW	30:31	commit_rate_1
3	0:15			c Bucket token fill rate
3	16:17	meter_sharing_mode	RW	0x0: Not SharingMode; 0x1: MIN_ONLY; 0x2: MAX_ONLY; 0x3: MIN_MAX
3	18	rfc4115_mode	RW	0x1: ffc4115 mode; 0x0: dual rate three color marking mode;
3	19	sr_tcm_mode	RW	0x1: single rate three-color marking mode; 0x0: non-single rate three-color marking mode
3	20	global_c_flag	Global	C bucket to E bucket coupling flag
3	twenty one	color_blind	RW	0x0: color-aware mode; 0x1: color-blind mode.
3	twenty two	g_change_drop	RW	Green message update drop enable
3	twenty three	y_change_drop	RW	Yellow message update drop enable
3	twenty four	r_change_drop	RW	Red message update drop enable
3	25	g_change_pri	RW	Green message update pri enable
3	26	y_change_pri	RW	Yellow message update pri enable
3	27	r_change_pri	RW	Red message update pri enable
3	28:30	g_pri	RW	new pri value of the green message (color == 2'b10)
3	31	y_pri_0	RW	The new pri value of the yellow message (color == 2'b01)
4	0:1	y_pri_1	RW	The new pri value of the yellow message (color == 2'b01)
4	2:4	r_pri	WO	The new pri value of the red message (color == 2'b00)

5.7.14 macro_meter_cnt_srm

Storage register description: Token bucket counter, NumOfEntries is 35, words is 2.

Offset Bits		Name	R/W	Description
0	0:31	excess_cnt	RO	E Bucket token counter.
1	0:31	commit_cnt	WO	C Bucket token counter.

5.8 idst_reg

The idst_reg register block contains 7 registers and 3 storage registers.

The register list is as follows:

Register Offset	Register Name	Description
15'b000_0000_0000_0000	loop_ctl	loopback processing configuration information srm_reg
15'b000_0000_0000_0001	ctl	Global configuration information
15'b000_0000_0000_0010:15'b000_0000_0000_0011	prot_ctl	Protection Configuration
15'b000_0000_0000_0100:15'b000_0000_0000_0101	mc_bmp	multicast configuration
15'b000_0000_0000_0110	tx_prot_ctl	protected send port
15'b000_0000_0000_1000:15'b000_0000_0000_1010	drop_ctl	discard configuration information srm_reg
15'b000_0000_0000_1010	out_cnt_ctl	loopback processing configuration information srm_reg

The storage register list is as follows:

Register Offset	Register Name	Description
15'b010_0000_0000_0000:15'b011_1111_1111_1111	mc_grp_srm	Multicast group member index configuration
15'b100_0000_0000_0000:15'b100_0000_0011_1111	drop_cnt_code	srm Ingress statistics drop reason
15'b101_0000_0000_0000:15'b101_1111_1111_1111	drop_cnt	srm Ingress drop reason statistics

5.8.1 loop_ctl

Register offset: 15'b000_0000_0000_0000

Register Description: Loopback processing configuration information srm_reg

Bits	Name	R/W	Description	Default
0:7	loop_ctl_loop_bypass0	RW	Loopback packet bypass indication, 0: no bypass; 1: bypass	8'd0
8:15	loop_ctl_loop_bypass1	RW	Loopback packet bypass indication, 0: no bypass; 1: bypass	8'd0

5.8.2 ctl

Register offset: 15'b000_0000_0000_0001

Register Description: Global Configuration Information

Bits	Name	R/W	Description	Default
0	ctl_trap_to_cpu_port	R W	message update to CPU port enable cpu port	1'd0
1:6	ctl_cpu_port	R W	number bypass	6'd0
7	ctl_bypass_over_flow_cnt	RW	statistics overflow indication	1'd0
8	ctl_trap_no_vld_fld_bmp	RW	Flood portBmp invalid trap to CPU enable	1'd0
9	ctl_prot_oam_en	R W	oam packet sending enable port bmp	1'd0
10:14	ctl_port_bmp_hi	R W	during protection	5'd0

5.8.3 prot_ctl

Register offset: 15'b000_0000_0000_0010:15'b000_0000_0000_0011

Register Description: Discard configuration information srm_reg

Offset	Bits	Name	R/W	Description	Port	Default
0:29	0:30:31	prot_ctl_port_en	R W	when		30'd1073741823
1:0:5		prot_ctl_lag_en_0	RW			2'd3
		prot_ctl_lag_en_1	RW	protectedEnabled	Protection lagEnabled	6'd63

5.8.4 mc_bmp_ctl

Register offset: 15'b000_0000_0000_0100:15'b000_0000_0000_0101

Register Description: Discard configuration information srm_reg

Offset	Bits	Name	R/W	Description	Default
0:0:29	mc_bmp_ctl_port_en	RW	0:30:31	Enable the port for multicast	30'd1073741823
mc_bmp_ctl_lag_en_0	RW	1:0:5	mc_bmp_ctl_lag_en_1		2'd3
	RW				6'd63

5.8.5 tx_prot_ctl

Register offset: 15'b000_0000_0000_0110

Register Description: Discard configuration information srm_reg

Bits	Name	R/W	Description	Default
0:27	tx_prot_ctl_port	R W	Protected sending port	28'd0

5.8.6 drop_ctl

Register offset: 15'b000_0000_0000_1000:15'b000_0000_0000_1010

Register Description: Discard configuration information srm_reg

Offset	Bits	Name	R/W	Description	Trap	Default
0	0:31	drop_ctl_drop_trap_bmp_0	RW	discarded packets to the CPU Yes, each bit corresponds to a dropCode coding		32'd0
1	0:31	drop_ctl_drop_trap_bmp_1	RW	Traps discarded packets to the CPU Yes, each bit corresponds to a dropCode coding		32'd0

5.8.7 out_cnt_ctl

Register offset: 15'b000_0000_0000_1010

Register Description: Loopback processing configuration information srm_reg

Bits	Name	R/W	Description	Module	Default
0:15	out_cnt_ctl_pkt_cnt	RW/RC		output statistics	16'd0

5.8.8 mc_grp_srm

Storage register description: Multicast group member index configuration, NumOfEntries is 4096, words is 2.

Offset	Bits	Name	R/W	Description
0	0:29	port_bmp	RO	Multicast port indication
0	30:31	lag_bmp_0	R W	Multicast trunk port indication
1	0:5	lag_bmp_1	WO	Multicast trunk port indication

5.8.9 drop_cnt_code_srm

Storage register description: Entry statistics discard reason, NumOfEntries is 64, words is 1.

Bits	Name	R/W	Description
0:4	cnt_code	R W	The reason code for discarded packets statistics

5.8.10 drop_cnt_srm

Storage register description: Entry discard reason statistics, NumOfEntries is 2048, words is 2.

Offset	Bits	Name	R/W	Description
0	0:31	pkt_cnt_0	RO	Statistics of discarded packets based on reasons
1	0:3	pkt_cnt_1	WO	Statistics of discarded packets based on reasons

5.9 eee_reg

The eee_reg register module contains 5 registers and 10 storage registers.

The register list is as follows:

Register Offset	Register Name	Description
17'b0_0000_0000_0000_0000	loop_ctl	Loopback processing configuration information
17'b0_0000_0000_0000_1000: 17'b0_0000_0000_0000_1100	def_vlan_ctl	Default VLAN attributes
17'b0_0000_0000_0001_0000: 17'b0_0000_0000_0001_0001	xlate_hash_alg_ctl[2] Note	xlate table Hash algorithm configuration, implementation When actually generated, it is placed at an address
17'b0_0000_0000_0001_0010: 17'b0_0000_0000_0001_0101	xlate_key_ctl[4] Note	Xlate table Hash algorithm configuration srm_reg
17'b0_0000_0000_0001_0110 out_cnt_ctl Note: Each register list contains multiple (such as 2/4) identical registers, that is, the register word value, register threshold, etc. are the same.		Loopback processing configuration information srm_reg

The storage register list is as follows:

Register Offset	Register Name	Description
17'b0_0000_0001_0000_0000: 17'b0_0000_0001_1000_0000	port_srm	Port attributes
17'b0_1000_0000_0000_0000: 17'b0_1100_1111_1111_1111	vlan_srm	Vlan Properties
17'b1_0000_0000_0000_0000: 17'b1_0000_0011_1111_1111	xlate_key_left_srm[4] Note	egress vlan xlate key

17'b1_0000_0100_0000_0000: 17'b1_0000_0111_1111_1111	xlate_key_right_srm[4] Note the key of the export vlan xlate	
17'b1_0000_1000_0000_0000: 17'b1_0000_1011_1111_1111	xlate_left_srm[4] Note	Egress vlan xlate behavior
17'b1_0000_1100_0000_0000: 17'b1_0000_1111_1111_1111	xlate_right_srm[4] Note	Egress vlan xlate behavior
17'b1_0001_0000_0000_0000: 17'b1_0001_0000_0101_1111	xlate_tcm	Tcam key
17'b1_0001_0000_1000_0000: 17'b1_0001_0000_1011_1111	xlate_tcm_srm	Tcam Behavior
17'b1_0001_0000_1100_0000: 17'b1_0001_0000_1101_1111	vlan_op_srm	Vlan Operation Behavior
17'b1_0001_0001_0000_0000: 17'b1_0001_0001_1111_1111 Note: Each	erps_srm	Erps status

register list contains 4 identical registers, that is, the register word value, register threshold, etc. are all the same.

5.9.1 loop_ctl

Register offset: 17'b0_0000_0000_0000_0000

Register Description: Loopback processing configuration information.

Bits	Name	R/W	Description	Default
0:7	loop_ctl_loop_bypass	RW	Loopback packet bypass indication, 0: no bypass; 1: bypass	3'd0
8:9	loop_ctl_erps_num	RW	0:16; 1:32; 2:64; 3:128 2'd0	

5.9.2 def_vlan_ctl

Register offset: 17'b0_0000_0000_0000_1000:17'b0_0000_0000_0000_1100

Register Description: Default VLAN attributes.

Offset	Bits	Name	R/W	Description	Default
0	0	DescriptionBypass	RO		1'd0
0	1	enabledef_vlan_ctl_en	RW	bypass_en Drop	1'd0
0	2	def_vlan_ctl_queue_num	RW	trap to CPU enable def_vlan_ctl_trap_en	1'd0
0	3:5	RW queue number def_vlan_ctl_queue	RW	queueNum valid indication	3'd0
0	6	def_vlan_ctl_out_fpol_vld	RW	egress hierarchical meter small pipe valid indication	1'd0
0	7	1'd0			
0	8	def_vlan_ctl_rmk_pri_ptr_vld	RW	Priority reverse label information template valid indication	1'd0
0	9:16	information template def_vlan_ctl_rmk	RW	pri_pt 8'd0 Priority reverse label	
0	17:25	def_vlan_ctl_stp_id_port	RW	spanning tree ID	9'd0
0	RW def_vlan_ctl_un_stag_bmp_1	RW	port unstag indication	26:31 def_vlan_ctl_un_stag_bmp_0	6'd0
1	0:28	port untag indication	29:31 def_vlan_ctl_un_ctag_bmp_0	RW	29'd0
1	def_vlan_ctl_un_ctag_bmp_1	RW	port unctag indication		3'd0
2	0:31	egress mirroring enable	def_vlan_ctl_out_vlan_mir_en	RW	32'd0
3	0	def_vlan_ctl_out_vlan_cnt_idx	vld	RW egress	1'd0
3		vlan statistics enable			1'd0
3	1:2:3	def_vlan_ctl_erps_id	RW	Erps id	2'd0

3	4:31	def_vlan_ctl_port_bmp_0 RW	Port member, bit 0 represents port 0, and so on Push; default value: case (std_meta.padHubMode) 3'd0: 0x300000ff // 8port, corresponding to logical port 0~7,24,25; 3'd1: 0x3000000f // 4port, corresponding to logical port 0~3,24,25; 3'd2: 0x30000fff // 12port, corresponding logic Port 0~11,24,25; 3'd3: 0x3000ffff // 16port, corresponding to logical ports 0~15,24,25; 3'd4: 0x300fffff // 20port, corresponding to the logical port 0~19,24,25; 3'd5: 0x30fffff // 24port, corresponding to logical port 0~23,24,25; 3'd6: 0x30003fff // 14port, corresponding to the logical port Port 0~13,24,25; 3'd7: 0x30000fff // 12port, corresponding to logical ports 0~11,24,25.	def_std_meta_padhubmode_0
4	0:1	def_vlan_ctl_port_bmp_1 RW	Port member, bit 0 represents port 0, and so on Push; default value: case (std_meta.padHubMode) 3'd0: 0x300000ff // 8port, corresponding to logical port 0~7,24,25; 3'd1: 0x3000000f // 4port, corresponding to logical port 0~3,24,25; 3'd2: 0x30000fff // 12port, corresponding logic Port 0~11,24,25; 3'd3: 0x3000ffff // 16port, corresponding to logical ports 0~15,24,25; 3'd4: 0x300fffff // 20port, corresponding to the logical port 0~19,24,25; 3'd5: 0x30fffff // 24port, corresponding to logical port 0~23,24,25; 3'd6: 0x30003fff // 14port, corresponding to the logical port Port 0~13,24,25; 3'd7: 0x30000fff // 12port, corresponding to logical ports 0~11,24,25.	def_std_meta_padhubmode_1
4	2:9	def_vlan_ctl_lag_bmp WO	Lag port mbp	8'd0

5.9.3 xlate_hash_alg_ctl[2]

Register offset: 17'b0_0000_0000_0001_0000:17'b0_0000_0000_0001_0001

Register Description: xlate table Hash algorithm configuration, placed at an address when actually generated.

Note: Each register list contains 2 identical registers, that is, the register word value, register threshold, etc. are the same.

Bits	Name	R/W	Description Left	Default
0:1	xlate_hash_alg_ctl_left_alg_tp RW		hash table algorithm, the specific encoding is as follows: 0x0: use crc32 operation result low bit; 0x1: use crc16-BISYNC Operation result low bit; 0x2: use crc16-CCITT operation result 0x3: Use the low bit of the key value	2'd0
2:3	xlate_hash_alg_ctl_right_alg_tp RW		Right hash table algorithm, the specific encoding is as follows: 0x0: use crc32 operation result low bit; 0x1: use crc16-BISYNC Operation result low bit; 0x2: use crc16-CCITT operation result 0x3: Use the low bit of the key value	2'd0

5.9.4 xlate_key_ctl[4]

Register offset: 17'b0_0000_0000_0001_0010:17'b0_0000_0000_0001_0101

Register Description: xlate table Hash algorithm configuration srm_reg

Note: Each register list contains 4 identical registers, that is, the register word value, register threshold, etc. are all the same.

Bits	Name	R/W	Description	Default
0	xlate_key_ctl_xlate1_use_ccfi RW		xlate1 uses ccfi or not, high effective	1'd0
1	xlate_key_ctl_xlate0_use_ccfi RW		xlate0 uses ccfi or not, high effective	1'd0
2	xlate_key_ctl_xlate1_use_ccos RW		xlate1 uses ccos or not, high effective	1'd0
3	xlate_key_ctl_xlate0_use_ccos RW		xlate0 uses ccos or not, high effective	1'd0
4	xlate_key_ctl_xlate1_use_cvid RW		xlate1 uses cvid or not, high effective	1'd0
5	xlate_key_ctl_xlate0_use_cvid RW		xlate0 uses cvid or not, high effective	1'd0
6	xlate_key_ctl_xlate1_use_scfi RW		xlate1 uses scfi or not, high effective	1'd0
7	xlate_key_ctl_xlate0_use_scfi RW		xlate0 uses scfi or not, high effective	1'd0
8	xlate_key_ctl_xlate1_use_scos RW		xlate1 uses scos or not, high effective	1'd0
9	xlate_key_ctl_xlate0_use_scos RW		xlate0 uses scos or not, high effective	1'd0
10	xlate_key_ctl_xlate1_use_svid RW		xlate1 uses svid or not, high effective	1'd0
11	xlate_key_ctl_xlate0_use_svid RW		xlate0 uses svid or not, high effective	1'd0
12	xlate_key_ctl_xlate1_use_port RW		xlate1 uses port or not, high effective	1'd0
13	xlate_key_ctl_xlate0_use_port RW		xlate0 uses port or not, high effective	1'd0
14	xlate_key_ctl_e_vt_tcam_en RW		eVt tcam search enable, high	1'd0
15	xlate_key_ctl_e_vt_en1	RW	effective eVt1 search enable,	1'd0
16	xlate_key_ctl_e_vt_en0	R W	high effective eVt0 search enable, high effective	1'd0

5.9.5 out_cnt_ctl

Register offset: 17'b0_0000_0000_0001_0110

Register Description: Loopback processing configuration information srm_reg

Bits	Name	R/W	Description	Default
0:15	out_cnt_ctl_pkt_cnt	RW/RC	Module output statistics	16'd0

5.9.6 port_srm

Storage register description: port attributes, NumOfEntries is 43, words is 3.

Offset	Bits	Name	R/W	Description
0	0:2	queue_num	RO	Queue Number
0	3	queue_vld	R W	queueNum valid indication
0	4	rmk_pri_ptr_vld RW		Priority reverse label information template valid indication
0	5:12	rmk_pri_ptr	RW	Priority reverse label information template
0	13	def_cfi	R W	Port default cfi
0	14:16	def_cos	R W	Port default cos
0	17:28	def_ovid	R W	Port default ovid
0	29:31	def_ivid_0	R W	Port default ivid
1	0:8	def_ivid_1	R W	Port default ivid

1	9	e_vt_miss_bypass_en	R W	eVt Miss bypass Enable, high effective
1	10	e_vt_miss_trap_en	R W	eVt Miss trap enabled, high effective
1	11	e_vt_miss_drop_en	R W	eVt Miss discard enable, high effective
1	12:13	e_vt_tp	RW	evt type
1	14:25	svid	R W	svid
1	26:28	scos	R W	scos
1	29	scfi	R W	scfi
1	30:31	cvid_0	R W	cvid
2	0:9	cvid_1	R W	cvid
2	10:12	ccos	R W	ccos
2	13	ccfi	R W	ccfi
2	14:17	vlan_op_idx	R W	vlan processing behavior index
2	18	e_vt_edit_en	R W	evt modify vlan enable
2	19	out_port_mir_en	R W	Mirror enable of output port
2	20	erps_lkp_en	RW	Erps search enable
2	tearby one	vlan_filter_en	WO	Vlan filtering enable

5.9.7 vlan_srm

Storage register description: Vlan attribute, NumOfEntries is 4096, words is 5.

Offset	Bits	Name	R/W	Description
0	0	valid	RO	Effective instructions
0	1	bypass_en	R W	Bypass Enable
0	2	drop_en	R W	Discard Enable
0	3	trap_en	R W	Trap to CPU enable
0	4:6	queue_num	R W	Queue Number
0	7	queue_vld	R W	queueNum valid indication
0	8	out_fpol_vld	R W	Export hierarchical metering, effective indication of small and medium pipelines
0	9	rmk_pri_ptr_vld	RW	Priority reverse label information template valid indication
0	10:17	rmk_pri_ptr	RW	Priority reverse label information template
0	18:26	stp_id	R W	Spanning Tree ID
0	27:31	un_stag bmp_0	RW	Port untag indication
1	0:29	un_stag bmp_1	RW	Port untag indication
1	30:31	un_ctag bmp_0	RW	Port untag indication
2	0:31	un_ctag bmp_1	RW	Port untag indication
3	0	un_ctag bmp_2	RW	Port untag indication
3	1	out_vlan_mir_en	R W	Enable mirroring of the egress
3	2	out_vlan_cnt_idx_vld	RW	Egress vlan statistics enable
3	3:4	erps_id	RW	Erps
3	5:31	port bmp_0	R W	Port bmp
4	0:2	port bmp_1	R W	Port bmp
4	3:10	lag bmp	WO	Lag bmp

5.9.8 xlate_key_left_srm[4]

Storage register description: key of egress vlan xlate, NumOfEntries is 128, words is 2.

Note: Each register list contains 4 identical registers, that is, the register word value, register threshold, etc. are all the same.

Offset Bits		Name	R/W	Description
0		valid	RO	Effective instructions
0	0	svid	R W	svid
0		scfi	R W	scfi
0	1:12	scos	R W	scos
0	13	cvid	R W	cvid
0		ccfi	R W	ccfi
0	14:16	ccos_0	R W	ccos
1	17:28	ccos_1	R W	ccos
1	1:6	out_lport	R W	The internal logical port number of the output. When outIsLag is valid, it indicates LAG port, otherwise it indicates a normal port.
1	7	out_is_lag	RW	Indicates whether the output internal logic port number is a LAG port, high effective
1	8:9	e_vt_tp	WO	evt key type

5.9.9 xlate_key_right_srm[4]

Storage register description: key of egress vlan xlate, NumOfEntries is 128, words is 2.

Note: Each register list contains 4 identical registers, that is, the register word value, register threshold, etc. are all the same.

Offset Bits	Description	Name	R/W	
0		valid	RO	Effective instructions
0	0	svid	R W	svid
0		scfi	R W	scfi
0	1:12	scos	R W	scos
0	13	cvid	R W	cvid
0		ccfi	R W	ccfi
0	14:16	ccos_0	R W	ccos
1	17:28	ccos_1	R W	ccos
1	1:6	out_lport	R W	The internal logical port number of the output. When outIsLag is valid, it indicates LAG port, otherwise it indicates a normal port.
1	7	out_is_lag	RW	Indicates whether the output internal logic port number is a LAG port, high effective
1	8:9	e_vt_tp	WO	evt key type

5.9.10 xlate_left_srm[4]

Storage register description: behavior of egress vlan xlate, NumOfEntries is 128, words is 2.

Note: Each register list contains 4 identical registers, that is, the register word value, register threshold, etc. are all the same.

Offset Bits		Name	R/W	Description
0	0:2	queue_num	RO	Queue Number
0	3	queue_vld	R W	queueNum valid indication
0	4:15	svid	R W	Modified svid
0	16:18	scos	R W	Modified scos
0	19	scfi	R W	Modified scfi
0	20:31	cvid	R W	Modified cvid
1	0:2	ccos	R W	Modified ccos
1	3	ccfi	R W	Modified ccfi
1	4:7	vlan_op_idx	R W	vlan processing behavior index
1	8	bypass_en	R W	Bypass Enable
1	9	trap_en	R W	Trap to CPU enable
1	10	drop_en	WO	Discard Enable

5.9.11 xlate_right_srm[4]

Storage register description: behavior of egress vlan xlate, NumOfEntries is 128, words is 2.

Note: Each register list contains 4 identical registers, that is, the register word value, register threshold, etc. are all the same.

Offset	Bits	Description	Name	R/W	
0	0:2	queue num	RO		Queue Number
0	3	queue vld	R W		queueNum valid indication
0	4:15	svid	R W		Modified svид
0	16:18	scos	R W		Modified scos
0	19	scfi	R W		Modified scfi
0	20:31	cvid	R W		Modified cvid
1	0:2	ccos	R W		Modified ccos
1	3	ccfi	R W		Modified ccfi
1	4:7	vlan_op_idx	R W		vlan processing behavior index
1	8	bypass_en	R W		Bypass Enable
1	9	trap_en	R W		Trap to CPU enable
1	10	drop_en	WO		Discard Enable

5.9.12 xlate_tcm

Storage register description: Tcam key, NumOfEntries is 32, words is 3.

Offset	Bits	Name	R/W	Description
0	0:1	queue_num	RO	evt key type
0		queue_vld	R W	ccfi
0	2	svid	R W	ccos
0	3:5	scos	R W	cvid
0		scfi	R W	scfi
0	6:17	cvid	R W	scos
0	18	ccos	R W	svid
1	19:21 22:31 0:1	ccfi	R W	svid
1	2:7	vlan_op_idx	R W	The internal logical port number of the output. When outLag is valid, it indicates that the LAG port Otherwise, it indicates a common port.
1	8	bypass_en	RW	Indicates whether the output internal logic port number is a LAG port, high effective
1	9:11	trap_en	RW	Trap Enable
1	12	drop_en	RW	Drop Enable
1	13:14	queue_vld	R W	eVtTp Mask
1	15	svid	R W	ccfi mask
1	16:18	scos	R W	ccos mask
1	19:30	scfi	R W	cvid mask
1	31	cvid	R W	scfi mask
2	0:2	ccos	R W	scos mask
2	3:14	ccfi	R W	svid mask
2	15:20	vlan_op_idx	R W	outLport mask
2	21:22	bypass_en	R W	outLag mask
2	22:24	trap_en	R W	Trap Enable
2	25	drop_en	WO	Drop Enable

5.9.13 xlate_tcm_srm

Storage register description: Tcam behavior, NumOfEntries is 32, words is 2.

Offset Bits		Name	R/W	Description
0	0:2	queue_num	RO	Queue Number
0	3	queue_vld	R W	queueNum valid indication
0	4:15	svid	R W	Modified svид
0	16:18	scos	R W	Modified scos
0	19	scfi	R W	Modified scfi
0	20:31	cvid	R W	Modified cvid
1	0:2	ccos	R W	Modified ccos
1	3	ccfi	R W	Modified ccfi
1	4:7	vlan_op_idx	R W	vlan processing behavior index
1	8	bypass_en	R W	Bypass Enable
1	9	trap_en	R W	Trap to CPU enable
1	10	drop_en	WO	Discard Enable

5.9.14 vlan_op_srm

Storage register description: Vlan operation behavior, NumOfEntries is 16, words is 2.

Offset Bits	0 0 0	Name	R/W	Description
1 0 2 0 3		ut_ovid	RO	0:noop; 1:add
		ut_opri	R W	0:noop; 1:add
		ut_ivid	R W	0:noop; 1:add
		ut_ipri	R W	0:noop; 1:add
0	4:5	sit_ovid	R W	0:noop; 1:add 2:copy
0	6:7	sit_opri	R W	0:noop; 1:add 2:copy
0	8:9	sit_pivid	R W	0:noop; 2:replace 3:delete 0:noop; 2:replace 3:delete
0	10:11	sit_ivid	R W	0:noop; 2:replace 3:delete 0:noop; 2:replace 3:delete
0	12:13	sit_ipri	R W	0:noop; 2:replace 3:delete 0:noop; 2:replace 3:delete
0	14:15	sot_povid	R W	0:noop; 1:add 2:copy
0	16:17	sot_ovid	R W	
0	18:19	sot_opri	R W	
0	20:21	sot_ivid	R W	
0	22:23	sot_ipri	R W	0:noop; 1:add 2:copy
0	24:25	dt_povid	R W	0:noop; 1:copy 2:replace 3:delete
0	26:27	dt_ovid	R W	0:noop; 1:copy 2:replace 3:delete
0	28:29	dt_opri	R W	0:noop; 1:copy 2:replace 3:delete
0	30:31	dt_pivid	R W	0:noop; 1:copy 2:replace 3:delete
1	0:1	dt_ivid	R W	0:noop; 1:copy 2:replace 3:delete
1	2:3	dt_ipri	WO	0:noop; 1:copy 2:replace 3:delete

5.9.15 erps_srm

Storage register description: Erps status, NumOfEntries is 128, words is 2.

Offset Bits		Name	R/W	Description

0	0:29	port_bmp	RO	Port bmp
0	30:31	lag_bmp_0	R W	Lag bmp
1	0:5	lag_bmp_1	WO	Lag bmp

5.10 epf_reg

The epf_reg register block contains 5 registers and 10 storage registers.

The register list is as follows:

Register Offset	Register Name	Description
13'b0_0000_0000_0000		Global configuration information
13'b0_0000_0000_0001	loop_ctl	loopback processing configuration information srm_reg
13'b0_0000_0000_0010	in_port_ctl	Port configuration information
13'b0_0000_0000_0011	hash_ctl	hash algorithm random seed
13'b0_0000_0000_0100:13'b0_0000_0010_0001 13'b0_0000_0010_0010	port_ctl[30]	Note port configuration srm_reg
13'b0_0000_0010_0011	sta_ctl	link status configuration information
13'b0_0000_0010_0100	Link_upd_sta	LinkUpd operation status configuration
13'b0_0000_0010_0101	cnt_ctl	lag statistics count clear enable configuration
13'b0_0000_0010_0110	cnt	group member update statistics count
13'b0_0000_0010_0111 Note:	pdu_ctl	PDU global configuration srm_reg
Each register list contains 30 identical registers, that is, the register word value, register threshold, etc. are all the same.	out_cnt_ctl	loopback processing configuration information srm_reg

The storage register list is as follows:

Register Offset	Register Name	Description
13'b0_0000_0011_0000:13'b0_0000_0011_1111	lag_grp_alg_srm	LAG group hash algorithm configuration information
13'b0_0000_0100_0000:13'b0_0000_0100_0111	lag_grp_srm	LAG group configuration information
13'b0_0001_0000_0000:13'b0_0001_1111_1111	lag_srm_port	LAG member configuration information
13'b0_0010_0000_0000:13'b0_0010_0010_0010	port_srm	port configuration information
13'b0_0010_0100_0000:13'b0_0010_0110_0010	out_port_srm	configuration information
13'b0_1000_0000_0000:13'b0_1101_1111_1111	stp_srm	state table
13'b1_0000_0000_0000:13'b1_0011_1111_1111	vlan_isot_srm	port isolation table

5.10.1 ctl

Register offset: 13'b0_0000_0000_0000

Register Description: Global Configuration Information

Bits	Name	R/W	Description	Default
0	Enable_ctl_horizon_split_en	R W	Horizontal Split	1'd0
1	ctl_disable_loop_avoid	R W	Disable port loopback suppression	1'd0
2	ctl_disable_stp_chk_fail_drop	R W	ctrl_disable_stp_chk_fail_drop	1'd0
3	ctl_stp_disable_drop_en	R W	Enable drop when spanning tree is in Disable state	1'd0
4	port_ctl_link_sta_get_en	R W	Link status acquisition enable of this	1'd0

5	ctl_link_sta_init_en		The link status update state machine of the RW port remains in the initialization state.	1'd0
6	ctl_link_sta_upd_en	R W	Enable port link status update	1'd0
7	ctl_link_sta_chk_en	R W	Enable port link status detection	1'd0
8:12	ctl_port_bmp_hi	R W	Enable port bmp	5'd0

5.10.2 loop_ctl

Register offset: 13'b0_0000_0000_0001

Register Description: Loopback processing configuration information srm_reg

Bits	Name	R/W	Description	Default
0:7	loop_ctl_loop_bypass0	RW	Bypass indication of loopback packet, 0: no bypass; 1: bypass	8'd0
8:15	loop_ctl_loop_bypass1	RW	Loopback packet bypass indication, 0: no bypass; 1: bypass	8'd0

5.10.3 in_port_ctl

Register offset: 13'b0_0000_0000_0010

Register Description: Port Configuration Information

Bits	Name	R/W	Description	Default
0:29	in_port_ctl_network_port	RW	Network side port indication	30'd0

5.10.4 hash_ctl

Register offset: 13'b0_0000_0000_0011

Register Description: Hash algorithm random seed

Bits	Name	R/W	Description	Default
0:31	hash_ctl_seed	R W	hash algorithm random seed	32'd0

5.10.5 port_ctl[30]

Register offset: 13'b0_0000_0000_0100:13'b0_0000_0010_0001

Register Description: Port Configuration srm_reg

Note: Each register list contains 30 identical registers, that is, the register word value, register threshold, etc. are all the same.

Bits Name	Description	R/W		Default
0:5	port_ctl_lbn	R W	Indicates that the link status of the port is determined by the configuration.	6'd0
6	port_ctl_link_sta_cfg_en	RW		1'd0

5.10.6 sta_ctl

Register offset: 13'b0_0000_0010_0010

Register description: link status configuration information

Bits	Name	R/W	Description	Default
0:29	sta_ctl_link_sta	RW	Each bit corresponds to the link status of different ports, the specific encoding is as follows Down: 0x0: link down; 0x1: link up	30'd0

5.10.7 link_upd_sta

Register offset: 13'b0_0000_0010_0011

Register Description: LinkUpd Operation Status Configuration

Bits	Name	R/W	Description	Default
0:1	link_upd_sta_lag_upd_state RO		LinkUpd Operation status indication, 0 means INIT, 1 means GET_LINKSTA,2 means UPD_LINKSTA	2'd0

5.10.8 cnt_ctl

Register offset: 13'b0_0000_0010_0100

Register Description: Statistics count clear enable configuration

Bits	Name	R/W	Description	Default
0:1	cnt_ctl_clr_en	RW/RC	Statistics count clear enable	1'd0

5.10.9 cnt

Register offset: 13'b0_0000_0010_0101

Register Description: lag group member update statistics count

Bits	Name	R/W	Description	Default
0:7	cnt_lag_add_member_cnt RW/RC		the number of times group members are added lag	8'd0
8:15	cnt_lag_del_member_cnt RW/RC		Statistics of the number of times group members are reduced	8'd0

5.10.10 pdu_ctl

Register offset: 13'b0_0000_0010_0110

Register Description: PDU Global Configuration srm_reg

Bits	Name	R/W	Description	Default
0:23	pdu_ctl_drop_bmp RW	Drop the 12PDU message in the spanning tree DISABLE state	24'd0	

5.10.11 out_cnt_ctl

Register offset: 13'b0_0000_0010_0111

Register Description: Loopback processing configuration information srm_reg

Bits	Name	R/W	Description	Default

0:15	out_cnt_ctl_pkt_cnt RW/RC		Module output statistics	16'd0
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5.10.12 lag_grp_alg_srm

Storage register description: loopback processing configuration information srm_reg, NumOfEntries is 8, words is 2.

Offset	Bits	Name	R/W	Description
0	0:3	port_bmp	RO	The starting address of the operation result, the minimum value is 0 and the maximum value is 8
0	4	lag_bmp_0 RW		Operation result selection, the specific description is as follows: 0x0: select hash algorithm result; 0x1: Select the port's lbn
0	5:8	lag_bmp_1 RW		<p>Hash algorithm selection, detailed description is as follows:</p> <p>0x1: the lower 16 bits of the crc32 operation result;</p> <p>0x2: high 16 bits of crc32 operation result;</p> <p>0x3: crc16-bitsync operation result;</p> <p>0x4: crc16-ccitt operation result;</p> <p>0x5: the result of xor16 operation;</p> <p>0x6: The high 8 bits of the crc16-bitsync operation result and the xor8 operation result are combined;</p> <p>0x7: The high 8 bits of the crc16-bitsync operation result and the xor4 operation result are combined;</p> <p>0x8: The high 8 bits of the crc16-bitsync operation result and the xor2 operation result are combined;</p> <p>0x9: The high 8 bits of the crc16-bitsync operation result and the xor1 operation result are combined;</p> <p>Other values: crc8 calculation results.</p>
0	9	port_bmp RW		Hashkey shift enable, when it is 1, the hashKey is grouped into 16 bits Perform shift operations
0	10	lag_bmp_0 RW	lag_bmp_1	Select enable based on hashKey valid indication
0	11	RW		Hash algorithm selection based on port information,
0	12:19	port_bmp RW		Based on the hash algorithm selection of the original message L4 field, each bit corresponds to a different hashkey, the specific description is as follows: [0:1]:tcp.{srcport,dstport} [2:3]:udp.{srcport,dstport} [4:5]:icmp.{type,code} [6:7]:igmp.{type,code}
0	20:28	lag_bmp_0 RW		Based on the hash algorithm selection of the L3 field of the original message, each bit corresponds to a different hashkey, the specific description is as follows: [0:3]:ipv4.{sip,dip,proto,tos} [4:8]:ipv6.{sip,dip,proto,tos,flowLabel}
0	29:31	lag_bmp_1 RW		Based on the hash algorithm selection of the L2 field of the original message, each bit corresponds to a different hashkey, the specific description is as follows: [0:5]:{dmac,smac,ethType,stag,ctag}
1	0:1	port_bmp RW		Based on the hash algorithm selection of the L2 field of the original message, each bit corresponds to a different hashkey, the specific description is as follows: [0:5]:{dmac,smac,ethType,stag,ctag}
1	2:3	lag_bmp_0 RW		Based on the hash algorithm selection of the update message field, each bit corresponds to a different hashkey, the specific description is as follows: [0:1]:{stag,ctag}
1	4:6	lag_bmp_1 RW		The hash algorithm based on the ctag subdomain is enabled, and each bit corresponds to a different subdomain. The specific descriptions are as follows: [0]: vid; [1]: cfi; [2]: cos
1	7:9	lag_bmp_1 WO		The hash algorithm based on the stag subfield is enabled. Each bit corresponds to a different subfield. The specific descriptions are as follows: [0]: vid; [1]: cfi; [2]: cos

5.10.13 lag_grp_srm

Storage register description: LAG group member configuration information, NumOfEntries is 8, words is 1.

Bits	Name	R/W	Description
0:7	port_bmp	RO	lag group start pointer
8:12	lag_bmp_0	WO	Number of lag group members, where 1 means there is 1 member in the lag group, and so on

5.10.14 lag_srm

Storage register description: LAG member configuration information, NumOfEntries is 256, words is 1.

Bits	Name	R/W	Description
0:5	port	R W	lag member port number in the group

5.10.15 port_srm

Storage register description: port configuration information, NumOfEntries is 35, words is 1.

Bits	Name	R/W	Description
0	upd_en	RO	Member Update Enable
1	link_sta	RW	port link status, the specific encoding is as follows: 0x0: link down; 0x1: link up
2:6	chan_id	R W	Physical port number
7	is_lag	R W	lag port valid indication, high effective
8:10	lag_id	R W	lag port number
11:15	offset	WO	lag The offset address of the group member

5.10.16 out_port_srm

Storage register description: port configuration information, NumOfEntries is 35, words is 1.

Bits	Name	R/W	Description
0	bypass_en	RO	Bypass Enable
1	drop_en	R W	Discard Enable
2	trap_en	R W	Trap to CPU enable
3	port_isot_en	RW	Port isolation enable
4	vlan_filter_en	RW	vlan filter enable
5	stp_chk_en	R W	Spanning tree check enable
6	network_port	RW 6:7	Network side port indication
out_port_is_un_ctag	RW 8		The output port does not have Ctag, high effective
out_port_is_un_stag	WO		The output port does not have a stag, high validity

5.10.17 stp_srm

Storage register description: stp state table, NumOfEntries is 512, words is 3.

Offset	Bits	Name	R/W	Description
0	0:31	stp_status_0	RO	The spanning tree status of the port, where bits [1:0] correspond to port 0, and the other ports correspond to And so on. The specific coding is as follows:

				0x0: STP_DISABLE; 0x1: STP_BLOCKING; 0x2: STP_LEARNING; 0x3: STP_FORWARDING;
1	0:31	stp_status_1 RW		The spanning tree status of the port, where bits [1:0] correspond to port 0, and the other ports correspond to And so on. The specific coding is as follows: 0x0: STP_DISABLE; 0x1: STP_BLOCKING; 0x2: STP_LEARNING; 0x3: STP_FORWARDING;
2	0:21	stp_status_2 RW		The spanning tree status of the port, where bits [1:0] correspond to port 0, and the other ports correspond to And so on. The specific coding is as follows: 0x0: STP_DISABLE; 0x1: STP_BLOCKING; 0x2: STP_LEARNING; 0x3: STP_FORWARDING;

5.10.18 vlan_isot_srm

Storage register description: Port isolation table, NumOfEntries is 1024, words is 1.

Bits	Name	R/W	Description
0:29	port_bmp	R W	Port member, bit 0 represents port 0, and so on

5.11 eacl_reg

The eacl_reg register block contains 6 registers and 4 storage registers.

The register list is as follows:

Register Offset	Register Name	Description
14'b00_0000_0000_0000	loop_ctl	Loopback processing configuration information
14'b00_0000_0000_0010:14'b00_0000_0000_0011	lkp_ctl	Discard search configuration information srm_reg
14'b00_0000_0000_0100:14'b00_0000_0000_0111	ctl	Configuration Entries
14'b00_0000_0000_1000	rst_sample_ctl	Sampling statistics configuration
14'b00_0000_0001_0000:14'b00_0000_0001_0111	rst_ctl	acl search result configuration information
14'b00_0000_0011_0000	out_cnt_ctl	loopback processing configuration information srm_reg

The storage register list is as follows:

Register Offset	Register Name	Description
13'b00_0000_0100_0000: 13'b00_0000_0110_0010	port_srm	Port configuration information
13'b01_0000_0000_0000: 13'b01_1010_1111_1111	tcm	Find Key Table
13'b10_0000_0000_0000: 13'b10_0010_1111_1111	tcm_srm	Lookup behavior table
13'b10_0100_0000_0000: 13'b10_0110_1111_1111	out_flow_srm	Statistics based on OutFlow

5.11.1 loop_ctl

Register offset: 14'b00_0000_0000_0000

Register Description: Loopback processing configuration information

Bits	Name	R/W	Description	Default
0:7	loop_ctl_loop_bypass	RW	Loopback packet bypass indication, 0: no bypass; 1: bypass	8'd0

5.11.2 lkp_ctl

Register offset: 14'b00_0000_0000_0010:14'b00_0000_0000_0011

Register Description: Discard search configuration information srm_reg

Offset	Bits 0	Name	R/W	Description	Default
	0:31	lkp_ctl_drop bmp 0	RW	the search for various packet loss reasons	32'd0
1	0:31	lkp_ctl_drop bmp 1	RW	Enables the search for various packet loss reasons	32'd0

5.11.3 ctl

Register offset: 14'b00_0000_0000_0100:14'b00_0000_0000_0111

Register Description: Configuration Entries

Offset	Bits 0	Name	R/W	Description	Default
0:17	0:18:31	ctl_mac_key_rst_ctl	RW	{indexBase[7:0].keySize[1:0].tableBase[7:0]}	18'd0
		ctl_ipv4_key_rst_ctl	0	RW Same as macKeyRstCtl	14'd0
1	0:3	macKeyRstCtl_ctl_ipv4_key_rst_ctl 1		Same as	4'd0
1	4:21	RW_ctl_ipv6_key_rst_ctl	RW	Same as macKeyRstCtl	18'd0
1	22:31	ctl_mix_key_rst_ctl 0	RW	Same as macKeyRstCtl	10'd0
2	0:7	ctl_mix_key_rst_ctl 1	RW	Same as macKeyRstCtl	8'd0

5.11.4 rst_sample_ctl

Register offset: 14'b00_0000_0000_1000

Register Description: Sampling Statistics Configuration

Bits	Name	R/W	Description	Default
0:15	rst_sample_ctl_sample_cnt_en	RW/RC	Sampling statistics enable	16'd0

5.11.5 rst_ctl

Register offset: 14'b00_0000_0001_0000:14'b00_0000_0001_0111

Register Description: acl search result configuration information

Offset	Bits	Name	R/W	Description	Default
0	0:14	rst_ctl_sample_cnt0	RW	rst_ctl res0 value of sampling statistics	15'd0
0	15		RW	res	1'd0
0	16:30	rst_ctl_sample_cnt1	RW	rst_ctl res1 Sampling statistics maximum value	15'd0
0	31		RW	res	1'd0
1	0:14	rst_ctl_sample_cnt2	RW	rst_ctl res2 Sampling statistics maximum value	15'd0

1	15	rst_ctl_res2	RW	res	1'd0
	16:30	rst_ctl_sample_cnt3 RW	rst_ctl	res3 Sampling statistics maximum value	15'd0
11	31		RW	res	1'd0
	0:14	rst_ctl_sample_cnt4 RW	rst_ctl	res4 Sampling statistics maximum value	15'd0
bentity test	15		RW	res	1'd0
	16:30	rst_ctl_sample_cnt5 RW	rst_ctl	res5 Sampling statistics maximum value	15'd0
bentity test	31		RW	res	1'd0
	3	0:14	rst_ctl_sample_cnt6 RW	rst_ctl	res6 Sampling statistics maximum value
3	15		RW	res	1'd0
3	16:30	rst_ctl_sample_cnt7 RW	rst_ctl	res7 Sampling statistics maximum value	15'd0
3	31		RW	res	1'd0
4	0:14	rst_ctl_sample_cnt8 RW	rst_ctl	res8 Sampling statistics maximum value	15'd0
4	15		RW	res	1'd0
4	16:30	rst_ctl_sample_cnt9 RW	rst_ctl	res9 Sampling statistics maximum value	15'd0
4	31		RW	res	1'd0
5	0:14	rst_ctl_sample_cnt10 RW	rst_ctl	res10 Sampling statistics maximum value	15'd0
5	15		RW	res	1'd0
5	16:30	rst_ctl_sample_cnt11 RW	rst_ctl	res11 Sampling statistics maximum value	15'd0
5	31		RW	res	1'd0
6	0:14	rst_ctl_sample_cnt12 RW	rst_ctl	res12 Sampling statistics maximum value	15'd0
6	15		RW	res	1'd0
6	16:30	rst_ctl_sample_cnt13 RW	rst_ctl	res13 Sampling statistics maximum value	15'd0
6	31		RW	res	1'd0
7	0:14	rst_ctl_sample_cnt14 RW	rst_ctl	res14 Sampling statistics maximum value	15'd0
7	15		RW	res	1'd0
7	16:30	rst_ctl_sample_cnt15 RW		Sampling statistics maximum value	15'd0

5.11.6 out_cnt_ctl

Register offset: 14'b00_0000_0011_0000

Register Description: Loopback processing configuration information srm_reg

Bits	Name	R/W	DescriptionModule	Default
0:15	out_cnt_ctl_pkt_cnt	RW/RC	output statistics	16'd0

5.11.7 port_srm

Storage register description: port configuration information, NumOfEntries is 35, words is 1.

Bits	Name	R/W	Description
0	acl0_lkp_vld	RO	Acl0 search enable
1	acl1_lkp_vld	R W	Acl1 search enable
2	mac_key_use_llc	R W	Using LLC Domains
3	ipv4_force_mix_key0	R W	Acl0 lookup, IPv4 packets use mix key
4	ipv4_force_mac_key0	R W	Acl0 search, IPv4 packets use mac key
5	ipv4_force_ipv6_key0	R W	Acl0 search, IPv4 packets use IPv6 key
6	ipv6_force_mix_key0	R W	Acl0 lookup, IPv6 packets use mix key
7	ipv6_force_mac_key0	R W	Acl0 search, IPv6 packet uses mac key
8	ipv6_force_ipv4_key0	R W	Acl0 lookup, IPv6 packets use IPv4 key

9	mac_force_mix_key0	R W	Acl0 search, Ethernet packets use mix key
10	mac_force_ipv6_key0	R W	Acl0 search, Ethernet packets use ipv6 key
11	mac_force_ipv4_key0	R W	Acl0 search, Ethernet packets use ipv4 key
12	ipv4_force_mix_key1	R W	Acl1 lookup, IPv4 packets use mix key
13	ipv4_force_mac_key1	R W	Acl1 search, IPv4 packets use mac key
14	ipv4_force_ipv6_key1	R W	Acl1 search, IPv4 packet uses IPv6 key
15	ipv6_force_mix_key1	R W	Acl1 lookup, IPv6 packets use mix key
16	ipv6_force_mac_key1	R W	Acl1 search, IPv6 packet uses mac key
17	ipv6_force_ipv4_key1	R W	Acl1 lookup, IPv6 packets use IPv4 key
18	mac_force_mix_key1	R W	Acl1 search, Ethernet packets use mix key
19	mac_force_ipv6_key1	R W	Acl1 search, Ethernet packets use ipv6 key
20	mac_force_ipv4_key1	WO	Acl1 search, Ethernet packets use ipv4 key

5.11.8 tcm

Storage register description: Look up the Key table, NumOfEntries is 256, words is 11.

Offset	Bits	Name	R/W	Description
0	0:31	key_0	RO	Find key
1	0:31	key_1	R W	Find key
2	0:31	key_2	R W	Find key
3	0:31	key_3	R W	Find key
4	0:31	key_4	R W	Find key
5	0	valid	R W	Effective instructions
5	1:31	key_mask_0	R W	Find key mask
6	0:31	key_mask_1	R W	Find key mask
7	0:31	key_mask_2	R W	Find key mask
8	0:31	key_mask_3	R W	Find key mask
9	0:31	key_mask_4	R W	Find key mask
10	0	key_mask_5	R W	Find key mask
10	1	valid_mask	WO	Valid indication mask

5.11.9 tcm_srm

Storage register description: Lookup behavior table, NumOfEntries is 256, words is 3.

Offset	Bits	Name	R/W	Description
0	0:5	out_port	RO	The internal port number of the output, 0~24 are all valid.
0	6	port_vld	R W	Logical port enable
0	7:9	fwd_tp	R W	Service forwarding type, the specific encoding is as follows: 0x0: NOP; 0x1: PORT; 0x2: L2; 0x3: SCC; 0x4: DCC; other values are reserved
0	10	fwd_tp_vld	R W	Service forwarding type enable
0	11:14	sample_thrd_shift	RW	controls ipfix random stream sampling rate (1/2, 1/4, ...)
0	15	ipfix_en	RW	ipfix enable
0	16:27	out_fpol_idx	R W	hierarchical meter small and medium pipeline index
0	28	out_fpol_vld	RW	hierarchical meter small and medium pipeline effective indication
0	29:31	queue_num	R W	Queue Number

1	0	queue_vld	R W	queueNum valid indication
1	1	rmk_pri_ptr_vld	R W	Priority reverse label information template valid indication
1	2:9	rmk_pri_ptr	R W	Priority reverse label information template
1	10:17	out_flow_cnt_idx	R W	Flow Count Index
1	18	out_flow_cnt_idx_vld	RW	Flow count index enable
1	19	trap_en	RW	Redirect to CPU Enable
1	20	drop_en	R W	Discard Enable
1	twenty one	bypass_en	R W	Bypass Enable
1	twenty two	permit	R W	Permit Enable
1	twenty three	upd_stag_vld	R W	Update stag valid indication
1	24:26	upd_scos	R W	Update scos value
1	27	upd_scfi	R W	Update scfi value
1	28:31	upd_svrid_0	R W	Update svrid value
2	0:7	upd_svrid_1	R W	Update svrid value
2	8	upd_ctag_vld	R W	Update ctag valid instructions
2	9:11	upd_ccos	R W	Update ccos value
2	12	upd_ccfi	R W	Update ccfi value
2	13:24	upd_cvvid	R W	Update cvivid value
2	25:26	upd_bmp	R W	Update information enable, each bit corresponds to a different updInfo, the specific description is as follows: [0]:{updStagVId,updScos,updScfi,updSvid} [1]:{updCtagVId,updCcoss,updCcfi,updCvivid}
2	27	sample_mode	RW Sampling	Sampling mode, 1 means fixed sampling, 0 means random sampling
2	28:31	sample_profile	WO fixed	sampling template

5.11.10 out_flow_srm

Storage register description: Based on OutFlow statistics, NumOfEntries is 256 and words is 1.

Offset 0	Bits	Name	R/W	Description
	0:31	pkt_cnt_0	RO	Frame Statistics
1	0:3	pkt_cnt_1	R W	Frame Statistics
1	4:31	byte_cnt_0	R W	Byte Statistics
2	0:13	byte_cnt_1	WO	Byte Statistics

5.12 epol_reg

The epol_reg register module contains 7 registers and 4 storage registers.

The register list is as follows:

Register Offset	Register Name	Description
17'b0_0000_0000_0000_0000	loop_ctl	Loopback processing configuration information srm_reg
17'b0_0000_0000_0000_0001	ctl	ePolicing configuration information
17'b0_0000_0000_0000_0010: 17'b0_0000_0000_0000_0011	mpol_ctl	mpol enable
17'b0_0000_0000_0000_0100: 17'b0_0000_0000_0000_0101	flow_upd_ctl	Update configuration of policing srm_reg

17'b0_0000_0000_0000_0110: 17'b0_0000_0000_0000_0111	macro_upd_ctl_alm	Update configuration of policing srm_reg
17'b0_0000_0000_0000_1000		Policing alarm register
17'b0_0000_0000_0000_1001	out_cnt_ctl	Loopback processing configuration information srm_reg

The storage register list is as follows:

Register Offset	Register Name	Description
17'b0_1000_0000_0000_0000: 17'b0_1100_1111_1111_1111	flow_meter_srm	Meter parameter table needs to be split into 32 tables
17'b1_0000_0000_0000_0000: 17'b1_0001_1111_1111_1111	flow_meter_cnt_srm	token bucket counter, needs to be split into 32 tables
17'b1_0010_0000_0000_0000: 17'b1_0010_0000_1010_1110	macro_meter_srm	Meter parameter table needs to be split into 32 tables
17'b1_0010_0010_0000_0000: 17'b1_0010_0010_0100_0101	macro_meter_cnt_srm	token bucket counter, needs to be split into 32 tables

5.12.1 loop_ctl

Register Description: Loopback processing configuration information

Register offset: 17'b0_0000_0000_0000_0000

Bits	Name	R/W	Description	Default
0:7	loop_ctl_loop_bypass	RW	Loopback packet bypass indication, 0: no bypass; 1: bypass	8'd0

5.12.2 ctl

Register Description: ePolicing Configuration Information

Register offset: 17'b0_0000_0000_0000_0001

Bits	Name	R/W	Description	Default
0:5	ctl_preamble_len	RW	and interframe gap equivalent packet length	6'd0
6:9	ctl_meter_gran	RW	4'd0 control granularity	
10	ctl_flow_pkt_bytes	RW	flow mode: 0x0: byte-based policing; 0x1: packet-based policing	1'd0
11:25	ctl_macro_pkt_bytes	RW	macro mode: 0x0: byte-based policing; 0x1: packet-based policing	1'd0
ctl_pkt_en_use_pkt			Equivalent packet length when policing is based on packets	14'd0

5.12.3 mpol_ctl

Register Description: mpol enable

Register offset: 17'b0_0000_0000_0000_0010: 17'b0_0000_0000_0000_0011

Offset	Bits 0	Name	R/W	Description	Default
	0:31	mpol_ctl_m_pol_en_0	RW	mpol enable, one bit per port mpol	32'd0
1	0:2	mpol_ctl_m_pol_en_1	RW	enable, one bit per port	3'd0

5.12.4 flow_upd_ctl

Register Description: Update configuration of policing

Register offset: 17'b0_0000_0000_0000_0100: 17'b0_0000_0000_0000_0101

Offset	Bits 0	Name	R/W	Description	Default
0:14		bucket refresh cycle parameter		Description Token	15'd0
0	15:29	cycle parameter flow_upd_ctl timer1	RW	Token bucket refresh	15'd0
0	30:31	flow_upd_ctl reserved	RW	Reserved	2'd0
1	0:3	flow_upd_ctl_timer1_num	RW	Token bucket refresh cycle parameter	4'd0
1	4:7	flow_upd_ctl_timer0_num	RW	8:16 bucket refresh cycle parameter	4'd0
1		flow_upd_ctl_max_upd_idx	RW	Maximum address of the token bucket filled in each physical table	9'd0
1	17	flow_upd_ctl_upd_en	RW	Fill token bucket enable	1'd0

5.12.5 macro_upd_ctl

Register Description: Update configuration of policing

Register offset: 17'b0_0000_0000_0000_0110: 17'b0_0000_0000_0000_0111

Offset	Bits 0	Name	R/W	Description	Default
0:14		bucket refresh cycle parameter		Description Token	15'd0
0	15:29	cycle parameter macro_upd_ctl timer1	RW	Token bucket refresh	15'd0
0	30:31	macro_upd_ctl reserved	RW	Reserved	2'd0
1	macro_upd_ctl_timer1_num	RW	Token bucket	refresh cycle parameter 0:3	4'd0
1	macro_upd_ctl_timer0_num	RW	8:13	refresh cycle parameter 4:7	4'd0
1	macro_upd_ctl_max_upd_idx	RW	Maximum address of each physical table filling token bucket	6'd0	
1	14	macro_upd_ctl_upd_en	RW	Fill token bucket enable	1'd0

5.12.6 alm

Register Description: Policing alarm register

Register offset: 17'b0_0000_0000_0000_1000

Bits	Name	R/W	Description	Default
0	alm_rate_exd	RW/RC	Speeding warning	1'd0

5.12.7 out_cnt_ctl

Register Description: Loopback processing configuration information

Register offset: 17'b0_0000_0000_0000_1001

Bits	Name	R/W	Description	Default
0:15	out_cnt_ctl_pkt_cnt	RW/RC	Module output statistics	16'd0

5.12.8 flow_meter_srm

Storage register description: Meter parameter table, NumOfEntries is 4096, words is 5.

Offset Bits		Name	R/W	Description
0	0:3	excess_thrd_shift RO e Bucket size parameter: ebs = excessThrd << excessThrdShift		
0	4:19	excess_thrd	RW e Bucket size parameter: ebs = excessThrd << excessThrdShift	
0	20:31	excess_rate_max_0 RW		e The maximum token added to the bucket
1	0:5	excess_rate_max_1 RW excess_rate		e The maximum token added to the bucket
1	6:23		RW	e Bucket token fill rate
1	24:27	commit_thrd_shift RW c Bucket size parameter: cbs = commitThrd << commitThrdShift		
1	28:31	commit_thrd_0 RW c Bucket size parameter: cbs = commitThrd << commitThrdShift		
2	0:11	commit_thrd_1 RW c Bucket size parameter: cbs = commitThrd << commitThrdShift		
2	12:29	commit_rate_max RW c Bucket		c The maximum number of tokens added to bucket
2	30:31	commit_rate_0 RW c Bucket token fill rate		
3	0:15	commit_rate_1 RW 0x0: not token filling rate		
3	16:17		RW	SharingMode: 0x1: MIN_ONLY;
3	18	rfc4115_mode RW 0x1: rfc4115 mode; 0x0: dual rate three color marking mode;		
3	19	sr_tcm_mode RW 0x1: single rate three-color marking mode; 0x0: non-single rate three-color marking mode		
3	20	global_c_flag RW 0x0: color-		Global C bucket to E bucket coupling flag
3	twenty one	color_blind RW Green message		update mode; 0x1: color-blind mode.
3	twenty two	g_change_drop RW Yellow		update drop enable
3	twenty three	y_change_drop RW Red		message update drop enable
3	twenty four	r_change_drop RW Green		message update drop enable
3	25	g_change_pri RW Yellow		message update pri enable
3	26	y_change_pri RW Red		message update pri enable
3	27	r_change_pri RW New		message update pri enable
3	28:30	g_pri	RW	Value for green message (color == 2'b11)
3	31	y_pri	RW	The new pri value of the yellow message (color == 2'b01)
4	0:1	y_pri_1 New pri value	RW	for yellow message (color == 2'b01)
4	2:4	r_pri	WO	The new pri value of the red message (color == 2'b00)

5.12.9 flow_meter_cnt_srm

Storage register description: flow_meter_cnt_srm, NumOfEntries is 4096, words is 2.

Offset Bits		Name	R/W	Description
0	0:31	excess_cnt	RO	E Bucket token counter.
1	0:31	commit_cnt	WQ	C Bucket token counter.

5.12.10 macro_meter_srm

Storage register description: macro_meter_srm, NumOfEntries is 35, words is 5.

Offset Bits		Name	R/W	Description
0	0:3	excess_thrd_shift RO e Bucket size parameter: ebs = excessThrd << excessThrdShift		
0	4:19	excess_thrd	RW e Bucket size parameter: ebs = excessThrd << excessThrdShift	
0	20:31	excess_rate_max_0 RW		e The maximum token added to the bucket

1	0:5	excess_rate_max_1 RW		e The maximum token added to the bucket
1	6:23	excess_rate	RW	e Bucket token fill rate
1	24:27	commit_thrd_shift RW c Bucket size parameter: cbs = commitThrd << commitThrdShift		
1	28:31	commit_thrd_0 RW c Bucket size parameter: cbs = commitThrd << commitThrdShift		
2	0:11	commit_thrd_1 RW c Bucket size parameter: cbs = commitThrd << commitThrdShift		
2	12:29	commit_rate_max RW c Bucket		c The maximum number of tokens added to bucket
2	30:31	commit_rate_0 RW c Bucket token fill rate		
3	0:15	commit_rate_1 RW 0x0: npt token filling rate		
3	16:17	meter_sharing_mode RW		SharingMode; 0x1: MIN_ONLY; 0x2: MAX_ONLY; 0x3: MIN_MAX
3	18	rfc4115_mode RW 0x1: rfc4115 mode; 0x0: dual rate three color marking mode;		
3	19	sr_tcm_mode RW 0x1: single rate three-color marking mode; 0x0: non-single rate three-color marking mode		
3	20	global_c_flag RW 0x0: color-		Global C bucket to E bucket coupling flag
3	twenty one	color_blind	RW	RWare mode; 0x1: color-blind mode.
3	twenty two	g_change_drop Green message update drop enable		
3	twenty three	y_change_drop RW Red message update drop enable		
3	twenty four	r_change_drop RW Green		update drop enable
3	25	g_change_pri RW Yellow message update pri enable		
3	26	y_change_pri RW Red message update pri enable		
3	27	r_change_pri RW New pri value update pri enable		
3	28:30	g_pri	RW	for green message (color == 2'b11)
3	31	y_pri_0 New pri value	RW	for yellow message (color == 2'b01)
4	0:1	y_pri_1 New pri value	RW	for yellow message (color == 2'b01)
4	2:4	r_pri_0 MO	MO	The new pri value of the red message (color == 2'b00)

5.12.11 macro_meter_cnt_srm

Storage register description: macro_meter_cnt_srm, NumOfEntries is 35, words is 2.

Offset Bits		Name	R/W	Description
0	0:31	excess_cnt	RO	E Bucket token counter.
1	0:31	commit_cnt	WQ	C Bucket token counter.

5.13 edst_reg

The edst_reg register block contains 4 registers and 8 storage registers.

The register list is as follows:

Register Offset	Register Name	Description
16'b0000_0000_0000_0000	loop_ctl	Loopback processing configuration information srm_reg
16'b0000_0000_0000_0001	ctl	ePolicing configuration information
16'b0000_0000_0000_0010: 16'b0000_0000_0000_0011	pri_rmk_ctl	mpol enable
16'b0000_0000_0000_0100	out_cnt_ctl	Update configuration of policing srm_reg

The storage register list is as follows:

Register Offset	Register Name	Description

16'b0000_0000_0100_0000: 16'b0000_0000_0111_1111	trap_que_srm	Port Configuration
16'b0000_0000_1000_0000: 16'b0000_0000_1010_0010	port_que_srm	Port Configuration
16'b0010_0000_0000_0000: 16'b0010_1101_0001_1111	queue_srm	Queue-based statistics
16'b0100_0000_0000_0000: 16'b0110_1111_1111_1111	out_vlan_cnt_srm	vlan statistics
16'b1000_0000_0000_0000: 16'b1000_0011_1111_1111	pri_rmk_srm	Priority domain back-labeling table
16'b1000_0100_0000_0000: 16'b1000_0100_0111_1111	rmk_info_srm	Priority domain remapping table
16'b1000_0100_1000_0000: 16'b1000_0100_1011_1111	drop_cnt_code_srm	Export Statistics Drop Reason
16'b1001_0000_0000_0000: 16'b1001_1111_1111_1111	drop_cnt_srm	Egress drop reason statistics

5.13.1 loop_ctl

Register offset: 16'b0000_0000_0000_0000

Register Description: Loopback processing configuration information srm_reg

Bits	Name	R/W	Description	Default
0:7	loop_ctl_loop_bypass RW	Loopback packet bypass	bypass indication, 0: no bypass; 1: bypass 8'd0	
8:15	loop_ctl_loop_bypass1 RW	Loopback packet bypass	bypass indication, 0: no bypass; 1: bypass 8'd16	

5.13.2 ctl

Register offset: 16'b0000_0000_0000_0001

Register Description: ePolicing Configuration Information

Bits	Name	R/W	Description queue	Default
0	ctl_queue_cnt_en	R W	statistics enable bypass	1'd0
1	ctl_bypass_over_flow_cnt RW		statistics overflow indication	1'd0
2:4	ctl_mir_queue	RW	mir packet queue	3'd0
5	ctl_mc_que_en	R W	number mc packet specify queue	1'd0
6:8	ctl_mc_queue	R W	enable mc packet	3'd0
9	ctl_flood_que_en	R W	queue number flood packet specify	1'd0
10:12	ctl_flood_queue	R W	queue enable flood packet queue number	3'd0

5.13.3 pri_rmk_ctl

Register offset: 16'b0000_0000_0000_0010:16'b0000_0000_0000_0011

Register Description: mpol enable

Offset	Bits 0	Name	R/W	DescriptionPriority	Default
	0:31	pri_rmk_ctl_pri_remark_en_0	RW 0:2	inverse marking is	32'd0
1		pri_rmk_ctl_pri_remark_en_1	RW	enabledPriority inverse marking is enabled	3'd0

5.13.4 out_cnt_ctl

Register offset: 16'b0000_0000_0000_0100

Register Description: policing update configuration srm_reg

Bits	Name	R/W	Description	Default
0:15	out_cnt_ctl_pkt_cnt	RW/RC	DescriptionModule output statistics	16'd0

5.13.5 trap_que_srm

Storage register description: port configuration, NumOfEntries is 64, words is 1.

Bits	Name	R/W	Description
0:2	que_num	R W	Queue Number

5.13.6 port_que_srm

Storage register description: port configuration, NumOfEntries is 35, words is 1.

Bits	Name	R/W	Description
0:23	que_num	R W	Queue Number

5.13.7 queue_srm

Storage register description: Based on Queue statistics, NumOfEntries is 1120 and words is 3.

Offset 0	Bits	Name	R/W	Description
	0:31	pkt_cnt_0	RO	Frame Statistics
1	0:3	pkt_cnt_1	R W	Frame Statistics
1	4:31	byte_cnt_0	R W	Byte Statistics
2	0:13	byte_cnt_1	WO	Byte Statistics

5.13.8 out_vlan_cnt_srm

Storage register description: vlan statistics, NumOfEntries is 4096, words is 3.

Offset 0	Bits	Name	R/W	Description
	0:31	pkt_cnt_0	RO	Frame Statistics
1	0:3	pkt_cnt_1	R W	Frame Statistics
1	4:31	byte_cnt_0	R W	Byte Statistics
2	0:13	byte_cnt_1	WO	Byte Statistics

5.13.9 pri_rmk_srm

Storage register description: Priority domain back-label table, NumOfEntries is 512, words is 2.

Offset	Bits	Name	R/W	Description
0	0	rmk_cfi0	RO	Remapped cfi value
0	1:3	rmk_pri0	R W	Remapped pri value

0	4:11	rmk_tos0	R W	Remapped tos value
0	12	rmk_cfi1	R W	Remapped cfi value
0	13:15	rmk_pri1	R W	Remapped pri value
0	16:23	rmk_tos1	R W	Remapped tos value
0	^{twenty four}	rmk_cfi2	R W	Remapped cfi value
0	25:27	rmk_pri2	R W	Remapped pri value
0	28:31	rmk_tos2_0	R W	Remapped tos value
1	0:3	rmk_tos2_1 WO		Remapped tos value

5.13.10 rmk_info_srm

Storage register description: Priority domain remapping table, NumOfEntries is 128, words is 1.

Bits	Name	R/W	Description
0	only_chg_dscp0	RO	Only modify dscp
1	brg_chg_tos0	RW	L2 forwarding remap tos enable
2	ctag_rmk_use_phb_cos0 RW		remap ccos enable
3	stag_rmk_use_phb_cos0 RW index0		remap scos enable
4:9		RW	Remapped index
10	only_chg_dscp1	R W	Only modify dscp
11	brg_chg_tos1	R W	L2 forwarding remap tos enable
12	ctag_rmk_use_phb_cos1 RW		remap ccos enable
13	stag_rmk_use_phb_cos1 RW		remap scos enable
14:19	index1	WO	Remapped index

5.13.11 drop_cnt_code_srm

Storage register description: Egress statistics discard reason, NumOfEntries is 64, words is 1.

Bits	Name	R/W	Description
0:4	cnt_code	RO	The reason code for discarded packets statistics
5	use_in_port	WO	Enable statistics using ingress port

5.13.12 drop_cnt_srm

Storage register description: Egress discard reason statistics, NumOfEntries is 2048, words is 2.

Offset Bits		Name	R/W	Description
0	0:31	pkt_cnt_0	RO	Statistics of discarded packets based on reasons
1	0:3	pkt_cnt_1	R W	Statistics of discarded packets based on reasons

6 SOC

6.1 GPIO

GPIO stands for General Purpose I/O, which is mainly used to provide a set of general purpose input and output interfaces for I/O. The software is configured as input or output. If it is output, the specific output value can be set.

The mapping relationship of GPIO registers is shown in the following table:

Register Offset	Register Name	Description
0x00	IVAL	Pin Value
0x04	IEN	Pin input enable
0x08	OEN	Output enable of Pin
0x0C	OVAL	Output port value
0x10	PUE	Pull-up enable
0x14	DS	Drive Strength
0x18	PDE	Pull-down enable
0x1C	OPEN DRAIN	Open drain enable
0x20	PUP	Push-pull enable
0x24	RISE_IE	Rising edge interrupt enable
0x28	RISE_IP	Rising edge interrupt wait flag
0x2C	FALL_IE	Falling edge interrupt enable
0x30	FALL_IP	Falling edge interrupt wait flag
0x34	HIGH_IE	High level interrupt enable
0x38	HIGH_IP	High level interrupt wait flag
0x3C	LOW_IE	Low level interrupt enable
0x40	LOW_IP	Low level interrupt wait flag
0x44	IOF_EN	HW I/O function enable
0x48	IOF_SEL0	HW I/O function select 0
0x4C	IOF_SEL1	HW I/O function select 1
0x50	EVENT_RISE_EN	Rising edge event enable
0x54	EVENT_FALL_EN	Falling edge event enable
0x58	OUT_XOR	Output XOR
0x5C	SW_FILTER_EN	Active Schmitt trigger input

6.1.1 IVAL

Register offset: 0x00

Register Description: Pin Value

Bits	Name	R/W	Description	Input	Default
[0:31]	ival	RO		value	0x0

6.1.2 IEN

Register offset: 0x04

Register Description: Pin input enable

Bits	Name	R/W	Description	Default
0:31	ien	R W	Input Enable 0: Input disabled 1: Input Enable	0x0

6.1.3 OEN

Register offset: 0x08

Register Description: Pin output enable

Bits	Name	R/W	Description	Default
0:31	oen	R W	Output Enable 0: Output disabled 1: Output Enable	0x0

6.1.4 OVAL

Register offset: 0x0C

Register Description: Output Port Value

Bits	Name	R/W	Description	Default
0:31	oval	R W	Output value	0x0

6.1.5 PUE

Register offset: 0x10

Register Description: Pull-up Enable

Bits	Name	R/W	Description	Default
0:31	pue	R W	Pull mode: 0: Disable 1: Enable	0x0

6.1.6 DS

Register offset: 0x14

Register Description: Drive Strength

Bits	Name R/W	Description	Default
0:31	ds	RW When configured as an output, each pin has a SW controllable drive strength 0x0	

			0: Disable 1: Enable	
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6.1.7 PDE

Register offset: 0x18

Register Description: Pull-down Enable

Bits	Name	R/W	Description	Default
[0:31]	pde	R W	drop-down mode: 0: Disable 1: Enable	0x0

6.1.8 OPEN DRAIN

Register offset: 0x1C

Register Description: Open Drain Enable

Bits	Name	R/W	DescriptionOpen	Default
0:31	open drain	R W	drain mode: 0: Disable 1: Enable	0x0

6.1.9 PUP

Register offset: 0x20

Register Description: Push-Pull Enable

Bits	Name	R/W	DescriptionPull	Default
0:31	pull-up enable RW		-up mode: 0: Disable 1: Enable	0x0

6.1.10 RISE_IE

Register offset: 0x24

Register Description: Rising edge interrupt enable

Bits	Name	R/W	DescriptionRising	Default
0:31	rise ie	R W	edge interrupt mode: 0: Disable 1: Enable	0x0

6.1.11 RISE_IP

Register offset: 0x28

Register Description: Rising edge interrupt wait flag

Bits	Name	R/W	Description	Default
0:31	rise ip	R W	Rising edge interrupt pending: 0: Rising edge interrupt driven by GPIO rising edge 1: Rising edge interrupt driven by software	0x0

6.1.12 FALL_IE

Register offset: 0x2C

Register Description: Falling Edge Interrupt Enable

Bits	Name	R/W	Description	Default
0:31	fall ie	R W	Falling edge interrupt enable: 0: Disable 1: Enable	0x0

6.1.13 FALL_IP

Register offset: 0x30

Register Description: Falling edge interrupt wait flag

Bits	Name	R/W	Description	Default
0:31	fall ip	R W	Falling edge interrupt wait flag: 0: Falling edge interrupt driven by the falling edge of GPIO 1: Falling edge interrupt driven by software	0x0

6.1.14 HIGH_IE

Register offset: 0x34

Register Description: High level interrupt enable

Bits	Name	R/W	Description	Default
0:31	high ie	R W	High level interrupt enable: 0: Disable 1: Enable	0x0

6.1.15 HIGH_IP

Register offset: 0x38

Register Description: High level interrupt wait flag

Bits	Name	R/W	DescriptionHigh	Default
0:31	high ip	R W	level interrupt waiting flag: 0: Falling edge interrupt driven by the falling edge of GPIO 1: Falling edge interrupt driven by software	0x0

6.1.16 LOW_IP

Register offset: 0x40

Register Description: Low level interrupt wait flag

Bits	Name	R/W	DescriptionLow	Default
0:31	low ip	R W	level interrupt wait flag: 0: Low level interrupt driven by the falling edge of GPIO 1: Low level interrupt driven by software	0x0

6.1.17 IOF_EN

Register offset: 0x44

Register Description: HW I/O function enable

Bits	Name	R/W	Description	Default
[0:31]	iof en	R W	HW I/O function enable	0x0

6.1.18 IOF_SEL0

Register offset: 0x48

Register Description: HW I/O Function Selection 0

Bits	Name	R/W	DescriptionEach	Default
0:31	iof sel0	R W	GPIO pin can implement up to 4 HW driver functions (Based on {iof_sel1,iof_sel0}) 00: Select HW IOF0 01: Select HW IOF1 10/11: Reversal	0x0

6.1.19 LOW_IE

Register offset: 0x3C

Register Description: Low level interrupt enable

Bits	Name	R/W	DescriptionLow	Default
0:31	low ie	R W	level interrupt enable: 0: Disable 1: Enable	0x0

6.1.20 IOF_SEL1

Register offset: 0x4C

Register Description: HW I/O Function Selection 1

Bits	Name	R/W	DescriptionEach	Default
0:31	iof sel1	R W	GPIO pin can implement up to 4 HW driver functions (Based on {iof_sel1,iof_sel0}) 00: Select HW IOF0 01: Select HW IOF1 10/11: Reversal	0x0

6.1.21 EVENT_RISE_EN

Register offset: 0x50

Register Description: Rising Edge Event Enable

Bits	Name	R/W	Description	Default
0:31	event rise en	RW	Rising edge event enable: 0: Disable 1: Enable	0x0

6.1.22 EVENT_FALL_EN

Register offset: 0x54

Register Description: Falling Edge Event Enable

Bits	Name	R/W	Description	Default
0:31	event fell in	RW	Falling edge event enable: 0: Disable 1: Enable	0x0

6.1.23 OUT_XOR

Register offset: 0x58

Register Description:

Bits	Name	R/W	DescriptionOutput	Default
0:31	out xor	R W	inversion enable: 0: Disable 1: Enable	0x0

6.1.24 SW_FILTER_EN

Register offset: 0x5C

Register Description:

Bits	Name	R/W	Description	Default
0:31	sw filter en	R W	Effective Schmitt trigger input in PAD interface: 0: Disable 1: Enable	0x0

6.2 QSPI

QSPI is Quad-SPI, which supports sending and receiving FIFO buffers, and also supports software programmable thresholds (Watermark) to generate an interrupt. Supports configuring the polarity and phase of the SPI clock signal SCK through registers.

QSPI registers are memory address mapped registers. SPI is mounted on the private device bus of SoC as a slave module. The list of configurable registers of SPI and their offset addresses are shown in the following table:

Register Offset	Register Name	Description
0x000	SPI_SCKDIV	SCK clock frequency division factor register (xip/normal mode)
0x004	SPI_SCKMODE	SCK mode configuration register (xip/normal mode)
0x00C	SPI_FORCE	SPI unused interface forced output 1 enabled
0x010	SPI_CSID	CS strobe identification (ID) register (xip/normal mode)
0x014	SPI_CSDEF	CS Idle Value Register
0x018	SPI_CSMODE	CS Mode Register
0x01C	SPI_VISION	SPI Version Register Version 1.0
0x028	SPI_DELAY0	XIP transmission delay control register 0 (xip/normal mode)
0x02C	SPI_DELAY1	XIP transmission delay control register 1 (xip/normal mode)
0x040	SPI_FMT	Transfer parameter configuration register (xip/normal mode)
0x07C	SPI_STATUS	Transfer Status Register (Normal Mode)
0x048	SPI_TXDATA	Send data register (normal mode)
0x04C	SPI_RXDATA	Receive data register (normal mode)
0x060	SPI_FCTRL	XIP Mode Control Register (xip)
0x064	SPI_FFMT	XIP transfer parameter control register (xip)
0x078	SPI_FFMT1	XIP transfer parameter control register 1 (xip)
0x080	SPI_RXEDGE	SPI receive data sampling edge control register
0x050	SPI_TXMARK	SPI transmit fifo water level register
0x054	SPI_RXMARK	SPI receive fifo water level register
0x070	SPI_IE	SPI Interrupt Enable Register
0x074	SPI_IP	SPI interrupt pending register

6.2.1 SPI_SCKDIV

Register offset: 0x000

Register Description: Used to set the SCK clock frequency of SPI

Bits	Name	R/W	Description is used	Default
0:11	div	R W	to configure the frequency division coefficient of the SCK signal.	0x3

6.2.2 SPI_SCKMODE

Register offset: 0x004

Register Description: Used to set the SCK clock frequency of SPI

Bits	Name	R/W	Description	Default
0	pha	R W	Used to configure	0x0
1	pol	R W	CPHA. Used to configure CPOL.	0x0

6.2.3 SPI_CSID

Register offset: 0x00C

Register Description: The SPI interface can have multiple enable signals. Multiple enable signals are used to connect multiple SPI slave devices on the same bus.

It is possible, but only one SPI slave device can be enabled at a time. The SPI_CSID register is used to select the enable signal for the SPI.

Bits	Name	R/W	Description	Default
0:1	csid	R W	<p>The value of this field is used to select the index of the enable signal.</p> <p>00: No selection 01: Select SS0 10: Choose SS1 11: Choose SS2</p>	0x0

6.2.4 SPI_CSDEF

Register offset: 0x014

Register Description: CS Idle Register.

Bits	Name	R/W	Description	Default
0	cs0def	R W	value of this field indicates the idle value of the CS0 enable	0x1
1	cs1def	R W	signal. The value of this field indicates the idle value of the CS1	0x1
2	cs2def	R W	enable signal. The value of this field indicates the idle value of the	0x1
3	cs3def	R W	CS2 enable signal. The value of this field indicates the idle value of the CS3 enable signal.	0x1

6.2.5 SPI_CSMODE

Register offset: 0x018

Register Description: CS Mode Register.

Bits	Name	R/W	Description	Default
0:1	mode	indicating	<p>RW Assume that the value of this field is 0, indicating that the configuration enable signal is in AUTO mode.</p> <p>Assume that the value of this field is 2, indicating that the configuration enable signal is in HOLD mode.</p> <p>Assume that the value of this field is 3, indicating that the configuration enable signal is in OFF mode.</p>	0x0

6.2.6 SPI_DELAY0

Register offset: 0x028

Register Description: Used to configure the delay period parameters.

Bits	Name	R/W	Description	Default
0:7	cssck	R W	The value of this field specifies the first How many cycles before the SCK clock edge will the The enable signal (SS) is set to a valid value.	0x0
16:23	sckcs	R W	The value of this field specifies the last How many cycles will the SCK clock continue to Keep the enable signal (SS) at a valid value.	0x0

6.2.7 SPI_DELAY1

Register offset: 0x02C

Register Description: Used to configure several delay cycle parameters.

Bits	Name	R/W	Description	Default
0:7	intercs	R W	this field specifies whether the enable signal can be restored from the "valid value to the idle value" (de-assertion)" to "reset to a valid value" The minimum number of idle cycles that should last between "assertions" (Minimum CS inactive time).	0x0

6.2.8 SPI_FMT

Register offset: 0x040

Register Description: In FIFO transmit/receive mode, data can be sent through the SPI_TXDATA and SPI_RXDATA registers.

When the SPI_TXDATA and SPI_RXDATA are used to send and receive data, the SPI_FMT register

Can be used to configure several transmission parameters.

Bits	Name	R/W	Description	Default
0:1	proto	RW	the value of this field is 2, the transmission protocol is configured as Quad-SPI. There are four data lines DQ0, DQ1, DQ2, and DQ3 working. If the value of this field is 1, the transmission protocol is configured as Dual-SPI. There are two data lines DQ0 and DQ1 working. If the value of this field is 0, the transmission protocol is configured as Single-SPI. There are two data lines DQ0 (working as MOSI) and DQ1 (working as MISO).	0x0
2	endian	RW	If the value of this field is 1, the data is sent low bit first (LSB first). If the value of this field is 0, the data is sent high first (MSB first). If the	0x0
3	dir	R W	value of this field is 1, it means TX, that is, sending. In this mode, the RX-FIFO No data will be received. If the value of this field is 0, it means RX, that is, receiving. In this mode, the RX-FIFO Will receive data: If the proto domain is configured for Dual or Quad-SPI protocol, all DQ The data lines are all in the input state to accept data. If the proto domain is configured with the Single-SPI protocol, then according to the common SPI protocol, DQ0 (MOSI) will still be output, and DQ1 (MISO) will be input. Receive data.	0x0

16:19	len	R W	The value of this field specifies the number of bits (length value) to send a frame of data. The valid length value The range is 0 to 8.	0x1
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6.2.9 SPI_STATUS

Register offset: 0x07C

Register Description: Used to indicate the current transmission status.

Bits	Name	R/W	Description: The value of this field is used to indicate the current transmission status.	Default
0	tip	RO		0x0

6.2.10 SPI_TXDATA

Register offset: 0x048

Register Description: In FIFO transmit/receive mode, data can be sent through the SPI_TXDATA register.

Bits	Name	R/W	Description /	Default
0		txdata		0x0
31	full	RO	This bit is a read-only field used to indicate whether the SPI TX-FIFO is full. If the full bit is 1, it means that the current SPI-TX-FIFO is full and the txdata field is written. The data in the txdata field will be ignored; otherwise, if it is not full, the data written into the txdata field will be received.	0x0

6.2.11 SPI_RXDATA

Register offset: 0x04C

Register Description: In FIFO transmit/receive mode, data can be received through the SPI_RXDATA register.

Bits	Name	R/W	Description If	Default
0:7	rxdata	RO	the empty field is 0, the data in the txdata field read by the software is valid data If the empty field is 1, the data read from the txdata field by the software is invalid data. This	0x0
31	empty	RO	bit is a read-only field and is used to indicate whether the SPI RX-FIFO status is full. If the full bit is 1, it means that the current SPI-TX-FIFO is full and is written to the rxdata domain. The data in the rxdata field will be ignored; otherwise, it is not full and the data written to the rxdata field will be received.	0x0

6.2.12 SPI_FCTRL

Register offset: 0x060

Register Description: Enable Flash Xip mode of QSPI0 through SPI_FCTRL register.

Bits	Name	R/W	Description If	Default
0	flash_en	R W	this field is 1, it means that the Flash XiP mode of QSPI0 is enabled. If this field is 0, it means that the Flash XiP mode of QSPI0 is not enabled. QSPI0 is in normal FIFO transmit/receive mode.	0x0
1	flash_wen	RW	If this field is 1, it enables the Flash XiP write mode of QSPI0. If this field is 0, it means that the Flash XiP write mode of QSPI0 is not enabled. The Flash XiP mode of QSPI0 can only use the read mode.	0x0

3	flash_burst_en RW		If this field is 1, it indicates that the burst mode of Flash XiP of QSPI0 is enabled. If this field is 0, it means that the burst mode of Flash XiP of QSPI0 is not enabled. Only Flash XiP single mode is supported.	Mode. 0x1
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6.2.13 SPI_FFMT

Register offset: 0x064

Register Description: When QSPI0 is in Flash Xip mode, the entire QSPI0 (external Flash) is mapped as a read-only address.

Reading data or fetching instructions directly from this interval will automatically trigger QSPI0 to read through the SPI protocol

External Flash. The specific SPI protocol behavior of QSPI0 reading external Flash through the SPI interface is controlled by the SPI_FFMT register.

Bits	Name R/W	cmd_en	Description	Default
0	RW		Whether to enable sending commands.	0x1
1:3	addr_len RW		Address bits consist of how many bytes (0 to 4). The default is 3 bytes (i.e. 24 bits).	0x3
4:7	pad_cnt RW		How many Dummy read cycles are sent.	0x0
8:9	cmd_proto RW		The SPI protocol used in the command sending stage, see SPI_FMT. <small>Definition of the proto field of the register.</small>	0x0
10:11	addr_proto RW		The SPI protocol used in the address sending phase is described in the SPI_FMT register. <small>The definition of the proto field of the device.</small>	0x0
12:13	data_proto RW		The SPI protocol used in the data transmission phase, see the SPI_FMT register <small>The definition of the proto domain.</small>	0x0
14	data_endian RW		If the value of this field is 1, the data is sent low bit first (LSB first). If the value of this field is 0, the data is sent high bit first (MSB first).	0x0
16:23	cmd_code RW		Specific command value. The default value is 0x3. It is the commonly used Winbond/Numonx Flash serial READ command (0x03).	0x3
24:31	pad_code RW		The first 8 bits sent in Dummay Cycles.	0x0

6.2.14 SPI_FFMT1

Register offset: 0x078

Register Description: XIP transfer parameter control register 1 (xip).

Bits	Name	R/W	Description	Default
0:7	wcmd_code	R W	Flash XiP mode specific write command value. How many	0x2
8:11	wpad_cnt	R W	Dummy write cycles are sent?	0x0

6.2.15 SPI_RXEDGE

Register offset: 0x080

Register Description: SPI receive data sampling edge control register.

Bits	Name	R/W	Description	Rx Receive edge control	Default
0	rxedge	register	0 means receiving at the rising edge of SCK Data, 1 means receiving data at the falling edge of SCK.		0x0

6.2.16 SPI_TXMARK

Register offset: 0x050

Register Description: SPI transmit FIFO water level register.

Bits	Name	R/W	Description	Default
0:2	txmark	R W	value of this field indicates the threshold for TX-FIFO to generate an interrupt (Watermark).	0x0

6.2.17 SPI_RXMARK

Register offset: 0x054

Register Description: SPI receive FIFO water level register.

Bits	Name	R/W	Description	Default
0:2	rxmark	R W	value of this field indicates the threshold for RX-FIFO to generate an interrupt (Watermark).	0x0

6.2.18 SPI_IE

Register offset: 0x070

Register Description: SPI interrupt enable register.

Bits	Name	R/W	Description If	Default
0	txie	R W	the txie field is 1, it means enabling the SPI transmit interrupt. If the txie field is 0, it means that the SPI transmit interrupt is disabled.	0x0
1	rxie	R W	If the rxie field is 1, it means that the SPI receive interrupt is enabled. If the rxie field is 0, it means that the SPI receive interrupt is not enabled.	0x0

6.2.19 SPI_IP

Register offset: 0x070

Register Description: SPI interrupt enable register.

Bits	Name	R/W	Description If this	Default
0	txip	R W	field is 1, it indicates that a transmit interrupt is currently being generated. If this field is 0, it means that no transmit interrupt is currently generated.	0x0
1	rxip	R W	If this field is 1, it means that a receive interrupt is currently generated. If this field is 0, it means that no receive interrupt has occurred.	0x0

6.3 UART

UART stands for Universal Asynchronous Receiver-Transmitter, which provides a

A flexible and convenient serial data exchange interface, data frames can be transmitted in an asynchronous manner. UART provides a programmable baud rate. The default baud rate is 38400bps, which can generate the specific frequency required for UART transmission and reception. There are two in this SoC. Independent UART, both UARTs reuse the top-level GPIO pins to communicate with the outside world.

The UART register mapping relationship is shown in the following table:

Register Offset	Register Name	Description
0x00	UART_TXDATA	Send data register
0x04	UART_RXDATA	Receive data register
0x08	UART_TXCTRL	Transmit Control Register
0x0c	UART_RXCTRL	Receive Control Register
0x10	UART_IE	UART Interrupt Enable Register
0x14	UART_IP	UART interrupt wait register
0x18	UART_DIV	Baud Rate Divisor Register
0x1c	UART_STATUS	RX/TX busy status register
0x20	UART_SETUP	UART setup register
0x24	UART_ERROR	UART Receive Error Status Register
0x28	UART_IRQ_EN	UART Interrupt Request Enable Register

6.3.1 UART_TXDATA

Register offset: 0x00

Register Description: Transmit data register. If the FIFO can receive new data, writing to the txdata register will

The characters contained in the register are written into the transmit FIFO in sequence; the full flag and data field are returned from the txdata register; the full flag indicates that the transmit Whether FIFO can receive new data. When the full flag is valid, the data written will be ignored.

Bits	Name	R/W	Description	Default
0:8	txdata	R W	data is	0x0
9:30	/	/		/
31	full	R W	reserved. Transmit FIFO is full.	0x0

6.3.2 UART_RXDATA

Register offset: 0x04

Register Description: Receive data register. Reading the rxdata register returns the value of the data field. The empty flag indicates whether the receive FIFO is empty.

Empty, if valid, there is no valid data in the data field.

Bits	Name	R/W	Description	Default
0:8	rxdata	R W	data	0x0
9:30	/	/		/
31	full	R W	Reserved Receive data Empty	0x0

6.3.3 UART_TXCTRL

Register offset: 0x08

Register Description: Transmit control register. Reading and writing the txctrl register controls the operation of the transmit channel. The txen bit controls whether the tx channel is in

When cleared, disables transmission of data in the tx FIFO and drives the txd pin high.

Bits	Name	R/W	DescriptionSend	Default
0	txen	R W	enable stop	0x0
1:2	nstop	R W	bit configuration: 00: 1 bit 01: 2bit 10: 0.5bit 11: 1.5bit	0x0
3:15	/	/	Retain	/
16:19	txcnt	R W	Send Watermark Level	0x0
20:31	/	/	Retain	/

6.3.4 UART_RXCTRL

Register offset: 0x0C

Register Description: Receive control register. Reading and writing the rxctrl register controls the operation of the receive channel. The rxen bit controls the rx channel. When cleared, the state of the rxd pin is ignored and data is not written to the rx FIFO.

Bits	Name	R/W	Description Send	Default
0	txen	R W	Enable	0x0
1:15	/	/		/
16:19	rxcnt	R W	Reserve Receive	0x0
20:31	/	/	Watermark Level Reserve	/

6.3.5 UART_IE

Register offset: 0x10

Register Description: UART interrupt enable register.

Bits	Name	R/W	Description Send	Default
0	txie	R W	watermark interrupt	0x0
1	rxie	R W	enableReceive watermark	0x0
2:31	/	/	interrupt enableReserve	/

6.3.6 UART_IP

Register offset: 0x14

Register Description: UART interrupt wait register.

Bits	Name	R/W	Description Send	Default
0	txip	R W	watermark interrupt	0x0
1	rxip /	R W	waitingReceive watermark	0x0
2:31		/	interrupt waiting reserved	/

6.3.7 UART_DIV

Register offset: 0x18

Register Description: Baud rate divisor register. The baud rate divisor used to generate the baud rate in the tx and rx channels is specified by reading and writing the baud div register. Divisor. The input clock and baud rate can be converted using the following formula: fbaud = fclk_in/(div+1).

Bits	Name	R/W	DescriptionBaud	Default
0:15	baud div	R W	rate divisor	0x21e
16:31	/	/	reserved	/

6.3.8 UART_STATUS

Register offset: 0x1C

Register Description: Uart status register.

Bits	Name	R/W	Description	Default
0	rx_busy	R W		0x0
1	tx_busy /	R W		0x0
2:31		/	Receiving dataSending dataReserved	

6.3.9 UART_SETUP

Register offset: 0x20

Register Description: Uart setup register.

Bits	Name	R/W	DescriptionParity	Default
0	parity_en	R W	bit generation and checking configuration fields: 0: Disable 1: Enable	0x0
1	parity_sel	R W	Parity mode selection: 0: Even parity 1: Odd parity	0x0
2	/	/		/
3	clean_fifo	R W	Reserved to clear rx FIFO, set to 0/1 to reset FIFO: 0: Stop clearing the RX FIFO. 1: Clear RX FIFO.	0x0
4:6	bit_length	R W	Character length field: 0x0: 5 bits 0x1: 6 bits 0x2: 7 bits 0x3: 8 bits 0x4: 9 bits	0x0
7:31	/	/	reserve	/

6.3.10 UART_ERROR

Register offset: 0x24

Register Description: Uart receive error status register. The error register is a read-only register, and the error status is set by hardware. Software can The rx fifo overflow and parity check results are obtained by sending a read command. If an overflow or parity check error occurs, the software can Send a read command to clear the error status.

Bits	Name	R/W	Description	Default
0	rx_error_overflow	RO	RX FIFO overflow error flag: 0: True 1: RX FIFO overflow error occurred	0x0
1	rx_error_parity	RO	RX parity error flag: 0: Yes 1: RX parity error occurred	0x0
2:31	/	/	reserve	/

6.3.11 UART_IRQ_EN

Register offset: 0x28

Register Description: Uart interrupt request enable register.

Bits	Name	R/W	Description	Default
0	rx_error_overflow	R W	RX FIFO overflow error flag: 0: True 1: RX FIFO overflow error occurred	0x0
1	rx_error_parity	R W	RX parity error flag: 0: Yes 1: RX parity error occurred	0x0
2:31	/	/	reserve	/

6.4 DMA

A DMA controller is a hardware method for transferring data directly between peripherals/memory and memory without CPU intervention.

Can offload large amounts of data blocks.

The register mapping (offset) relationship of the DMA controller part is shown in the following table:

Register Offset	Register Name	Description
0x008+0x14	DMA_CFG_MSRCADDR	Source data base address
0x00C+0x14	DMA_CFG_MDSTADDR	Destination base address
0x010+0x14	DMA_CFG_MCTRL	Control Register
0x014+0x14	DMA_CFG_RPT	Transmission repetition times
0x018+0x14	DMA_CFG_MSIZE	Transfer size
0x100+0xC	DMA_CHX_IRQ_EN	M2M interrupt enable
0x104+0xC	DMA_CHX_IRQ_STAT	M2M Interrupt Status
0x108+0xC	DMA_CHX_IRQ_CLR	M2M interrupt clear

6.4.1 DMA_CFG_MSRCADDR

Register offset: 0x008+0x14

Register Description: Source address base register.

Bits	Name	R/W	Description	Default
0:31	src_base	R W	The base address of the source data block	0x0

6.4.2 DMA_CFG_MDSTADDR

Register offset: 0x00C+0x14

Register Description: Destination data base address register.

Bits	Name	R/W	Description	Default
0:31	dst_base	R W	The base address of the destination data block	0x0

6.4.3 DMA_CFG_MCTRL

Register offset: 0x010+0x14

Register Description: Control register.

Bits	Name	R/W	Description	Default
0	trans_en	R W	DMA transfer enable, asserting this bit will start mem2mem DMA transfer, it can be cleared by SW and is After the burst ends, the transmission stops. When a transmission error occurs, the hardware can also clear it. In this case, the current transfer will be aborted. This bit can only be set if all other configuration bits are configured correctly.	0x0
1:2	trans_type	R W	mem2mem is fixed to 2'b00 to retain	0x0
3:5	trans_per_sel	R W	the transfer mode selection 2'b00: single mode transmission; 2'b01: Continuous mode transmission, in this mode, complete the current transfer, a new transfer will be automatically started with the same transfer configuration; 2'b10: Transmission repeat mode, using the same transmission configuration, The transmission will be repeated N times continuously (defined in the "Transmission Repeat Number Register"). 2'b11: Reserved	0x0
8:9	priority	R W		0x0
12	mdna	R W	Reserves the next address generation algorithm for transferring data to the target memory 1'b0: Add address mode 1'b1: Fixed address If fixed addresses are configured, force the start target address to be aligned	0x0
13	msna	R W	Next address generation algorithm for fetching data from source memory 1'b0: Add address mode 1'b1: Fixed address If a fixed address is configured, the starting source address is forced to be aligned	0x0
16:18	mdwidth	R W	The transfer width used to transfer data to the destination:	0x0

			3'b000: 8 bits 3'b001: 16 bits 3'b010: 32 bits 3'b011: 64 bits 3'b100: 128 bits Others: Reserved	
21:23	mswidth	R W	The transfer width obtained from the source 3'b000: 8 bits 3'b001: 16 bits 3'b010: 32 bits 3'b011: 64 bits 3'b100: 128 bits Others: Reserved	0x0
24:27	mdburst	R W	The number of transfers in a burst used to transfer data to the destination memory 4'b0000: 1 transfer 4'b0001: 2 transfers 4'b0010: 3 transfers 4'b0011: 4 transfers 4'b0100: 5 transfers 4'b0101: 6 transfers 4'b0110: 7 transmissions ... 4'b1111: 16 transfers	0x0
28:31	msburst	R W	The number of transfers in a burst used to transfer data to the destination memory 4'b0000: 1 transfer 4'b0001: 2 transfers 4'b0010: 3 transfers 4'b0011: 4 transfers 4'b0100: 5 transfers 4'b0101: 6 transfers 4'b0110: 7 transfers ... 4'b1111: 16 transfers	0x0

6.4.4 DMA_CFG_RPT

Register offset: 0x014+0x14

Register Description: Transmission repetition count register.

Bits	Name	R/W	DescriptionWhen	Default
0:11	trans_rpt	R W	the trans_mode of the DMA_CFG_MCTRL register is configured When set to b10 transmission repeat mode, this field defines the number of repeat cycles. number.	0x0

6.4.5 DMA_CFG_MSIZE

Register offset: 0x018+0x14

Register Description: Transfer size register.

Bits	Name	R/W	DescriptionThe	Default
0:19	tsize	R W	<p>transfer size of a DMA transfer.</p> <p>Do not allow transmission to start with 0; doing so may lead to unexpected results.</p> <p>During a DMA transfer, these bits indicate the remaining words to be transferred.</p> <p>If the DMA_CFG_MCTRL register trans_mode is configured as b01 or b10 (i.e. continuous or repetitive mode), it will automatically reload when the current transfer is completed to the original value for a new transfer; DMA transfer errors may freeze registers to the values of the last successful transfer, but it restarts and automatically records the correct remaining number for the next new transfer</p> <p>According to the number.</p>	0x0

6.4.6 DMA_CHX_IRQ_EN

Register offset: 0x100+0xC

Register Description: Interrupt enable register.

Bits	Name	R/W	DescriptionFull	Default
0	ftrans_irq_en RW		output interrupt enable. Half	0x0
1	htrans_irq_en RW		transfer interrupt enable.	0x0
2	rsp_err_irq_en RW		DMA access error interrupt	0x0
3:31	/	/	enable. Reserved	/

6.4.7 DMA_CHX_IRQ_STAT

Register offset: 0x104+0xC

Register Description: Interrupt Status Register.

Bits	Name	R/W	Description	Default
0	ftrans_irq_stat	RO	Interrupt status flag	0x0
1	htrans_irq_stat RO		for full transfer. Interrupt status	0x0
2	rsp_err_irq_stat RO		flag for half transfer. Interrupt status flag for	0x0
3:31	/	/	DMA access error. Reserved.	/

6.4.8 DMA_CHX_IRQ_CLR

Register offset: 0x108+0xC

Register Description: Interrupt clear register.

Bits	Name	R/W	Description	Default
0	ftrans_irq_clr WO		Interrupt status flag	0x0
1	htrans_irq_clr WO		for full transfer. Interrupt status	0x0
2	rsp_err_irq_clr WO		flag for half transfer. Interrupt status flag for	0x0
3:31	/	/	DMA access error. Reserved.	/

6.5 I2C

The I2C register mapping relationship is shown in the following table:

Register Offset 0x00	Register Name	Description
	I2C_PRERlo	Prescaler register lower 8 bytes
0x01	I2C_PRERhi	Prescaler register high 8 bytes
0x02	I2C_CTR	Control Register
0x03	I2C_TXR	Send Register
0x05	I2C_RXR	Receive Register
0x06	I2C_CR	Command Register
0x04	I2C_SR	Status Register
0x07	I2C_TRISE	scl delay register
0x08	I2C_FLTER	Filter register

6.5.1 I2C_PRERlo

Register offset: 0x00

Register Description: Prescaler SCL clock line. Due to the structure of the I2C interface, the core uses 4 * SCL clock internally.

The register must be set to 4 * SCL bit rate. Change the value of the prescaler register only when the 'EN' bit is clear.

Bits	Name	R/W	Description	Default
0:7	prerlo	R W	Prescaler register low byte.	0xffff

6.5.2 I2C_PRERhi

Register offset: 0x01

Register Description: Prescaler SCL clock line. Due to the structure of the I2C interface, the core uses 4 * SCL clock internally.

The register must be set to 4 * SCL bit rate. Change the value of the prescaler register only when the 'EN' bit is clear.

Bits	Name	R/W	Description	Default
0:7	prerhi	R W	Prescaler register high byte.	0xffff

6.5.3 I2C_CTR

Register offset: 0x02

Register Description: Control Register. The core will respond to new commands only when the 'EN' bit is set to 1. Pending commands have completed.

The 'EN' bit is cleared only when no transmission is in progress (ie after a STOP command) or when the STO bit of the Command Register is set.

The core can suspend the I2C bus when a transfer is paused.

Bits	Name /	R/W	Description	Default
0:5		R W	reserved.	/
6	ctr_en	R W	I2C core enable bits: 1: Enable 0: Disable	0x00
7	ctr_in	R W	I2C core interrupt enable bit: 1: Enable 0: Disable	0x00

6.5.4 I2C_TXR

Register offset: 0x03

Register Description: Send register.

Bits	Name	R/W	Description	Default
0	txr	WO	next byte to be transmitted	0x00
1:7	txr_data	WO	during data transmission, this bit represents the LSB of the data. If it is a slave address transmission, this bit represents the RW bit. 1: Read slave 0: write slave	0x00

6.5.5 I2C_RXR

Register offset: 0x05

Register Description: Receive register.

Bits	Name	R/W	Description	Default
0:7	rxr	RO	The last byte received	0x00

6.5.6 I2C_CR

Register offset: 0x06

Register Description: Command register.

Bits	Name	R/W	Description	Default
0	lack	R W	response, when set, clear the pending interrupt.	0x00
1:2	/	R W	Reserved	/
3	ack	R W	The receiver sends ACK (ACK = '0') or NACK (ACK = '1')	0x00
4	wr	R W	Write to slave	0x00
5	rd	R W	Read from	0x00
6	sto	R W	slave Generate stop	0x00
7	sta	R W	condition Generate (repeated) start condition	0x00

6.5.7 I2C_SR

Register offset: 0x04

Register Description: Status Register.

Bits	Name	R/W	Description	Default
0	if	RO	Description The Interrupt flag . When an interrupt is pending, this position is 1. Setting the IEN bit to 1 will cause a processor interrupt request. The interrupt flag is set when: Completes a byte transfer.	0x00
1	tip	RO	Transfer in progress.	

			1: Transmitting 0: Transfer completed	
2:5	/	RO		/
6	busy	RO	Reserved to write slave I2C bus busy signal. "1" after detecting START signal After the STOP signal is detected, it is "0"	0x00
7	rxack	RO	Receive a response from the slave. This flag indicates the response of the addressed slave. 1: No response received 0: Received a response	0x00

6.5.8 I2C_TRISE

Register offset: 0x07

Register Description: Delay register, used to shield the frequency division error caused by slave waiting time.

Bits	Name	R/W	Description	Used to shield the frequency division error caused by slave waiting time.	Default
0:7	trise				0x00

6.5.9 I2C_FLTER

Register offset: 0x08

Register Description: Filter register, used to adjust the filter frequency.

Bits	Name	R/W	Description	is used to adjust the configuration filter frequency size.	Default
0:4	filter	R W			0x00

Note:

1. The registers should satisfy the following relationship:

I2C_FLTR < I2C_PRER;

I2C_TRISE > I2C_FLTR * 2 + 3;

(scl frequency) scl = (I2C_PRER * (5 + 1) + I2C_TRISE) (main frequency)

2. Both the transmit register and the command register are mapped to address 0x02. The transmit register is the MSB and the command register is the LSB.

3. Both the receive register and the status register are mapped to address 0x03. The receive register is the MSB and the status register is the LSB.

7 Revision Information

Revision	Version	describe
date: 2021.4.18	A	initial version.
2021.5.14	B	Manual optimization, supplemented "Revision Information" chapter.
2022.7.22	C	Updated lrm_int_lrn_int parameter description.
2022.8.23	D	Updated an_ctrl and mode_ctrl parameter descriptions.