



Wuhan FisiLink Microelectronics Technology Co., Ltd

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# FSL91030M chip

## Data Sheet

Manual version: **G**

Wuhan Feisiling Microelectronics Technology Co., Ltd.

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## 1 Product Overview

FSL91030M is a 32G bandwidth Layer 2 Ethernet switch chip, using WireBond BGA676 package.

FSL91030M integrates 8-way Gigabit electrical PHY, supporting 10/100/1000BASE-T and 100BASE-FX functions; integrates 2-way 10G Serdes, supporting 1000BASE-X, SGMII, QSGMII, O-USGMII and 10G BASE-R functions; integrates 4-way 1G Serdes, supporting 1000BASE-X and SGMII functions; 4-way 1G Serdes and 4-way Gigabit electrical PHY combination can be configured into 4-way Combo port. FSL91030M also supports 2-way RGMII/GMII/MII interface as an expandable management interface.

FSL91030M integrates RISC\_CPU, main frequency 400MHz, supports 8/16bits DDR3 interface, maximum supports 2Gb DDR, rate 1600MHz (clock frequency 800MHz) memory; supports 2 UART interfaces, 1 JTAG interface, 2 QSPI interfaces, 1 I2C/MDIO interface and 24 GPIO interfaces.

FSL91030M supports flexible service port function selection. Through 10G Serdes using QSGMII/O-USGMII to connect external PHY, it can support up to 30 ports to meet a variety of application scenarios. Typical application scenarios include: 8 Gigabit electrical ports, 8 Gigabit electrical ports + 4 Gigabit optical ports, 8 Gigabit electrical ports and 2 10 Gigabit optical ports, and 24 Gigabit electrical ports + 4 Gigabit optical ports.

FSL91030M supports CPU using Linux operating system or UCOS system. In UCOS system, external DDR can be omitted to reduce equipment cost.

FSL91030M supports complete Layer 2 network protocol processing functions, including L2 bridging, L2 multicast and storm suppression, etc.; supports VLAN functions based on flow, port, protocol and subnet; supports STP, RSTP and QinQ functions; supports anti-DOS attack, blacklist and whitelist and protocol packet filtering functions; supports filters, link aggregation, OAM message sending and port protection functions; supports ingress and egress ACL functions, and also supports synchronous Ethernet and 1588 functions.

FSL91030M supports QoS functions based on 802.1p and DSCP standards; supports 1.5MB of on-chip data cache, and each port supports 8 queues; supports port-based single-rate shaping and queue-based dual-rate shaping, and queue scheduling supports SP/WRR/DWRR and SP+WRR/DWRR, etc.

FSL91030M supports remote configuration.

## 2. Features

- ÿ Integrated RISC-V CPU
- ÿ Integrated 8-way Gigabit electrical port PHY, supporting 10/100/1000BASE-T and 100BASE-FX functions
- ÿ Integrates 4-way 1G Serdes, supports 1000BASE-X and SGMII functions; 4-way 1G Serdes and 4-way Gigabit electrical port PHY
  - The combination can be configured as a 4-way Combo port
- ÿ Integrates 2-way 10G Serdes, supports 1000BASE-X, SGMII, QSGMII, O-USGMII and 10G BASE-R functions
- ÿ Support 2-way MII/GMII/RGMII interface
- ÿ Support Linux/UCOS (no need to plug in DDR)
- ÿ Support 8/16 bits DDR3, the highest speed can reach 1066MHz
- ÿ Support QSPI/SPI NOR-Flash loading
- ÿ Support I2C/MDIO (Clause22/45)/SPI input
- ÿ Supports 2 UARTs, 1 I2C, MDIO (Clause22/45), QSPI/SPI and 24 GPIO outputs
- ÿ Support on-chip packet cache, ACL, QinQ
- ÿ Support 8 queues per port, SP/WRR/DWRR and mixed scheduling
- ÿ Support port-based single-rate shaping and queue-based dual-rate shaping
- ÿ Support hierarchical policing
- Support VLAN based on port, protocol, IP subnet and flow
  - ÿ Support Spanning Tree Protocol (STP) and Rapid Spanning Tree Protocol (RSTP)
  - ÿ Support L2 bridging and storm control
  - ÿ Support L2 multicast, VLAN conversion, and 8 groups of link aggregation
  - ÿ Support QoS based on 802.1p/dscp
  - ÿ Support anti-DoS attack, protocol packet filtering and black and white lists
  - ÿ Support IEEE802.1x
  - ÿ Support mirroring and remote configuration
  - ÿ Support hardware to periodically send OAM messages
  - ÿ Support Synchronous Ethernet (SyncE)
- Support 1588 function
  - ÿ Support 1+1/1:1 port protection
- ÿ WireBond BGA676 package, size 22mm×22mm

### 3 Product specifications

project	Specification
CPU performance	400M
Maximum frame length On-chip cache	16000 bytes 1.5MB
MAC	16K
VLAN	4K
L2 Multicast	4K
ACL	256
Meter minimum granularity based on the number of streams Policing Typical	8Kbps 4K
power consumption	4.5W

#### 4 Application Scenarios

- ÿ 28-port Layer 2 Gigabit switch
- ÿ 8+4 Gigabit/8+2 10 Gigabit video surveillance switches

## 5 Application Examples

### 5.1 Typical scenario 1: 28 -port Gigabit Layer 2 switch

The hardware block diagram of the 28-port Layer 2 Gigabit switch is shown in Figure 5-1.

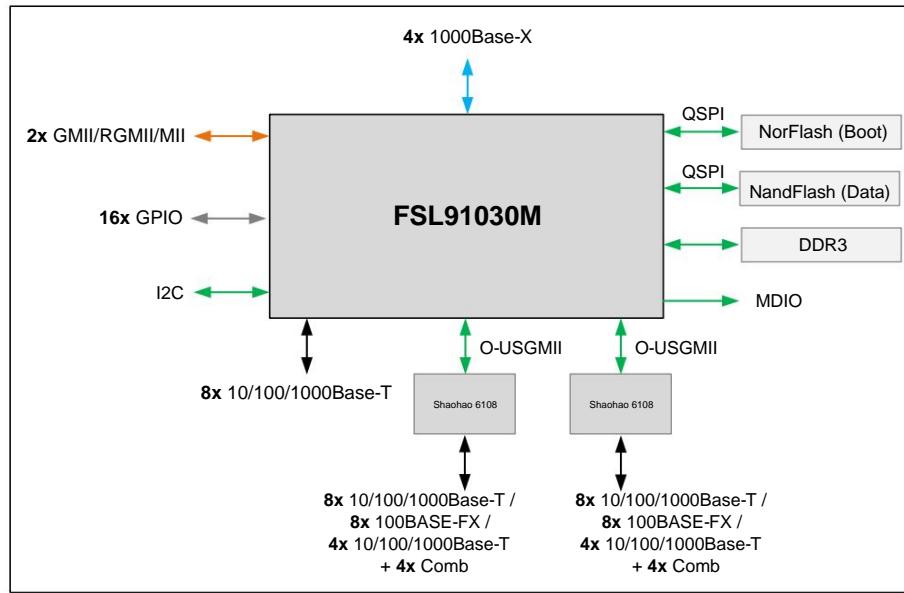


Figure 5-1 28-port Gigabit Layer 2 switch

### 5.2 Typical Scenario 2: 8+4 Gigabit/8+20 Gigabit Video Surveillance Switch

The hardware block diagram of the 8+4 Gigabit/8+20 Gigabit video surveillance switch is shown in Figure 5-2.

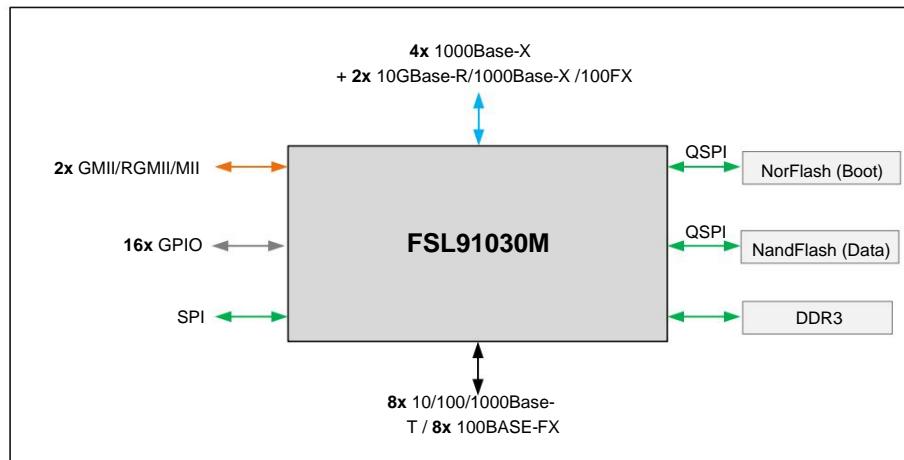


Figure 5-2 8+4 Gigabit/8+20 Gigabit video surveillance switch

## 6 Logic block diagram

The FSL91030M logic block diagram is shown in Figure 6-1.

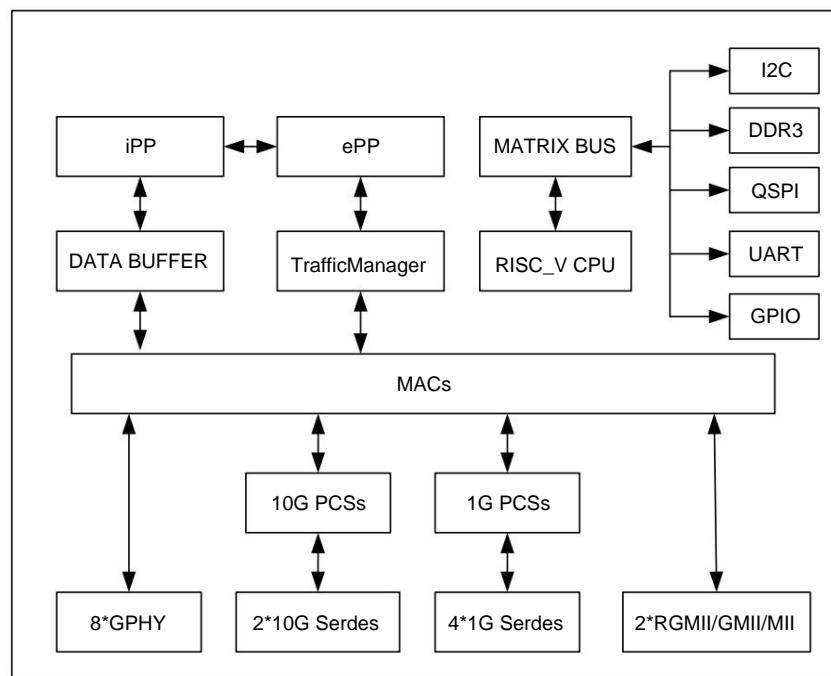


Figure 6-1 Logic block diagram

## 7 pin assignment

### 7.1 Pin Assignment Table

The pin type abbreviations are shown in Table 7-1.

Table 7-1 Pin type abbreviations

parameter	Value	parameter	Value
I	input pin	AI	Analog input pins
O	Output pin	AO	Analog output pin
I/O	Bidirectional input/output	AI/O	Bidirectional analog input/output pins
P	pin Digital power	AP	Analog power pin
G	pin Digital ground pin	AG	Analog ground pin

The pin assignment table is shown in Table 7-2.

Table 7-2 Pin assignment table

Pin Name	Pin number	Type
GNDA SDXG0	A1	AG
X SDXG0 BA TX M L0	A2	AO
GNDA SDXG0	A3	AG
X SDXG0 BA RX M L0	A4	AI
GNDA SDXG1	A5	AG
X SDXG1 BA TX M L0	A6	AO
GNDA SDXG1	A7	AG
X SDXG1 BA RX M L0	A8	AI
GNDA SDXG1	A9	AG
X RECOV CLK1 VLD	A10	I/O
X RECOV CLK SEL 3	A11	I/O
X SD1G1 LED0	A12	I/O
X SDXG1 LED2	A13	I/O
X GPIO23	A14	I/O
X TOD OUT	A15	I/O
GNDK	A16	G
U_REFERENCE_PTP_CLK_CRY	A17	AO
U_REFERENCE_PTP_CLK_GNDIO	A18	AG
X GPIO21	A19	I/O
X XMII1_RXD7	A20	I/O
X XMII1_RXD5	A21	I/O
X XMII1_RXD3	A22	I/O
X XMII1_RXD2	A23	I/O
GNDK	A24	G
GNDK	A25	G
GNDK	A26	G

Pin Name	Pin Number	Type	
X_GEPHY0_P2_MDIC_P	P1	AI/O	
X_GEPHY0_P2_MDIC_N	P2	AI/O	
GNDK	P3	G	
U_REFERENCE_SYS_CLK_OSC_P4		AI/O	
X_SCL	P5	AO	
VCC11A_GEPHY0	P6	G	
VCC11K	P7	AP	
GNDK	P8	G	
VCC11K	P9	AP	
GNDK	P10G		
GNDK	P11	G	
GNDK	P12G		
GNDK	P13G		
GNDK	P14G		
GNDK	P15G		
GNDK	P16G		
GNDK	P17G		
VCC11K	P18	AP	
GNDK	P19G		
VCC11A_GEPHY1	P20	AI/O	
GNDK	P21G		
RSET_BG_GEPHY1	P22	AI/O	
VCC33A_GEPHY1	P23	AI/O	
GNDK	P24G		
X_GEPHY1_P0_MDID_N	P25	AI/O	
X_GEPHY1_P0_MDID_P	P26	AI/O	

Pin Name	Pin number	type
GNDA SDXG0	B1	AG
X SDXG0 BA TX P L0	B2	AO
GNDA SDXG0	B3	AG
X SDXG0 BA RX P L0	B4	AI
GNDA SDXG0	B5	AG
X SDXG1 BA TX P L0	B6	AO
GNDA SDXG1	B7	AG
X SDXG1 BA RX P L0	B8	AI
GNDA SDXG1	B9	AG
X RECOV CLK SEL 6	B10	I/O
X RECOV CLK1	B11	I/O
X SD1G0 LED1	B12	I/O
X SDXG0 LED1	B13	I/O
X GPIO22	B14	I/O
X TOD IN	B15	I/O
GNDK	B16	G
U_REFERENCE_PTP_CLK_OSC	B17	AI
U_REFERENCE_PTP_CLK_VCC3IO	B18	P
X GPIO20	B19	I/O
X XMII1 RXDV	B20	I/O
X XMII1 RXD6	B21	I/O
GNDK	B22	G
X XMII1 RXC	B23	I/O
GNDK	B24	G
X GEPHY1 P3 MDID P	B25	AI/O
X GEPHY1 P3 MDID N	B26	AI/O
GNDA SDXG0	C1	AG
GNDA SDXG0	C2	AG
GNDA SDXG0	C3	AG
GNDA SDXG0	C4	AG
GNDA SDXG0	C5	AG
GNDA SDXG1	C6	AG
GNDA SDXG1	C7	AG
GNDA SDXG1	C8	AG
GNDA SDXG1	C9	AG
X CPU SDA	C10	I/O
X RECOV CLK SEL 0	C11	I/O
X SD1G2 LED1	C12	I/O
X SD1G1 LED1	C13	I/O
GNDK	C14	G
GNDK	C15	G
GNDK	C16	G
GNDK	C17	G
X UART0 TX	C18	I/O
Reserved	C19	I/O
X XMII1 TXER	C20	I/O

Pin Name	Pin number	type
X GEPHY0 P2 MDID P	R1	AI/O
X GEPHY0 P2 MDID N	R2	AI/O
GNDK	R3	G
VCC33A GEPHY0	R4	I/O
VCC33A GEPHY0	R5	AI/O
VCC11A GEPHY0	R6	AI/O
GNDK	R7	G
VCC11K	R8	AP
GNDK	R9	G
VCC11K	R10	AP
GNDK	R11	G
GNDK	R12	G
GNDK	R13	G
GNDK	R14	G
GNDK	R15	G
GNDK	R16	G
VCC11K	R17	AP
GNDK	R18	G
VCC11A GEPHY1	R19	AI/O
GNDK	R20	G
GNDK	R21	G
P1 SD GEPHY1	R22	AI/O
VCC33A GEPHY1	R23	AI/O
GNDK	R24	G
X GEPHY1 P0 MDIC N	R25	AI/O
X GEPHY1 P0 MDIC P	R26	AI/O
X GEPHY0 P3 MDIA P	T1	AI/O
X GEPHY0 P3 MDIA N	T2	AI/O
GNDK	T3	G
VCC33A GEPHY0	T4	G
P0 SD GEPHY0	T5	AI/O
VCC11A GEPHY0	T6	AI/O
GNDK	T7	G
VCC11K	T8	AP
GNDK	T9	G
GNDK	T10	G
GNDK	T11	G
GNDK	T12	G
VCC11K	T13	AP
GNDK	T14	G
VCC11K	T15	AP
GNDK	T16	G
GNDK	T17	G
VCC11K	T18	AP
GNDK	T19	G
VCC11A GEPHY1	T20	AI/O

Pin Name	Pin number	type
X_XMII1_RXER	C21	I/O
GNDK	C22	G
X_XMII1_GTXC	C23	I/O
GNDK	C24	G
X_GEPHY1_P3_MDIC_P	C25	AI/O
X_GEPHY1_P3_MDIC_N	C26	AI/O
X_GEPHY0_P0_MDIA_P	D1	AI/O
X_GEPHY0_P0_MDIA_N	D2	AI/O
GNDK	D3	G
X_XMII0_CRS	D4	I/O
X_XMII0_COL	D5	I/O
X_XMII0_RXD7	D6	I/O
X_CPU_QSPI1_IO2	D7	I/O
X_CPU_QSPI1_IO1	D8	I/O
X_CPU_QSPI1_SCK	D9	I/O
X_CPU_QSPI0_SCK	D10	I/O
X_RECV CLK SEL_1	D11	I/O
X_SD1G3_LED2	D12	I/O
X_SD1G1_LED2	D13	I/O
X_PPS_OUT	D14	I/O
X_PPS_IN	D15	I/O
X_JTAG_TMS	D16	I/O
X_UART1_RX	D17	I/O
Reserved	D18	I/O
X_UART1_TX	D19	I/O
X_XMII1_TXCLK	D20	I/O
X_XMII1_RXD1	D21	I/O
X_XMII1_RXD0	D22	I/O
X_XMII1_RXD4	D23	I/O
GNDK	D24	G
X_GEPHY1_P3_MDIB_P	D25	AI/O
X_GEPHY1_P3_MDIB_N	D26	AI/O
X_GEPHY0_P0_MDIB_P	E1	AI/O
X_GEPHY0_P0_MDIB_N	E2	AI/O
GNDK	E3	G
X_XMII0_RXD6	E4	I/O
X_XMII0_RXD5	E5	I/O
X_XMII0_RXD4	E6	I/O
GNDK	E7	G
X_CPU_QSPI0_IO2	E8	I/O
X_CPU_QSPI0_IO1	E9	I/O
X_CPU_QSPI0_IO0	E10	I/O
X_RECV CLK SEL_8	E11	I/O
X_RECV CLK SEL_4	E12	I/O
X_SD1G0_LED2	E13	I/O
X_SDXG1_LED0	E14	I/O
X_JTAG_TDI	E15	I/O
X_JTAG_TCK	E16	I/O

Pin Name	Pin number	type
GNDK	T21	G
P0_SD_GEPHY1	T22	AI/O
VCC33A_GEPHY1	T23	AI/O
GNDK	T24	G
X_GEPHY1_P0_MDIB_P	T25	AI/O
X_GEPHY1_P0_MDIB_N	T26	AI/O
X_GEPHY0_P3_MDIB_P	U1	AI/O
X_GEPHY0_P3_MDIB_N	U2	AI/O
GNDK	U3	G
VCC33A_GEPHY0	U4	AI/O
P1_SD_GEPHY0	U5	AI/O
VCC11A_GEPHY0	U6	AI/O
GNDK	U7	G
GNDK	U8	G
VCC25A_SD1G2	U9	AP
VCC11K	U10	AP
GNDK	U11	G
VCC11K	U12	AP
GNDK	U13	G
VCC11K	U14	AP
GNDK	U15	G
VCC11K	U16	AP
GNDK	U17	G
GNDK	U18	G
GNDK	U19	G
GNDK	U20	G
GNDK	U21	G
VCC33A_GEPHY1	U22	AI/O
VCC33A_GEPHY1	U23	AI/O
GNDK	U24	G
X_GEPHY1_P0_MDIA_P	U25	AI/O
X_GEPHY1_P0_MDIA_N	U26	AI/O
X_GEPHY0_P3_MDIC_P	V1	AI/O
X_GEPHY0_P3_MDIC_N	V2	AI/O
GNDK	V3	G
VCC33A_GEPHY0	V4	AI/O
RSET_BG_GEPHY0	V5	AI/O
VCC11A_GEPHY0	V6	AI/O
GNDK	V7	G
VCC25A_SD1G3	V8	AP
GNDK	V9	G
GNDK	V10	G
VCC11K	V11	AP
GNDK	V12	G
VCC33IO	V13	AP
GNDK	V14	G
VCC33IO	V15	AP
GNDK	V16	G

Pin Name	Pin number	type
Reserved	E17	I/O
GNDK	E18	G
X GPIO18	E19	I/O
X GPIO19	E20	I/O
X GPIO15	E21	I/O
X GPIO14	E22	I/O
X GPIO13	E23	I/O
GNDK	E24	G
X GEPHY1 P3 MDIA P	E25	AI/O
X GEPHY1 P3 MDIA N	E26	AI/O
X GEPHY0 P0 MDIC P	F1	AI/O
X GEPHY0 P0 MDIC N	F2	AI/O
GNDK	F3	G
X XMII0 RXD3	F4	I/O
X XMII0 RXD2	F5	I/O
X XMII0 RXD1	F6	I/O
X XMII0 RXD0	F7	I/O
X CPU QSPI1 SS	F8	I/O
X CPU QSPI1 IO0	F9	I/O
X CPU SCL	F10	I/O
X RECOV CLK SEL 5	F11	I/O
X RECOV CLK SEL 2	F12	I/O
X SD1G3 LED0	F13	I/O
X SDXG1 LED1	F14	I/O
X JTAG TDO	F15	I/O
X UART0 RX	F16	I/O
Reserved	F17	I/O
X GPIO17	F18	I/O
X GPIO16	F19	I/O
GNDGPIO	F20	G
X GPIO12	F21	I/O
X GPIO11	F22	I/O
X GPIO10	F23	I/O
GNDK	F24	G
X GEPHY1 P2 MDID P	F25	AI/O
X GEPHY1 P2 MDID N	F26	AI/O
X GEPHY0 P0 MDID P	G1	AI/O
X GEPHY0 P0 MDID N	G2	AI/O
GNDK	G3	G
X XMII0 RXC	G4	I/O
GNDK	G5	G
X XMII0 RXER	G6	I/O
X XMII0 TXER	G7	I/O
X CPU QSPI1 IO3	G8	I/O
X CPU QSPI0 IO3	G9	I/O
X CPU QSPI0 SS	G10	I/O
X RECOV CLK SEL 9	G11	I/O
X RECOV CLK SEL 7	G12	I/O

Pin Name	Pin number	type
VCC11K	V17 AP	
GND DDR	V18 AG	
GND DDR	V19 AG	
GND DDR	V20 AG	
GND DDR	V21 AG	
GND DDR	V22 AG	
GND DDR	V23 AG	
GND DDR	V24 AG	
GND DDR	V25 AG	
GND DDR	V26 AG	
X GEPHY0 P3 MDID P	W1 AI/O	
X GEPHY0 P3 MDID N	W2 AI/O	
GNDK	W3G	
VCC33A_GEPHY0	W4 AI/O	
P2 SD GEPHY0	W5 AI/O	
VCC11A_GEPHY0	W6 AI/O	
GNDK	W7G	
VCC11A_SD1G2	W8AP	
GNDK	W 9	
VCC25A_SD1G1	W10 AP	
GNDGPIO	W11G	
VCC25A_SD1G0	W12 AP	
GNDGPIO	W13G	
X DFT TEST2	W14 I/O	
X CP CTRL	W15 I/O	
GND DDR	W16 AG	
VCC11K_DDR	W17 AP	
GND DDR	W18 AG	
VCC15O_DDRCK_ADDR	W19 AP	
GND DDR	W20 AG	
X DDRD1_VREF	W21 AI	
GND DDR	W22 AG	
GND DDR	W23 AG	
X DDRA WE N	W24 AO	
VCC15O_DDR_DATACMR	W25 AP	
X DDRA RAS N	W26 AO	
GNDA_SD1G3	Y1	
GNDA_SD1G3	Y2	
GNDA_SD1G3	Y3	
VCC33A_GEPHY0	Y4 AI/O	
P3 SD GEPHY0	Y5 G	
VCC11A_GEPHY0	Y6 AI/O	
GNDK	Y7 G	
GNDGPIO	Y8 G	
VCC11A_SD1G1	Y9 AP	
GNDGPIO	Y10G	
VCC11A_SD1G0	Y11 AP	
GNDGPIO	Y12	

Pin Name	Pin number	type
X SD1G2 LED0	G13	I/O
X SD1G0 LED0	G14	I/O
X SDXG0 LED0	G15	I/O
VCC33IO	G16 AP	
X DDR 200 SEL	G17	I/O
X QSPI 32B SEL	G18	I/O
GNDGPIO	G19	G
VCC33IO	G20	AP
X GPIO9	G21	I/O
X GPIO8	G22	I/O
X XMII1 TXEN	G23	I/O
GNDK	G24	G
X GEPHY1 P2 MDIC P	G25	AI/O
X GEPHY1 P2 MDIC N	G26	AI/O
X GEPHY0 P1 MDIA P	H1	AI/O
X GEPHY0 P1 MDIA N	H2	AI/O
GNDK	H3	G
X XMII0 GTXC	H4	I/O
GNDK	H5	G
X XMII0 TXEN	H6	I/O
VCC11A SDXG0	H7	AP
VCC11A SDXG0	H8	AP
VCC11A SDXG1	H9	AP
VCC11A SDXG1	H10	AP
GNDGPIO	H11	G
GNDGPIO	H12	G
X SD1G3 LED1	H13	I/O
X SD1G2 LED2	H14	I/O
X SDXG0 LED2	H15	I/O
GNDGPIO	H16	G
X QSPI SPARE SEL	H17	I/O
X CPU NMI	H18	I
VCC33IO	H19	AP
GNDGPIO	H20	G
X XMII1 TXD0	H21	I/O
X XMII1 TXD3	H22	I/O
X XMII1 TXD4	H23	I/O
GNDK	H24	G
X GEPHY1 P2 MDIB P	H25	AI/O
X GEPHY1 P2 MDIB N	H26	AI/O
X GEPHY0 P1 MDIB P	J1	AI/O
X GEPHY0 P1 MDIB N	J2	AI/O
GNDK	J3	G
X XMII0 RXDV	J4	I/O
X XMII0 TXCLK	J5	I/O
X XMII0 TXD0	J6	I/O
AGND11 CDRPLL	J7	AG
AGND33 CDRPLL	J8	AG

Pin Name	Pin number	type
X MDIREF	Y13	I
X DFT TEST1	Y14	I/O
VCC15O DDR DATACMR	Y15 AP	
VCC11A PLL ADDR	Y16 AP	
GND DDR	Y17 AG	
GND DDR	Y18 AG	
X DDRA CA ADDR6	Y19 AO	
X DDRA CA ADDR15	Y20 AO	
VCC15O DDR DATACMR	Y21 AP	
X DDRA CA ADDR11	Y22 AO	
X DDRA BA0	Y23 AO	
GND DDR	Y24 AG	
X DDRA ODT1	Y25 AO	
X DDRA CAS N	Y26 AO	
X SD1G3 BA TX P L0	AA1 AO	
X SD1G3 BA TX M L0	AA2 AO	
GNDA SD1G3	AA3 AG	
VCC33A GEPHY0	AA4 AI/O	
GNDK	AA5 AI/O	
GNDK	AA6 AP	
AVDD33 PTPSD1GPLL	AA7AP	
AVDD11 PTPSD1GPLL	AA8AP	
AGND33 PTPSD1GPLL	AA9AG	
AGND11 PTPSD1GPLL	AA10 AG	
X RECOV CLK0	AA11	I/O
X RECOV CLK0 VLD	AA12	I/O
VCC11K DDR	AA13 AP	
GND DDR	AA14 AG	
X DDRRLTCOMP RDRVUP	AA15 AO	
GND11A PLL ADDR	AA16 AG	
VCC15O DDR DATACMR	AA17 AP	
X DDRA CKE0	AA18 AO	
X DDRA BA1	AA19 AO	
GND DDR	AA20 AG	
X DDRA CA ADDR8	AA21 AO	
X DDRA BA2	AA22 AO	
VCC15O DDR DATACMR	AA23 AP	
X DDRA CS N1	AA24 AO	
X DDRA CS N0	AA25 AO	
GND DDR	AA26 AG	
GNDA SD1G3	AB1 AG	
GNDA SD1G3	AB2 AG	
GNDA SD1G3	AB3 AG	
VCC33A GEPHY0	AB4 AI/O	
VCC11A SD1G3	AB5 AP	
VCC11A SD1G3	AB6G	
X INTERRUPT	AB7 I/O	
GNDGPIO	AB8G	

Pin Name	Pin number	type
GNDGPIO	J9	G
VCC25A_SDXG0	J10	AP
GNDGPIO	J11	G
VCC25A_SDXG1	J12	AP
VCC25A_SDXG1	J13	AP
GNDGPIO	J14	G
GNDGPIO	J15	G
VCC33IO	J16	AP
GNDGPIO	J17	G
VCC33IO	J18	AP
X_XMII1_TXD2	J19	I/O
X_XMII1_TXD1	J20	I/O
X_XMII1_COL	J21	I/O
X_XMII1_TXD7	J22	I/O
VCC33A_GEPHY1	J23	AI/O
GNDK	J24	G
X_GEPHY1_P2_MDIA_P	J25	AI/O
X_GEPHY1_P2_MDIA_N	J26	AI/O
X_GEPHY0_P1_MDIC_P	K1	AI/O
X_GEPHY0_P1_MDIC_N	K2	AI/O
GNDK	K3	G
X_XMII0_TXD1	K4	I/O
X_XMII0_TXD2	K5	I/O
X_XMII0_TXD4	K6	I/O
AVDD11_CDRPLL	K7	AP
AVDD33_CDRPLL	K8	AP
GNDGPIO	K9	G
GNDGPIO	K10	G
VCC25A_SDXG0	K11	AP
GNDGPIO	K12	G
VCC11K	K13	AP
GNDK	K14	G
VCC11K	K15	AP
GNDK	K16	G
VCC11K	K17	AP
X_XMII1_TXD6	K18	G
U_REFERENCE_SERDES_CLK_VCC33IO	K19	I/O
X_XMII1_TXD5	K20	I/O
X_XMII1_CRS	K21	I/O
U_REFERENCE_SERDES_CLK_GND	K22	AG
VCC33A_GEPHY1	K23	AI/O
GNDK	K24	G
X_GEPHY1_P1_MDID_P	K25	AI/O
X_GEPHY1_P1_MDID_N	K26	AI/O
X_GEPHY0_P1_MDID_P	L1	AI/O
X_GEPHY0_P1_MDID_N	L2	AI/O

Pin Name	Pin number	type
VDDQ_EFFUSE	AB9	I/O
AVDD33_TDC	AB10	AP
AGND33_TDC	AB11	AG
GNDGPIO	AB12	G
GND_DDR	AB13	AG
GND_DDR	AB14	AG
X_DDRLTCOMP_RDRVND	AB15	AO
GND_DDR	AB16	AG
X_DDRD0_DQ7	AB17	AI/O
X_DDRD1_DQ6	AB18	AI/O
VCC15O_DDR_DATACMR	AB19	AP
X_DDRD1_DQ3	AB20	AI/O
X_DDRA_CKE1	AB21	AO
GND_DDR	AB22	AG
X_DDRA_CA_ADDR5	AB23	AO
X_DDRA_CA_ADDR9	AB24	AO
VCC15O_DDR_DATACMR	AB25	AP
X_DDRA_ODT0	AB26	AO
X_SD1G3_BA_RX_P_L0	AC1	AI
X_SD1G3_BA_RX_M_L0	AC2	AI
GNDK_SD1G3	AC3	AG
VCC33A_GEPHY0	AC4	AI/O
GNDK	AC5G	
GNDK	AC6G	
VCC11A_SD1G2	AC7	AP
GNDK	AC8G	
VCC11A_SD1G1	AC9	AP
GNDK	AC10G	
VCC11A_SD1G0	AC11	AP
GNDK	AC12G	
GND_DDR	AC13	AG
X_DDRD0_DQ2	AC14	AI/O
VCC15O_DDR_DATACMR	AC15	AP
X_DDRD0_DM	AC16	AO
X_DDRD0_DQ3	AC17	AI/O
GND_DDR	AC18	AG
X_DDRD1_DQ4	AC19	AI/O
X_DDRD1_DM	AC20	AO
VCC15O_DDR_DATACMR	AC21	AP
X_DDRA_CA_ADDR4	AC22	AO
X_DDRA_CA_ADDR1	AC23	AO
GND_DDR	AC24	AG
X_DDRA_CA_ADDR7	AC25	AO
X_DDRA_CA_ADDR3	AC26	AO
GNDK_SD1G2	AD1	AG
GNDK_SD1G2	AD2	AG

Pin Name	Pin number	type
GNDK	L3	G
X XMII0 TXD7	L4	I/O
X XMII0 TXD3	L5	I/O
X LED CLK	L6	I/O
AVDD11 CDRPLL	L7	AP
AVDD33 SYSPLL	L8	AP
AGND33 SYSPLL	L9	AG
AVDD11 SDXGPLLS2D	L10	AP
AGND11 SDXGPLLS2D	L11	AG
AVDD33 SDXGPLL	L12	AP
AGND33 SDXGPLL	L13	AG
VCC11K	L14	AP
GNDK	L15	G
VCC11K	L16	AP
GNDK	L17	G
VCC33IO	L18	AP
GNDGPIO	L19	G
U_REFERENCE_SERDES_CLK_CRY	L20	AI
GNDK	L21	AI
GNDK	L22	AO
VCC33A_GEPHY1	L23	AI/O
GNDK	L24	G
X GEPHY1 P1 MDIC N	L25	AI/O
X GEPHY1 P1 MDIC P	L26	AI/O
X GEPHY0 P2 MDIA P	M1	AI/O
X GEPHY0 P2 MDIA N	M2	AI/O
GNDK	M3	G
X XMII0 TXD6	M4	I/O
X XMII0 TXD5	M5	I/O
X LED DA	M6	I/O
U_REFERENCE_SYS_CLK_VCC33IO	M7	G
AVDD11 SYSPLL	M8	AP
AGND33 SYSPLL	M9	AG
AGND11 SYSPLL	M10	AG
VCC11K	M11	AP
GNDK	M12	G
GNDK	M13	G
GNDK	M14	G
GNDK	M15	G
GNDK	M16	G
GNDK	M17	G
GNDK	M18	G
U_REFERENCE_SERDES_CLK_OSC	M19	AI/O
VCC11A_GEPHY1	M20	AI/O
GNDK	M21	G
P3 SD GEPHY1	M22	AI/O

Pin Name	Pin number	type
GND_A_SD1G2	AD3	AG
GND_A_SD1G2	AD4	AG
GND_A_SD1G2	AD5	AG
GND_A_SD1G1	AD6	AG
GND_A_SD1G1	AD7	AG
GND_A_SD1G1	AD8	AG
GND_A_SD1G1	AD9	AG
GND_A_SD1G0	AD10	AG
GND_A_SD1G0	AD11	AG
GND_A_SD1G0	AD12	AG
GND_A_SD1G0	AD13	AG
GND_DDR	AD14	AG
X DDRD0 DQ6	AD15	AI/O
X DDRD0 DQ4	AD16	AI/O
VCC15O DDR DATAACMR	AD17	AP
X DDRD1 DQ2	AD18	AI/O
X DDRD1 DQ0	AD19	AI/O
GND_DDR	AD20	AG
X DDRD1 DQ5	AD21	AI/O
X DDRA RESET_N DRAM	AD22	AO
VCC15O DDR DATAACMR	AD23	AP
X DDRA CA ADDR10	AD24	AO
X DDRA CA ADDR13	AD25	AO
GND_DDR	AD26	AG
GND_A_SD1G2	AE1	AG
X SD1G2 BA TX P L0	AE2	AO
GND_A_SD1G2	AE3	AG
X SD1G2 BA RX P L0	AE4	AI
GND_A_SD1G2	AE5	AG
X SD1G1 BA TX P L0	AE6	AO
GND_A_SD1G1	AE7	AG
X SD1G1 BA RX P L0	AE8	AI
GND_A_SD1G1	AE9	AG
X SD1G0 BA TX P L0	AE10	AO
GND_A_SD1G0	AE11	AG
X SD1G0 BA RX P L0	AE12	AI
GND_A_SD1G0	AE13	AG
GND_DDR	AE14	AG
X DDRD0 DQ0	AE15	AI/O
GND_DDR	AE16	AG
X DDRD0 DQ1	AE17	AI/O
X DDRD0 DQ5	AE18	AI/O
VCC15O_DDR_DATAACMR	AE19	AP
X DDRD1 DQ1	AE20	AI/O
X DDRD1 DQ7	AE21	AI/O
GND_DDR	AE22	AG

Pin Name	Pin number	type
VCC33A_GEPHY1	M23	AI/O
GNDK	M24	G
X_GEPHY1_P1_MDIB_P	M25	AI/O
X_GEPHY1_P1_MDIB_N	M26	AI/O
X_GEPHY0_P2_MDIB_P	N1	AI/O
X_GEPHY0_P2_MDIB_N	N2	AI/O
GNDK	N3	G
X_CHIP_RST_N	N4	I
X_SDA	N5	I/O
U_REFERENCE_SYS_CLK_GND	N6	AG
U_REFERENCE_SYS_CLK_CRY	N7	AI
VCC11K	N8	AP
GNDK	N9	G
VCC11K	N10	AP
GNDK	N11	G
GNDK	N12	G
GNDK	N13	G
GNDK	N14	G
GNDK	N15	G
GNDK	N16	G
VCC11K	N17	AP
GNDK	N18	G
VCC11A_GEPHY1	N19	AI/O
GNDK	N20	G
GNDK	N21	G
P2_SD_GEPHY1	N22	AI/O
VCC33A_GEPHY1	N23	AI/O
GNDK	N24	G
X_GEPHY1_P1_MDIA_P	N25	AI/O
X_GEPHY1_P1_MDIA_N	N26	AI/O

Pin Name	Pin number	type
X_DDRA_CA_ADDR14	AE23	AO
X_DDRA_CA_ADDR12	AE24	AO
VCC15O_DDR_DATACMR	AE25	AP
X_DDRA_CA_ADDR2	AE26	AO
GND_A_SD1G2	AF1	AG
X_SD1G2_BA_RX_M_L0	AF2	AO
GND_A_SD1G2	AF3	AG
X_SD1G2_BA_RX_M_L0	AF4	AI
GND_A_SD1G2	AF5AG	
X_SD1G1_BA_TX_M_L0	AF6	AO
GND_A_SD1G1	AF7AG	
X_SD1G1_BA_RX_M_L0	AF8	AI
GND_A_SD1G1	AF9AG	
X_SD1G0_BA_TX_M_L0	AF10	AO
GND_A_SD1G0	AF11AG	
X_SD1G0_BA_RX_M_L0	AF12	AI
GND_A_SD1G0	AF13AG	
X_DDRD0_VREF	AF14	AI
VCC15O_DDR_DATACMR	AF15	AP
X_DDRD0_DQS	AF16	AI/O
X_DDRD0_DQSB	AF17	AI/O
GND_DDR	AF18	AG
X_DDRD1_DQS	AF19	AI/O
X_DDRD1_DQSB	AF20	AI/O
VCC15O_DDR_DATACMR	AF21	AP
X_DDRA_CK	AF22	AO
X_DDRA_CKB	AF23	AO
GND_DDR	AF24	AG
X_DDRA_CA_ADDR0	AF25	AO
GND_DDR	AF26	AG

## 8 Pin Description

The pin type abbreviations are shown in Table 8-1.

Table 8-1 Pin type abbreviations

parameter	Value	parameter	Value
I	input pin	AI	Analog input pins
O	Output pin	AO	Analog output pin
I/O	Bidirectional input/output	AI/O	Bidirectional analog input/output pins
P	pin Digital power	AP	Analog power pin
G	pin Digital ground pin	AG	Analog ground pin

### 8.1 Clock reset interface

The clock reset interface description table pins are shown in Table 8-2.

Table 8-2 Clock reset interface pin description

Pin Name	Pin No. Pin	Type	Description Note
U_REFERENCE_SYS_CLK_CRY	N7	AI	As the reference clock of the system. When connected to a crystal, 25MHz clock input; when connected to a crystal oscillator, this pin needs to be left floating
U_REFERENCE_SYS_CLK_OSC	P4	AI/O	As the reference clock of the system. When connected to a crystal, 25MHz clock output; when connected to a crystal oscillator, this pin serves as 25MHz clock input
U_REFERENCE_SERDES_CLK_CRY L20		AI	As the reference clock of Serdes and GPHY. When connected to a crystal oscillator, this tube Feet should be suspended
U_REFERENCE_SERDES_CLK_OSC M19		AI/O	As the reference clock of Serdes and GPHY. When connected to a crystal oscillator, this tube Pin as 25MHz clock input
U_REFERENCE_PTP_CLK_CRY	A17	AI	As 1588 reference clock. When connected to a crystal, it is used as 25MHz Clock input; when connected to a crystal oscillator, this pin needs to be left floating
U_REFERENCE_PTP_CLK_OSC	B17	AI/O	As 1588 reference clock. When connected to a crystal, it is used as 25MHz Clock output; when connected to a crystal oscillator, this pin is used as a 25MHz Clock Input

Note: When the corresponding function of the clock pin is not used, the pin can be left floating.

The reset and interrupt interface description table pins are shown in Table 8-3.

Table 8-3 Reset and interrupt interface pin description

Pin Name	Pin No. Pin	Type	describe
X_INTERRUPT	AB7	I/O	chip interrupt output signal, high effective; when not in use, this pin can be left floating
X_CHIP_RST_N	N4	I	Chip reset signal, low effective

## 8.2 Electrical PHY Interface

The electrical port PHY interface pin description is shown in Table 8-4.

Table 8-4 Electrical port PHY interface pin description

Pin Name	Pin No.	Type	describe
<b>GEPHY0 Interface</b>			
RSET_BG_GEPHY0	V5	AI/O	External reference resistor, connect $3k\Omega$ ( $\pm 1\%$ ) resistor to ground  In optical port (100BASE-FX) mode, connect the optical fiber transceiver SD pin; pull down to ground in electrical mode
P0_SD_GEPHY0	T5	AI/O	
P1_SD_GEPHY0	U5	AI/O	
P2_SD_GEPHY0	W5	AI/O	
P3_SD_GEPHY0	Y5	AI/O	
X_GEPHY0_P0_MDIA_P	D1	AI/O	In AI/O electrical port mode, the differential signal pair of lane A of port P0; optical port (100BASE-FX) mode, as the differential signal pair of RX
X_GEPHY0_P0_MDIA_N	D2	AI/O	
X_GEPHY0_P0_MDIB_P	E1	AI/O	In AI/O electrical port mode, the differential signal pair of lane B of P0 port; optical port
X_GEPHY0_P0_MDIB_N	E2	AI/O	In 100BASE-FX mode, the differential signal pair is used as TX
X_GEPHY0_P0_MDIC_P	F1	AI/O	In AI/O electrical port mode, the differential signal pair of lane C of port P0; optical port
X_GEPHY0_P0_MDIC_N	F2	AI/O	In (100BASE-FX) mode, this pin can be left floating.
X_GEPHY0_P0_MDID_P	G1	AI/O	In AI/O electrical port mode, the differential signal pair of lane D of port P0; optical port
X_GEPHY0_P0_MDID_N	G2	AI/O	In (100BASE-FX) mode, this pin can be left floating.
X_GEPHY0_P1_MDIA_P	H1	AI/O	P1 port lane A differential signal pair
X_GEPHY0_P1_MDIA_N	H2	AI/O	
X_GEPHY0_P1_MDIB_P	J1	AI/O	P1 port lane B differential signal pair
X_GEPHY0_P1_MDIB_N	J2	AI/O	
X_GEPHY0_P1_MDIC_P	K1	AI/O	P1 port lane C differential signal pair
X_GEPHY0_P1_MDIC_N	K2	AI/O	
X_GEPHY0_P1_MDID_P	L1	AI/O	P1 port lane D differential signal pair
X_GEPHY0_P1_MDID_N	L2	AI/O	
X_GEPHY0_P2_MDIA_P	M1	AI/O	P2 port lane A differential signal pair
X_GEPHY0_P2_MDIA_N	M2	AI/O	
X_GEPHY0_P2_MDIB_P	N1	AI/O	P2 port lane B differential signal pair
X_GEPHY0_P2_MDIB_N	N2	AI/O	
X_GEPHY0_P2_MDIC_P	P1	AI/O	P2 port lane C differential signal pair
X_GEPHY0_P2_MDIC_N	P2	AI/O	
X_GEPHY0_P2_MDID_P	R1	AI/O	P2 port lane D differential signal pair
X_GEPHY0_P2_MDID_N	R2	AI/O	
X_GEPHY0_P3_MDIA_P	T1	AI/O	P3 port lane A differential signal pair
X_GEPHY0_P3_MDIA_N	T2	AI/O	
X_GEPHY0_P3_MDIB_P	U1	AI/O	P3 port lane B differential signal pair
X_GEPHY0_P3_MDIB_N	U2	AI/O	
X_GEPHY0_P3_MDIC_P	V1	AI/O	P3 port lane C differential signal pair

Pin Name	Pin No. Pin	Type	describe
X_GEPHY0_P3_MDIC_N	V2	AI/O	P3 port lane D differential signal pair
X_GEPHY0_P3_MDID_P	W1	AI/O	
X_GEPHY0_P3_MDID_N	W2	AI/O	
<b>GEPHY1 Interface</b>			
RSET_BG_GEPHY1	P22	AI/O	External reference resistor, connect 3kΩ resistor to ground
P0_SD_GEPHY1	T22	AI/O	In optical port (100BASE-FX) mode, connect the optical fiber transceiver SD pin; ground under the electrical port module
P1_SD_GEPHY1	R22	AI/O	
P2_SD_GEPHY1	N22	AI/O	
P3_SD_GEPHY1	M22	AI/O	
X_GEPHY1_P0_MDIA_P	U25	AI/O	P0 port lane A differential signal pair
X_GEPHY1_P0_MDIA_N	U26	AI/O	
X_GEPHY1_P0_MDIB_P	T25	AI/O	P0 port lane B differential signal pair
X_GEPHY1_P0_MDIB_N	T26	AI/O	
X_GEPHY1_P0_MDIC_P	R26	AI/O	Differential signal pair of lane C of P0 port
X_GEPHY1_P0_MDIC_N	R25	AI/O	
X_GEPHY1_P0_MDID_P	P26	AI/O	Differential signal pair of lane D of port P0
X_GEPHY1_P0_MDID_N	P25	AI/O	
X_GEPHY1_P1_MDIA_P	N25	AI/O	P1 port lane A differential signal pair
X_GEPHY1_P1_MDIA_N	N26	AI/O	
X_GEPHY1_P1_MDIB_P	M25	AI/O	P1 port lane B differential signal pair
X_GEPHY1_P1_MDIB_N	M26	AI/O	
X_GEPHY1_P1_MDIC_P	L26	AI/O	P1 port lane C differential signal pair
X_GEPHY1_P1_MDIC_N	L25	AI/O	
X_GEPHY1_P1_MDID_P	K25	AI/O	P1 port lane D differential signal pair
X_GEPHY1_P1_MDID_N	K26	AI/O	
X_GEPHY1_P2_MDIA_P	J25	AI/O	P2 port lane A differential signal pair
X_GEPHY1_P2_MDIA_N	J26	AI/O	
X_GEPHY1_P2_MDIB_P	H25	AI/O	P2 port lane B differential signal pair
X_GEPHY1_P2_MDIB_N	H26	AI/O	
X_GEPHY1_P2_MDIC_P	G25	AI/O	P2 port lane C differential signal pair
X_GEPHY1_P2_MDIC_N	G26	AI/O	
X_GEPHY1_P2_MDID_P	F25	AI/O	P2 port lane D differential signal pair
X_GEPHY1_P2_MDID_N	F26	AI/O	
X_GEPHY1_P3_MDIA_P	E25	AI/O	P3 port lane A differential signal pair
X_GEPHY1_P3_MDIA_N	E26	AI/O	
X_GEPHY1_P3_MDIB_P	D25	AI/O	P3 port lane B differential signal pair
X_GEPHY1_P3_MDIB_N	D26	AI/O	
X_GEPHY1_P3_MDIC_P	C25	AI/O	P3 port lane C differential signal pair
X_GEPHY1_P3_MDIC_N	C26	AI/O	

Pin Name	Pin No. Pin	Type	describe
X_GEPHY1_P3_MDID_P	B25	AI/O	
X_GEPHY1_P3_MDID_N	B26	AI/O	P3 port lane D differential signal pair

## 8.3 10G Serdes Interface

The 10G Serdes interface pin description is shown in Table 8-5.

Table 8-5 10G Serdes interface pin description

Pin Name	Pin No. Pin	Type	describe
X_SDXG0_BA_TX_M_L0	A2	AO	10G Serdes0 transmit signal differential pair
X_SDXG0_BA_TX_P_L0	B2	AO	
X_SDXG0_BA_RX_M_L0	A4	AI	10G Serdes0 receive signal differential pair
X_SDXG0_BA_RX_P_L0	B4	AI	
X_SDXG1_BA_TX_M_L0	A6	AO	10G Serdes1 transmit signal differential pair
X_SDXG1_BA_TX_P_L0	B6	AO	
X_SDXG1_BA_RX_M_L0	A8	AI	10G Serdes1 receive signal differential pair
X_SDXG1_BA_RX_P_L0	B8	AI	

## 8.4 1G Serdes Interface

The 1G Serdes interface pin description is shown in Table 8-6.

Table 8-6 1G Serdes interface pin description

Pin Name	Pin No. Pin	Type	describe
X_SD1G0_BA_TX_M_L0	AF10	AO	1G Serdes0 transmit signal differential pair
X_SD1G0_BA_TX_P_L0	AE10	AO	
X_SD1G0_BA_RX_M_L0	AF12	AI	1G Serdes0 receive signal differential pair
X_SD1G0_BA_RX_P_L0	AE12	AI	
X_SD1G1_BA_TX_M_L0	AF6	AO	1G Serdes1 transmit signal differential pair
X_SD1G1_BA_TX_P_L0	AE6	AO	
X_SD1G1_BA_RX_M_L0	AF8	AI	1G Serdes1 receive signal differential pair
X_SD1G1_BA_RX_P_L0	AE8	AI	
X_SD1G2_BA_TX_M_L0	AF2	AO	1G Serdes2 transmit signal differential pair
X_SD1G2_BA_TX_P_L0	AE2	AO	
X_SD1G2_BA_RX_M_L0	AF4	AI	1G Serdes2 receive signal differential pair
X_SD1G2_BA_RX_P_L0	AE4	AI	
X_SD1G3_BA_TX_M_L0	AA2	AO	1G Serdes3 transmit signal differential pair
X_SD1G3_BA_TX_P_L0	AA1	AO	
X_SD1G3_BA_RX_M_L0	AC2	AI	1G Serdes3 receive signal differential pair
X_SD1G3_BA_RX_P_L0	AC1	AI	

## 8.5 GMII/RGMII/MII Interface

The GMII/RGMII/MII interface pin description table is shown in Table 8-7.

Table 8-7 GMII/RGMII/MII interface pin description

Pin Name	Pin No.	Pin Type	describe
<b>X_XMII1 Interface</b>			
X_XMII1_CRS	K21	I/O	Carrier detect input signal for GMII1/RGMII1/MII1 interface
X_XMII1_COL	J21	I/O	GMII1/RGMII1/MII1 interface carrier detection input signal
X_XMII1_TXD7	J22	I/O	GMII1/RGMII1/MII1 interface transmit data signal; pin connection The methods are shown in Figure 8-1, Figure 8-2, Figure 8-3, Figure 8-4, Figure 8-5, and Figure 8-6 As shown in Figure 8-7 and Figure 8-8
X_XMII1_TXD6	K18	I/O	
X_XMII1_TXD5	K20	I/O	
X_XMII1_TXD4	H23	I/O	
X_XMII1_TXD3	H22	I/O	
X_XMII1_TXD2	J19	I/O	
X_XMII1_TXD1	J20	I/O	
X_XMII1_TXD0	H21	I/O	
X_XMII1_TXEN	G23	I/O	GMII1/MII1/RGMII1 interface transmit data valid indication
X_XMII1_GTXC	C23	I/O	GMII1/MII1/RGMII1 interface sends clock signal
X_XMII1_TXCLK	D20	I/O	reserve
X_XMII1_TXER	C20	I/O	GMII1/MII1/RGMII1 interface transmit data error indication
X_XMII1_RXER	C21	I/O	Input data error indication for GMII1/MII1/RGMII1 interfaces
X_XMII1_RXC	B23	I/O	GMII1/RGMII1/MII1 interface input clock
X_XMII1_RXDV	B20	I/O	GMII1/RGMII1/MII1 interface receive data valid indication
X_XMII1_RXD7	A20	I/O	GMII1/RGMII1/MII1 interface receive data signal; pin connection The methods are shown in Figure 8-1, Figure 8-2, Figure 8-3, Figure 8-4, Figure 8-5, and Figure 8-6 As shown in Figure 8-7 and Figure 8-8
X_XMII1_RXD6	B21	I/O	
X_XMII1_RXD5	A21	I/O	
X_XMII1_RXD4	D23	I/O	
X_XMII1_RXD3	A22	I/O	
X_XMII1_RXD2	A23	I/O	
X_XMII1_RXD1	D21	I/O	
X_XMII1_RXD0	D22	I/O	
<b>X_XMII0 interface</b>			
X_XMII0_CRS	D4	I/O	Carrier detect input signal for GMII0/RGMII0/MII0 interface
X_XMII0_COL	D5	I/O	GMII0/RGMII0/MII0 interface carrier detection input signal
X_XMII0_TXD7	L4	I/O	GMII0/RGMII0/MII0 interface transmit data signal; pin connection The methods are shown in Figure 8-1, Figure 8-2, Figure 8-3, Figure 8-4, Figure 8-5, and Figure 8-6 As shown in Figure 8-7 and Figure 8-8
X_XMII0_TXD6	M4	I/O	
X_XMII0_TXD5	M5	I/O	
X_XMII0_TXD4	K6	I/O	
X_XMII0_TXD3	L5	I/O	

Pin Name	Pin No.	Pin Type	describe
X_XMII0_TXD2	K5	I/O	
X_XMII0_TXD1	K4	I/O	
X_XMII0_TXD0	J6	I/O	
X_XMII0_TXEN	H6	I/O	GMII0/MII0/RGMII0 interface transmit data valid indication
X_XMII0_GTXC	H4	I/O	GMII0/MII0/RGMII0 interface sends clock signal
X_XMII0_TXCLK	J5	I/O	reserve
X_XMII0_TXER	G7	I/O	GMII0/MII0/RGMII0 interface transmit data error indication
X_XMII0_RXER	G6	I/O	Input data error indication for GMII0/MII0/RGMII0 interface
X_XMII0_RXC	G4	I/O	GMII0/RGMII0/MII0 interface input clock
X_XMII0_RXDV	J4	I/O	GMII0/RGMII0/MII0 interface receive data valid indication
X_XMII0_RXD7	D6	I/O	GMII0/RGMII0/MII0 interface receive data signal; pin connection The methods are shown in Figure 8-1, Figure 8-2, Figure 8-3, Figure 8-4, Figure 8-5, and Figure 8-6 As shown in Figure 8-7 and Figure 8-8
X_XMII0_RXD6	E4	I/O	
X_XMII0_RXD5	E5	I/O	
X_XMII0_RXD4	E6	I/O	
X_XMII0_RXD3	F4	I/O	
X_XMII0_RXD2	F5	I/O	
X_XMII0_RXD1	F6	I/O	
X_XMII0_RXD0	F7	I/O	

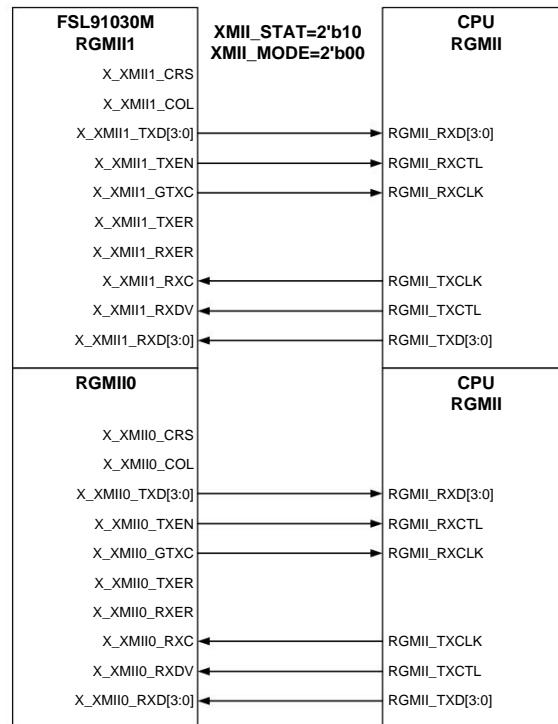


Figure 8-1 GMII/RGMII/MII interface connection method 1

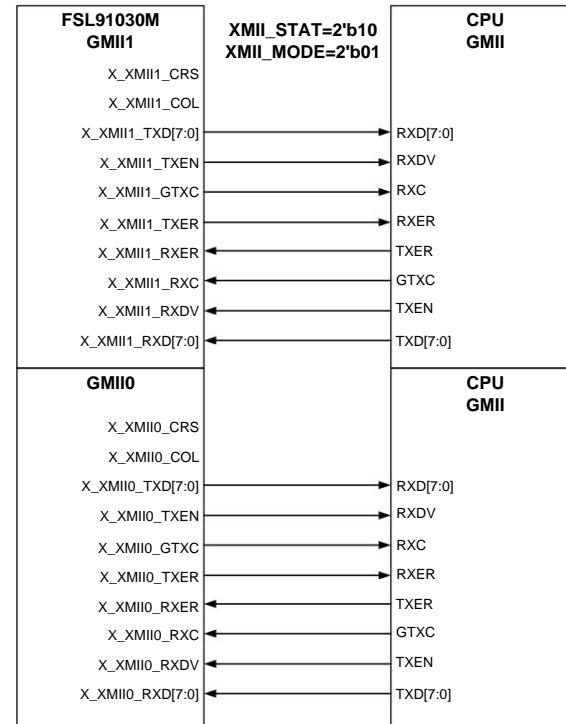


Figure 8-2 GMII/RGMII/MII interface connection method 2

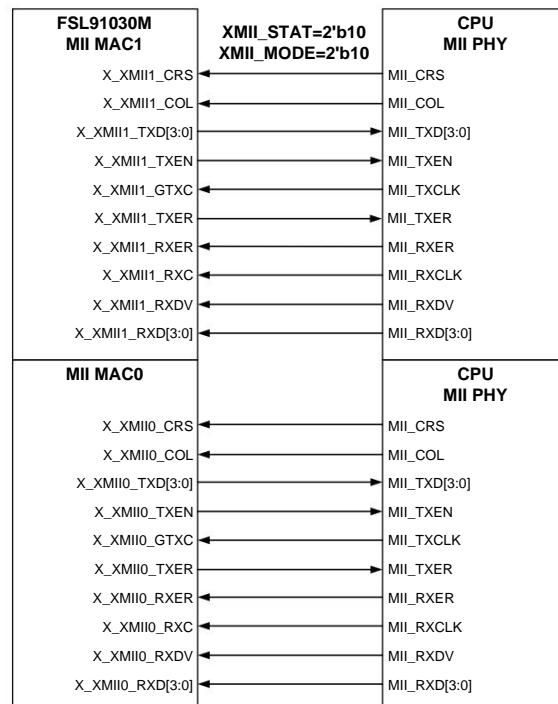


Figure 8-3 GMII/RGMII/MII interface connection method 3

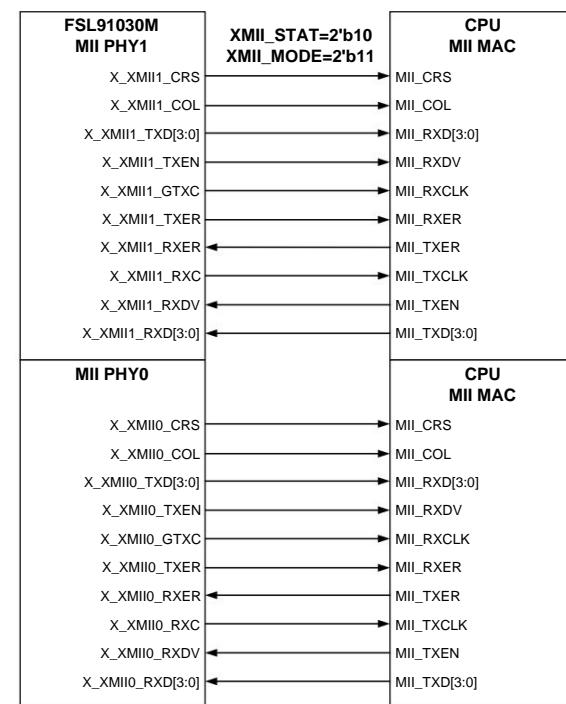


Figure 8-4 GMII/RGMII/MII interface connection method 4

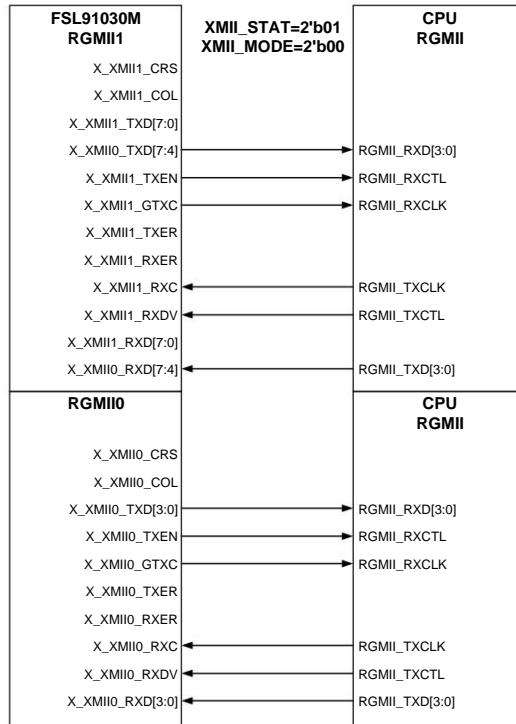


Figure 8-5 GMII/RGMII/MII interface connection method 5

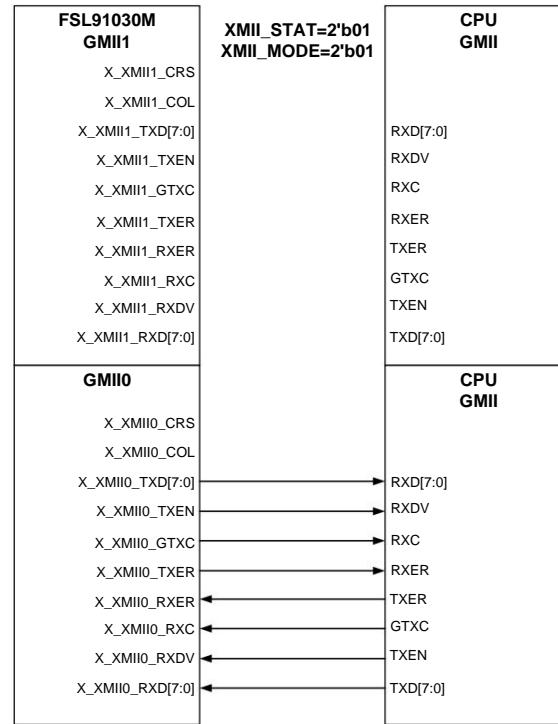


Figure 8-6 GMII/RGMII/MII interface connection method 6

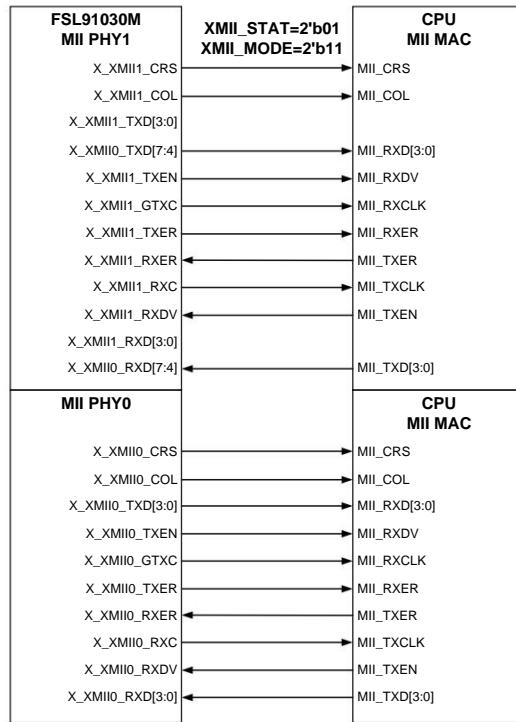


Figure 8-7 GMII/RGMII/MII interface connection method 7

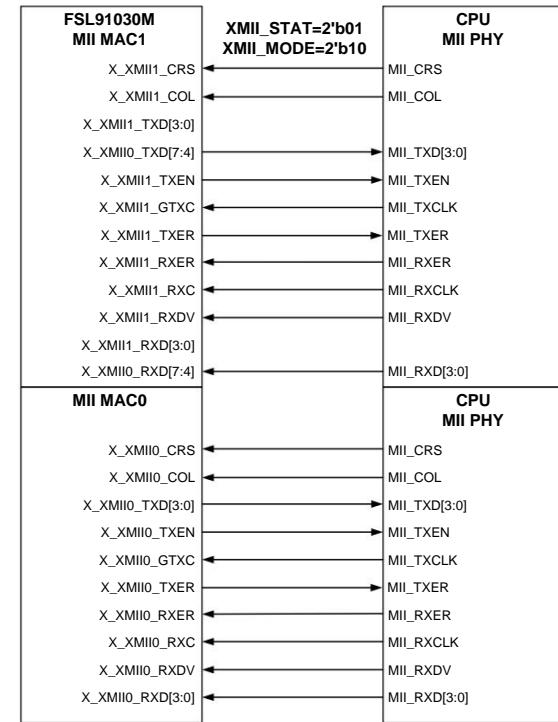


Figure 8-8 GMII/RGMII/MII interface connection mode 8

## 8.6 Time/Clock Synchronization Interface

Table 8-8 shows the pin description of the PTP time synchronization interface.

Table 8-8 PTP time synchronization interface pin description

Pin Name	Pin No.	Pin Type	Description Note
X_PPS_OUT	D14	I/O	PPS output signal
X_TOD_OUT	A15	I/O	TOD output signal
X_PPS_IN	D15	I/O	PPS Input Signal
X_TOD_IN Note:	B15	I/O	TOD Input Signal

When the corresponding function of the PTP time synchronization pin is not used, the pin can be left floating.

The synchronous Ethernet interface pin description is shown in Table 8-9.

Table 8-9 Synchronous Ethernet interface pin description

Pin Name	Pin Number	Pin Type	Description Note
X_RECov_CLK_SEL_0 C11		I/O	0th channel recovery clock port selection configuration, according to X_RECov_CLK_SEL_[4:0] selects X_RECov_CLK0 clock
X_RECov_CLK_SEL_1 D11		I/O	Output pin clock source: 5'd0: GEPHY0 recovered clock, 25MHz; 5'd1: GEPHY1 recovered clock, 25MHz 5'd2: GEPHY2 recovered clock, 25MHz 5'd3: GEPHY3 recovered clock, 25MHz 5'd4: GEPHY4 recovered clock, 25MHz 5'd5: GEPHY5 recovered clock, 25MHz 5'd6: GEPHY6 recovered clock, 25MHz 5'd7: GEPHY7 recovered clock, 25MHz 5'd8: 10G SerDes (left) recovered clock, 25MHz 5'd9: 10G SerDes (right) recovered clock, 25MHz 5'd10: 1G SerDes (0) recovered clock, 25MHz 5'd11: 1G SerDes (1) recovered clock, 25MHz 5'd12: 1G SerDes (2) recovered clock, 25MHz 5'd13: 1G SerDes (3) recovered clock, 25MHz 5'd14: Internal clock observation, derived from system clock, 2.5 MHz 5'd15: Internal clock observation, derived from the switch core clock, 15~30MHz 5'd16: Internal clock observation, derived from 1G SerDes reference clock, 12.5MHz 5'd16: Internal clock observation, derived from the 10G SerDes (left) reference clock, 12.5/15.625MHz 5'd17: Internal clock observation, derived from PTP PLL, 12.5 MHz 5'd18: Internal clock observation, from SOC PLL 5'd19: Internal clock observation, from CDR PLL, 25 MHz
X_RECov_CLK_SEL_4 E12		I/O	1st recovery clock port selection configuration, according to X_RECov_CLK_SEL_[9:5] selects X_RECov_CLK1 clock
X_RECov_CLK_SEL_5 F11		I/O	
X_RECov_CLK_SEL_6 B10		I/O	

X_RECov_CLK_SEL_7 G12		The clock source of the I/O output pin is selected in the same way as X_RECov_CLK_SEL_[4:0]	
X_RECov_CLK_SEL_8 E11		I/O	
X_RECov_CLK_SEL_9 G11		I/O	
X_RECov_CLK0	AA11	I/O	Channel 0 recovered clock output signal, 25MHz
X_RECov_CLK0_VLD AA12		I/O	Channel 0 recovery clock valid indication
X_RECov_CLK1	B11	I/O	1st recovered clock output signal, 25MHz
X_RECov_CLK1_VLD A10 Note: When		I/O	The first channel recovery clock is valid.

the corresponding function of the PTP time synchronization pin is not used, the pin can be left floating.

## 8.7 DDR3 Interface

The DDR3 interface pin description table is shown in Table 8-10.

Table 8-10 DDR3 interface pin description

Pin Name	Pin No. Pin	Type	describe
X_DDRD0_DQ7	AB17	AI/O	Data Signal
X_DDRD0_DQ6	AD15	AI/O	
X_DDRD0_DQ5	AE18	AI/O	
X_DDRD0_DQ4	AD16	AI/O	
X_DDRD0_DQ3	AC17	AI/O	
X_DDRD0_DQ2	AC14	AI/O	
X_DDRD0_DQ1	AE17	AI/O	
X_DDRD0_DQ0	AE15	AI/O	
X_DDRD0_DQS	AF16	AI/O	
X_DDRD0_DQSB	AF17	AI/O	
X_DDRD0_DM	AC16	AO	Data mask signal
X_DDRD0_VREF	AF14	AI	Receive reference voltage
X_DDRD1_DQ7	AE21	AI/O	Data clock signal
X_DDRD1_DQ6	AB18	AI/O	
X_DDRD1_DQ5	AD21	AI/O	
X_DDRD1_DQ4	AC19	AI/O	
X_DDRD1_DQ3	AB20	AI/O	
X_DDRD1_DQ2	AD18	AI/O	
X_DDRD1_DQ1	AE20	AI/O	
X_DDRD1_DQ0	AD19	AI/O	
X_DDRD1_DQS	AF19	AI/O	
X_DDRD1_DQSB	AF20	AI/O	
X_DDRD1_DM	AC20	AO	Data mask signal
X_DDRD1_VREF	W21	AI	Receive reference voltage
X_DDRA_BA2	AA22	AO	DDR bank address signal
X_DDRA_BA1	AA19	AO	

X_DDRA_BA0	Y23	AO	
X_DDRA_ODT1	Y25	AO	ODT resistance control
X_DDRA_ODT0	AB26	AO	
X_DDRA_CS_N1	AA24	AO	
X_DDRA_CS_N0	AA25	AO	Chip select signal
X_DDRA_CK	AF22	AO	
X_DDRA_CKB	AF23	AO	
X_DDRA_CA_ADDR15	Y20	AO	
X_DDRA_CA_ADDR14	AE23	AO	
X_DDRA_CA_ADDR13	AD25	AO	
X_DDRA_CA_ADDR12	AE24	AO	
X_DDRA_CA_ADDR11	Y22	AO	
X_DDRA_CA_ADDR10	AD24	AO	
X_DDRA_CA_ADDR9	AB24	AO	
X_DDRA_CA_ADDR8	AA21	AO	
X_DDRA_CA_ADDR7	AC25	AO	Address signal
X_DDRA_CA_ADDR6	Y19	AO	
X_DDRA_CA_ADDR5	AB23	AO	
X_DDRA_CA_ADDR4	AC22	AO	
X_DDRA_CA_ADDR3	AC26	AO	
X_DDRA_CA_ADDR2	AE26	AO	
X_DDRA_CA_ADDR1	AC23	AO	
X_DDRA_CA_ADDR0	AF25	AO	
X_DDRA_RESET_N_DRAM	AD22	AO	DRAM reset signal
X_DDRA_CAS_N	Y26	AO	DDR CAS_N signal
X_DDRA_CKE1	AB21	AO	Clock enable signal
X_DDRA_CKE0	AA18	AO	
X_DDRA_WE_N	W24	AO	DDR write indication signal
X_DDRA_RAS_N	W26	AO	DDR RAS_N signal
X_DDRRLTCOMP_RDRVUP	AA15	AO pull-down	drive compensation; a 240 $\Omega$ ( $\pm 1\%$ ) resistor should be connected in series to ground
X_DDRRLTCOMP_RDRVDN	AB15	AO pull-up	drive compensation; a 240 $\Omega$ ( $\pm 1\%$ ) resistor should be connected in series to POWER

## 8.8 UART Interface

The UART interface pin description table is shown in Table 8-11.

Table 8-11 UART interface pin description

Pin Name	Pin No.	Pin Type	describe
X_UART0_RX	F16	I/O	Serial input data signal
X_UART0_TX	C18	I/O	Serial output data signal
X_UART1_RX	D17	I/O	Serial input data signal

X_UART1_TX	D19	I/O	Serial output data signal
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## 8.9 JTAG Interface

The JTAG interface pin description table is shown in Table 8-12.

Table 8-12 JTAG interface pin description

Pin Name	Pin No.	Pin Type	Description Note
X_JTAG_TDI	E15	I/O	Input data signal
X_JTAG_TCK	E16	I/O	Clock signal
X_JTAG_TDO	F15	I/O	Output data signal
X_JTAG_TMS	D16	I/O	Mode selection signal

Note: When the corresponding function of the JTAG interface pin is not used, the pin can be left floating.

## 8.10 QSPI Interface

The QSPI interface pin description table is shown in Table 8-13.

When the device is powered on, it reads the program from QSPI0 by default, so QSPI0 must be connected to Nor Flash.

Table 8-13 QSPI interface pin description

Pin Name	Pin Number	Pin Type	Description Note
X_CPU_QSPI0_SCK	D10	I/O	Clock signal
X_CPU_QSPI0_IO0	E10	I/O	Bidirectional data signal
X_CPU_QSPI0_IO1	E9	I/O	
X_CPU_QSPI0_IO2	E8	I/O	
X_CPU_QSPI0_IO3	G9	I/O	
X_CPU_QSPI0_SS	G10	I/O	Chip Select
X_CPU_QSPI1_SCK	D9	I/O	Clock signal
X_CPU_QSPI1_IO0	F9	I/O	Bidirectional data signal
X_CPU_QSPI1_IO1	D8	I/O	
X_CPU_QSPI1_IO2	D7	I/O	
X_CPU_QSPI1_IO3	G8	I/O	
X_CPU_QSPI1_SS	F8	I/O	Chip Select

Note: When the corresponding function of the QSPI interface pin is not used, the pin needs to be pulled up.

## 8.11 I2C/SMI Interface

The I2C/MDIO interface pin description is shown in Table 8-14.

Table 8-14 I2C/MDIO interface pin description

Pin Name	Pin Number	Pin Type	Description Note

X_CPU_SDA C10		I/O	Master mode I2C interface, data signal, the I2C interface is directly controlled by the chip's built-in CPU Use
X_CPU_SCL	F10	I/O	Master mode I2C interface, clock signal, the I2C interface is directly controlled by the chip's built-in CPU Use
X_SCL	P5	I/O	<p>I2C and SMI interface multiplex pins, and the pin mode is configured by SMI_SEL. (See 8.15 for details.) Configuration Pins Chapter)</p> <p>In SMI mode, X_SCL is the SMI interface clock signal (MDC), and the chip internal CPU It is the SMI bus master node. In addition, there are 9 SMI slave nodes inside the chip. It includes 8 electrical port EPHYs and 1 switch chip itself. For details, see 8.15 Description of PHYADDR in the Configuration Pins section</p> <p>In I2C mode, X_SCL is the I2C slave interface clock signal (SCL), and the external controller The switch chip can be controlled through this set of I2C interfaces. The chip's built-in CPU cannot use this interface. Group I2C interface.</p>
X_SDA	N5	I/O	<p>I2C and SMI interface multiplex pins, and the pin mode is configured by SMI_SEL. (See 8.15 for details.) Configuration Pins Chapter)</p> <p>In SMI mode, X_SDA is the SMI interface clock signal (MDIO), and the chip internal CPU It is the SMI bus master node. In addition, there are 9 SMI slave nodes inside the chip. It includes 8 electrical port EPHYs and 1 switch chip itself. For details, see 8.15 Configuration Pins chapter for description of PHYADDR.</p> <p>In I2C mode, X_SDA is the I2C slave interface clock signal (SCL), and the external controller The switch chip can be controlled through this set of I2C interfaces. The chip's built-in CPU cannot use this interface. Group I2C interface.</p>

Note: When the corresponding function of the I2C/MDIO interface pin is not used, the pin can be left floating.

## 8.12 GPIO Interface

The GPIO interface pin description table is shown in Table 8-15.

Table 8-15 GPIO interface pin description

Pin Name	Pin	Pin Type	describe
X_GPIO0	number Multiplexed with	I/O	GPIO Signals
X_GPIO1	X_XMII1_RXD5 Multiplexed with	I/O	GPIO Signals
X_GPIO2	X_XMII1_TXCLK Multiplexed	I/O	GPIO Signals
X_GPIO3	with X_XMII0_TXD7 Multiplexed	I/O	GPIO Signals
X_GPIO4	with X_XMII0_CRS Multiplexed	I/O	GPIO Signals
X_GPIO5	with X_XMII0_TXD3 Multiplexed	I/O	GPIO Signals
X_GPIO6	with X_XMII0_GTCX Multiplexed	I/O	GPIO Signals
X_GPIO7	with X_XMII0_RXDV Multiplexed with X_XMII0_RXER	I/O	GPIO Signals
X_GPIO8	G22	I/O	GPIO Signals
X_GPIO9	G21	I/O	GPIO Signals
X_GPIO10	F23	I/O	GPIO Signals
X_GPIO11	F22	I/O	GPIO Signals
X_GPIO12	F21	I/O	GPIO Signals

X_GPIO13	E23	I/O	GPIO Signals
X_GPIO14	E22	I/O	GPIO Signals
X_GPIO15	E21	I/O	GPIO Signals
X_GPIO16	F19	I/O	GPIO Signals
X_GPIO17	F18	I/O	GPIO Signals
X_GPIO18	E19	I/O	GPIO Signals
X_GPIO19	E20	I/O	GPIO Signals
X_GPIO20	B19	I/O	GPIO Signals
X_GPIO21	A19	I/O	GPIO Signals
X_GPIO22	B14	I/O	GPIO Signals
X_GPIO23	A14	I/O	GPIO Signals

## 8.13 Other Pins

The description of other pins is shown in Table 8-16.

Table 8-16 Other pin descriptions

Pin Name	Pin Number	Pin Type Description	
X_MDIREF	Y13	I is used as a configuration pin and needs to be pulled up	
X_DFT_TEST1	Y14	I/O	
X_DFT_TEST2	W14	I/O	Internal DFT use, pull down to ground
X_CP_CTRL	W15	I/O configuration message enable signal, connect 1 to allow remote message configuration; connect 0 to prohibit	
X_CPU_NMI	H18	I External interrupt input, high effective; when not used, pull down to ground	
X_QSPI_32B_SEL	G18	I/O pull-down to ground	
X_QSPI_SPARE_SEL H17		I/O pull-down to ground	
X_DDR_200_SEL	G17	I/O	DDR control signals: 0 = internal icache is used as RAM, use JTAG to connect the chip to flash nor When flashing, the X_DDR_200_SEL pin needs to be pulled low; 1 = Enable icache. In this case, external DDR must be used as RAM. When running the Linux system, the X_DDR_200_SEL pin needs to be pulled high.
XMII_DELAY	C20	I/O test pin, pulled up to 3.3V.	

## 8.14 Power and Ground Pins

The power and ground pin descriptions are shown in Table 8-17.

Table 8-17 Power and ground pin description

Pin Name	Pin Number	Pin Type	describe
U_REFERENCE_PTP_CLK_ VCC3IO	B18	P	PTP Clock Power Supply

Pin Name	Pin Number	Pin Type	describe
U_REFERENCE_SERDES_CLK_VCC33IO	K19	P	SERDES Clock Power Supply
U_REFERENCE_SYS_CLK_VCC33IO	M7	AP	SYS clock power supply
VCC11A_GEPHY0	P6,R6,T6,U6,V6,W6,Y6	AP	GEPHY0 Power Supply
VCC11A_GEPHY1	M20,N19,P20,R19,T20	AP	GEPHY1 Power Supply
VCC11A_PLL_ADDR	Y16	AP	PLL1 Power Supply
VCC11A_SD1G0	Y11,AC11	AP	SD1G0 Power Supply
VCC11A_SD1G1	Y9,AC9	AP	SD1G1 Power Supply
VCC11A_SD1G2	W8,AC7	AP	SD1G2 Power Supply
VCC11A_SD1G3	AB5,AB6	AP	SD1G3 Power Supply
VCC11A_SDXG0	H7,H8	AP	SDXG0 Power Supply
VCC11A_SDXG1	H9,H10	AP	SDXG1 Power Supply
VCC11K	K13,K15,K17,L14,L16,M11,N8, N10,N17,P7,P9,P18,R8,R10,R17, T8,T13,T15,T18,U10,U12,U14, U16,V11,V17	AP	power supply
VCC11K_DDR	W17,AA13	AP	DDR Power Supply
VCC15O_DDR_DATACMR	W25,Y15,Y21,AA17,AA23,AB19, AB25,AC15,AC21,AD17,AD23, AE19,AE25,AF15,AF21	AP	power supply
VCC25A_SD1G0	W12	AP	SD1G0 Power Supply
VCC25A_SD1G1	W10	AP	SD1G1 Power Supply
VCC25A_SD1G2	U9	AP	SD1G2 Power Supply
VCC25A_SD1G3	V8	AP	SD1G3 Power Supply
VCC25A_SDXG0	J10,K11	AP	SDXG0 Power Supply
VCC25A_SDXG1	J12,J13	AP	SDXG1 Power Supply
VCC33A_GEPHY0	R4,R5,T4,U4,V4,W4,Y4,AA4, AB4,AC4	AP	GEPHY0 Power Supply
VCC33A_GEPHY1	J23,K23,L23,M23,N23,P23,R23, T23,U22,U23	AP	GEPHY1 Power Supply
VCC33IO	G16,G20,H19,J16,J18,L18,V13, V15	AP	Analog Power Supply
AVDD11_CDRPLL	K7,L7	AP	Analog Power Supply
AVDD11_PTPSD1GPLL	AA8	AP	Analog Power Supply
AVDD11_SDXGPLLS2D	L10	AP	Analog Power Supply
AVDD11_SYSPLL	M8	AP	Analog Power Supply
AVDD33_CDRPLL	K8	AP	Analog Power Supply
AVDD33_PTPSD1GPLL	AA7	AP	Analog Power Supply
AVDD33_SDXGPLL	L12	AP	Analog Power Supply
AVDD33_SYSPLL	L8	AP	Analog Power Supply
AVDD33_TDC	AB10	AP	Analog Power Supply
VDDQ_EFFUSE	AB9	AP	Pull down to ground

Pin Name	Pin Number	Pin Type	describe
AGND11_CDRPLL	J7	AG	CDRPLL Analog Ground
AGND11_PTPSD1GPLL	AA10	AG	PTPSD1GPLL analog ground
AGND11_SDXGPLL2D	L11	AG	SDXGPLL2D Analog ground
AGND11_SYSPLL	M10	AG	SYSPLL analog ground
AGND33_CDRPLL	J8	AG	CDRPLL Analog Ground
AGND33_PTPSD1GPLL	AA9	AG	PTPSD1GPLL analog ground
AGND33_SDXGPLL	L13	AG	SDXGPLL Analog Ground
AGND33_SYSPLL	L9,M9	AG	SYSPLL analog ground
AGND33_TDC	AB11	AG	TDC analog ground
GNDK	A16,A24,A25,A26,B16,B22,B24, C14,C15,C16,C17,C22,C24,D3, D24,E3,E7,E18,E24,F3,F24,G3, G5,G24,H3,H5,H24,J3,J24,K3, K14,K16,K24,L3,L15,L17,L22,L24 ,M3,M12,M13,M14,M15,M16,M17 ,M18,M21,M24,N3,N9,N11,N12,N 13,N14,N15,N16,N18,N20,N21, N24,P3,P8,P10,P11,P12,P13,P14 ,P15,P16,P17,P19,P21,P24,R3, R7, R9, R11, R12, R13, R14, R15, R16, R18, R20, R21, R24, T3, T7, T9, T10,T11,T12,T14,T16,T17,T19, T21,T24,U3,U7,U8,U11,U13,U15, U17,U18,U19,U20,U21,U24,V3, V7,V9,V10,V12,V14,V16,W3,W7, W9,¥7,AA5,AA6,AC5,AC6,AC8, AC10,AC12	G	Digitally
GNDGPIO	F20,G19,H11,H12,H16,H20,J9, J11,J14,J15,J17,K9,K10,K12,L19, W11,W13,Y8,Y10,Y12,AB8,AB12	AG	GPIO Ground
GND_DDR	V18, V19, V20, V21, V22, V23, V24, V25, V26, W16, W18, W20, W22, W23,Y17,Y18,Y24,AA14,AA20, AA26,AB13,AB14,AB16,AB22, AC13,AC18,AC24,AD14,AD20, AD26,AE14,AE16,AE22,AF18, AF24,AF26	AG	DDR Ground
GND11A_PLL_ADDR	AA16	AG	ADDR
GNDA_SD1G0	AD10,AD11,AD12,AD13,AE11, AE13,AF11,AF13	AG	SD1G0 Ground
GNDA_SD1G1	AD6,AD7,AD8,AD9,AE7,AE9, AF7,AF9	AG	SD1G1 Land
GNDA_SD1G2	AD1,AD2,AD3,AD4,AD5,AE1, AE3,AE5,AF1,AF3,AF5	AG	SD1G2 Ground
GNDA_SD1G3	Y1,Y2,Y3,AA3,AB1,AB2,AB3,AC3 AG		SD1G3 Ground
GNDA_SDXG0	A1,A3,B1,B3,B5,C1, C2,C3,C4,C5	AG	SDXG0 Ground

Pin Name	Pin Number	Pin Type	describe
GNDA_SDXG1	A7,A9,B7,B9,C6,C7,C8,C9	AG	SDXG1 Ground
U_REFERENCE_PTP_CLK_GNDIO	A18	AG	PTP clock ground
U_REFERENCE_SERDES_CLK_GND	K22	AG	SERDES clock ground
U_REFERENCE_SYS_CLK_GND	N6	AG	SYS clock ground

## 8.15 Configuration Pins

The configuration pin description table is shown in Table 8-18.

Table 8-18 Configuration Pin Description Notes

Pin Name	Pin number	configuration pin	describe
X_RECov_CLK0_AA11		GEPHY0_OFF	Electrical port 0~3 switch 0 = On 1=GEPHY0~3 off;
X_RECov_CLK0_VLD	AA12	GEPHY1_OFF	Electrical port 4~7 switch 0 = On 1=GEPHY4~7 off;
X_MDIREF	Y13	SWITCH_EN	Configure chip working mode 0=PHY mode 1=switch mode;
X_XMII0_TxD4	K6	SDXG0_EN0 configures	10G SerDes0 and the corresponding PCS working protocol and rate: 0 = Off; 1=QSGMII; 2=O-USGMII; 3 = 10G BASE-R; 4 = 1000BASE-X/SGMII
X_XMII0_TxD5	M5	SDXG0_EN1	
X_XMII0_TxD6	M4	SDXG0_EN2	
X_INTERRUPT	AB7	SDXG1_EN0 configures	10G SerDes1 and the corresponding PCS working protocol and speed Rate: 0 = Off; 1=QSGMII; 2=O-USGMII; 3 = 10G BASE-R; 4=1000BASE-X/SGMI
X_XMII0_CRS	D4	SDXG1_EN1	
X_XMII0_COL	D5	SDXG1_EN2	
X_CP_CTRL	W15	IMP_EN	Remote management interface switch When the remote management interface is enabled, the chip can be configured through the service port Internal registers. 0 = Off 1=Remote management interface is enabled;
X_XMII1_CRS	K21	SD1G_EN1 configures	4 1G SerDes and the corresponding PCS working protocol and speed rate; the four 1G SerDes modes remain consistent:
X_XMII1_COL	J21	SD1G_EN0 0=off;	

			1 or 2 = 1000BASE-X/SGMII
X_XMII1_TXD7	J22	PHYADDR_0 PHYADDR[4:0], determines when the chip acts as an MDIO slave device	When the slave controller is connected, the starting address of the internal slave controller (MDIO MMD) is set. There are 9 MDIO MMDs in the chip, including 8 GEPHY (real PHY) and the chip itself (pseudo PHY), each MDIO MMD occupies one address, 9 MDIO MMDs occupy the same address. Continuation of 9 addresses.
X_XMII1_TXD6	K18	PHYADDR_1	
X_XMII1_TXD5	K20	PHYADDR_2	
X_XMII1_TXD4	H23	PHYADDR_3	
X_XMII1_TXCLK	D20	PHYADDR_4	The starting address of these 9 MDIO MMDs is PHYADDR[4:0]. The PHY addresses of GEPHY[0:7] are PHYADDR[4:0]+5'd0/5'd1/5'd2/5'd3/5'd4/5'd5/5'd6/ 5'd7, the chip itself is PHYADDR[4:0]+5'd8
X_XMII1_TXD1	J20	XMII_MODE_0 XMII interface mode configuration, see Section 8.5 XMII interface pin connections for details.	
X_XMII1_RXD0	H21	XMII_MODE_1 connection mode.	
X_XMII0_TXCLK	J5	XMII_STATE0 XMII interface status configuration, see Section 8.5 XMII interface pin connection for details.	
X_XMII0_TXEN	H6	XMII_STATE1 connection mode.	
X_XMII1_RXEN	G23	XMII_SPEED	Speed configuration in MII mode: 0=100M; 1=10M
X_XMII0_RXD7	D6	CP_SPI_MODE1 SPI slave interface mode, only generated when the SPI slave interface is enabled.	effect: bit0 is CPHA bit1 is CPOL; Note: The SPI slave interface is used by the external controller to control the switch chip. The pins are J22, K18, K20, H23. For details, see Section 8.16 Description of related pin function 4.
X_XMII0_RXD6	E4	CP_SPI_MODE0	
X_XMII0_RXD4	E6	MANAGE_MODE	Management mode switch 0 = Disable management mode 1 = Enable management mode
X_XMII0_TXD1	K4	DIS_CPU	Internal CPU enable switch 0=Enable CPU function; 1 = Turn off the CPU and related SOC interface circuits; at this time, the chip passes Controlled by external CPU
X_LED_CLK	L6	SMI_SEL	I2C/MDIO interface selection: 0=I2C slave interface; 1=MDIO interface.
X_RECov_CLK1	B11	CP_I2CA0	I2C slave address selection, 7-bit address when the chip is used as an I2C slave
X_RECov_CLK1_VLD	A10	CP_I2CA1	Bits {5'b10111, CP_I2CA1, CP_I2CA0}

Note: For detailed description of the use of configuration pins, see 8.16 Multiplexed Pin Function 1.

## 8.16 Multiplexing Pins

The pin multiplexing description table is shown in Table 8-19.

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Wuhan Feisiling Microelectronics Technology Co., Ltd.

Before power-on, the value of pin function 1 is determined by the pull-up and pull-down on the board. After power-on, during the reset phase, the value of pin function 1 is passed to The chip is internal, so that the corresponding function or mode takes effect; after the reset phase is over, the chip will release pin function 1, and then, according to different configurations In this case, the pin is controlled by other functions 2/3/4.

After the chip is powered on and reset, other functions (function 2/3/4) take effect. The specific function is selected through configuration.

If there is only one function besides function 1, after reset, the pin will work according to this function by default (for X\_XMII\* series pins,

The corresponding conditions need to be configured in advance, please refer to 8.5).

Table 8-19 Pin multiplexing description table

Pin Name	Pin Number	Feature 1	Feature 2	Feature 3	Feature 4	Configuration choose relation
X_RECV_CLK0	AA11	GEPHY0_OFF	RECOV_CLK0	-	-	-
X_RECV_CLK0_VLD AA12		GEPHY1_OFF_RECV_CLK0_VLD		-	-	-
X_INTERRUPT	AB7	SDXG1_EN0	INTERRUPT	-	-	-
X_XMII1_CRS	K21	SD1G_EN1	XMII1_CRS	-	-	-
X_XMII1_COL	J21	SD1G_EN0	XMII1_COL	-	-	-
X_XMII1_TXD7	J22	PHYADDR_0	XMII1_TXD7	P7LED2	SPI_CLK Note 1	
X_XMII1_TXD6	K18	PHYADDR_1	XMII1_TXD6	P7LED1	SPI_IO0 (MOSI)	Note 1
X_XMII1_TXD5	K20	PHYADDR_2	XMII1_TXD5	P7LED0	SPI_IO1 (MISO)	Note 1
X_XMII1_TXD4	H23	PHYADDR_3	XMII1_TXD4	P6LED2	SPI_CS Note 1	
X_XMII1_TXD3	H22	LED_MODE_0	XMII1_TXD3	-	-	-
X_XMII1_TXD2	J19	LED_MODE_1	XMII1_TXD2	-	-	-
X_XMII1_TXD1	J20	XMII_MODE_0	XMII1_TXD1	-	-	-
X_XMII1_TXD0	H21	XMII_MODE_1	XMII1_TXD0	-	-	-
X_XMII1_TXEN	G23	XMII_SPEED	XMII1_TXEN			-
X_XMII1_TXCLK	D20	PHYADDR_4	-	P6LED0	GPIO1 Note 2	
X_XMII1_TXER	C20	XMII_DELAY	XMII1_TXER	-	-	-
X_XMII0_CRS	D4	SDXG1_EN1	XMII0_CRS	P4LED2	GPIO3 Note 3	
X_XMII0_COL	D5	SDXG1_EN2	XMII0_COL	P4LED0	-	Note 3
X_XMII0_RXD7	D6	CP_SPI_MODE1	XMII0_RXD7	P4LED1	-	Note 4
X_XMII0_RXD6	E4	CP_SPI_MODE0	XMII0_RXD6	P3LED1	-	Note 4
X_XMII0_RXD5	E5	-	XMII0_RXD5	P3LED2	-	Note 4
X_XMII0_RXD4	E6	MANAGE_MODE	XMII0_RXD4	P3LED0	-	Note 4
X_XMII0_TXER	G7	E2PROM_MODE	XMII0_TXER	P2LED0	-	Note 5
X_XMII0_TXCLK	J5	XMII_STATE0	-	P2LED1	-	Note 2
X_XMII0_TXEN	H6	XMII_STATE1	XMII0_TXEN	-	-	-
X_XMII0_TXD0	J6	EN_FLASH	XMII0_TXD0	-	-	-
X_XMII0_TXD1	K4	DIS_CPU	XMII0_TXD1	-	-	-
X_XMII0_TXD2	K5	DISAUTOLOAD	XMII0_TXD2	-	-	-

Pin Name	Pin Number	Feature 1	Feature 2	Feature 3	Feature 4	Configuration choose relation
X_XMII0_TXD3	L5	-	XMII0_TXD3	-	GPIO4 Note 5	
X_XMII0_TXD4	K6	SDXG0_EN0	XMII0_TXD4	P1LED2	-	Note 6
X_XMII0_TXD5	M5	SDXG0_EN1	XMII0_TXD5	P1LED0	-	Note 6
X_XMII0_TXD6	M4	SDXG0_EN2	XMII0_TXD6	P1LED1	-	Note 6
X_XMII0_TXD7	L4	-	XMII0_TXD7	P0LED2	GPIO2 Note 6	
X_LED_DA	M6	LED_MODE_2	LED_DA	P0LED1	-	Note 7
X_LED_CLK	L6	SMI_SEL	LED_CLK	P0LED0	-	Note 7
X_RECov_CLK1	B11	CP_I2CA0	RECov_CLK1	-	-	-
X_RECov_CLK1_VLD A10		CP_I2CA1	RECov_CLK1_VLD	-	-	-
X_XMII1_RXD4	D23	-	XMII1_RXD4	P6LED1	-	Note 8
X_XMII1_RXD5	A21	-	XMII1_RXD5	P5LED2	GPIO0 Note 8	
X_XMII1_RXD6	B21	-	XMII1_RXD6	P5LED0	-	Note 8
X_XMII1_RXD7	A20	-	XMII1_RXD7	P5LED1	-	Note 8
X_XMII0_RXDV	J4	-	XMII0_RXDV	-	GPIO6 Note 5	
X_XMII0_RXER	G6	-	XMII0_RXER	P2LED2	GPIO7 Note 5	
X_XMII0_GTXC	H4	-	XMII0_GTXC		GPIO5 Note 5	
X_SCL	P5	-	SCL	MMD_MDC	-	Note 9
X_SDA	N5	-	SDA	MMD_MDIO	-	Note 9

Note 1: Function 2 is RGMII/GMII/MII interface, function 3 is parallel LED, function 4 is SPI slave interface.

- When XMII\_STATE is 2'b01 or 2'b10 and XMII\_MODE is 2'b01, function 2 is enabled. That is, the XMII interface is required to be used as a GMII. It should be noted that when XMII\_STATE is 2'b01, only one GMII port is supported. At this time, if XMII\_MODE is 2'b01 (GMII), Only the X\_XMII0\_\* pins will be used for the GMII interface, and the X\_XMII1\_\* pins will not be used. However, the pins are still occupied by function 2 and can be released through configuration registers.
- Function 3 requires the configuration register ReuseInd (located in work\_mode\_cfg of top\_cfg\_reg). When this register is set to 1, it is enabled. Function 3; when the value is 0, function 4 is enabled; the default value is 0.
- When condition 1 is not met and ReuseInd is 0 (default), enable function 4 and use it as a Spi slave interface.

Note 2: Function 3 is parallel LED, and function 4 is GPIO interface.

- Same as the description in Note 1.2. If the pin supports multiplexing of function 3 and function 4, the multiplexing condition is selected by configuring the register ReuseInd. If there is only function 3 or function 4, it will automatically work according to the corresponding function after the reset is completed.
- It should be noted that if you need to enable the parallel LED function, you need to enable all 24 LED pins. The necessary configuration is: XMII\_STATE The pin is configured as 2'b00 and the register ReuseInd is configured as 1'b1.

Note 3: Function 2 is the RGMII/GMII/MII interface, function 3 is the parallel LED, and function 4 is the GPIO interface.

- When XMII\_STATE is 2'b01 or 2'b10 and XMII\_MODE is 2'b10 (MII MAC) or 2'b11 (MII PHY), function 2 is enabled. Used when the XMII interface is required for MII mode.

2. When condition 1 is not effective, function 3 or function 4 is enabled, and the selection is the same as note 2.

Note 4: Function 2 is RGMII/GMII/MII interface, Function 3 is parallel LED.

1. When XMII\_STATE is 2'b01, or XMII\_STATE is 2'b10 and XMII\_MODE is 2'b01 (GMII), function 2 is enabled. This multiplexing is described in 8.5.

2. The activation of function 3 is the same as Note 2.

Note 5: Function 2 is the RGMII/GMII/MII interface, Function 3 is the parallel LED, Function 4 is the GPIO interface.

1. Function 2 is enabled in the required application scenario configuration. For details on the selection of XMII\_STATE pin and XMII\_MODE pin, refer to 8.5. For example XMII0\_TXER is enabled when the X\_XMII0\* series pins are used as GMII or MII. At this time, XMII\_STATE is 2'b01 or 2'b10, and XMII\_MODE is 2'b01/2'b10/2'b11.

2. When condition 1 is not effective, function 3 or function 4 is enabled, and the selection is the same as note 2.

Note 6: Function 2 is the RGMII/GMII/MII interface, Function 3 is the parallel LED, Function 4 is the GPIO interface.

1. When XMII\_STATE is 2'b01, or XMII\_STATE is 2'b10 and XMII\_MODE is 2'b01 (GMII), function 2 is enabled. This multiplexing behavior is detailed in 8.5.

2. When condition 1 is not effective, function 3 or function 4 is enabled, and the selection is the same as note 2.

Note 7: Function 2 is the serial LED interface, and function 3 is the parallel LED.

1. As described in Note 2, when the register ReuseInd is 1'b1, function 3 is enabled and the pin works as a parallel LED.

2. When the register ReuseInd is 1'b0, function 2 is enabled and the pin works as a serial LED.

Note 8: Function 2 is the RGMII/GMII/MII interface, Function 3 is the parallel LED, Function 4 is the GPIO interface.

1. The enabling conditions of function 2 are the same as those described in Note 1.1.

2. When condition 1 is not effective, function 3 or function 4 is enabled, and the selection is the same as C2.

Note 9: Function 2 is the I2C slave interface, and function 3 is the MDIO slave interface.

1. When the configuration pin SMI\_SEL is 1'b0, function 2 is enabled and the pin works as an I2C slave interface.

2. When the configuration pin SMI\_SEL is 1'b1, function 3 is enabled and the pin works as an MDIO slave interface.

## 9 Register Description

For register description, please refer to "FSL91030M Register Description".

## 10 Interface Timing

### 10.1 Timing diagram legend

The timing diagram is shown in Figure 10-1.

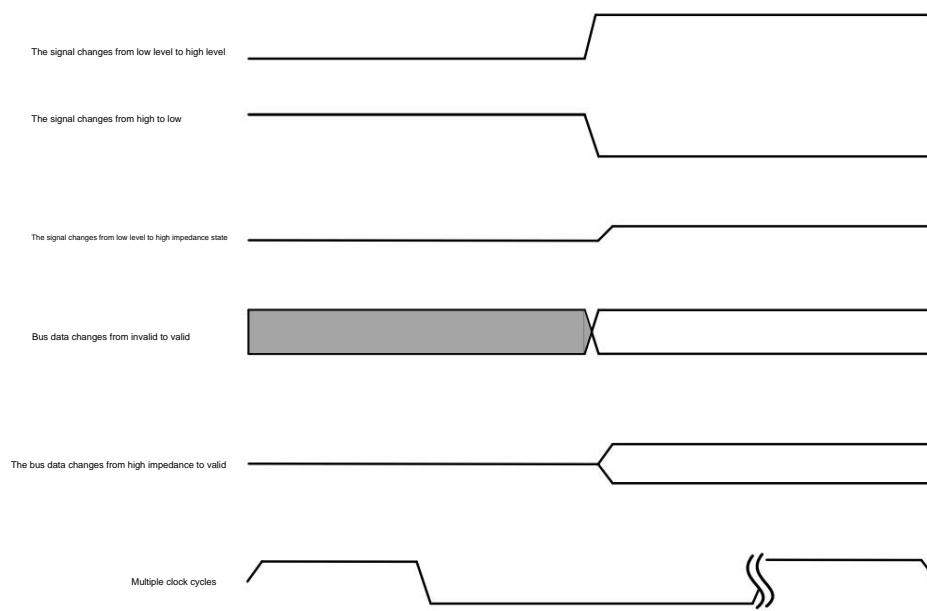


Figure 10-1 Timing diagram

## 10.2 DDR3 Interface

### 10.2.1 Write Operation Timing

#### 10.2.1.1 dqs\_out write timing relative to dq\_out

The main timing parameters of the write operation timing of dqs\_out relative to dq\_out are tDS and tDH. The timing diagram is shown in Figure 10-2.

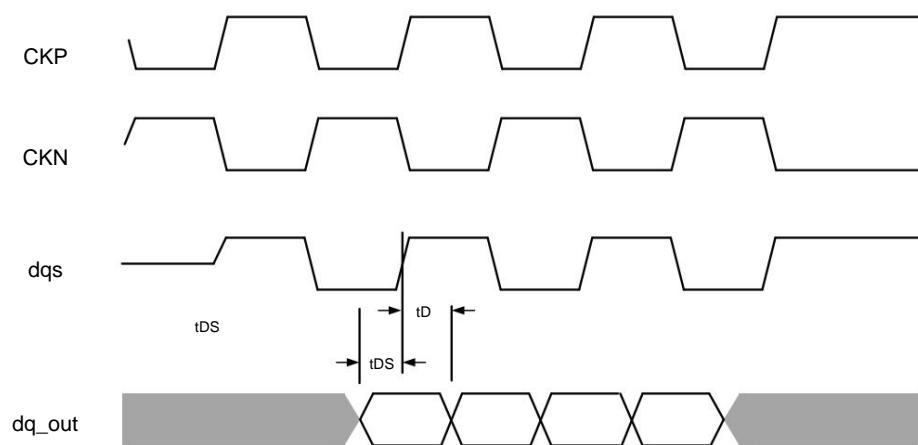


Figure 10-2 DDR3 write operation timing diagram of dqs\_out relative to dq\_out

#### 10.2.1.2 dqs\_out write operation timing relative to ck

The timing diagram of the write operation of dqs\_out relative to ck is shown in Figure 10-3.

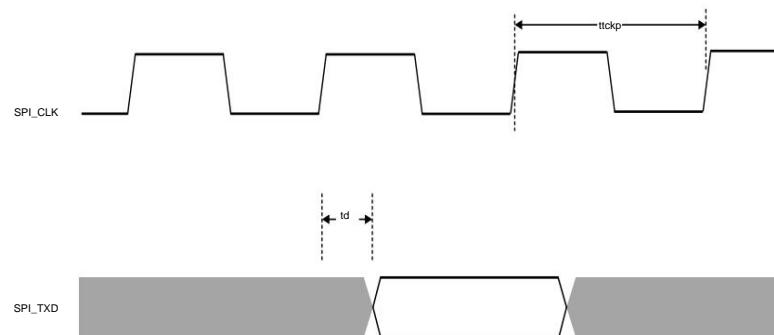


Figure 10-3 DDR3 dqs\_out write operation timing diagram relative to ck

#### 10.2.1.3 Timing of command and address write operations relative to ck

The command and address write operation timing relative to ck is shown in Figure 10-4.

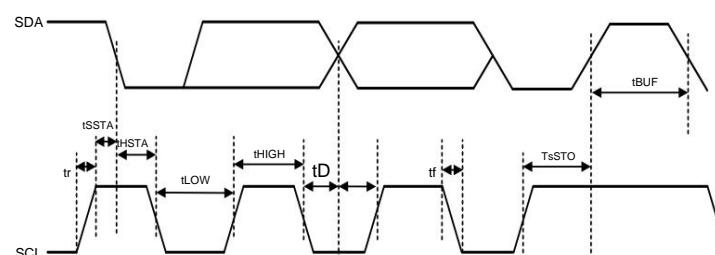


Figure 10-4 Command and address write operation timing diagram relative to ck

## 10.2.2 Read Operation Timing

### 10.2.2.1 Timing of command and address read operation relative to **ck**

The "read operation timing of commands and addresses relative to ck" is the same as the "write operation timing of commands and addresses relative to ck".

### 10.2.2.2 Read Operation Timing of dqs\_in Relative to **dq\_in**

The read operation timing of dqs\_in relative to dq\_in is divided into the DDR3 SDRAM output timing and the DDRPHY end dqs\_in and dq\_in timing.

For DDR SDRAM output timing, ideally, dqs and ck are in phase. In practice, dqs is out of phase with ck.

tDQSK is the skew of the dq signal. tDQSQ is the jitter between dq and dqs, which is the jitter of the latest valid dq relative to dqs. tQH is the read operation. The holding time of dq relative to dqs.

The DDR3 SDRAM output timing is shown in Figure 10-5.

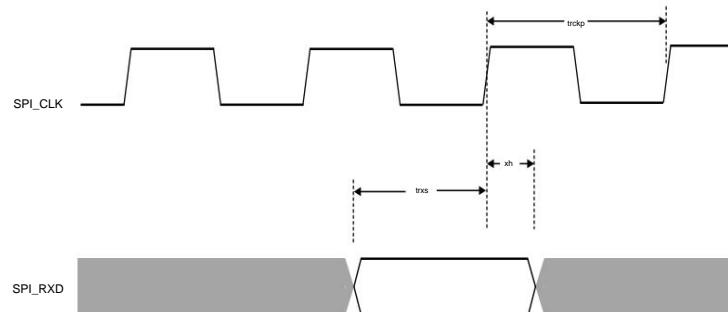


Figure 10-5 DDR3 SDRAM output timing diagram

## 10.2.3 Timing Parameters

The DDR interface timing complies with the JEDEC (JESD79-3E) standard protocol. The timing described in this article is the timing output by the DDR PHY side. The DDR3 SDRAM clock parameters are shown in Table 10-1 and Table 10-2.

Table 10-1 DDR3 clock parameter table

parameter	Minimum	Typical	Maximum	unit
Clock Frequency	-	value 800	-	MHz
Clock Period Jitter	-0.070	-	0.070	ns
Average high/low pulse width	47.000	-	53.000	%
Cycle to Cycle Period Jitter	-	-	0.140	ns

Table 10-2 DDR3 SDRAM clock parameter table

parameter	describe	Minimum	Maximum	Unit
tDSS	DQS falling edge setup time relative to DDR clock	0.180	-	tCK
dD	DQS falling edge hold time relative to DDR clock	0.180	-	tCK

tDS	Write operation DQ/DM setup time relative to DQS	0.100	-	ns
tD	Write operation DQ/DM hold time relative to DQS	0.110	-	ns
QDQ	DQS and DQ skew	-	0.100	ns
tl	Address and command setup time relative to DDR	0.300	-	ns
i	clock Address and command hold time relative to DDR clock	0.230	-	ns
tDQSCK	DQS output skew relative to DDR clock	-0.225	0.225	ns
	DQ output hold time relative to DQS	0.38	-	tCK

## 10.3 SPI Interface

The SPI interface only supports master mode. In addition to SPI\_CLK/SPI\_RXD/SPI\_TXD, there is also a chip select signal.

### 10.3.1 Receiving direction

The SPI interface input timing is shown in Figure 10-6.

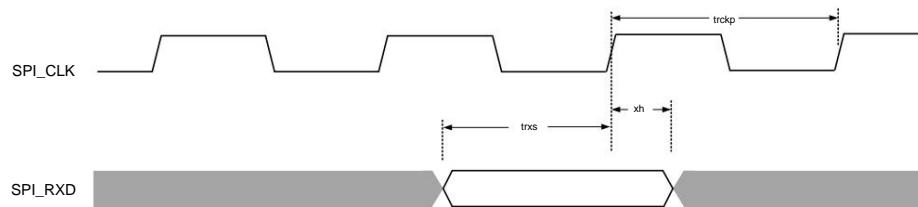


Figure 10-6 SPI interface input timing diagram

The SPI interface input timing parameters are shown in Table 10-3.

Table 10-3 SPI interface input timing parameters

Parameter Description	Min	Typ	Max	Unit			Register Configuration
txs Receive data setup time	7	txh	-	-	ns		-
Receive data hold time	2	trckp	-	-	ns		-
Receive clock cycle	-	-	40	-	ns		-

### 10.3.2 Sending direction

The SPI interface output timing is shown in Figure 10-7.

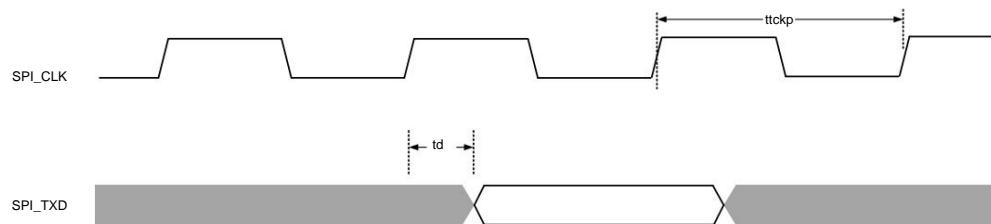


Figure 10-7 SPI interface output timing diagram

The SPI interface output timing parameters are shown in Table 10-4.

Table 10-4 SPI interface output timing parameters

parameter		Min	Typ	Max	Unit			Register Configuration
txd	Description	0	-	10	ns			-
Output delay ttckp	Send clock cycle	-	45	-	ns			-

## 10.4 I2C Interface

The timing relationship between SDA and SCL is shown in Figure 10-8.

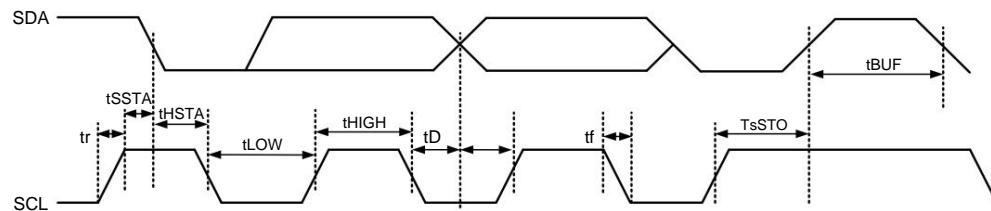


Figure 10-8 I2C interface timing diagram

The timing parameters in standard mode are shown in Table 10-5.

Table 10-5 Timing parameters in standard mode

parameter		Min	Typ	Max	Unit	Register Configuration		
Description	tSSTA Start and repeat start condition setup time	4.7	-	-	ns		-	
tHSTA	Start and repeat start condition hold time	4.0	tLOW SCL low	-	-	ns		-
time 4.7	SCL high time Data setup time	4.7	Data hold time	-	ns		-	
tHIGH	setup time Bus free	4.7	-	-	ns		-	
tD	time between	250	-	-	ns		-	
HkDJ	stop and start 4.7	0	-	3.45	ns		-	
TsSTO	SCL and SDA signal	4.0	-	-	ns		-	
tBUF	rise time SCL and SDA signal fall time	-	-	-	ns		-	
tr		-	-	1000	ns		-	
tf		-	-	300	ns		-	

The parameters in fast mode are shown in Table 10-6.

Table 10-6 Timing parameters in fast mode

Parameter	Description	Min	Typ	Max	Unit	Register Configuration		
tSSTA	start and repeat start condition setup time	0.6	tHSTA	start and repeat start condition hold time	-	-	ns	-
tLOW	SCL low level time	1.3	-	-	-	-	ns	-
							ns	-

tHIGH	SCL high time Data	0.6	-	-	ÿs	-
tD	setup time Data	100	-	-	ns	-
HkJD	hold time Stop	0	-	0.9	ÿs	-
TsSTO	condition setup time	0.6	-	-	ÿs	-
tBUF	Bus free time between stop and start 1.3 SCL and SDA		-	-	ÿs	-
tr	signal rise time 20 SCL and SDA signal fall time		-	300	ns	-
tf		20	-	300	ns	-

The parameters in high-speed mode are shown in Table 10-7.

Table 10-7 Timing parameters in high-speed mode

Parameter	Description	tSSTA start	Min	Typ	Max	Unit	Register	Configuration
and repeat	start condition setup time	160	tHSTA start and repeat		-	-	ns	-
start condition	hold time	160	tLOW		-	-	ns	-
	SCL low level time	160			-	-	ns	-
tHIGH	SCL high level time	60		-	-	-	ns	-
tD	Data setup time	10		-	-	-	ns	-
HkJD	Data hold time	0		-	70	-	ns	-
TsSTO	Stop condition setup time	160		-	-	-	ns	-
tr	SCL and SDA signal rise time	10		-	300	-	ns	-
tf	SCL and SDA signal fall time	10		-	300	-	ns	-

## 10.5 JTAG Interface

The JTAG interface timing diagram is shown in Figure 10-9.

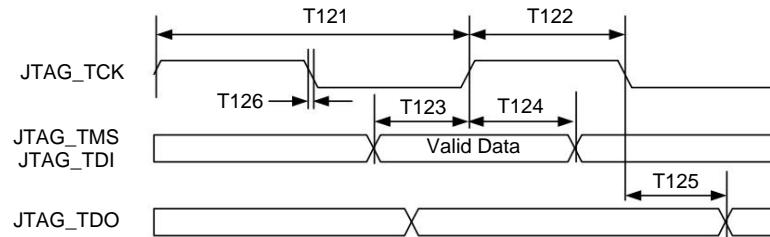


Figure 10-9 JTAG timing diagram

The JTAG interface timing parameters are shown in Table 10-8.

Table 10-8 JTAG interface timing parameters

parameter	describe	Min	Typ	Max	Unit	Register	Configuration
T121	JTAG_TCK cycles 100		-	-	-	ns	-
T122	JTAG_TCK high (or low) time 40		-	-	-	ns	-
T123	JTAG_TMS and JTAG_TDI setup time 20		-	-	-	ns	-

T124 JTAG_TMS and JTAG_TDI hold time 10		-	-	ns	-
T125 Falling edge from JTAG_TCK to JTAG_TDO 0		-	20	ns	-
T126 JTAG_TCK signal rise/fall time -		-	3	ns	-

## 10.6 UART Interface

The timing relationship between the UART interface input and output data and the clock pclk is shown in Figure 10-10.



Figure 10-10 UART interface timing diagram

The UART interface timing parameters are shown in Table 10-9.

Table 10-9 UART interface timing parameters

	describe	Min	Typ	Max	Unit	Register	Configuration
Parameter tbit	1bit time (start bit transmission time) 5333 data bit			104166	ns		-
td	transmission time	26665		833328	ns		-
tp	check bit transmission	5333		104166	ns		-
tstop	time stop bit transmission time	5333		208332	ns		-

## 10.7 MDIO Interface

The MDIO interface timing is shown in Figure 10-11.

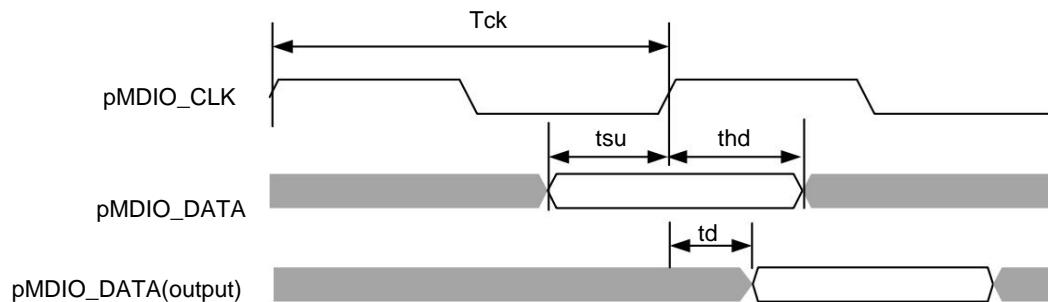


Figure 10-11 MDIO interface timing diagram

The MDIO interface timing parameters are shown in Table 10-10.

Table 10-10 MDIO interface timing parameters

Parameter Description	Min	Typ	Max	Unit	Register	Configuration
tsu Data input setup time 20		-	-	ns		-

thd	data input hold time 10 tdd	data	-	-	ns	-
output	delay time 0		-	10	ns	-
Tck	Clock cycle	-	96	-	ns	MDIO 10M mode: MDIO_CTRL0[1:0]=0b11
		-	200	-	ns	MDIO 5M mode: MDIO_CTRL0[1:0]=0b10
		-	800	-	ns	MDIO 1.25M mode: MDIO_CTRL0[1:0]=0b01
		-	400	-	ns	MDIO 2.5M mode: MDIO_CTRL0[1:0]=0b00

**11 Electrical Characteristics****11.1 Limit range**

Table 11-1 Extreme operating voltage range

Parameter	describe	Minimum	Maximum	unit
VCC15O_DDR_DATACMR VCC15O_DDRCK_ADDR	DDR IO 1V5 Power Supply	-0.3	1.65	V
AVDD11_CDRPLL AVDD11_PTPSD1GPLL AVDD11_SDXGPLLS2D AVDD11_SYSPLL	PLL 1V1 Power Supply	-0.3	1.155	V
AVDD11_SYSPLL AVDD33_CDRPLL AVDD33_PTPSD1GPLL AVDD33_SDXGPLL AVDD33_SYSPLL	PLL 3V3 power supply	-0.3	3.63	V
VCC33IO_0 VCC33IO_1	Digital IO Power Supply	-0.3	3.63	V
VCC25A_SD1G0 VCC25A_SD1G1 VCC25A_SD1G3 VCC25A_SDXG0 VCC25A_SDXG1	SerDes 2V5 power supply	-0.3	2.75	V
VCC11A_SD1G0 VCC11A_SD1G1 VCC11A_SD1G2 VCC11A_SD1G3 VCC11A_SDXG0 VCC11A_SDXG1	SerDes 1V1 Power Supply	-0.3	1.155	V
VCC11A_GEPHY0 VCC11A_GEPHY1 VCC11A_PLL_ADDR	GE PHY 1V1 Power Supply	-0.3	1.21	V
VCC33A_GEPHY0 VCC33A_GEPHY1 CORE	GE PHY 3V3 Power Supply	-0.3	3.63	V
Exceeding the limit range listed in Digital power supply VCC11K, VCC11K_CORE Note:		-0.3	1.155	V
may cause damage to the device. Long-term operation within the maximum rating range may affect the performance of the device.				

**11.2 Recommended scope of work**

Table 11-2 Recommended working range

parameter	describe	Min	Typ	Max	Unit		
VCC15O_DDR_DATACMR VCC15O_DDRCK_ADDR	DDR IO 1V5 Power Supply	1.425		1.5		1.575	V

	describe	Min	Typ	Max	Unit		
Parameters AVDD11_CDRPLL AVDD11_PTPSD1GPLL AVDD11_SDXGPLL2D AVDD11_SYSPLL	PLL 1V1 Power Supply	1.045		1.1	1.155	V	
AVDD11_SYSPLL AVDD33_CDRPLL AVDD33_PTPSD1GPLL AVDD33_SDXGPLL AVDD33_SYSPLL	PLL 3V3 power supply	3.135		3.3	3.465	V	
VCC33IO_0 VCC33IO_1	Digital IO Power Supply	3.135		3.3	3.465	V	
VCC25A_SD1G0 VCC25A_SD1G1 VCC25A_SD1G3 VCC25A_SDXG0 VCC25A_SDXG1	SerDes 2V5 power supply	2.375		2.5	2.625	V	
VCC11A_SD1G0 VCC11A_SD1G1 VCC11A_SD1G2 VCC11A_SD1G3	1G SerDes 1V1 Power	1.045		1.1	1.155	V	
VCC11A_SDXG0 VCC11A_SDXG1	10G SerDes 1V1 power supply	Note 1.045		1.1	1.155	V	
VCC11A_GEPHY0 VCC11A_GEPHY1 VCC11A_PLL_ADDR	GE PHY 1V1 Power Supply		1.045		1.1	1.155	V
VCC33A_GEPHY0 VCC33A_GEPHY1 VCC11K_CORE	GE PHY 3V3 Power Supply	3.135		3.3	3.465	V	
VCC11K_CORE	Digital power supply	1.045		1.1	1.155	V	

supply requirement is 1.15V; in other modes, please refer to the table above.

## 11.3 Oscillator

The chip's requirements for 25MHz single-ended clock and crystal oscillator are shown in Table 11-3 and

As shown in Table 11-4.

Table 11-3 25MHz single-ended crystal oscillator requirements

	Minimum	Typical Value	Maximum	unit
	-	25	-	MHz
Parameter	-50	-	+50	ppm
Frequency Frequency	-	-	6	ps
Stability Rise/Fall	-	-	25	ps
Time Jitter (Short Term) Jitter	-	-	200	ps
(Long Term) Load Capacitance Symmetry	15	-	40	pF
	40	-	60	%

Table 11-4 25MHz crystal oscillator requirements

Parameter	Minimum	Typical	Maximum	unit
Frequency	-	value 25	-	MHz
Frequency Stability	-50	-	+50	ppm
Frequency	-50	-	+50	ppm
Tolerance Load Capacitance	15	Neenly four	40	pF

#### 11.4 Thermal Characteristics

##### PCB Assembly Instructions

type	Size (Quantity)	unit
PCB Layers	4	layer
PCB size	101.22x114.5x1.564	mm
L1 layer thickness (40% Cu)	0.07	mm
FR4 12 Thickness	0.463	mm
L2 layer thickness (95% Cu)	0.035	mm
FR4 23 Thickness	0.463	mm
L4 layer thickness (40% Cu)	0.035	mm
FR4 34 Thickness	0.463	mm
L4 layer thickness (40% Cu)	0.035	mm

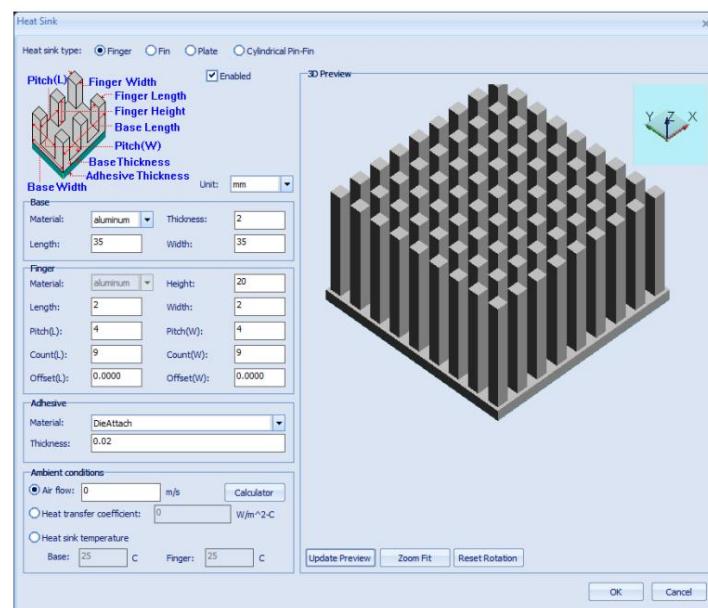
##### Material properties

Type	Material:	Thermal conductivity (W/m·K)
	Substrate,	0.8
	Tin Ball,	46
Substrate Solder Ball Chip	Silicon	148
PCB	FR4	0.35

##### Simulation conditions

Input Power	10.4W
Test Board (PCB)	4L (2S2P)
Control Conditions	Air Flow = 0 m/s

Thermal performance of **BGA676** with heat sink on **PCB** under still air convection , heat sink recommendation:



	$\bar{J}_{JA}$		$\bar{J}_{JC}$
4L PCB	6.214	$\bar{J}_{JB}$ 3.512	4.087

Note:  $\bar{J}$  $\bar{J}_{JA}$ : thermal resistance from junction to ambient  $\bar{J}$  $\bar{J}_{JB}$ : thermal resistance from junction to board  $\bar{J}$  $\bar{J}_{JC}$ : thermal resistance from junction to case

## 11.5 DDR3 Characteristics

Table 11-5 DDR3 power supply characteristics

Parameter	Description	Min.	Typ.	Max.	Unit
VCC1 1K	1.1-V digital power supply	0.99	1.1	1.21	V
VCC15O_DDR DDR	I/O power supply DDR I/O	1.425	1.5	1.575	V
VCC15O_DDRCK	power supply for CK/CKB	1.425	1.5	1.575	V
VREF	Reference voltage of VREF for receivers	0.49 <sup>*</sup> VCC15O_DDR	0.50 <sup>*</sup> VCC15O_DDR	0.51 <sup>*</sup> VCC15O_DDR	V
VIH (dc)	DC input logic high	VREF + 0.10	-	VCC15O_DDR	V
VIL(dc)	DC input logic low	0	-	VREF - 0.10	V
VIH (ac)	AC input logic high	VREF + 0.15	-	VCC15O_DDR + 0.4	V
VIL(ac)	AC input logic low	-0.4	-	VREF - 0.15	V

## 11.6 SerDes (SGMII) Features

Each SerDes interface of the chip uses the same set of IP, and the electrical performance of the interface is consistent.

Table 11-6 Transmitter interface electrical parameters

Parameter	Description	Min	Typical	Max	Unit
<b>Output Eye Specification</b>					
VTX-DIFF-PKPK	Backporch Transmit Amplitude Transmit	400		1400	mVdiff-pkpk
VTX-EYE-PKPK	Eye Voltage Opening N+1 precursor	400		1200	mVdiff-pkpk
DTX-N+1-DEEMP	Tap De-Emphasis N-1 postcursor Tap De-	0		5.0	dB
DTX-N-1-DEEMP	Emphasis N-2 postcursor Tap De-Emphasis	0		8.5	dB
DTX-N-2-DEEMP	Rise/Fall Time Transmit Dependant Jitter	0		2.0	dB
TTX-SLEW	(Inter-Symbol	30		120	ps
TTX-DDJ	Interference) at 8Gbps. Includes package model Transmit Periodic Jitter. Assumes a 1st order high pass jitter			0.05	Ulpkpk
TTX-PJ	measurement filter with a cutoff of  FBAUD/ FGPLL = NGPLL			0.05	Ulpkpk
TTX-RJ	Transmit Total Peak-Peak Random Jitter (assumes 14 $\sqrt{2}$ TXRJ-RMS). Assumes a 1st order high pass jitter measurement filter with a cutoff of  FBAUD/ FGPLL = NGPLL			0.15	Ulpkpk
TTX-TJ	Transmit Total Peak-Peak Jitter (Assumes TTX-TJ = TTX-DDJ + TTX-PJ + TTX-RJ). Assumes a 1st order high pass jitter measurement filter with a cutoff of  FBAUD/ FGPLL = NGPLL			0.25	Ulpkpk
NGPLL	F3dB cutoff frequency for the 1st Order High-Pass Jitter Measurement Filter. Defined as the ratio of the F3DB cutoff frequency, to the data rate		1667		FBAUD/ FGPLL
VTX-CM-PKPK-AC	Pk-PK AC Common Mode Voltage Variation at PCIe Gen2/Gen3 rate RMS AC			100	mV
VTX-CM-RMS-AC	Common Mode Voltage Variation at PCIe Gen1 rate			20	mV
<b>Transmitter DC Impedance</b>					
ZTX-DIFF-DC	Transmitter Output Differential DC Impedance	80	100	120	$\ddot{\gamma}$
ZTX-CM-DC	Transmitter Output Common-Mode DC Impedance 20		25	30	$\ddot{\gamma}$
ZTX-DIFF-HIZ	Transmitter Output Differential DC Impedance in Squelch Mode			>2k	$\ddot{\gamma}$
ZTX-CM-HIZ	Transmitter Output Common-Mode DC Impedance in Squelch Mode			>500	$\ddot{\gamma}$
<b>Transmitter Return Loss</b>					
ZRL-DIFF-DC	Transmitter Differential DC Return Loss			-20	dB
ZRL-DIFF-NYQ	Transmitter Differential Return Loss at 5GHz			-4	dB
ZRL-CM-DC	Transmitter Common-Mode DC Return Loss			-10	dB
ZRL-CM-NYQ	Transmitter Common-Mode Return Loss at 5GHz			-5	dB
<b>Electrical Idle</b>					
VTX-IDLE	Idle Output Voltage			20	mxD
VCM-DELTA-SQU	ELCH Maximum Common-Mode Step Entering/Exiting			50	mV

Parameter	Description	Min	Typical	Max	Unit
	Squelch Mode				
TTX-IDLE-LATENCY	Latency Entering/Exiting Idle			8	ns
	<b>Receiver Detect</b>				
VTX-RCV-DETECT	Voltage change allowed during receiver detection			600	mV

Table 11-7 Receiver interface electrical parameters

Parameter	Description	Min	Typical	Max	Unit
<b>Receiver Input Eye Specification</b>					
VRX-DIFF-PKPK	Receiver Input Differential Peak-Peak Voltage Closed eye			2000	mVdiff-pkpk
VRX-CM-DC	Receiver Input DC Common Mode Voltage		0		mVdiff-pkpk
VRX-CM-AC	Receiver Input AC Common Mode Voltage	-150		150	mVdiff-pkpk
VRX-SENS	Receiver Input Voltage Sensitivity Under the Following Conditions: 8.0Gbps 10G-Base KR channel (app 28dB of insertion loss at 5GHz) PRBS31 input data pattern	30			mVdiff-pkpk
TRX-DDJ	Receive Input Signal Data Dependant Jitter (Inter-Symbol Interference).			1	Ulpkpk
TRX-RJ	Receive Input Random Jitter			0.3	Ulpkpk
TRX-PJ	Receive Input Period Jitter (at high frequency)			0.1	Ulpkpk
TRX-TJ	Receive Input Total Jitter (DDJ + RJ + PJ).			1	Ulpkpk
NGPLL	F3dB cutoff frequency for the 1st Order High-Pass Jitter Measurement Filter. Defined as the ratio of the F3DB cutoff frequency, to the data rate		1667		FBAUD/ FGPLL
<b>Equalizer/Re-timer Mode Specifications</b>					
IINS-LOSS-8GBPS	Insertion Loss of channel at 8Gbps (Fbaud/2 is 4GHz, FR4 trace, vias and connectors)			28	dB
FPPM-OFFSET	Tolerable Data Frequency Offset	-5350		350	ppm
TRCLK-DJ	Recovered Clock Deterministic Jitter (in lock-to-data and in lock-to-reference modes)			0.075	Ulpkpk
TRCLK-RJ	Recovered Clock Random Jitter (at 1E-12 BER) (in lock-to-data and in lock-to-reference modes)			0.112	Ulpkpk
NRCLK-GPLL	F3dB cutoff frequency for the 1st Order High-Pass Jitter Measurement Filter. Defined as the ratio of the F3DB cutoff frequency, to the data rate		1667		FBAUD/ FGPLL
<b>Receiver Return Loss</b>					
ZRL-DIFF-DC	Receiver Differential DC Return Loss			-20	dB
ZRL-DIFF-NYQ	Receiver Differential Return Loss at 5GHz			-2.5	dB
ZRL-CM-DC	Receiver Common-Mode DC Return Loss			-10	dB
ZRL-CM-NYQ	Receiver Common-Mode Return Loss at 5GHz			-5	dB
<b>Receiver DC Impedance</b>					
RDIFF-DC	DC Differential Receive Impedance	80	100	110	Ohm
RCM-DC	DC Common-Mode Receive Impedance	20	25	27.5	Ohm

Parameter	Description	Min	Typical	Max		Unit
RDIFF-HIZ-POS	Differential Receive High Impedance for Input Voltage from 0V to 200mV	200k				Ohm
RCM-HIZ-POS	Common-mode Receive High Impedance for Input Voltage from 0V to 200mV	50k				Ohm
RDIFF-HIZ-NEG	Differential Receive High Impedance for Input Voltage from -150mV to 0mV	4k				Ohm
RCM-HIZ-NEG	Common-mode Receive High Impedance for Input Voltage from -150mV to 0mV	1k				Ohm
<b>Receiver Signal Detection</b>						
VIDLE-THRESH	Receiver Signal Detect Input Voltage Threshold	75	120	175 mV	diff-pkpk	
TSIGDET-ATTACK	Signal Detect Valid Signal Attack Time (Turn-on time) in SATA mode			15	N	
TSIGDET-DECAY	Signal Detect Valid Signal Decay Time (Turn-off time) in SATA mode			15	ns	
TSIGDET-ATT-DECAY-MIS	Signal Detect Attack / Decay Time Mismatch in SATA mode			5	ns	
<b>Repeater Receiver Input Eye Specification</b>						
VRX-DIFF-PKPK	Receiver Input Differential Peak-Peak Voltage	250		2000 mV	diff-pkpk	
VRX-CM-DC	Receiver Input DC Common Mode Voltage		0		mV	diff-pkpk
VRX-CM-AC	Receiver Input AC Common Mode Voltage	-150		150 mV	diff-pkpk	
VRX-SENS	Receiver Input Voltage Sensitivity Under the Following Conditions:50inch of FR4 6.25Gbps PRBS7 data pattern	40	50		mV	diff-pkpk
TRX-DDJ	Receive Input Signal Data Dependant Jitter (Inter-Symbol Interference).			1	Ulpkpk	
TRX-TJ	Receive Input Signal Total Jitter (Inter-Symbol Interference).			1	Ulpkpk	
NGPLL	F3dB cutoff frequency for the 1st Order High-Pass Jitter Measurement Filter. Defined as the ratio of the F3DB cutoff frequency, to the data rate		1667		FBAUD/ FGPLL	
<b>Equalizer/Repeater Mode Specifications</b>						
IINS-LOSS-5GBPS	Insertion Loss of 60-inch FR4 trace at 2.5GHz		15	20		dB
IINS-LOSS-6.25GBPS	Insertion Loss of 50-inch FR4 trace at 3.125GHz		15	20		dB
IINS-LOSS-8GBPS	Insertion Loss of 40-inch FR4 trace at 4GHz Post		15	20		dB
TRES-ISI-5GBPS	Equalizer Residual ISI after a signal has passed through 60-inch FR4 trace at 5Gbps Post			0.25	Ulpkpk	
TRES-ISI-6.25GBPS	Equalizer Residual ISI after a signal has passed through 50-inch FR4 trace at 6.25Gbps Post			0.25	Ulpkpk	
TRES-ISI-8GBPS	Equalizer Residual ISI after a signal has passed through 40-inch FR4 trace at 8Gbps			0.25	Ulpkpk	

Table 11-8 Receiver electrical parameters in repeater mode

Parameter	Description	Min	Typical	Max		Unit
<b>Repeater Receiver Input Eye Specification</b>						
VRX-DIFF-PKPK	Receiver Input Differential Peak-Peak Voltage	250		2000 mV	diff-pkpk	

VRX-CM-DC	Receiver Input DC Common Mode Voltage		0		mVdiff-pkpk
VRX-CM-AC	Receiver Input AC Common Mode Voltage	-150		150 mV	mVdiff-pkpk
VRX-SENS	Receiver Input Voltage Sensitivity Under the Following Conditions: 50inch of FR4 6.25Gbps PRBS7 data pattern	40	50		mVdiff-pkpk
TRX-DDJ	Receive Input Signal Data Dependant Jitter (Inter-Symbol Interference).			1	Ulpkpk
TRX-TJ	Receive Input Signal Total Jitter (Inter-Symbol Interference).			1	Ulpkpk
NGPLL	F3dB cutoff frequency for the 1st Order High-Pass Jitter Measurement Filter. Defined as the ratio of the F3DB cutoff frequency, to the data rate		1667		FBAUD/ FGPLL
<b>Equalizer/Repeater Mode Specifications</b>					
IINS-LOSS-5GBPS	Insertion Loss of 60-inch FR4 trace at 2.5GHz		15	20	dB
IINS-LOSS-6.25GBPS	Insertion Loss of 50-inch FR4 trace at 3.125GHz		15	20	dB
IINS-LOSS-8GBPS	Insertion Loss of 40-inch FR4 trace at 4GHz Post		15	20	dB
TRES-ISI-5GBPS	Equalizer Residual ISI after a signal has passed through 60-inch FR4 trace at 5Gbps Post Equalizer Residual ISI			0.25	Ulpkpk
TRES-ISI-6.25GBPS	after a signal has passed through 50-inch FR4 trace at 6.25Gbps Post Equalizer Residual ISI after a signal has			0.25	Ulpkpk
TRES-ISI-8GBPS	passed through 40-inch FR4 trace at 8Gbps			0.25	Ulpkpk

### 11.7 LVC MOS Characteristics

The chip 3.3V LVC MOS power supply characteristics are shown in Table 11-9.

Table 11-9 3.3V LVC MOS power supply characteristics

parameter	describe	Minimum	Typical Value	Maximum	unit
DVDD33	GPIO interface voltage	3.168	3.3	3.432	V

### 11.8 Power-On and Restart Characteristics

The power-on and restart characteristics are shown in Figure 11-1.

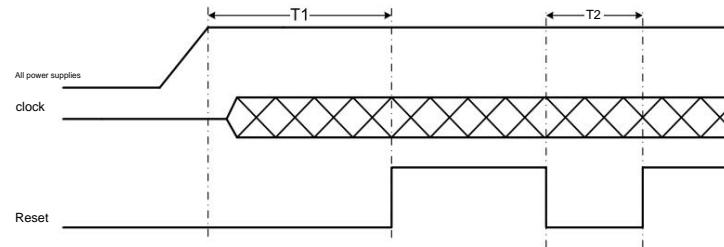


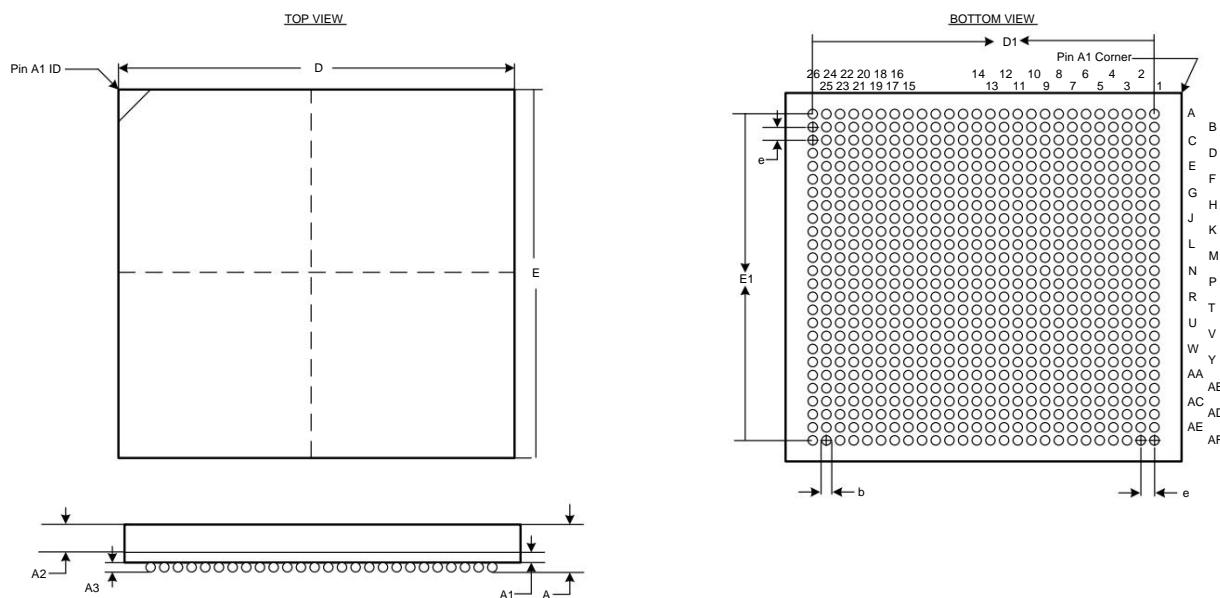
Figure 11-1 Power-on and restart characteristics

The power-on and restart characteristic parameters are shown in Table 11-10.

Table 11-10 Power-on and restart characteristics

Parameter Description	Description/Conditions	Type	Min	Typ	Max	Unit		
T1 Reset delay time	Reset delay time is the duration from when all power supplies are stable to when the reset signal reaches high level.			10	-	-		ms
T2 reset low level time	The internal POR circuit of FSL91030M generates a continuous low level Time	I		10	-	-		ms

Note: Since the chip integrates the POR circuit, there is no special requirement for the power-on sequence, and power-on can be performed at the same time.

**12 Packaging Information****12.1 WBBGA676**

parameter	Dimensions (mm)		
	Minimum	Normal	Maximum
A	1.21	value 1.37	1.53
A1	0.30	0.36	0.42
A2	0.65	0.70	0.75
A3	0.26	0.31	0.36
D	21.90	22.00	22.10
E	21.90	22.00	22.10
D1	19.95	20.00	20.05
E1	19.95	20.00	20.05
e	0.80BSC		
b	0.35	0.40	0.45

**13 Ordering Information**

chip	temperature range (T <sub>j</sub> )	Encapsulation		Top Label
		name	describe	
FSL91030M -40°C~+125°C	WBBGA676	Package size: 22x22mm, Ball pitch: 0.8mm.	Xuanyuan 1030M	

**14 Revision Information**

Revision	Version	describe
date: 2021.4.18	A	initial version.
2021.5.14	B	Manual optimization: Added thermal characteristics information.
2021.6.15	C	Modify the X_MDIREF pin description: Connect to 3.3V voltage; when modifying Clock pin description; supplemented the configuration pins and multiplexed pins chapters.
2021.7.13	D	Modified DDR3 interface timing description.
2022.1.12	E	Modify the chapters about configuration pins and multiplexing pins, etc.
2022.2.28	F	Modify the configuration pins and multiplexed pin numbers.
2022.11.7	G	Modify configuration pin description and optimize other contents.