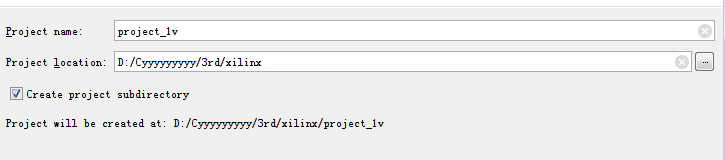
Launch Vivado and create an empty project targeting the ZYBO (having xc7z010clg400-1 device) and using the Verilog language.

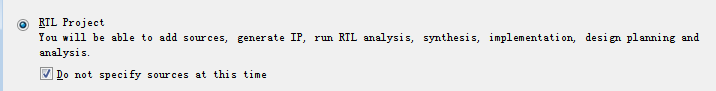
* + 1. Open Vivado by selecting **Start > All Programs > Xilinx Design Tools > Vivado 2013.4 > Vivado 2013.4**
    2. Click **Create New Project** to start the wizard. You will see the *Create a New Vivado Project* dialog box. Click **Next**.



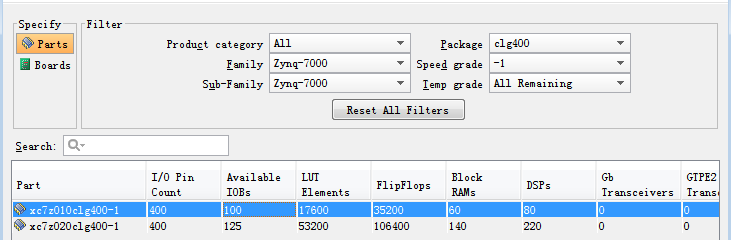
* + 1. Click the Browse button of the *Project Location* field of the **New Project** form, browse to **D:/Cyyyyyyyyy/3rd/xilinx** and click **Select**.
    2. Enter **lab1** in the *Project Name* field. Make sure that the *Create Project Subdirectory* box is checked. Click **Next**.



* + 1. Select **RTL Project** in the *Project Type* form, and click **Next**.



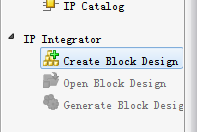
* + 1. Select **Verilog** as the *Target language* and **Mixed** as the*Simulator language* in the *Add Sources* form, and click **Next**.
    2. Click **Next** two more times to skip *Adding Existing IP* and *Add Constraints*
    3. In the *Default Part* form, select *Parts*, and using various filters shown in the figure below, select **xc7z010clg400-1** part as it is on the ZYBO board. Click **Next**.



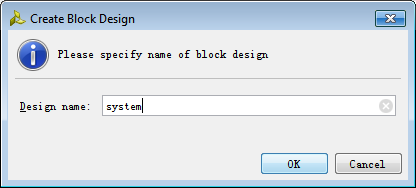
* + 1. Check the *Project Summary* and click **Finish** to create an empty Vivado project.

Use the IP Integrator to create a new Block Design, add the ZYNQ processing system block, and import the provided xml file for the ZYBO board.

* + 1. In the Flow Navigator, click **Create Block Design** under IP Integrator



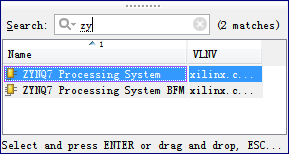
* + 1. Enter **system** for the design name and click **OK**



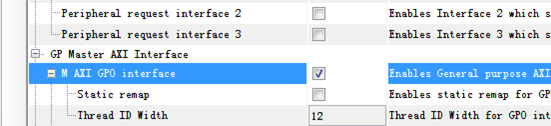
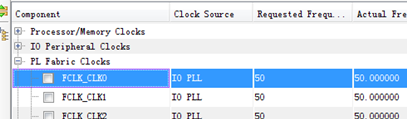
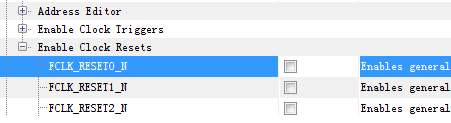
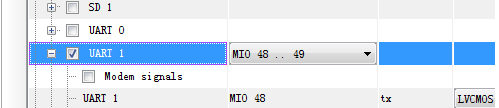
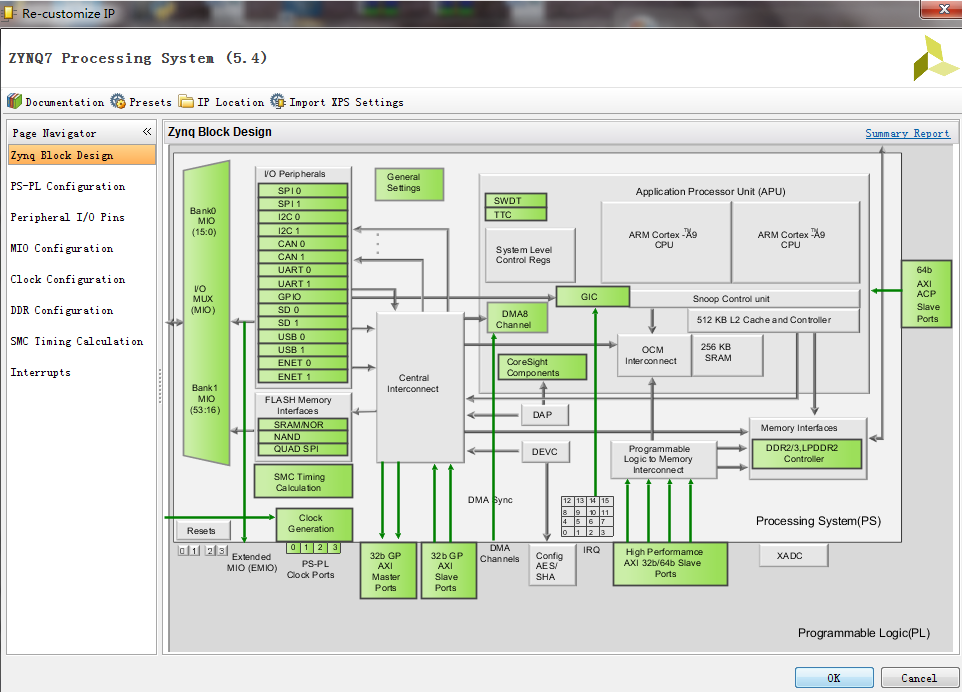
* + 1. click the *Add IP icon* in the block diagram side bar



* + 1. Once the IP Catalog is open, type “z” into the Search bar, find and double click on **ZYNQ7 Processing System** entry, or click on the entry and hit the Enter key to add it to the design.



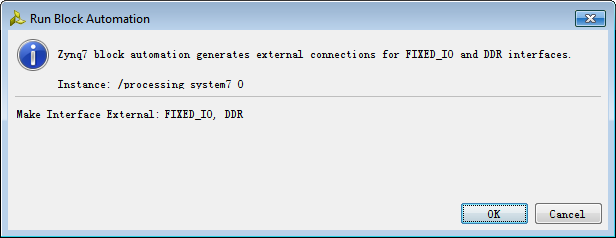
* + 1. Double-click on the added block to open its *Customization* window. Notice now the *Customization* window shows selected peripherals .



* + 1. Click **OK** to close the *Customization* window for now.



* + 1. Click on **Run Block Automation** and select **/processing\_system7\_1**, and click ok when prompted to run automation.

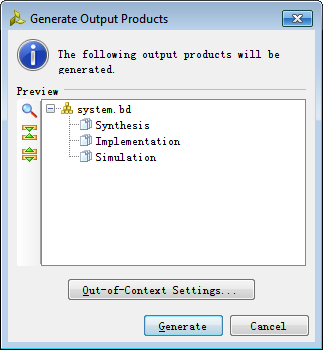
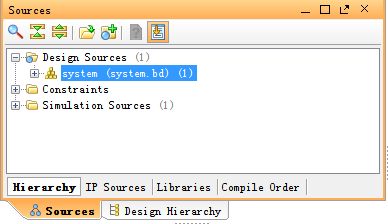


* + 1. Click on the (Validate Design) button and make sure that there are no errors.



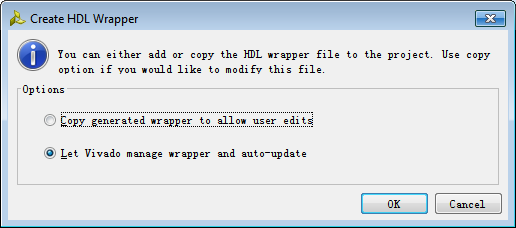
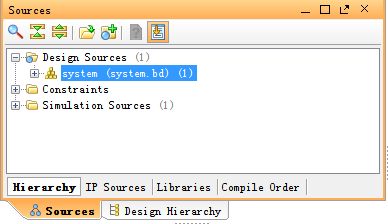
Generate IP Integrator Outputs, the top-level HDL, and start SDK by exporting the hardware.

* + 1. In the sources panel, right-click on *system.bd*, and select **Generate Output Products …** and click **Generate** to generate the Implementation, Simulation and Synthesis files for the design

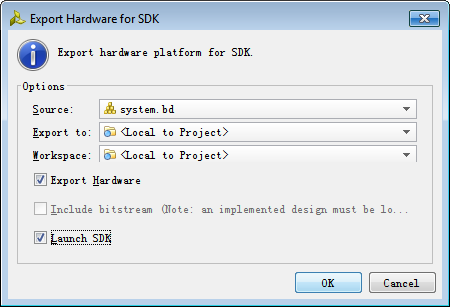


* + 1. Right-click again on *system.bd*, and select **Create HDL Wrapper…** to generate the top-level VHDL model. Leave the *Let Vivado manager wrapper and auto-update* option selected*,* and click **OK**

The *system\_wrapper.vhd* file will be created and added to the project. Double-click on the file to see the content in the Auxiliary pane.

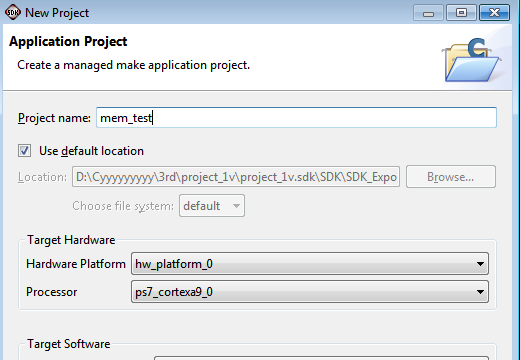


* + 1. Select **File >** **Export > Export hardware for SDK…**
    2. The *Export Hardware for SDK* GUI will be displayed. Select the **Launch SDK** box, and ensure that *Export Hardware* is already selected, and click **OK** to export to, and launch SDK. (**Save** the design if prompted.)

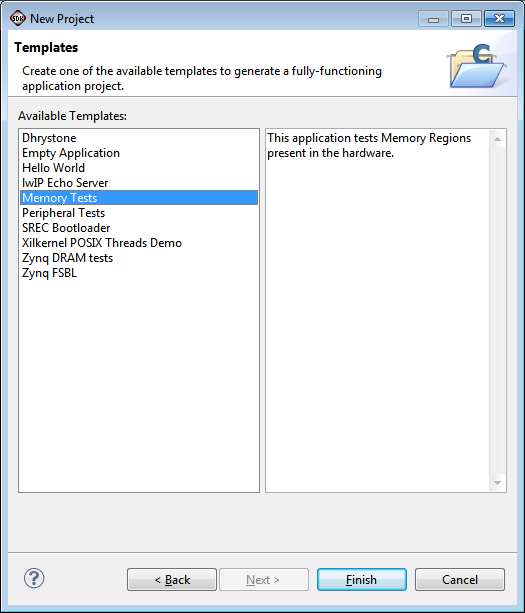


Generate memory test application using one of the standard projects template.

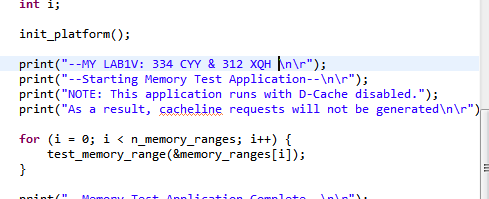
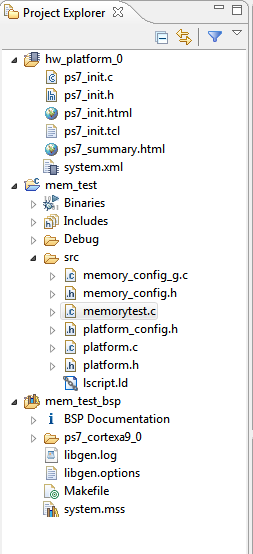
* + 1. In SDK, select **File** > **New** > **Application Project**
    2. Name the project **mem\_test**, and in the *Board Support Package* section, leave *Create New* selected and leave the default name *mem\_test\_bsp* and click **Next.**



* + 1. Select **Memory Tests** from the *Available Templates* window, and click **Finish.**



* + 1. Open the **memorytest.c** file in the mem\_test project (under *src*), and insert a line of code in this file.



Make sure that the JP7 is set to select USB power. Connect the board with a micro-usb cable and power it ON. Open the serial debugging software, set the baud rate is 172800

* + 1. Make sure that the JP7 is set to select USB power.
    2. Make sure that a micro-USB cable is connected to the connector. Turn ON the power.
    3. Run the mem\_test application. And you’ll see result in the serial debugging software.

