Cache report

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20206018
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Contents

1 Introduction

Lab5 is required to design a Cache. A cache processes three state–read and hit, read but miss, and write. And use cache to save data that use much to save time. We use multi cycle CPU link the cache.

1.1 Read Data

1. Processor send the address to the cache
2. Then use the valid digit and sign digit to find the data.
3. If the data exist then hit, and send the data to the processor.
4. If the data does not exist then send miss to the memory, the memory will send the data that according to the requirement to the specific position.

1.2 Write data

1. Memory send the address and the data to the cache
2. Then compare the valid digit and sign digit to find the specific position in the cache.
3. Write in the data.

2 Design

As the Description of TB file mentioned, We do not need to implement memory and register ourselves. So we design the path to connect them together.

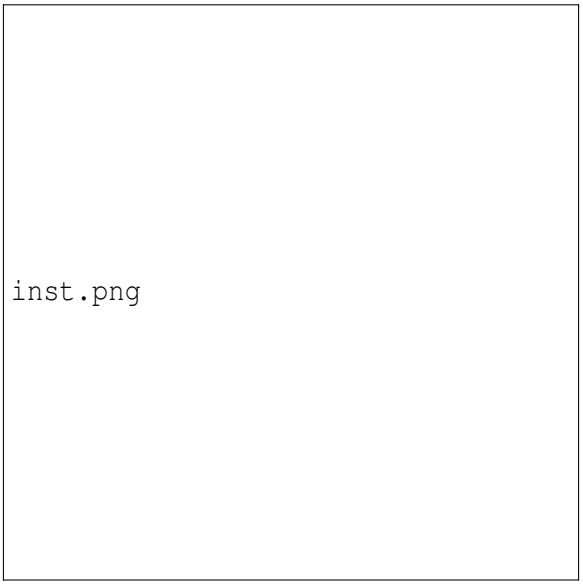
2.1 Module design

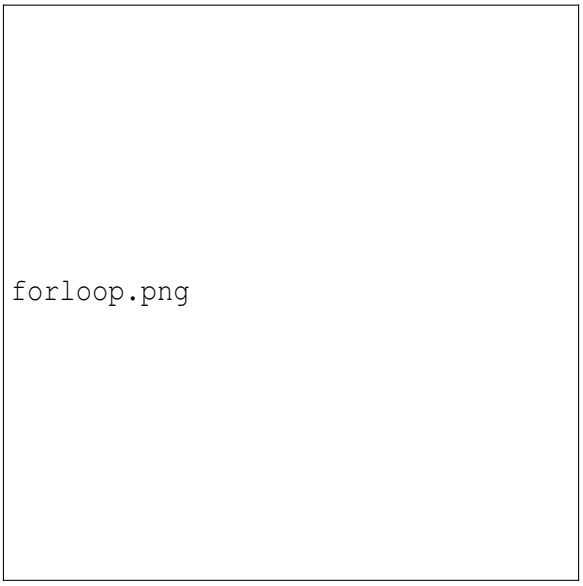
1. Write-through
2. Write-allocate
3. Blocking cache

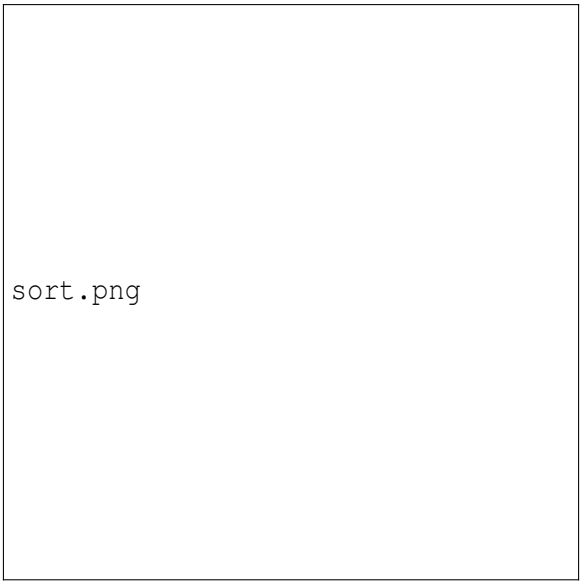
3 Implementation

4 Evaluation

I pass all the test in the testbench folder.







5 Conclusion

The cache is very useful in the CPU nowadays,it make the CPU quicker than the CPU last few years.