Charles Zhang
305413659
Academic Integrity:

CS M51A HW#4

1a)

A	B	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Z
0	0	L	H	H	L	L	H	1
0	1	L	H	H	L	H	L	0
1	0	H	L	L	H	L	H	1
1	1	H	L	L	H	H	L	1

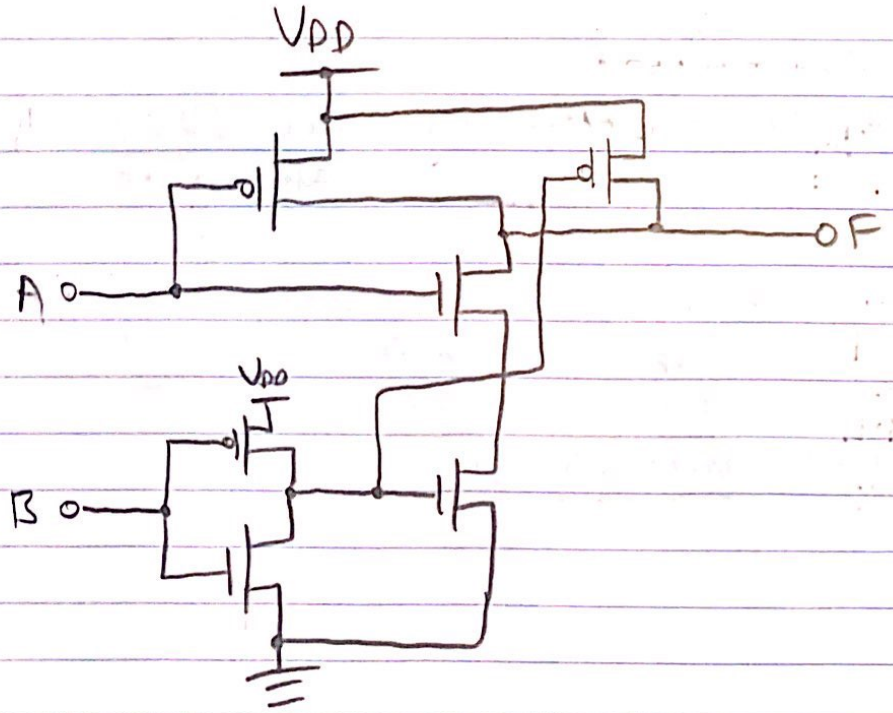
1b) $\Sigma m(0,2,3)$, $\Pi M(1)$

2a)

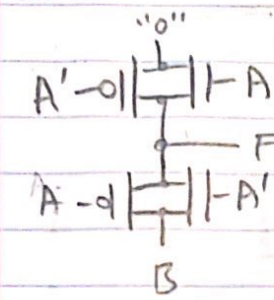
A	B	F
0	0	0
0	1	1
1	0	0
1	1	0

$\Sigma m(1) = \Pi M(0,2,3)$

2b) $F = A'B = (A+B')'$ → NOR gate



2c) $F = A'B = (A+B')'$ → AND gate



A	B	G_1	G_2	F
0	0	on	off	0 ✓
0	1	off	on	1 ✓
1	0	on	off	0 ✓
1	1	off	on	0 ✓

3a) L=4, find $t_{pLH}(d,z)$

$x = t_{pLH}(OR) + t_{pLH}(AND) + t_{pLH}(NOR) + t_{pLH}(NOR)$

$x = (0.08 + 0.075(2)) + (0.08 + 0.038) + (0.06 + 0.075(3)) + (0.06 + 0.075(4))$

$x = 0.23 + 0.118 + 0.135 + 0.36 = 0.843\,ns$

$y = t_{pLH}(OR) + t_{pLH}(NOR) + t_{pLH}(NOR)$

$y = (0.08 + 0.075(2)) + (0.06 + 0.075(1)) + (0.06 + 0.075(4))$

$y = 0.23 + 0.135 + 0.36 = 0.725\,ns$

$\boxed{t_{pLH}(d,z) = \max(x,y) = 0.843\,ns}$

3b) L=4, find $t_{pHL}(b,z)$

$x = t_{pHL}(AND) + t_{pHL}(AND) + t_{pHL}(NOR) + t_{pHL}(NOR)$

$x = (0.09 + 0.027(2)) + (0.01 + 0.027) + (0.07 + 0.016) + (0.07 + 0.016(4))$

$x = 0.144 + 0.117 + 0.086 + 0.134 = 0.481\,ns$

$y = t_{pHL}(AND) + t_{pHL}(NOR) + t_{pHL}(NOR)$

$y = 0.144 + 0.086 + 0.134 = 0.364\,ns$

$\boxed{t_{pHL}(b,z) = \max(x,y) = 0.481\,ns}$

4a) $S_0 = 1, S_1 = 0$

A → Z
B → B
C → Z
D → D
B → B
D → Z

$S_1 = 0$

$S_0 = 1$

Output = B

4b) $S_0 = 1, S_1 = 1$

A → A
B → Z
C → C
D → Z
A → A
C → Z

$S_1 = 1$

$S_0 = 1$

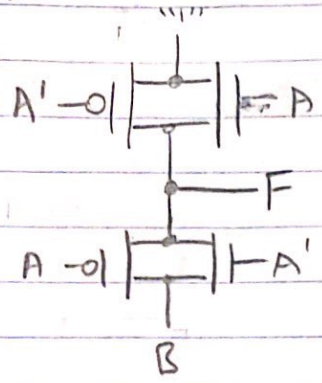
Output = A

4c)

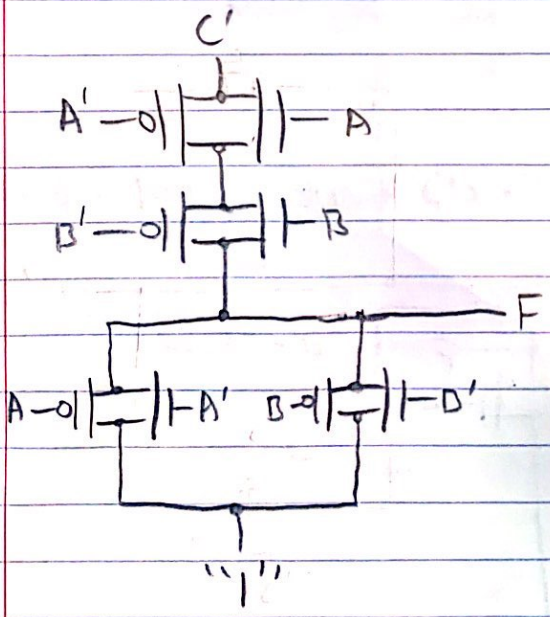
S_1	S_0	F
0	0	D
0	1	B
1	0	C
1	1	A

$(S_1' S_0' D) + (S_1' S_0 B) + (S_1 S_0' C) + (S_1 S_0 A)$

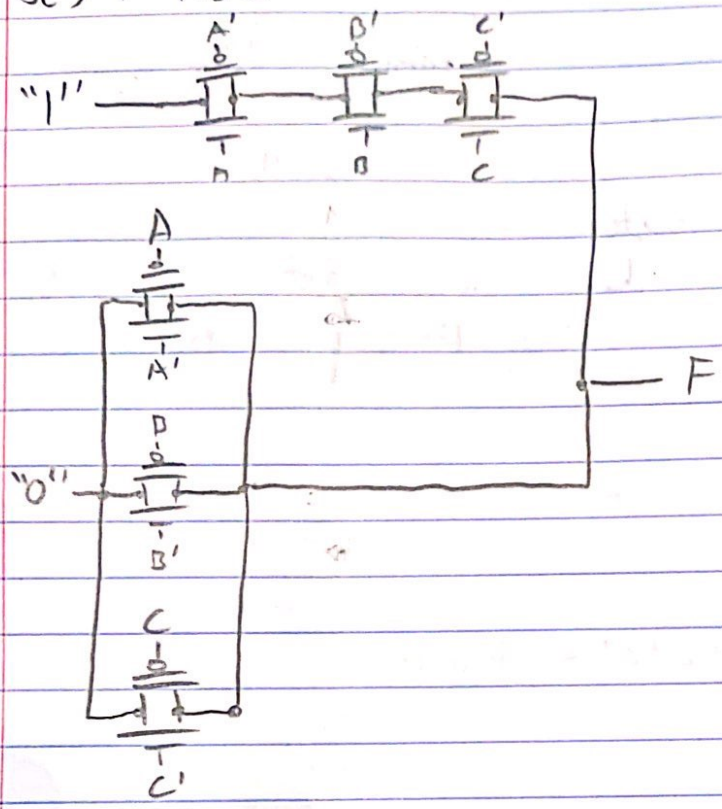
5a) $F = A + B \rightarrow$ OR gate $= (A'B')'$



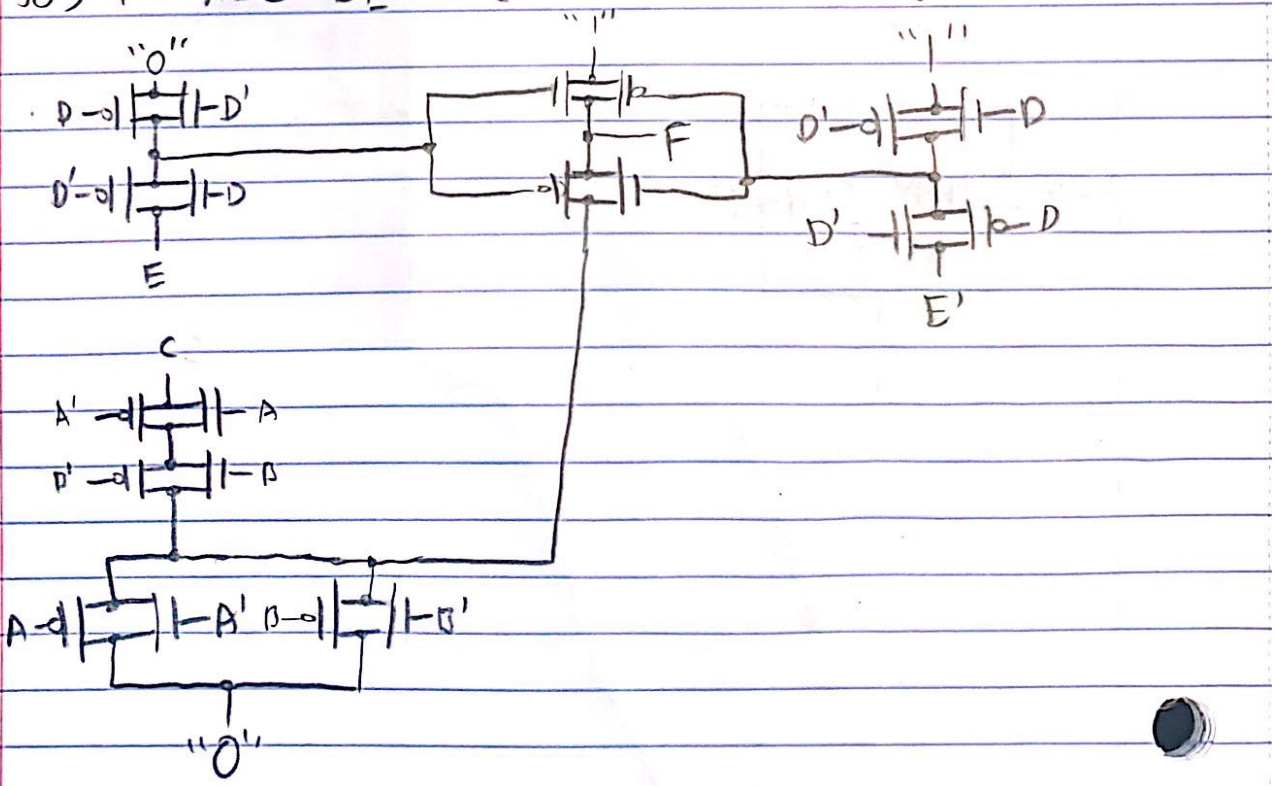
5b) $F = (ABC)' = A' + B' + C' \rightarrow$ OR gate



5c) $F = ABC$



5d) $F = ABC + DE = (A' + B' + C')' + DE \quad (DE)' = D' + E'$



6) Both PMOS and NMOS must be used to account for both high and low signals coming in. PMOS gates are only effective switches when connected to high voltage sources. Meanwhile, NMOS gates are only effective switches when connected to a low voltage source. Since the source of the transmission gate can be either high or low voltage, both PMOS and NMOS must be used to account for all possibilities.