

# **CS M51A**

## **Logic Design of Digital Systems**

### **Winter 2021**

Some slides borrowed and modified from:

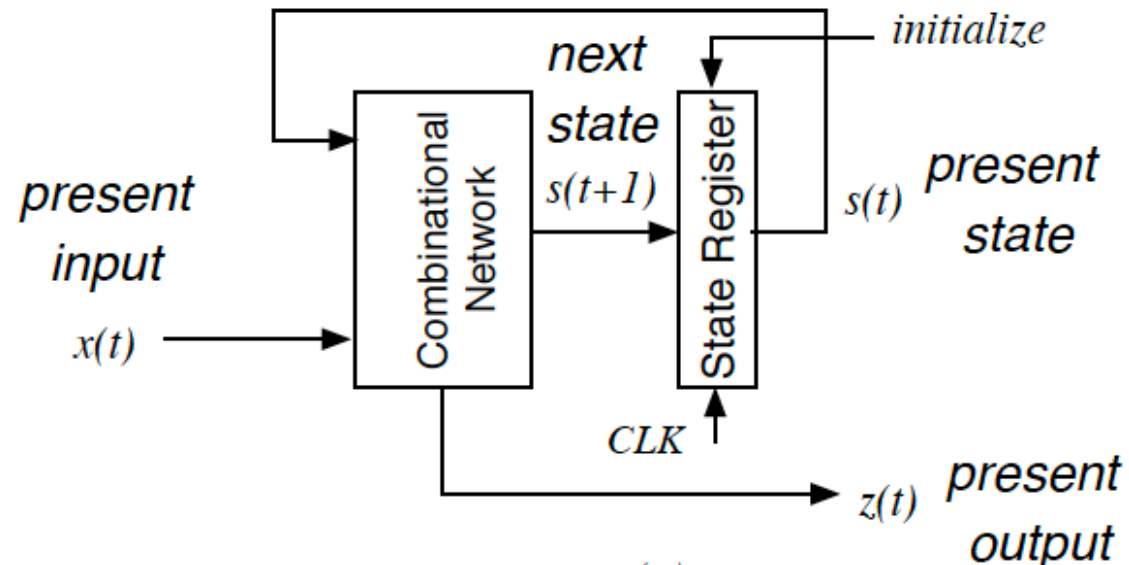
M.D. Ercegovic, T. Lang and J. Moreno, Introduction to Digital Systems.

# Sequential System Implementation

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State-transition function  $s(t+1) = G(s(t), x(t))$

Output function  $z(t) = H(s(t), x(t))$



# MEALY AND MOORE MACHINES

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## Mealy machine

$$z(t) = H(s(t), x(t))$$

$$s(t + 1) = G(s(t), x(t))$$

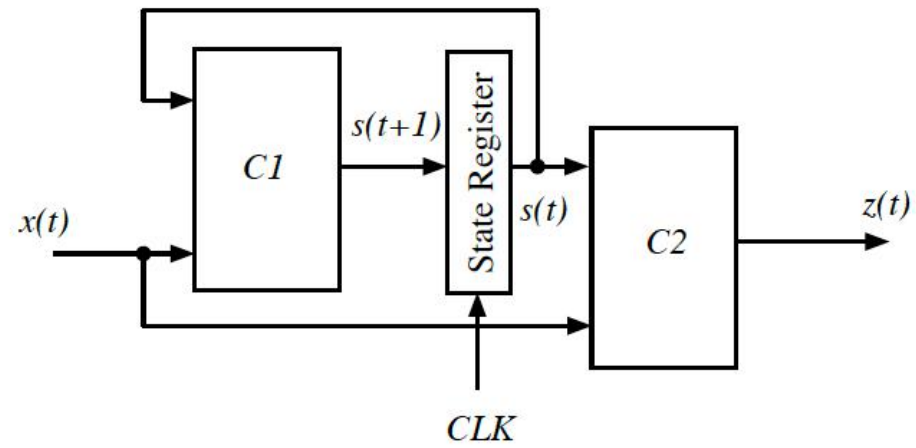
## Moore machine

$$z(t) = H(s(t))$$

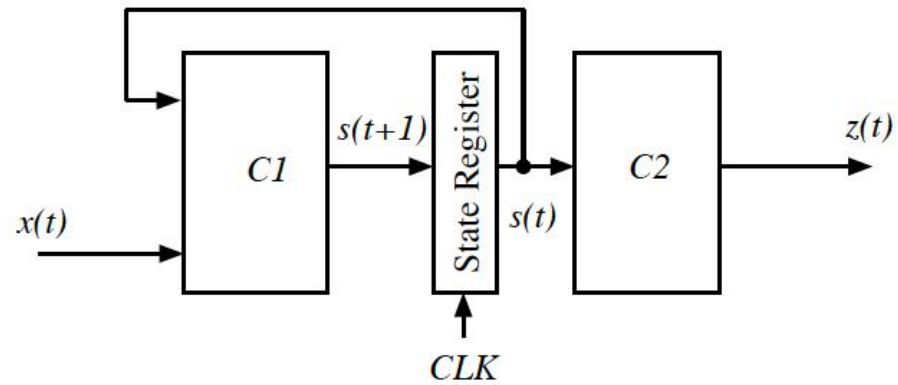
$$s(t + 1) = G(s(t), x(t))$$

# MEALY AND MOORE MACHINES

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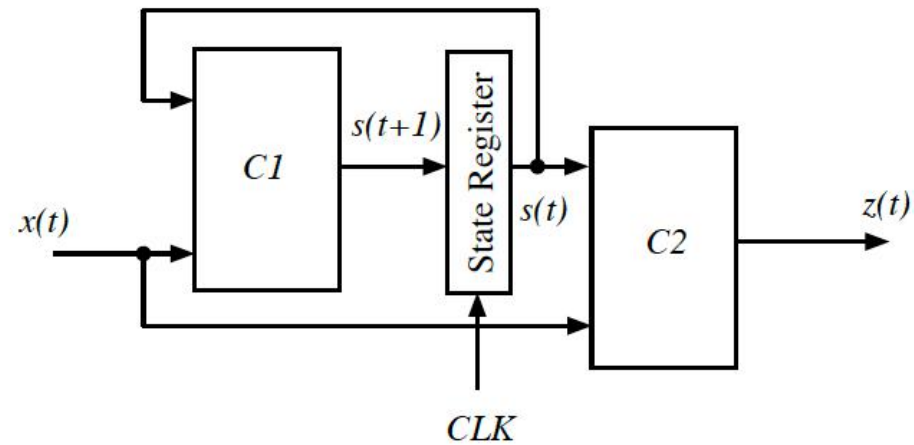


(a)

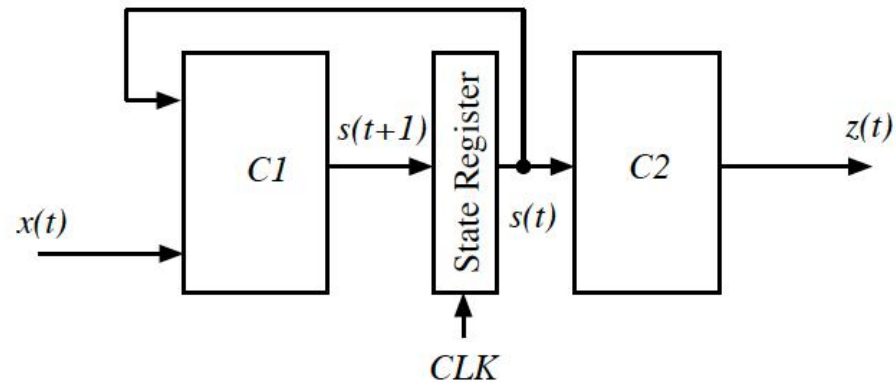


## MEALY AND MOORE MACHINES

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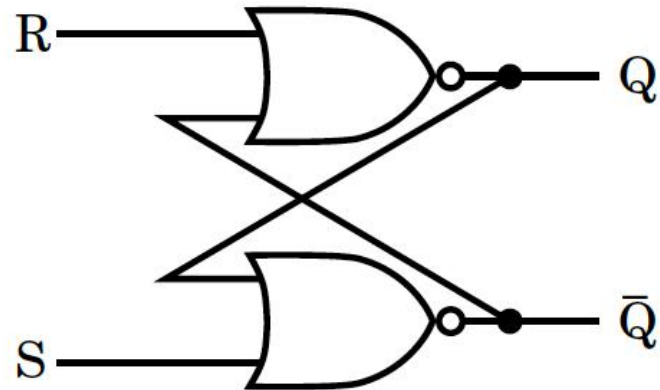
(a)



How to implement the state register?

## SR Latch with NOR gates

- SR Latch with NOR gates



### Functional Description of SR Latch

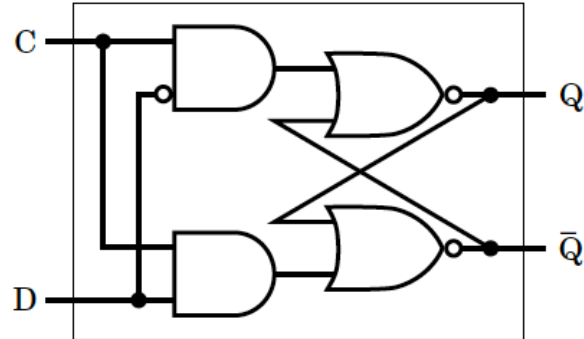
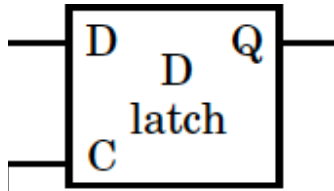
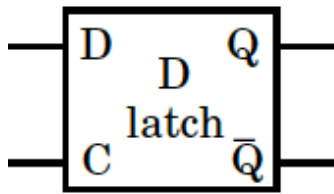
$S$	$R$	$Q$	$\bar{Q}$	
0	0	$Q$	$\bar{Q}$	Latch state (no change)
0	1	0	1	Reset state
1	0	1	0	Set state
1	1	?	?	Undefined

## Functional Description of SR Latch

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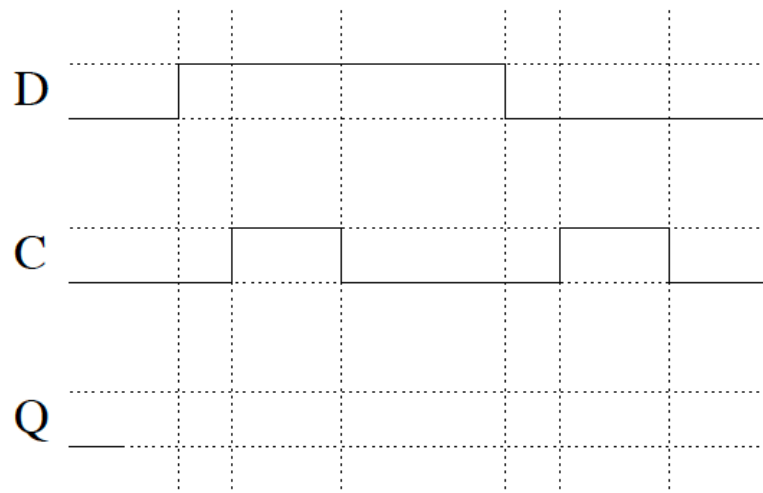
- Advantages:
  - Can “remember” value
  - Natural “reset” and “set” signals  
(SR=01 is “reset” to 0, SR=10 is “set” to 1)
- Disadvantages:
  - SR=11 input has to be avoided
  - No notion of a clock or change at discrete points in time yet

## The D Latch



$C$	$D$	Next state of $Q$
0	X	No change
1	0	$Q = 0$ (Reset)
1	1	$Q = 1$ (Set)

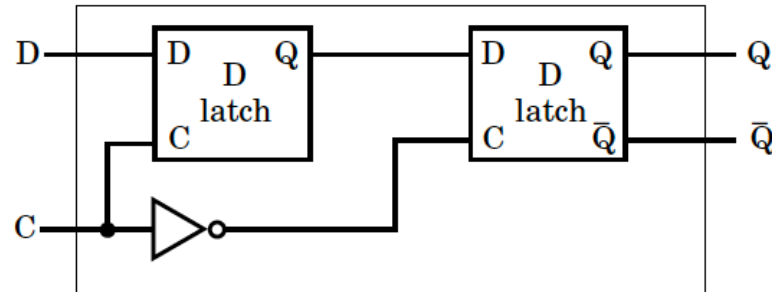
Graphical example:



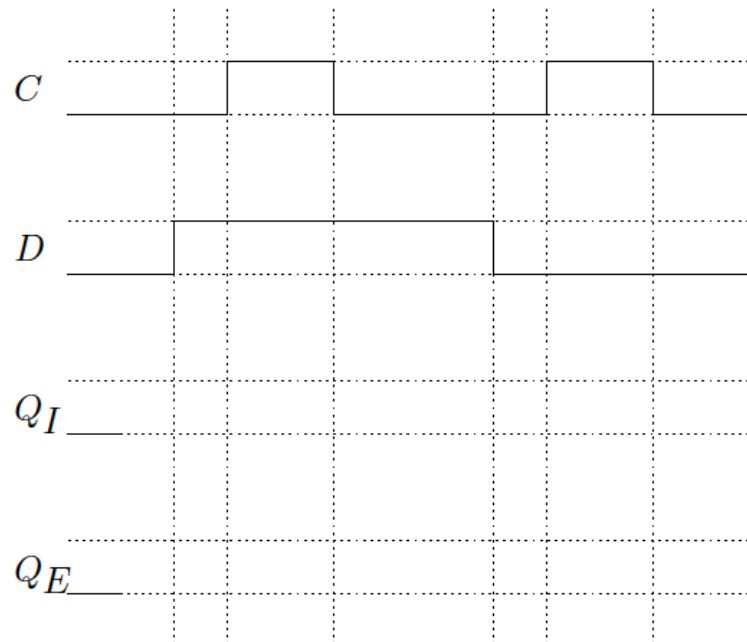


## The D Flip-Flop

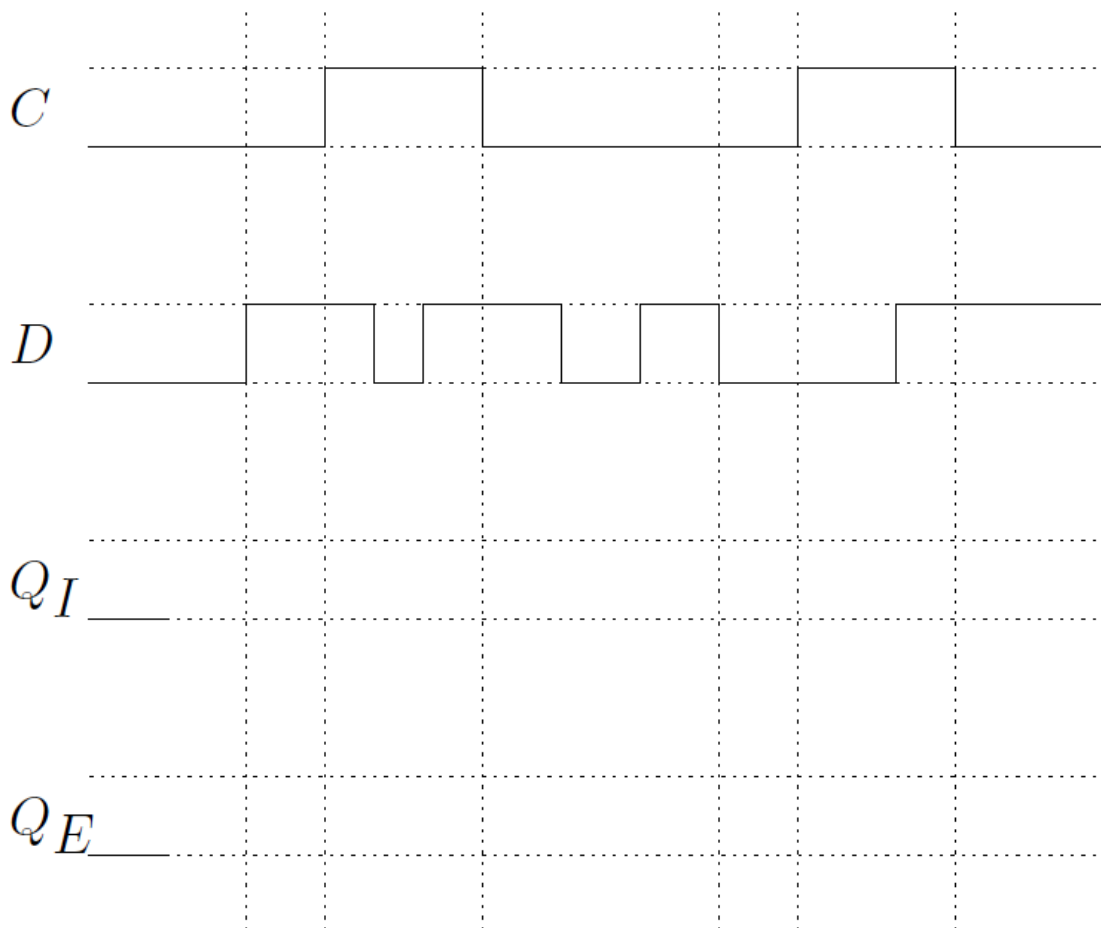
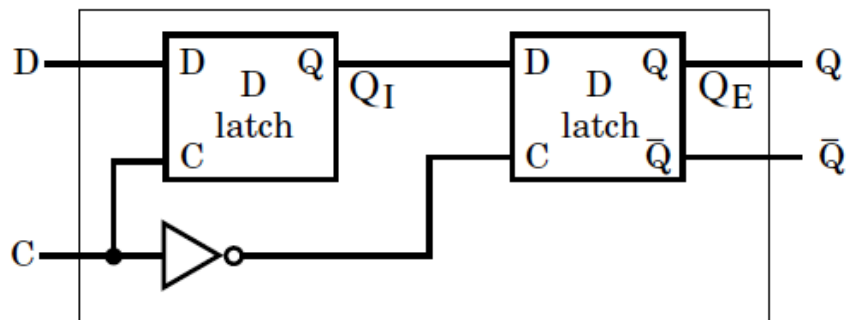
- We want state to be affected only at discrete points in time; a master-slave design achieves this.



- Graphical example:



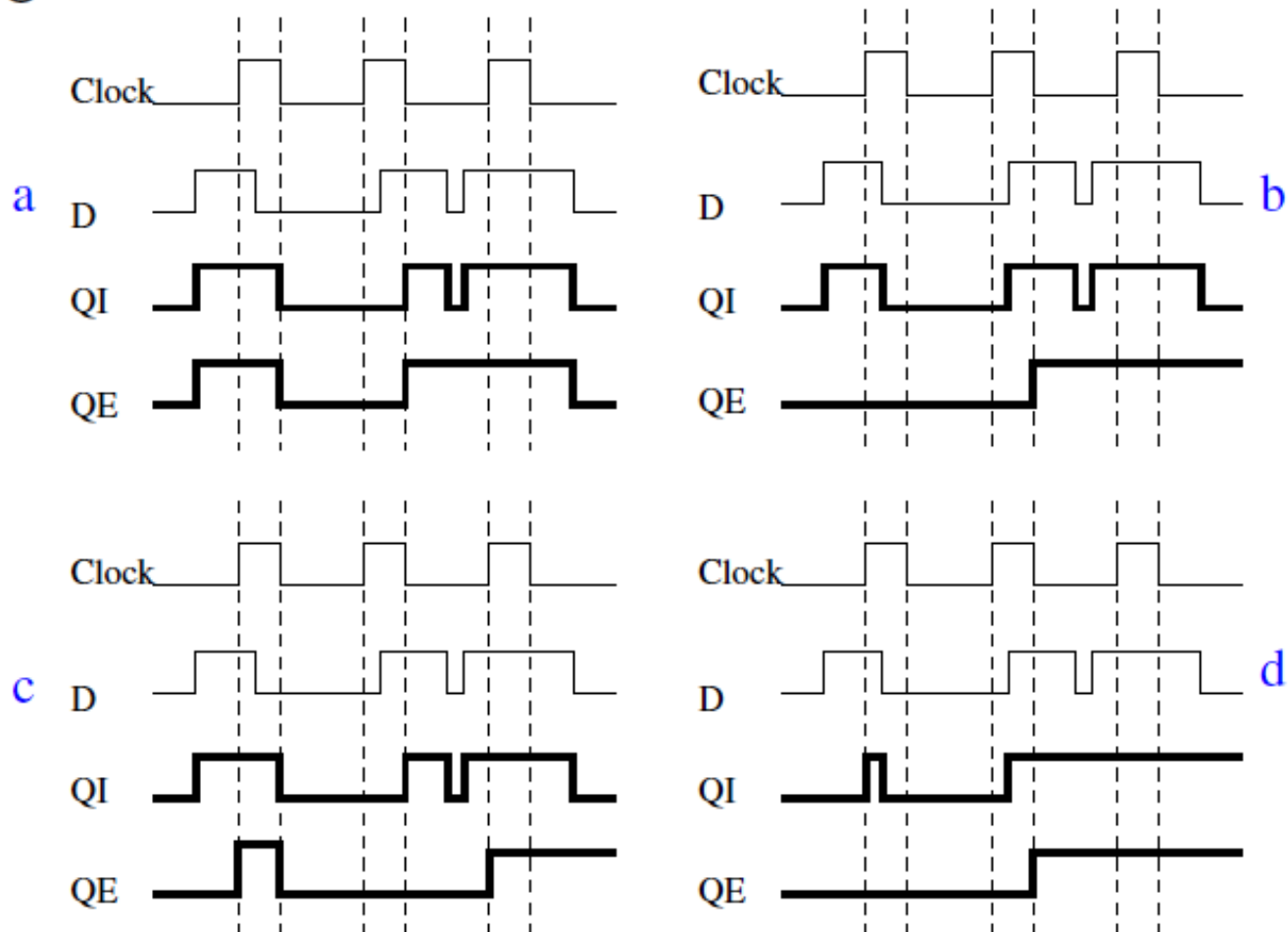
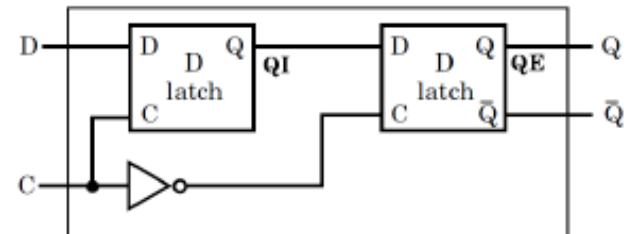
# D Flip-Flop



# Clicker Question

# Flipflops

Which of the following is a trace of  $QI$  and  $QE$  of a D-flipflop for the given D and Clock traces?



# Clicker Question

Question on previous midterm:

How many bits can you store in one flipflop? Circle one.

1   2   4   8   16

A) 1

B) 2

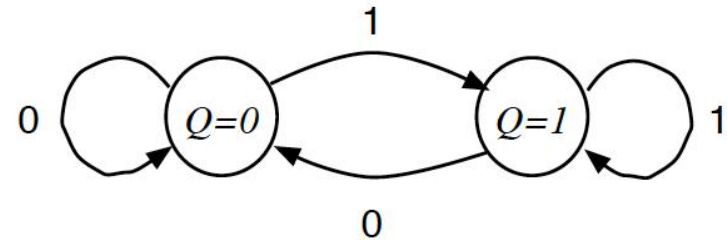
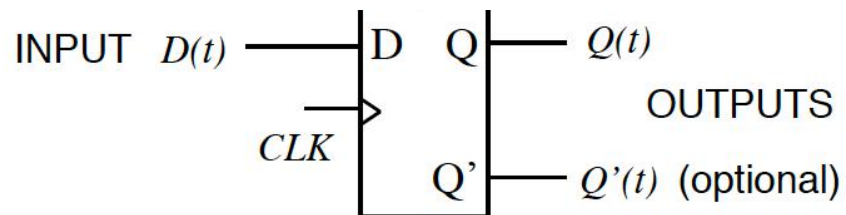
C) 4

D) 8

E) 16

# Flip-Flop: Master-Slave

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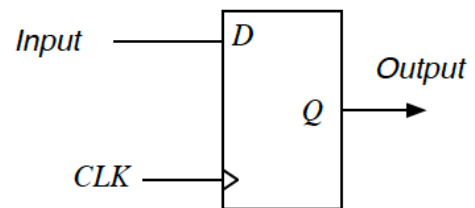


$PS = Q(t)$	$D(t)$	
	0	1
0	0	1
1	0	1
	$NS = Q(t + 1)$	

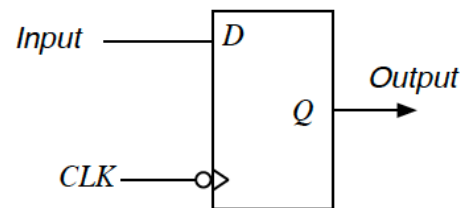
$$Q(t + 1) = D(t)$$

# Flip-Flop

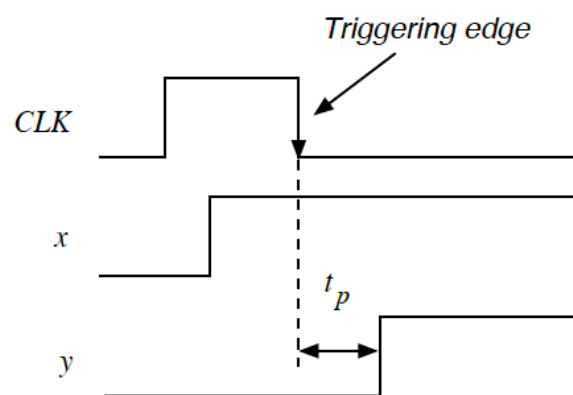
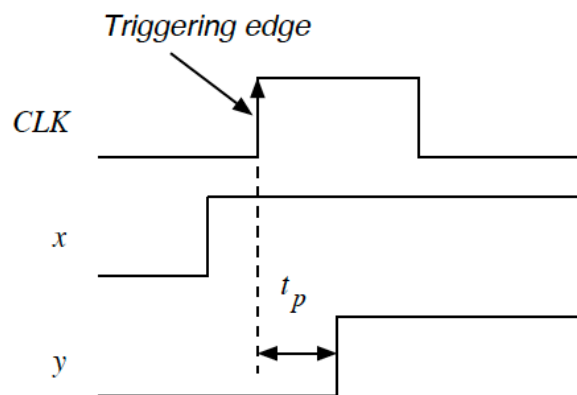
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(a)

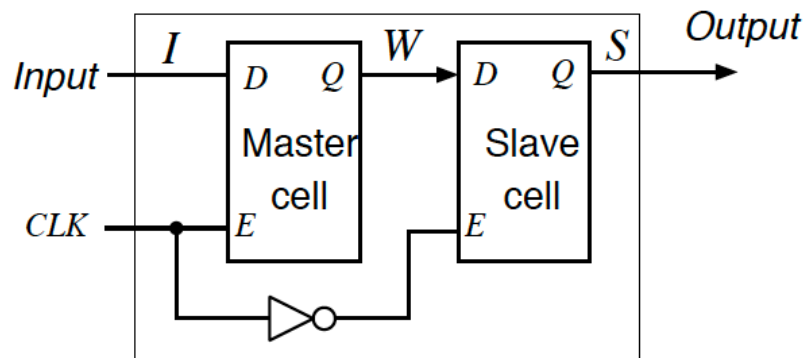


(b)

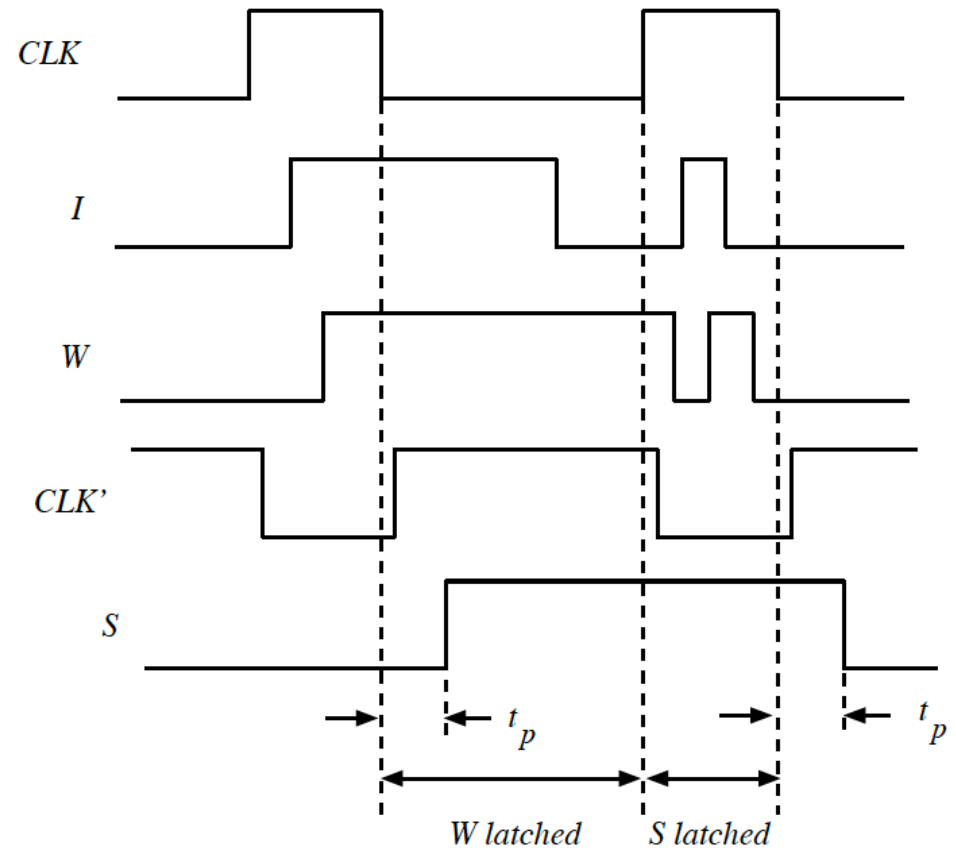




# Flip-Flop: Master-Slave



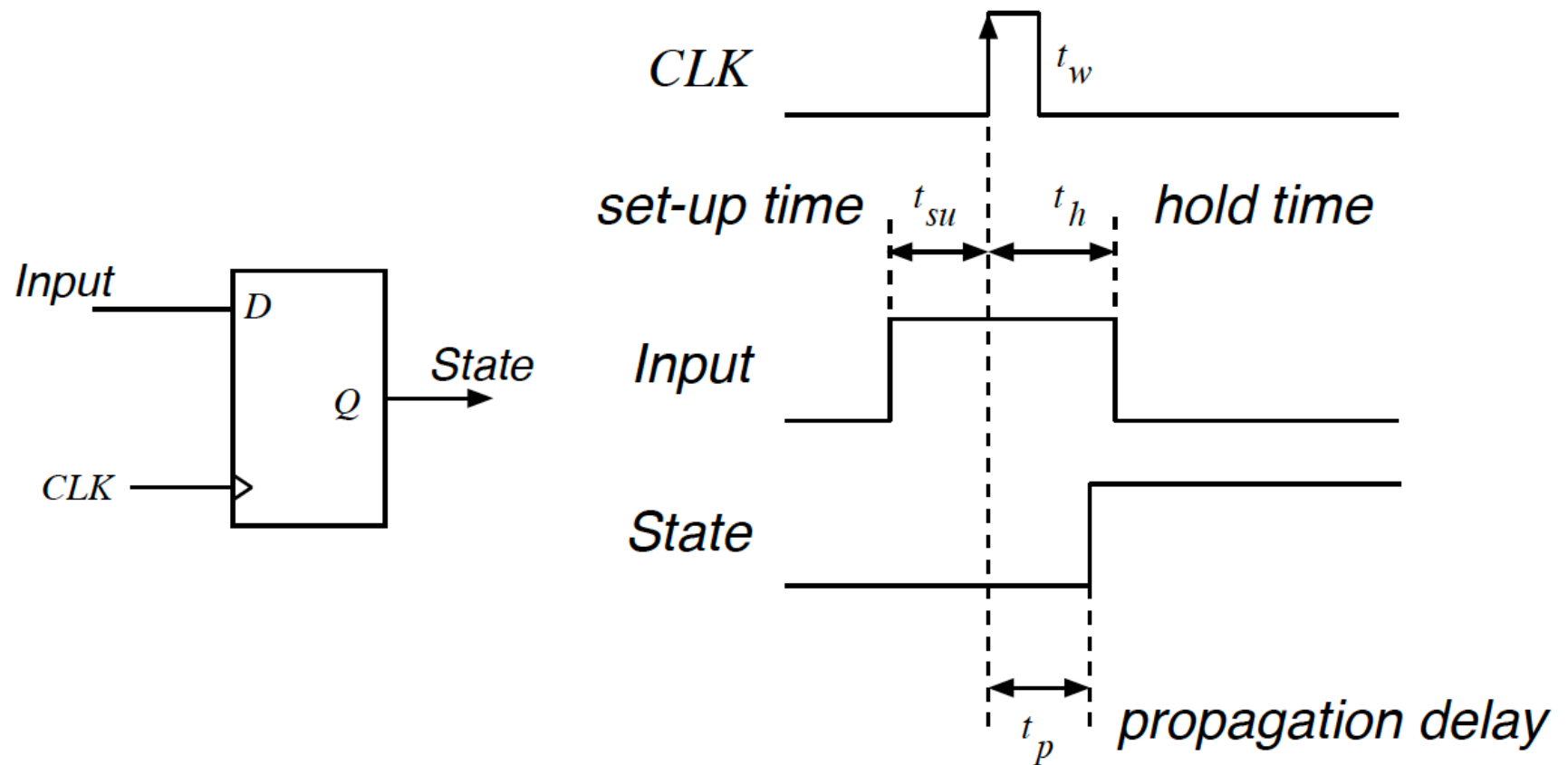
(a)



(b)

## TIMING PARAMETERS OF A BINARY CELL

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## CHARACTERISTICS OF A CMOS D flip-flop

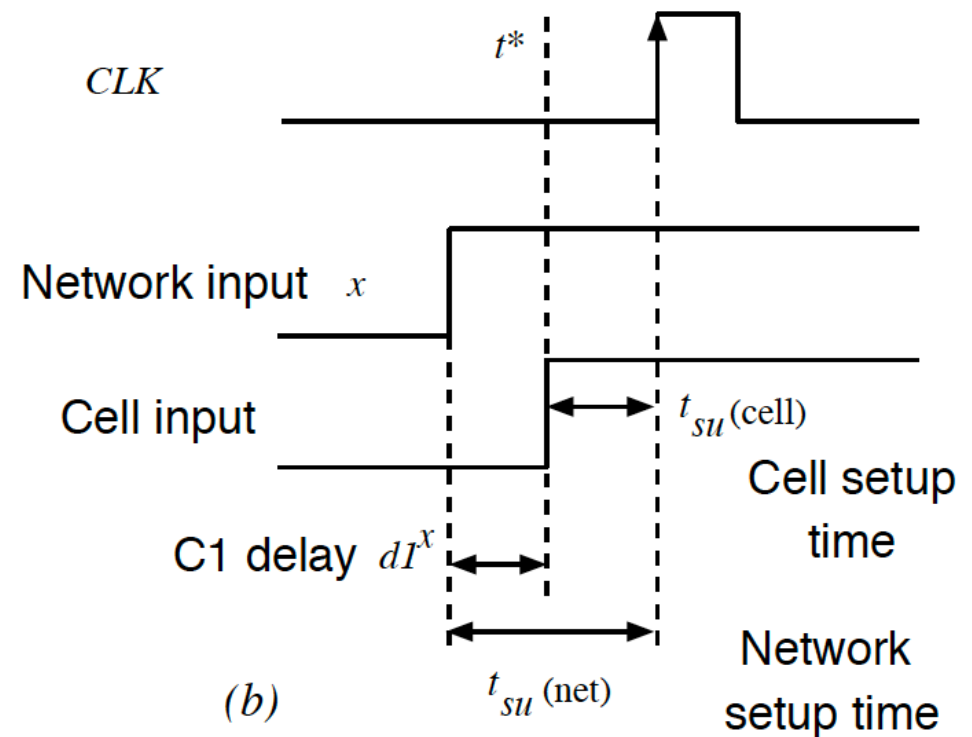
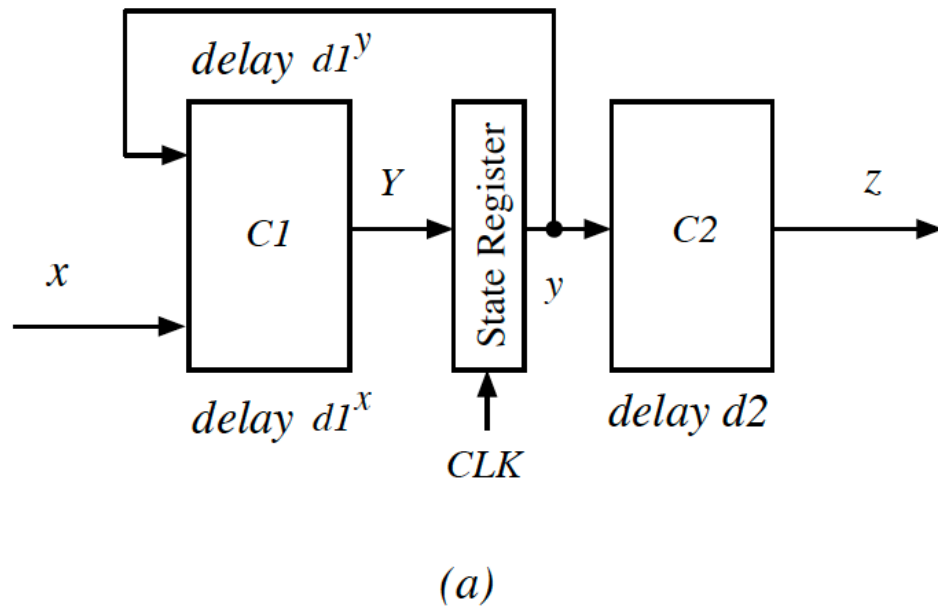
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Delays				
$t_{pLH}$ [ns]	$t_{pHL}$ [ns]	$t_{su}$ [ns]	$t_h$ [ns]	$t_w$ [ns]
$0.49 + 0.038L$	$0.54 + 0.019L$	0.30	0.14	0.2

$L$ : output load of the flip-flop

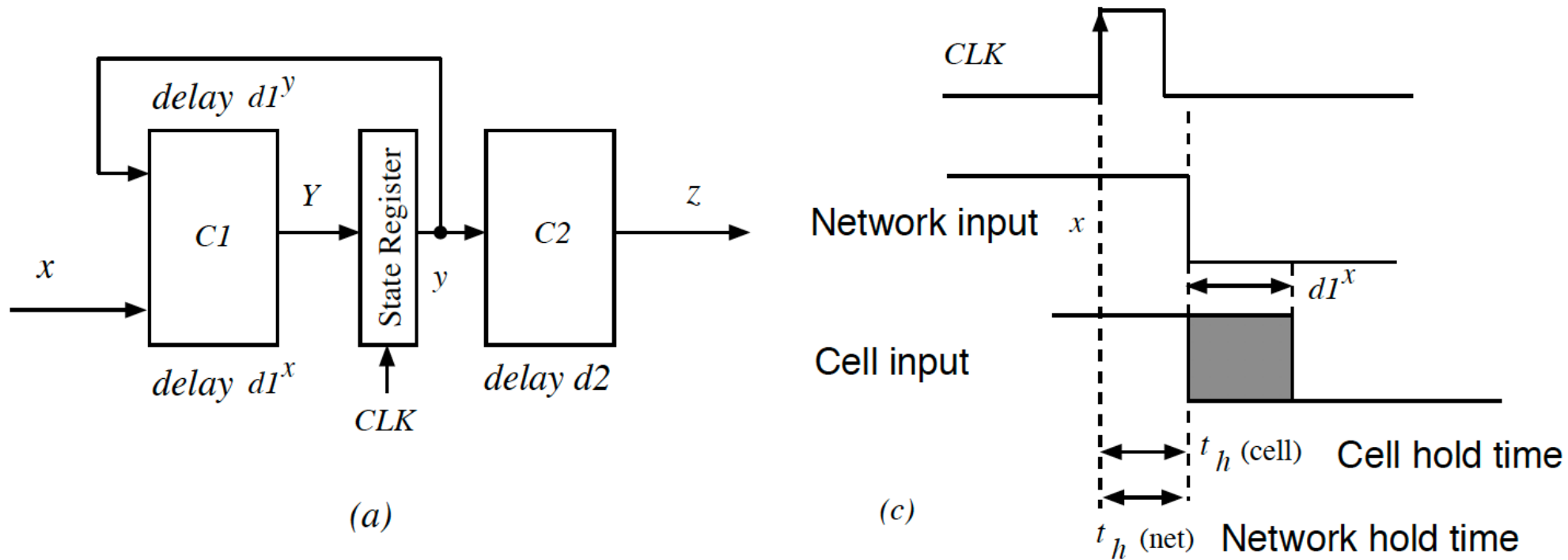
# TIMING CHARACTERISTICS OF SEQUENTIAL NETWORKS

- NETWORK SET-UP TIME:  $t_{su}^x(net) = d1^x + t_{su}(cell)$



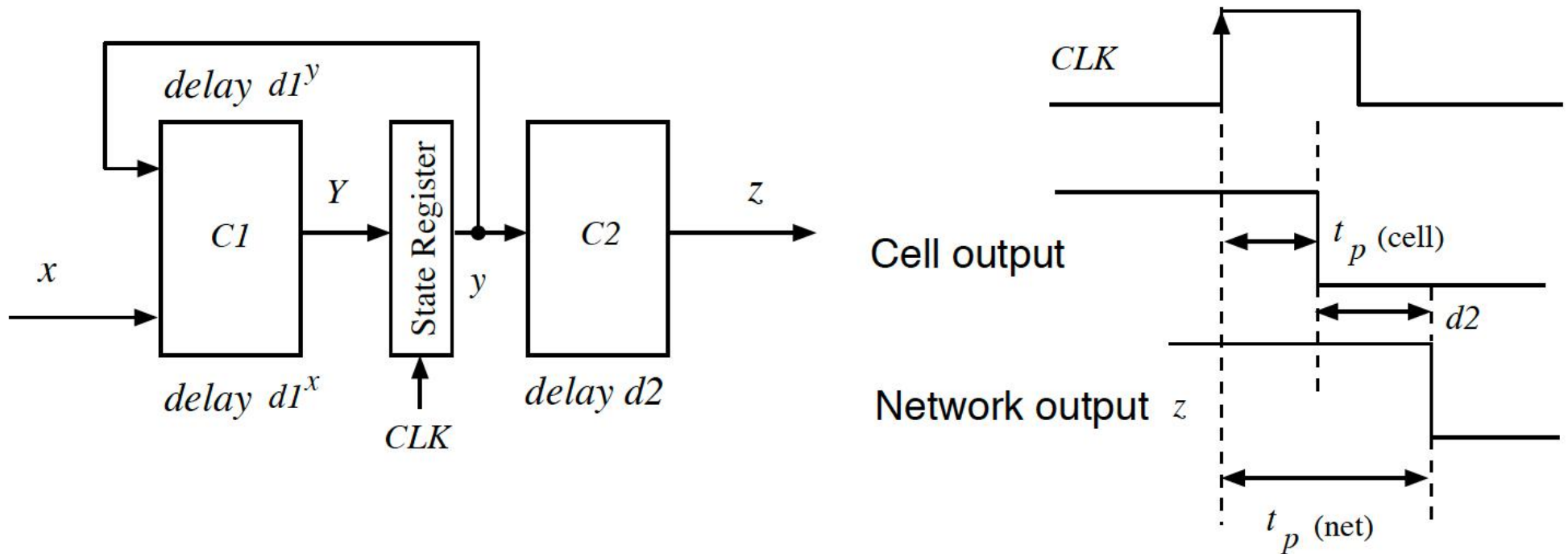
# TIMING FACTORS

- NETWORK HOLD TIME:  $t_h(net) = t_h(cell)$

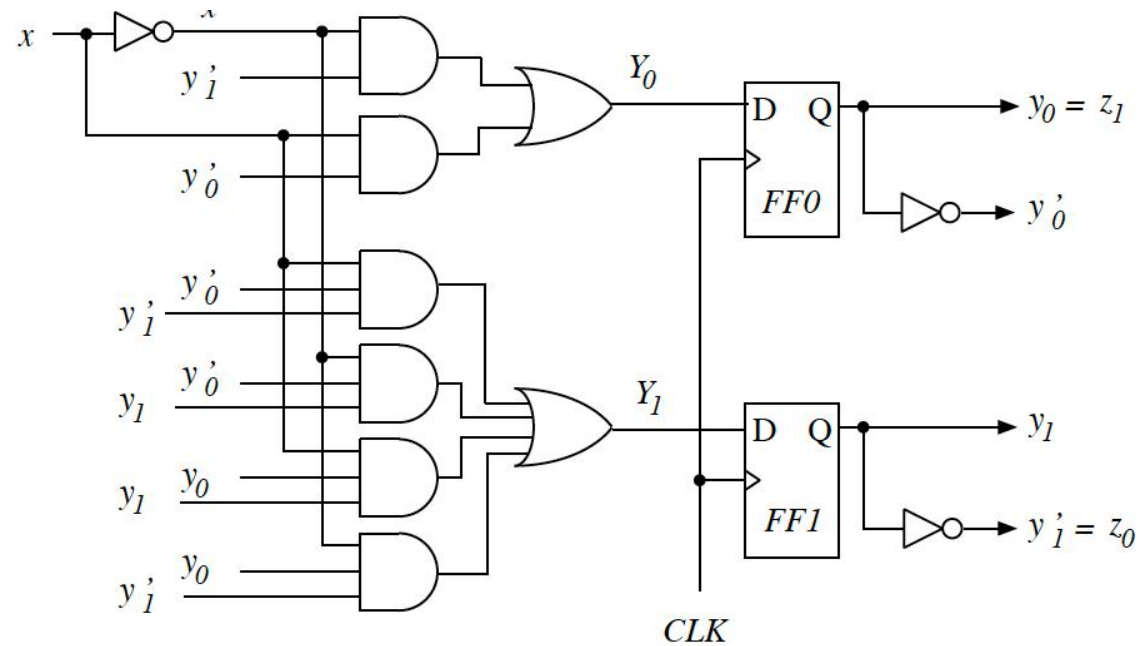


## TIMING FACTORS (Cont.)

- NETWORK PROPAGATION DELAY:  $t_p(net) = t_p(cell) + d2$



# ANALYSIS OF CANONICAL SEQUENTIAL NETWORKS



State transition  $Y_0 =$

$Y_1 =$

Output  $z_0 =$

$z_1 =$

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- STATE-TRANSITION AND OUTPUT FUNCTIONS:

$PS$	Input	
$y_1y_0$	$x = 0$	$x = 1$
00		
01		
10		
11		
	$Y_1Y_0$	$z_1z_0$
	$NS$	Output



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- CODES:

$x$	$x$	$z_1 z_0$	$z$	$y_1 y_0$	$s$
0	$a$	00	$c$	00	$S_0$
1	$b$	01	$d$	01	$S_1$
		10	$e$	10	$S_2$
		11	$f$	11	$S_3$

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- HIGH-LEVEL SPECIFICATION:

Input:  $x(t) \in \{a, b\}$

Output:  $z(t) \in \{c, d, e, f\}$

State:  $s(t) \in \{S_0, S_1, S_2, S_3\}$

Initial state:  $s(0) = S_2$

Functions: The state-transition and output functions

$PS$	$x(t) = a$	$x(t) = b$	
$S_0$	$S_1$	$S_3$	$d$
$S_1$	$S_3$	$S_0$	$f$
$S_2$	$S_2$	$S_1$	$c$
$S_3$	$S_0$	$S_2$	$e$
	$NS$		$z(t)$

$PS$	$x(t) = a$	$x(t) = b$	
$S_0$	$S_1$	$S_3$	$d$
$S_1$	$S_3$	$S_0$	$f$
$S_2$	$S_2$	$S_1$	$c$
$S_3$	$S_0$	$S_2$	$e$
	$NS$		$z(t)$

$x(t)$	$a$	$a$	$b$	$a$	$b$	$b$	$a$	$b$	$a$	$a$	$b$	$b$	$b$	$a$
$s(t)$	$S_2$													
$z(t)$	$c$													

## PROPAGATION DELAY $x$ to $z_0$ :

For  $x$  changes  $0 \rightarrow 1$  and  $z_0$  changes  $1 \rightarrow 0$

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SET-UP TIME:	$  \begin{aligned}  t_{su}(net) &= t_{pHL}(\text{NOT}) + t_{pHL}(\text{AND3}) \\  &\quad + t_{pHL}(\text{OR4}) + t_{su} \\  &= (0.05 + 0.017 \times 3) + (0.18 + 0.018) \\  &\quad + (0.45 + 0.025) + 0.3 \\  &= 1.07 \text{ [ns]}  \end{aligned}  $
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HOLD TIME:	$t_h(net) = 0.14 \text{ [ns]}$
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PROPAGATION DELAY:	$  \begin{aligned}  t_p(z_0) &= t_{pLH}(\text{FF}) + t_{pHL}(\text{NOT}) \\  &= (0.49 + 0.038 \times 3) \\  &\quad + (0.05 + 0.017 \times (L + 3)) \\  &= 0.70 + 0.017L \text{ [ns]} \\  &\quad (\text{load of NOT is } L + 3, \text{ load of FF is } 3)  \end{aligned}  $
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