CS M51A, Winter 2021, Assignment 10
(Total Mark: 90 points, 9%)

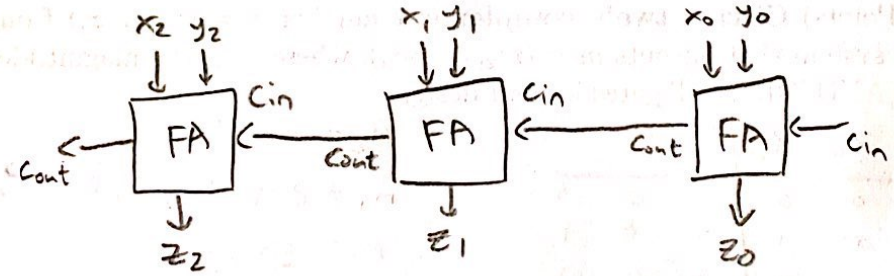
Due: Wed Mar 17rd, 10:00 AM Pacific Time

Student Name: Charles Zhang

Student ID: 305413659

Note: You must complete the assignments entirely on your own, without discussing with others.

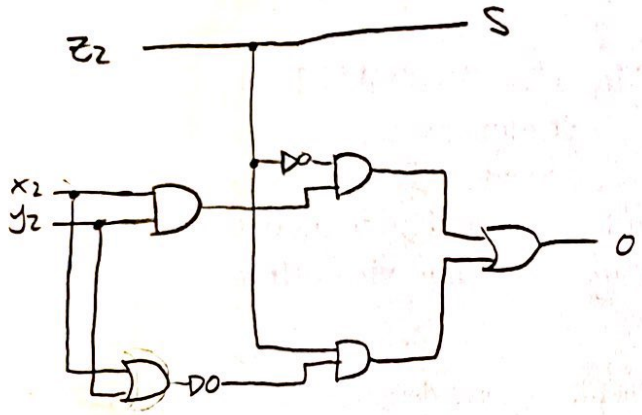
1. (a) (10 Points) Using only full adders, design an system that adds two 3-bit **2's complement** numbers, $x = (x_2, x_1, x_0)$ and $y = (y_2, y_1, y_0)$, and outputs the sum $z = (z_2, z_1, z_0)$. Assume that the addition will not overflow and label the inputs and outputs of the system.



(b) (15 Points) Given **2's complement** numbers $x = (x_2, x_1, x_0)$, $y = (y_2, y_1, y_0)$, and the sum $z = (z_2, z_1, z_0)$ from part (a), design a system that has two outputs, s and o. The output $s = 1$ when the sign of z is negative, and the output $o = 1$ if the addition from part (a) has overflown. You may use AND/OR/NOT gates in your design.

$S=1$ when $z_2=1$

$o=1$ if $x_2, y_2 = 0, z_2 = 1$
or $x_2, y_2 = 1, z_2 = 0$
or carry in $\neq$ carry out



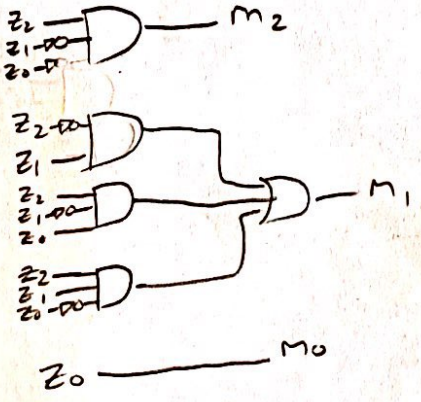
(c) (15 Points) Given a **two's complement** number $z = (z_2, z_1, z_0)$ from part (a), design a system that outputs $m = (m_2, m_1, m_0)$, where m is the magnitude of z. You may use AND/OR/NOT gates in your design.

z_2	z_1	z_0	m_2	m_1	m_0
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	0	1	1
1	1	0	0	1	0
1	1	1	0	0	1

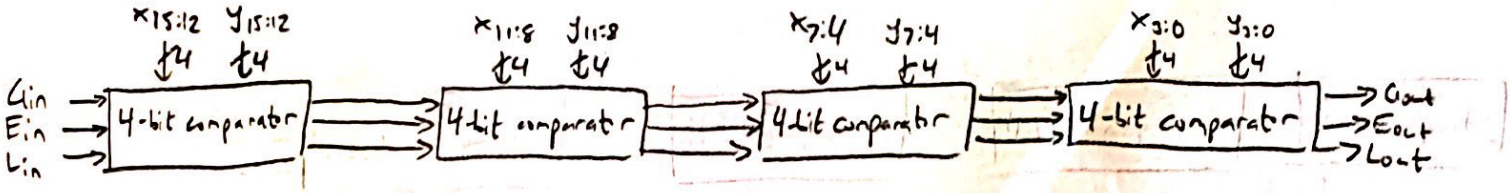
$m_2 = z_2 z_1' z_0'$

$m_1 = z_2' z_1 + z_2 z_1' z_0 + z_2 z_1 z_0'$

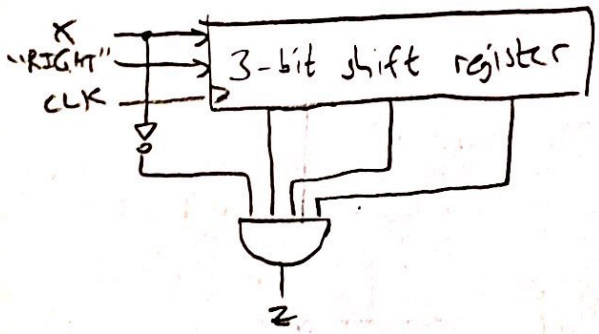
$m_0 = z_0$



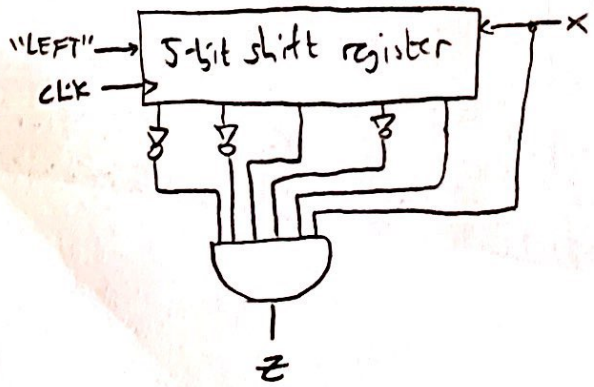
2. (10 Points) Design a 16-bit comparator using 4-bit comparators only.



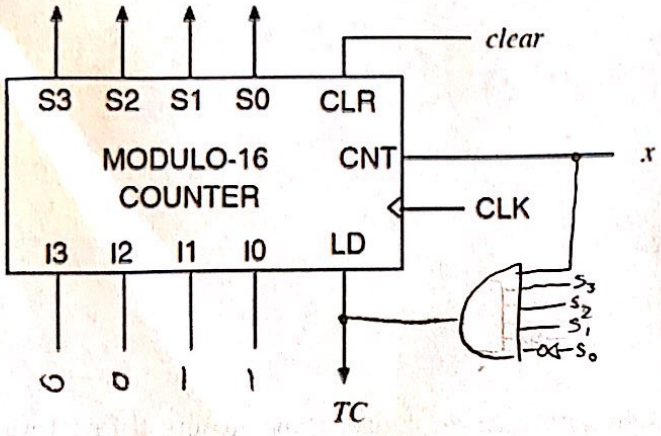
3. (10 Points) Design a pattern recognizer that outputs 1 if pattern 0111 is detected. You may use serial-in/parallel-out shift register and AND/OR/NOT gates in your design. **The shifting direction should be to the right.**



4. (10 Points) Design a pattern recognizer that outputs 1 if pattern 001011 is detected. You may use serial-in/parallel-out shift register and AND/OR/NOT gates in your design. **The shifting direction should be to the left.**



5. (10 Points) Using a modulo-16 counter and AND/OR/NOT gates, design a counter that counts from 3 to 14. → 1110



6. (10 Points) Using a modulo-16 counter and AND/OR/NOT gates, design a counter that outputs the following count: 14, 15, 0, 1, 2, 3, 14, 15, 0, 1, 2, 3, 14, 15, 0 ...

Load 14
by TC is 3 → 0011