

## CS151B/EE116C – Solutions to Sample Problem 1

Given a gate with an output signal O and k input signals I0, I1, I2, ..., Ik:

$$\text{DELAY}(O) = \text{MAX}(\text{DELAY}(I_0), \text{DELAY}(I_1), \dots, \text{DELAY}(I_k)) + \text{DELAY}(\text{k-input gate}).$$

Given a multiplexer with an output signal O, k input signals I0, I1, I2, ..., Ik, and selector S:

$$\text{DELAY}(O) = \text{MAX}(\text{DELAY}(S), \text{DELAY}(I_0), \text{DELAY}(I_1), \dots, \text{DELAY}(I_k)) + \text{DELAY}(\text{multiplexer}).$$

The sum of a 1-bit full adder is implemented as two cascaded 2-input XOR gates:

$$S_n = (A_n \wedge B_n) \wedge C_n$$

\*: AND

+: OR

^: XOR

**1.**

$$G_0 = A_0 * B_0$$

$$\text{Delay}(G_0) = 2T$$

**2.**

$$P_0 = A_0 \wedge B_0$$

$$\text{Delay}(P_0) = 2T$$

**3.**

$$G_3 = A_3 * B_3$$

$$\text{Delay}(G_3) = 2T$$

**4.**

$$P_3 = A_3 \wedge B_3$$

$$\text{Delay}(P_3) = 2T$$

- All  $G_n$  and  $P_n$  that govern a 1-bit adder have delay 2T.

**5.**

$$C_3 = G_2 + G_1 * P_2 + G_0 * P_1 * P_2 + C_0 * P_0 * P_1 * P_2$$

$$\text{Delay}(C_3) = 2T (P_0/P_1/P_2) + 7T (4\text{-input AND}) + 7T (4\text{-input OR}) = 16T$$

**6.**

$$C_4 = G_3 + G_2 * P_3 + G_1 * P_2 * P_3 + G_0 * P_1 * P_2 * P_3 + C_0 * P_0 * P_1 * P_2 * P_3$$

$$\text{Delay}(C_4) = 2T (P_0/P_1/P_2/P_3) + 9T (5\text{-input AND}) + 9T (5\text{-input OR}) = 20T$$

**7.**

$$S_3 = (A_3 \wedge B_3) \wedge C_3$$

$$\text{Delay}(S_3) = 16T (C_3) + 2T (2\text{-input XOR}) = 18T$$

**8.**

$$G\alpha = G3 + G2*P3 + G1*P2*P3 + G0*P1*P2*P3$$

- Delay( $G\alpha$ ) = 2T ( $G0/P1/P2/P3$ ) + 7T (4-input AND) + 7T (4-input OR) = 16T
- All  $Gx$  that govern a 4-bit CLA have delay 16T

**9.**

$$P\alpha = P0*P1*P2*P3$$

- Delay( $P\alpha$ ) = 2T ( $P0/P1/P2/P3$ ) + 7T (4-input AND) = 9T
- All  $Px$  that govern a 4-bit CLA have delay 9T.

**10.**

$$C12 = G\beta + G\alpha*P\beta + "C4"*P\alpha*P\beta$$

- “C4” is ready at time 0 due to the Carry Select technique. As a result, the product with “C4” has latency 9T ( $P\alpha/P\beta$ ) + 4T (3-input AND) = 13T while the  $G\alpha*P\beta$  term has delay 16T ( $G\alpha$ ) + 2T (2-input AND) = 18T. As a result the latter term is the product with the highest latency.
- Delay( $C12$ ) = 16T ( $G\alpha$ ) + 2T (2-input AND) + 4T (3-input OR) = 22T

**11.**

$$C16 = G\gamma + G\beta*P\gamma + G\alpha*P\beta*P\gamma + "C4"*P\alpha*P\beta*P\gamma$$

- Delay( $C16$ ) = 16T ( $G\alpha$ ) + 4T (3-input AND) + 7T (4-input OR) = 27T

**12.**

$$S15 = (A15 \wedge B15) \wedge C15$$

- To get the delay of  $S15$ , we need to find  $C15$  which is a function of the 4-bit CLA with label  $\gamma$ .

$$C15 = G14 + G13*P14 + G12*P13*P14 + C12*P12*P13*P14$$

- The formula for  $C15$  is comparable to the formula for  $C3$ . However, while  $C3$  dealt with  $C0$  which was ready at time 0,  $C15$  deals with the carry in to the 4-bit CLA which is  $C12$ .
- Delay( $C15$ ) = 22T ( $C12$ ) + 7T (4-input AND) + 7T (4-input OR) = 36T
- Delay( $S15$ ) = 36T ( $C15$ ) + 2T (2-input XOR) = 38T

**13.**

$$\text{Delay}(G\omega) = 16T$$

**14.**

$$\text{Delay}(P\omega) = 9T$$

**15.**

$$C28 = G\psi + G\chi*P\psi + G\phi*P\chi*P\psi + "C16"*P\phi*P\chi*P\psi$$

- The formula for  $C28$  is comparable to the formula for  $C16$ .  $C16$  dealt with carry-in “C4” which was ready at time 0 while  $C28$  deals with the carry-in “C16” which is also ready at time 0 due to the Carry Select technique. As a result, the latencies are identical.
- Delay( $C28$ ) = 16T ( $G\phi$ ) + 4T (3-input AND) + 7T (4-input OR) = 27T

**16.**

$$C32 = G\omega + G\psi * P\omega + G\chi * P\psi * P\omega + G\phi * P\chi * P\psi * P\omega + "C16" * P\phi * P\chi * P\psi * P\omega$$

- Delay(C32) = 16T (Gφ) + 7T (4-input AND) + 9T (5-input OR) = 32T

**17.**

$$S31 = (A31 \wedge B31) \wedge C31$$

- This process of determining S31 is comparable to determining the delay of S15 and requires C31.

$$C31 = G30 + G29 * P30 + G28 * P29 * P30 + C28 * P28 * P29 * P30$$

- Delay(C31) = 27T (C28) + 7T (4-input AND) + 7T (4-input OR) = 41T
- Delay(S31) = 41T (C31) + 2T (2-input XOR) = 43T

**18.**

C16(after) has inputs C16(before) (ready at 27T) and selector C4 (ready at 20T)

- Delay(C16(after)) = 27T (C16(before)) + 4T (latency of multiplexer) = 31T

**19.**

C32(after) has inputs C32(before) (ready at 32T) and selector C16(after) (ready at 31T)

- Delay(C32(after)) = 32T (C32) + 4T (latency of multiplexer) = 36T

The maximal delay is the maximum latency of the output signals:

- Delay(S3) = 20T
- Delay(S4-S15(after)) = 38T (S15) + 4T (latency of multiplexer) = 42T
- Delay(S16-S31(after)) = 43T (S31) + 4T (latency of multiplexer) = 47T
- Delay(C32(after)) = 36T

**Maximal Delay: 47T**