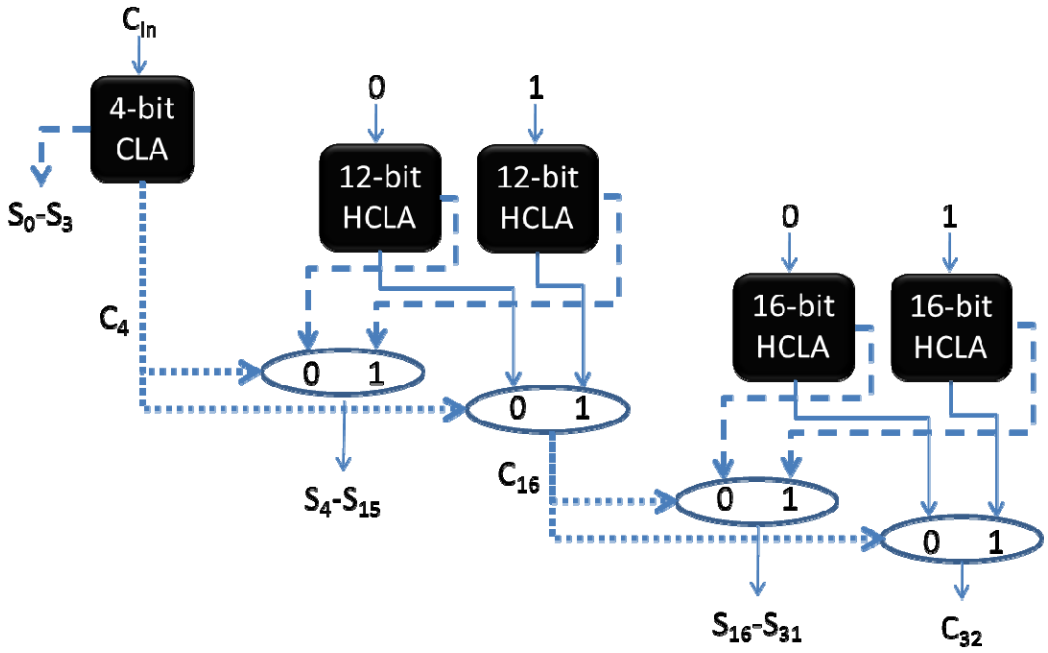
3. Assume for the rest of this problem that all logic gates have the following delays:

Fan In	Delay
1	T
2	2T
3	4T
4	7T
5	9T
6 or more	2T x fan-in

So a 2-input AND gate would have delay 2T and a 4-input OR gate would have delay 7T. For simplicity, assume that mux's have delay 4T regardless of fan-in.

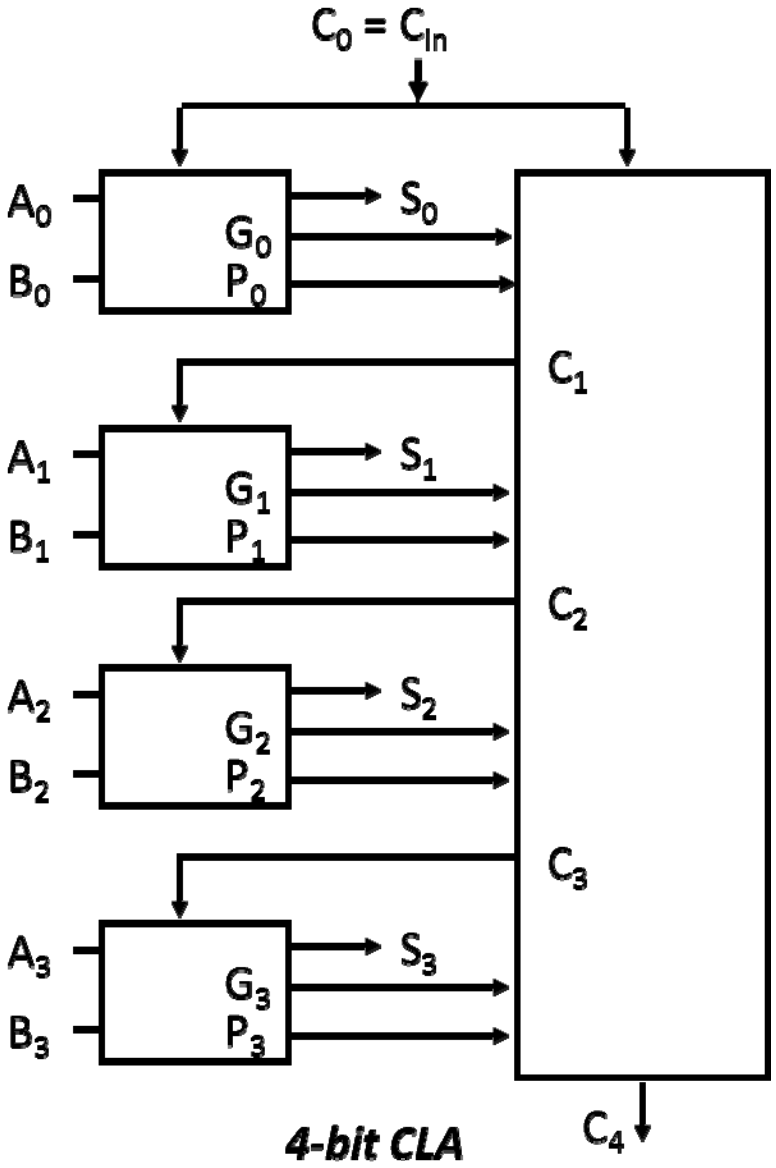
We will create a 32-bit adder out of some building blocks we've covered in class. We will use the 4-bit carry lookahead (4-bit CLA) that we covered in class as one basic building block of this design. And we will use it (as we did in class) to make a 16-bit hierarchical CLA (16-bit HCLA). And we will also use it to make a 12-bit hierarchical CLA (12-bit HCLA). But instead of connecting these in series to make a 32-bit adder, we will use carry select to speed up the 32-bit adder. The design will look as follows (be sure to note where we are using the 4-bit CLA and where we are using the 12-bit and 16-bit HCLAs):



Note that the 4-bit CLA is computing the sum of inputs A_0-A_3 and B_0-B_3 (i.e. producing sums S_0-S_3), the 12-bit HCLA is computing the sum of inputs A_4-A_{15} and B_4-B_{15} (i.e. producing sums S_4-S_{15}), the 16-bit HCLA is computing the sum of inputs A_{16}-A_{31} and B_{16}-B_{31} (i.e. producing sums S_{16}-S_{31}). The carry out of the 4-bit CLA selects the sums and carry out of the 12-bit HCLA. The carry out of the 12-bit HCLA selects the sums and carry out of the 16-bit HCLA. The 0 or 1 at the top of each HCLA is the hardwired C_{in}. Multiplexers are shown as ovals.

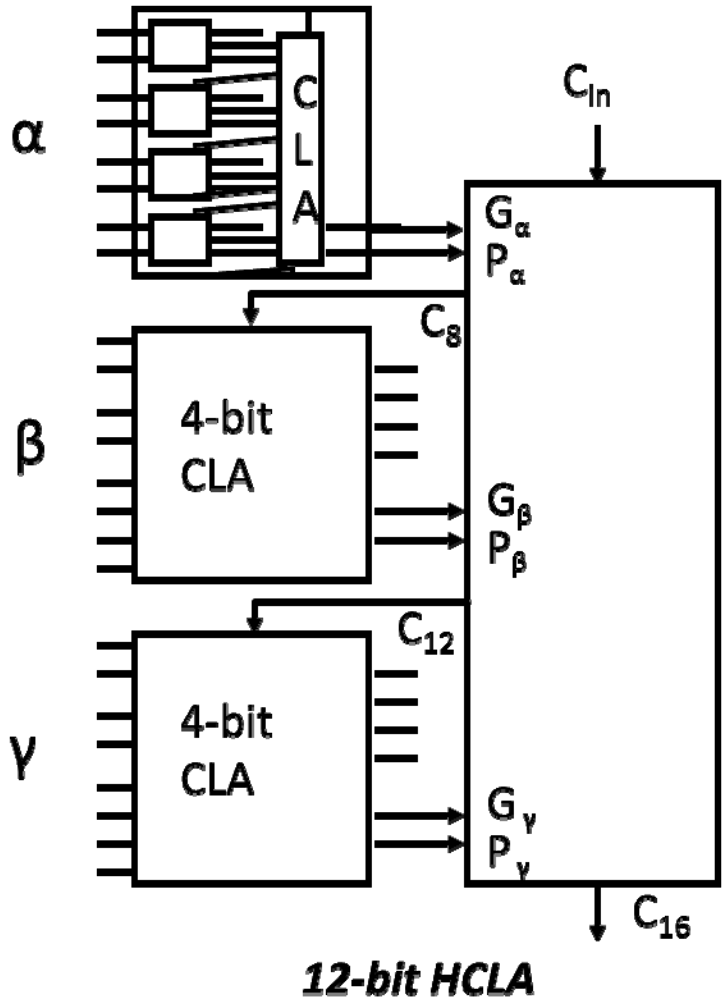
Your task is to find the maximal delay of this design – i.e. determine the delays of S_{0-31} and C_{32} – the maximal delay of these outputs will be the maximal delay of the entire design. To do this (and to help with possible partial credit) please use the diagrams on the following pages and fill in the tables in every page.

4-bit CLA:



Output	Delay (in terms of T)	
G0		*(2 points)*
P0		*(2 points)*
G3		*(2 points)*
P3		*(2 points)*
C3		*(2 points)*
C4 (just in this figure)		*(2 points)*
S3		*(2 points)*

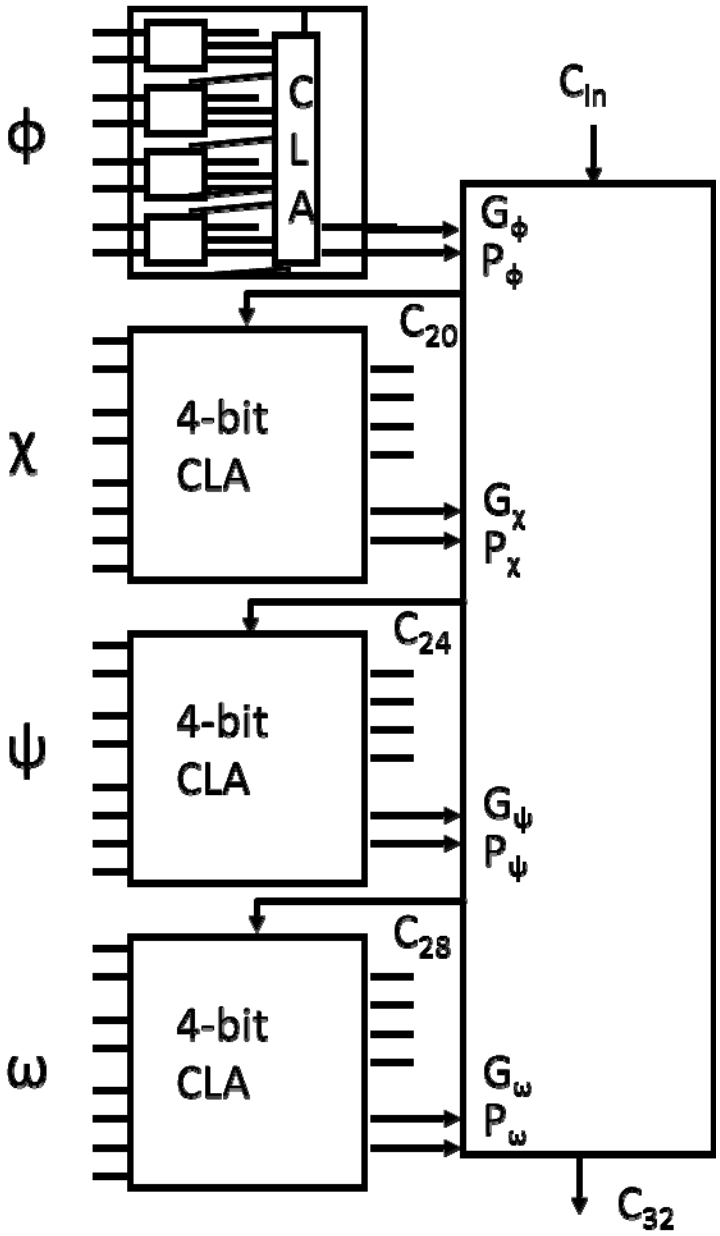
12-bit HCLA:



12-bit HCLA

Output	Delay (in terms of T)	
Gα		*(2 points)*
Pα		*(2 points)*
C12		*(2 points)*
C16 (just in this figure)		*(2 points)*
S15		*(2 points)*

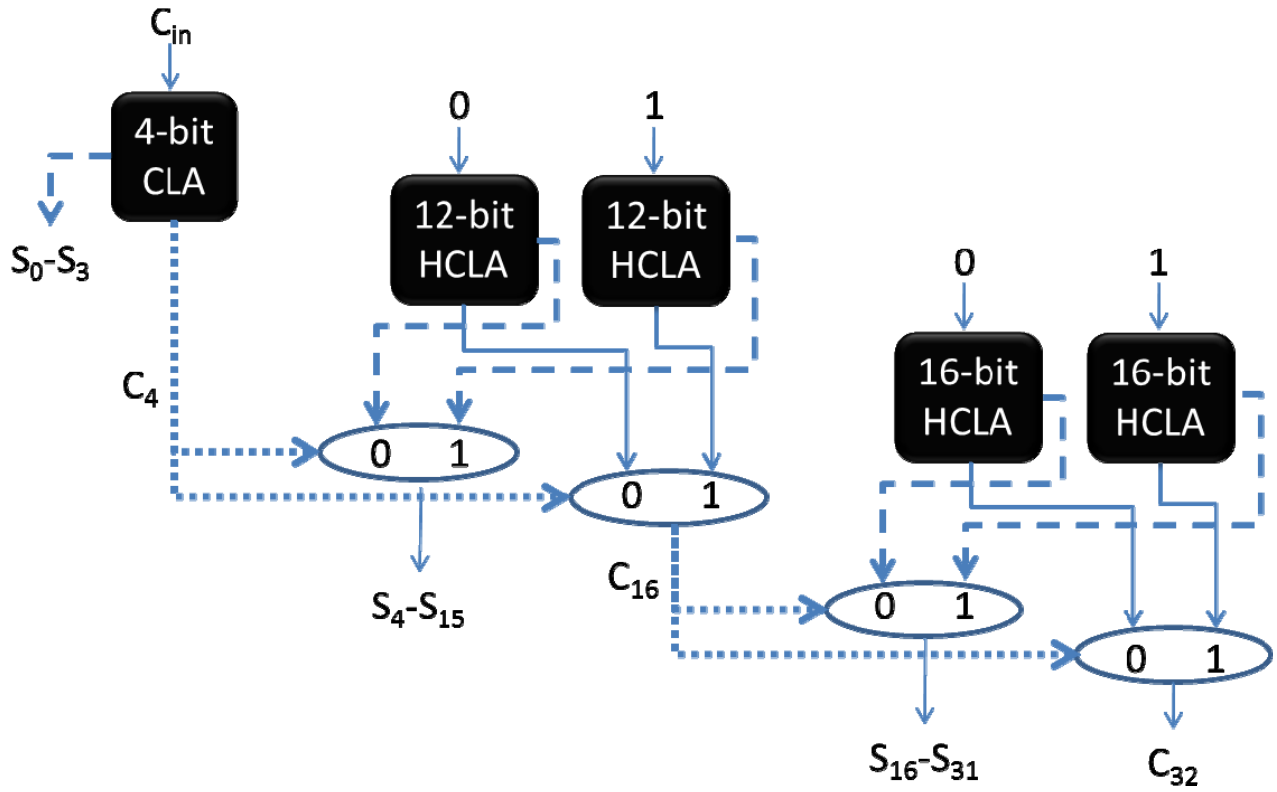
16-bit HCLA:



16-bit HCLA

Output	Delay (in terms of T)	
Gω		*(2 points)*
Pω		*(2 points)*
C28		*(2 points)*
C32 (just in this figure)		*(2 points)*
S31		*(2 points)*

Entire Design:



Output	Delay (in terms of T)
C16	
C32	

(2 points)
(2 points)

Find the maximum delay **in terms of T** of the 32-bit adder – take the maximum of all output bits – including the sum bits (S_0-S_{31}) and the final carry out (C_{32}).

Maximal Delay: _____ *(2 points)*