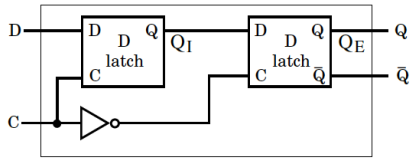
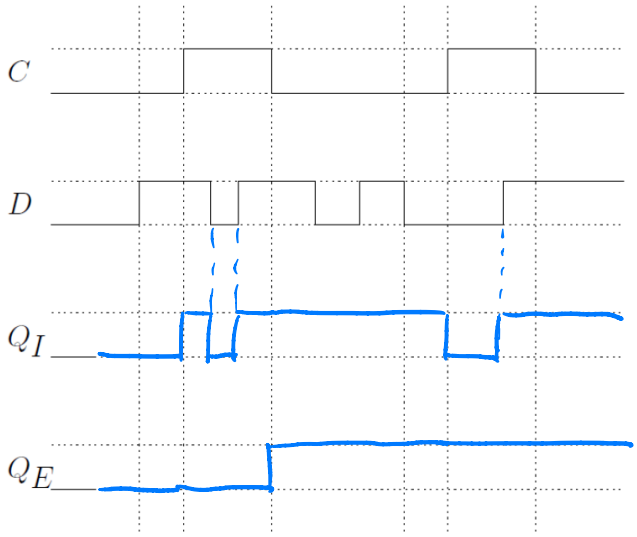
CS M51A, Winter 2021, Assignment 7
(Total Mark: 90 points, 9%)

Due: Wed Feb 24th, 10:00 AM Pacific Time
Student Name:
Student ID:
Note: You must complete the assignments entirely on your own, without discussing with others.

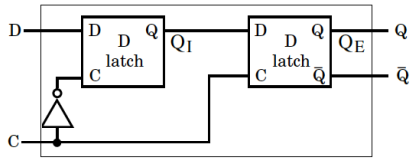
1. (10 Points) Consider the D flip-flop illustrated in the diagram below:



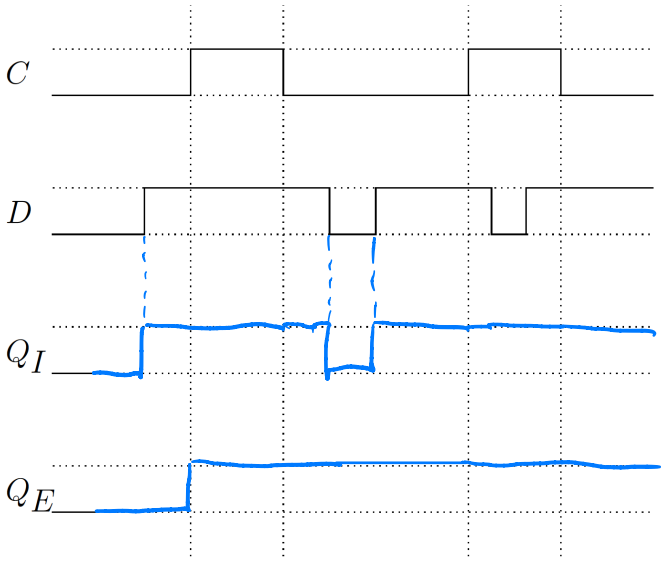
In the Figure below are traces of C and D; draw the resulting traces of QI and QE.



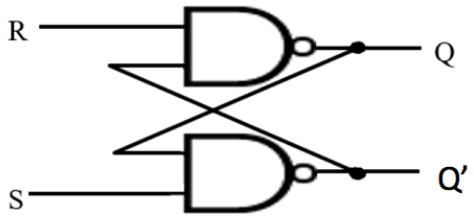
2. (10 Points) Now consider when we move the inverter in the D flip-flop illustrated in the diagram below:



In the Figure below are traces of C and D; draw the resulting traces of QI and QE.



3. In class, we designed an SR-latch using NOR gates. Suppose instead we try to implement it using NAND gates as given below:



(a) (4 Points) What setting of R and S sets Q to 1 and Q' to 0?

S = 1
R = 0

(b) (4 Points) What setting of R and S sets Q to 0 and Q' to 1?

S = 0
R = 1

(c) (4 Points) What setting of R and S sets Q to Q and Q' to Q'?

S = R = 1

4. A PN flip-flop has four operations: 0(reset), 1(set), no change (output remains unchanged) and toggle (output changes to its complement), when inputs P and N are 00, 01, 10, 11, respectively.

(a) (4 Points) If we use $Q(t)$ to represent the output of a PN flip-flop at time t, fill in the following table:

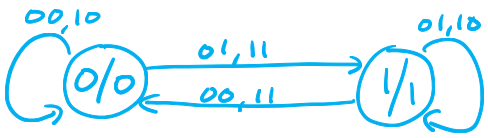
P	N	$Q(t+1)$
0	0	0
0	1	1
1	0	$Q(t)$
1	1	$Q(t)'$

(b) (4 Points) Write the expression for $Q(t+1)$ in terms of present input (P and N) and state $Q(t)$.

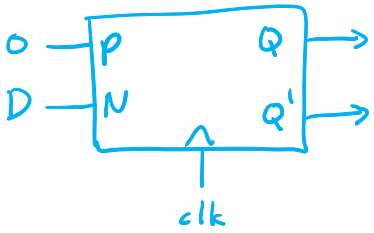
$$Q(t+1) = P'N + PN'Q(t) + PNQ(t)'$$

(c) (14 Points) Show the state transition table and state diagram of a PN flip-flop with input($P \in \{0,1\}$ and $N \in \{0,1\}$), output ($z = Q(t)$) and state ($Q(t) \in 0, 1$).

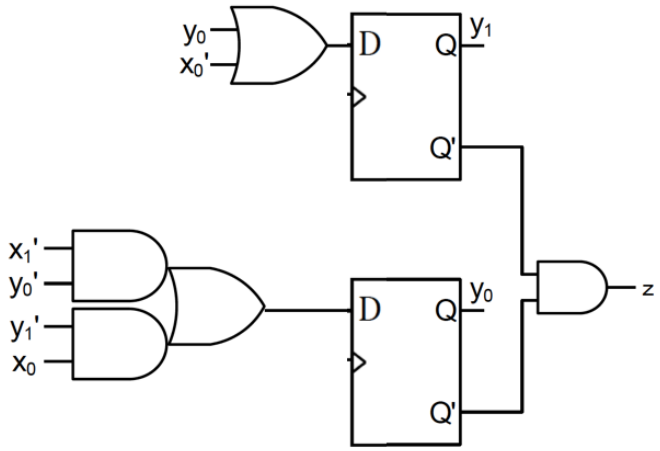
PS \ Input PN	00	01	10	11	output
0	0	1	0	1	0
1	0	1	1	0	1
NS					



(d) (4 Points) Show how a PN flip-flop can be converted to a D flip-flop.



5. We would like to analyze the following sequential network. It has two input bits x_1 and x_0, with a single output bit z. Note, both D Flip-flops connect to the same CLK, not shown in the figure for simplicity.



(a) (4 Points) Write expressions for z, $y_1(t+1)$ and $y_0(t+1)$ in terms of inputs (x_1 and x_0) and present states (y_1 and y_0).

$z = y_1' y_0'$ $\quad y_1(t+1) = y_0 + x_0'$

$y_0(t+1) = x_1' y_0' + y_1' x_0$

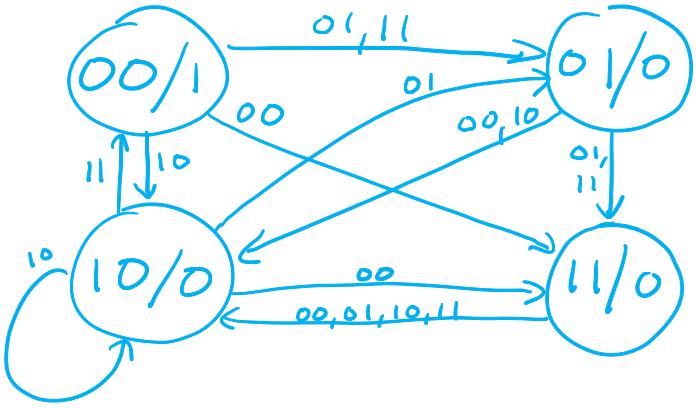
(b) (8 Points) Using the expressions, fill in the table below.

PS	Input $x_1(t)x_0(t)$				Output
$y_1(t)y_0(t)$	00	01	10	11	z
00	11	01	10	01	1
01	10	11	10	11	0
10	11	01	10	00	0
11	10	10	10	10	0
	$y_1(t+1)y_0(t+1)$				
	NS				

(c) (4 Points) Is this a Moore or Mealy machine?

Moore

(d) (8 Points) Draw the state diagram for this system



6. (4 Points) For a sequential network, what is a set-up time and hold time? Please describe.

set-up time: minimal time interval from input to the triggering edge

hold time: minimal time interval from the triggering edge to the next change of input

7. (4 Points) Explain how does the Master-slave architecture realize the edge-triggering mechanism. You may use the Master-slave D Flip-flip as an example.

(a) before the triggering edge, input is saved into the first latch but does not affect the second one.

(b) when the triggering edge comes, the saved input/output of the first latch is transmitted to the second one.(becomes output)

(c) after the triggering edge, the output of the first latch/the input of the second latch remain unchanged, therefore the output is also unchanged.