CS M51A, Winter 2021, Assignment 3
(Total Mark: 90 points, 9%)

Due: Wed Jan 27, 10:00 AM Pacific Time

Student Name:
Student ID:
Note: You must complete the assignments entirely on your own, without discussing with others.

1. (12 points) Obtain the equivalent sum of minterms and product of maxterms for the following expressions. You're required to use m- and M-notations ($\Sigma m(\cdots)$ and $\Pi M(\cdots)$).

   (a) A'B + AC + BC

   (b) A'B(AB + C)(B+A'C')

   (c) A' + A(A'B + B'C)'

2. F is a function that accepts inputs $x \in \{0, 1, 2\}$, $y \in \{1, 2, 3\}$ and outputs $z = max(x^2, y)$. Suppose you use unsigned binary code to encode x, y, and z. x is encoded as x_1x_0, y is encoded as y_1y_0, z is encoded as $z_2z_1z_0$.
(a) (6 Points) Fill the following table (Note: $z_2z_1z_0$ should output zero for invalid inputs)

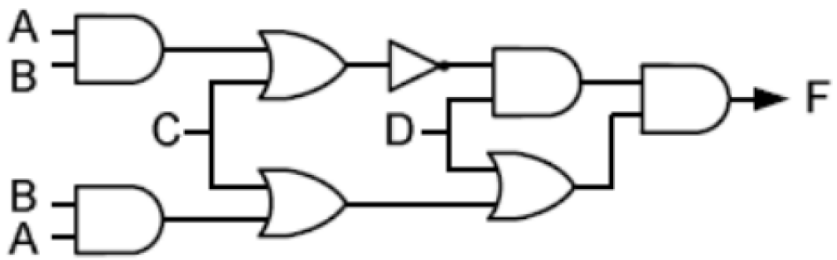
x_1	x_0	y_1	y_0	z_2	z_1	z_0
0	0	0	0			
0	0	0	1			
0	0	1	0			
0	0	1	1			
0	1	0	0			
0	1	0	1			
0	1	1	0			
0	1	1	1			
1	0	0	0			
1	0	0	1			
1	0	1	0			
1	0	1	1			
1	1	0	0			
1	1	0	1			
1	1	1	0			
1	1	1	1			

(b) (12 points) write the sum of minterms and product of maxterms expressions for z ($z_0 = \cdots$, $z_1 = \cdots$, $z_2 = \cdots$, the boolean variables are $\{x_0, x_1, y_0, y_1\}$).

3. (a) (6 Points) Given the following function: $F = AB + \bar{B}\bar{C} + \bar{A}C$. Draw a symbol level design to implement F using only AND gates, OR gates and NOT gates.

(b) (6 Points) Draw a design to implement F using only NAND gates and NOT gates.

4. (8 Points) For the switching circuit given below, give the Sum-of-Product (SOP) and Product-of-Sum (POS) expressions of F.



5. A logical family has the following ranges of voltages to represent the high and low values: HIGH=3.5V to 5.0V, LOW=0.0V to 1.5V.

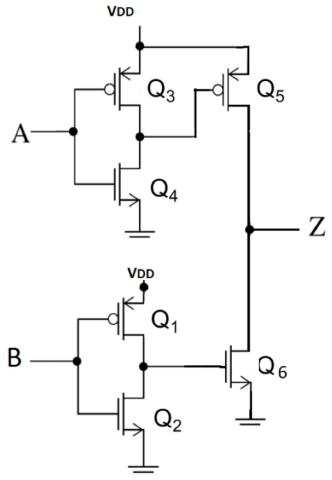
   (a) (4 Points) For the following signal values, determine the corresponding logic values:

   - 1.0V.
   - 4.5V.
   - 2.0V.
   - -1.0V.

   (b) (4 Points)For a module with inputs x and y and output z you have performed the following set of measures (all in volts): What type of gate does this circuit implement?

x	y	z
0.3	0.3	0.5
0.3	4.5	4.4
4.5	0.2	4.4
4.5	4.5	0.2

6. (a) (14 Points) Given the circuit below, complete the table below, determining the resistances for Q_1 to Q_6 and the final output Z. The transistors Q_1 to Q_6 should be High or Low (show by 'H' or 'L') resistance. The output Z may be 0, 1, float (show by –) or short (show by *). Remember short means the output is connected to both VDD and ground at the same time.



A	B	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Z
0	0							
0	1							
1	0							
1	1							

(b) (2 Points)Explain why we would not use the transistor configuration given above in practice.

7. (a) (4 Points) Draw a circuit (using PMOS and NMOS transistors) which performs F=(A+B+C). Do not use more than 8 transistors in total.

(b) (4 Points) Draw a circuit (using PMOS and NMOS transistors) which performs F=(A'+B'+C'). Do not use more than 6 transistors in total.

8. (a)(4 Points) Write the boolean algebra function for the following table.

A	B	F
0	0	1
0	1	0
1	0	1
1	1	1

(b) (4 Points) Implement the function from part (a) using PMOS and NMOS transistors. Use at most 6 transistors total.