LA Worksheet #10

1. RISC has fewer instructions with fixed address lengths, resulting in more memory usage, but easier translation.
CISC has more complex instructions of variable lengths, allowing for more efficient memory usage.

2. a) add 0x200(,%rdx,4),%rcx
add $t2, $t0, $t0 # 2*rdx
add $t2, $t2, $t2 # 4 rdx
addi $t2, $t2, 512 # add disp.
lw $t2, 0($t2) # get val.
add $t1, $t1, $t2 # add
b) lea 0xc(%rdi),%rax
%rdi = $t0, %rax = $t1
addi $t1, $t0, 12
c) mov 0x30(%rsp,%rbx,4),%rax
%rsp = $sp, %rbx = $t0, %rax = $t1
add $t2, $t0, $t0 # 2rbx
add $t2, $t2, $t2 # 4rbx
add $t3, $sp, $t2 # 4rbx + rsp
lw $t1, 48($t3) # mov
d) mov %rcx, -0x30(%rsp,%rdx,4)
%rsp = $sp, %rdx = $t0, %rcx = $t1
add $t2, $t0, $t0 # 2 rdx
add $t2, $t2, $t2, # 4rdx
add $t3, $t2, $sp # 4rdx + rsp
sw $t1, -48($t3) # mov

3. $s0 = rdi, $s1 = rsi, $t0 = rdx
li $t0, 0
.loop slt $t3, $t0, 5 # condition
beq $t2, 0, leaveloop
add $s0, $s0, $s1
addi $t0, $t0, 1
j loop

4. Iterates thru an array of pointers and adds ($s1) to each item.

5. False sharing is when one thread modifies the cache, and, in order to maintain cache coherence, other threads must update their cache, even if the updated variable wasn't being used.