CS M51A, Winter 2021, Assignment 7
(Total Mark: 90 points, 9%)

Due: Wed Feb 24th, 10:00 AM Pacific Time

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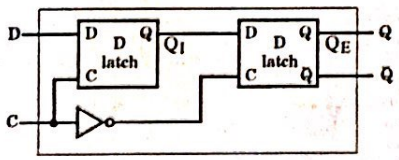
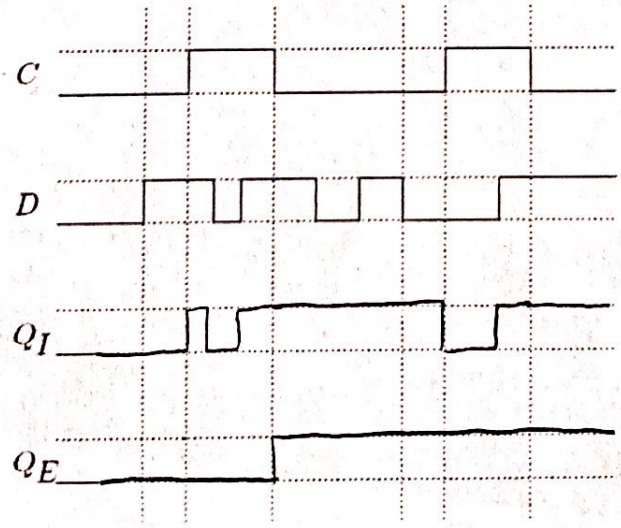
Note: You must complete the assignments entirely on your own, without discussing with others.

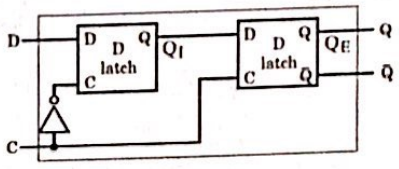
1. (10 Points) Consider the D flip-flop illustrated in the diagram below:



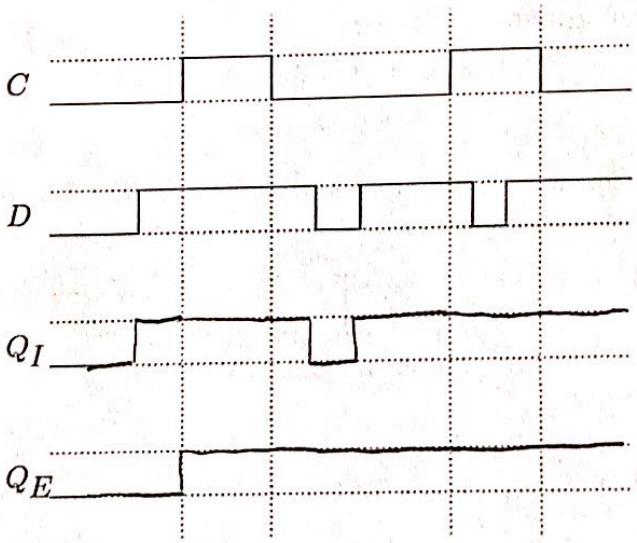
In the Figure below are traces of C and D; draw the resulting traces of QI and QE.



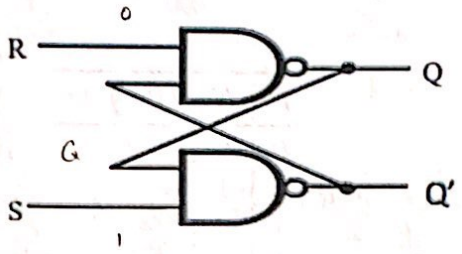
2. (10 Points) Now consider when we move the inverter in the D flip-flop illustrated in the diagram below:



In the Figure below are traces of C and D; draw the resulting traces of QI and QE.



3. In class, we designed an SR-latch using NOR gates. Suppose instead we try to implement it using NAND gates as given below:



(a) (4 Points) What setting of R and S sets Q to 1 and Q' to 0?

R=0, S=1

(b) (4 Points) What setting of R and S sets Q to 0 and Q' to 1?

R=1, S=0

(c) (4 Points) What setting of R and S sets Q to Q and Q' to Q'?

R=1, S=1

4. A PN flip-flop has four operations: 0(reset), 1(set), no change (output remains unchanged) and toggle (output changes to its complement), when inputs P and N are 00, 01, 10, 11, respectively.

(a) (4 Points) If we use $Q(t)$ to represent the output of a PN flip-flop at time t, fill in the following table:

P	N	$Q(t+1)$
0	0	0
0	1	1
1	0	$Q(t)$
1	1	$Q(t)'$

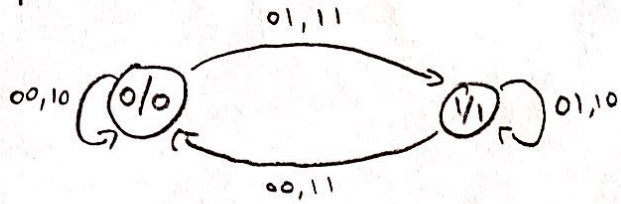
(b) (4 Points) Write the expression for $Q(t+1)$ in terms of present input (P and N) and state $Q(t)$.

P	N	Q(t)	Q(t+1)
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

$Q(t+1) = P'N + PN'Q(t) + PNQ(t)'$

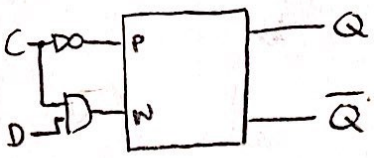
(c) (14 Points) Show the state transition table and state diagram of a PN flip-flop with input($P \in \{0,1\}$ and $N \in \{0,1\}$), output ($z = Q(t)$) and state ($Q(t) \in 0, 1$).

	Input (PN)				
PS: Q(t)	PN=00	PN=01	PN=10	PN=11	z
0	0	1	0	1	0
1	0	1	1	0	1
	NS, Q(t+1)				

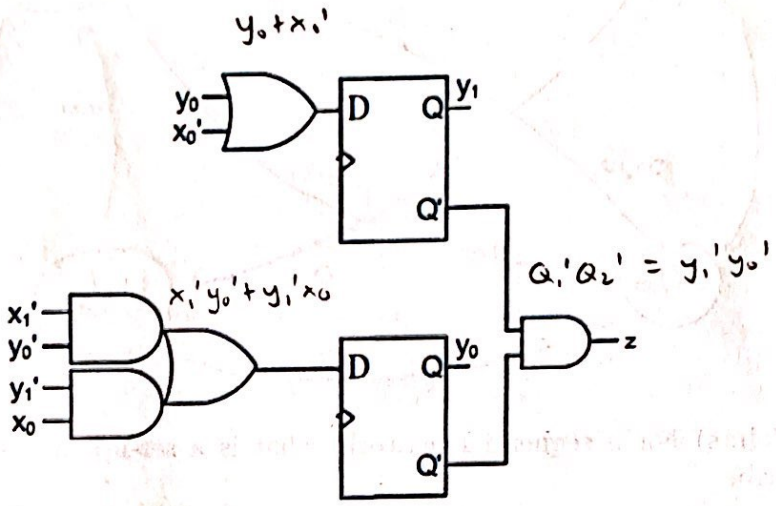


(d) (4 Points) Show how a PN flip-flop can be converted to a D flip-flop.

C	D	Q(t+1)	P	N
0	0	Q(t)	1	0
0	1	Q(t)	1	0
1	0	0	0	0
1	1	1	0	1



5. We would like to analyze the following sequential network. It has two input bits x_1 and x_0, with a single output bit z. Note, both D Flip-flops connect to the same CLK, not shown in the figure for simplicity.



(a) (4 Points) Write expressions for z, $y_1(t+1)$ and $y_0(t+1)$ in terms of inputs (x_1 and x_0) and present states (y_1 and y_0).

$z = y_1'y_0'$

$y_1(t+1) = x_0' + y_0$

$y_0(t+1) = x_1'y_0' + x_0y_1'$

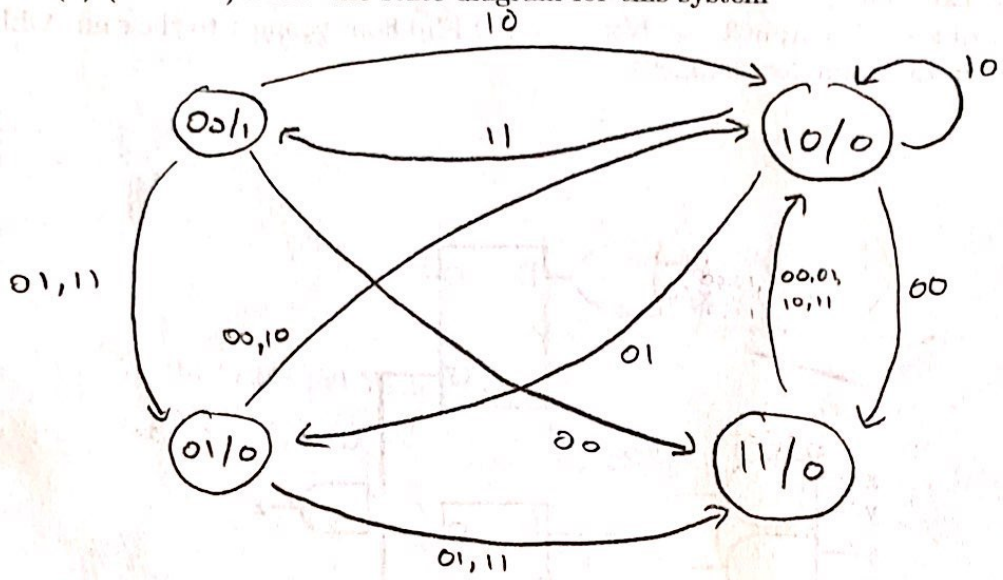
(b) (8 Points) Using the expressions, fill in the table below.

PS	Input $x_1(t)x_0(t)$				Output
$y_1(t)y_0(t)$	00	01	10	11	z
00	11	01	10	01	1
01	10	11	10	11	0
10	11	01	10	00	0
11	10	10	10	10	0
	$y_1(t+1)y_0(t+1)$				
	NS				

(c) (4 Points) Is this a Moore or Mealy machine?

Moore

(d) (8 Points) Draw the state diagram for this system

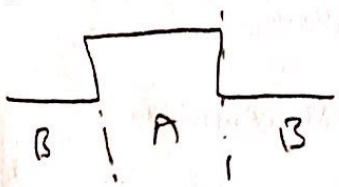


6. (4 Points) For a sequential network, what is a set-up time and hold time? Please describe.

Set-up time is the amount of time before a clock pulse (rising/falling edge) that you hold your input constant in order to account for the propagation delay of the preceding combinational network.
Hold time is the amount of time after a clock pulse that you hold your input constant in order to account for the propagation delay of the sequential network.

7. (4 Points) Explain how does the Master-slave architecture realize the edge-triggering mechanism. You may use the Master-slave D Flip-flip as an example.

By putting 2 D-latches in series and inverting the clock on one of them, one D-latch can change state when the clock is 1, and the other can change state when the clock is 0:



This filters out the original input so that any changes to the Q of the second D-latch only occur at the edges of the clock input.