21W-COMSCIM51A-1 Homework 7

CHARLES ZHANG

TOTAL POINTS

90 / 90

QUESTION 1

1 1 10 / 10

✓ - 0 pts Correct

![Screen_Shot_2021-02-19_at_5.22.01_PM.png](/files/f2892615-edcd-4548-a738-84dac38a56b0)

- **1 pts** Minor error in $$Q_I$$
- **3 pts** Major error in $$Q_I$$
- **5 pts** Blank in $$Q_I$$
- **1 pts** Minor error in $$Q_E$$
- **3 pts** Major error in $$Q_E$$
- **4 pts** Blank in $$Q_E$$

QUESTION 2

2 2 10 / 10

✓ - 0 pts Correct

![Screen_Shot_2021-02-19_at_5.23.24_PM.png](/files/aaaed2c0-9165-4bd3-b3d4-fedfb11eed4b)

- **1 pts** Minor error in $$Q_I$$
- **3 pts** Major error in $$Q_I$$
- **5 pts** Blank in $$Q_I$$
- **1 pts** Minor error in $$Q_E$$
- **3 pts** Major error in $$Q_E$$
- **5 pts** Blank in $$Q_E$$

QUESTION 3

3 12 pts

3.1 a 4 / 4

✓ - 0 pts Correct **$$S=1,R=0$$**

- **2 pts** Error in S
- **2 pts** Error in R

3.2 b 4 / 4

✓ - 0 pts Correct **$$S=0,R=1$$**

- **2 pts** Error in S
- **2 pts** Error in R

3.3 c 4 / 4

✓ - 0 pts Correct **$$S=1,R=1$$**

- **2 pts** Error in S
- **2 pts** Error in R

QUESTION 4

4 26 pts

4.1 a 4 / 4

✓ - 0 pts Correct

![4a.PNG](/files/93a78af4-4d53-417f-99ec-21e1bb3cceab)

- **1 pts** Error in first row
- **1 pts** Error in second row
- **1 pts** Error in third row
- **1 pts** Error in forth row

4.2 b 4 / 4

✓ - 0 pts Correct

![4b.PNG](/files/04b7a363-406f-4817-9c6e-6ff8221bbe2e)

- **0.5 pts** Contains constant 0 and 1 in expression
- **1 pts** Single error (missing / extra P or N or negation in a term)
- **3 pts** Incorrect expression
- **4 pts** Blank

4.3 c 14 / 14

✓ - 0 pts Correct

![4c.PNG](/files/ae238b0a-577f-4d5e-a92c-

7f94e3d0f591)

- **8 pts** More/less than 2 states
- **2 pts** Transition table: first row incorrect
- **2 pts** Transition table: second row incorrect
- **3 pts** State diagram outputs incorrect
- **2 pts** State diagram: one transition incorrect
- **4 pts** State diagram: two transitions incorrect
- **6 pts** State diagram: three transitions incorrect
- **8 pts** State diagram: all four transitions incorrect

4.4 d 4 / 4

✓ **- 0 pts Either is correct:**

![4d.PNG](/files/e1efabf0-94aa-40fc-a18b-2ff476c0ff5e)

![qq.png](/files/46e2d4e9-fbf6-4d44-9a29-2fd64894b9a4)

- **1 pts** Minor error (eg: used constant 1 instead of 0, or switched the two inputs, etc.)
- **2.5 pts** Incorrect
- **4 pts** Used D as input to P and D' as input to N
- **4 pts** Blank

QUESTION 5

5 24 pts

5.1 a 4 / 4

✓ **- 0 pts Correct**

![5a.PNG](/files/4af03f1e-c54e-40a2-b978-ad7759742382)

- **1 pts** z incorrect
- **1 pts** $$y_{0}(t+1)$$ incorrect
- **1 pts** $$y_{1}(t+1)$$ incorrect
- **4 pts** Blank

5.2 b 8 / 8

✓ **- 0 pts Correct**

![5b.PNG](/files/a9025a63-5864-4852-892c-aa2ac55fc934)

- **1.5 pts** Error in first row next states
- **1.5 pts** Error in second row next states
- **1.5 pts** Error in third row next states
- **1.5 pts** Error in forth row next states
- **2 pts** Error in output

5.3 c 4 / 4

✓ **- 0 pts Correct: Moore**

- **3.5 pts** Incorrect: Mealy
- **4 pts** Blank

5.4 d 8 / 8

✓ **- 0 pts Correct**

- **0.5 pts** State 00 incorrect output
- **1.5 pts** State 00 incorrect transitions
- **0.5 pts** State 01 incorrect output
- **1.5 pts** State 01 incorrect transitions
- **0.5 pts** State 10 incorrect output
- **1.5 pts** State 10 incorrect transitions
- **0.5 pts** State 11 incorrect output
- **1.5 pts** State 11 incorrect transitions

QUESTION 6

6 6 4 / 4

✓ **- 0 pts Correct; Example answer: `setup time`: minimal interval between the (stable) _input_ and the _triggering edge_ (_clock pulse_); `hold time`: minimal interval that the input should be _kept unchanged_(_hold_) after the _triggering edge_(_clock pulse_)**

- **1 pts** Minor error in set-up time
- **1 pts** Minor error in hold time
- **4 pts** Blank

QUESTION 7

7 7 4 / 4

✓ **- 0 pts Correct; Key statement: master and slave latch works on different but consecutive phases of a single clock pulse.**

- **1 pts** Minor error
- **4 pts** Blank

CS M51A, Winter 2021, Assignment 7
(Total Mark: 90 points, 9%)

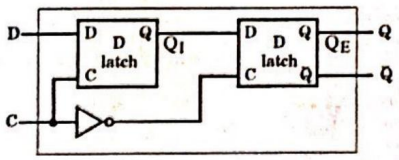
Due: Wed Feb 24th, 10:00 AM Pacific Time

Student Name: Charles Zhang

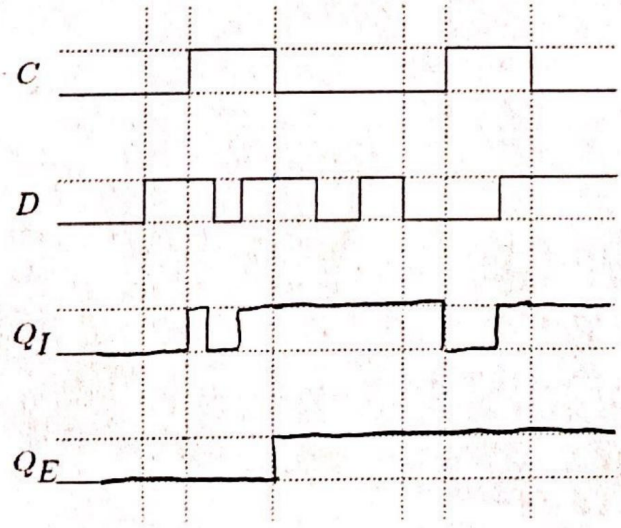
Student ID: 305-413-659

Note: You must complete the assignments entirely on your own, without discussing with others.

1. (10 Points) Consider the D flip-flop illustrated in the diagram below:



In the Figure below are traces of C and D; draw the resulting traces of QI and QE.



1 1 **10 / 10**

✓ **- 0 pts** **Correct**

![Screen_Shot_2021-02-19_at_5.22.01_PM.png](/files/f2892615-edcd-4548-a738-84dac38a56b0)

- 1 pts Minor error in $$Q_I$$

- 3 pts Major error in $$Q_I$$

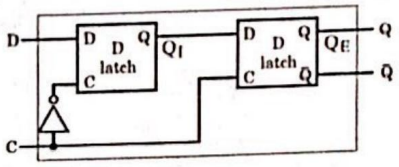
- 5 pts Blank in $$Q_I$$

- 1 pts Minor error in $$Q_E$$

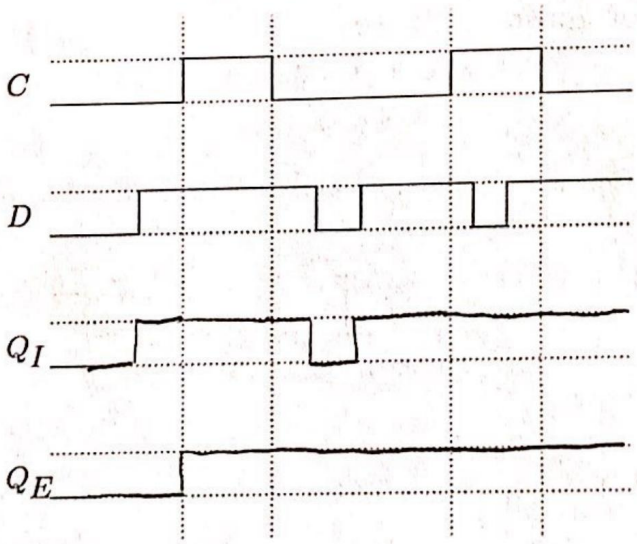
- 3 pts Major error in $$Q_E$$

- 4 pts Blank in $$Q_E$$

2. (10 Points) Now consider when we move the inverter in the D flip-flop illustrated in the diagram below:



In the Figure below are traces of C and D; draw the resulting traces of QI and QE.



2 2 **10 / 10**

✓ **- 0 pts** **Correct**

![Screen_Shot_2021-02-19_at_5.23.24_PM.png](/files/aaaed2c0-9165-4bd3-b3d4-fedfb11eed4b)

- 1 pts Minor error in $$Q_I$$

- 3 pts Major error in $$Q_I$$

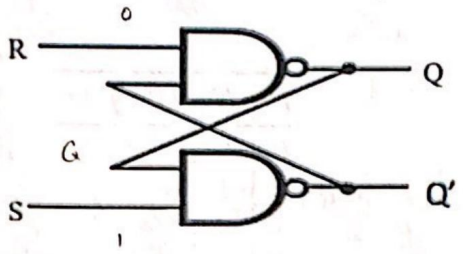
- 5 pts Blank in $$Q_I$$

- 1 pts Minor error in $$Q_E$$

- 3 pts Major error in $$Q_E$$

- 5 pts Blank in $$Q_E$$

3. In class, we designed an SR-latch using NOR gates. Suppose instead we try to implement it using NAND gates as given below:



(a) (4 Points) What setting of R and S sets Q to 1 and Q' to 0?

R=0, S=1

(b) (4 Points) What setting of R and S sets Q to 0 and Q' to 1?

R=1, S=0

(c) (4 Points) What setting of R and S sets Q to Q and Q' to Q'?

R=1, S=1

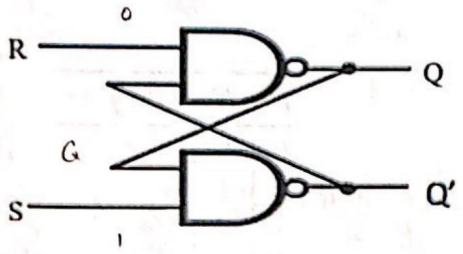
3.1 a **4 / 4**

✓ **- 0 pts** **Correct $$S=1,R=0$$**

- 2 pts Error in S

- 2 pts Error in R

3. In class, we designed an SR-latch using NOR gates. Suppose instead we try to implement it using NAND gates as given below:



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R=1, S=0

(c) (4 Points) What setting of R and S sets Q to Q and Q' to Q'?

R=1, S=1

3.2 b **4 / 4**

✓ **- 0 pts** **Correct $$S=0,R=1$$**

- 2 pts Error in S

- 2 pts Error in R

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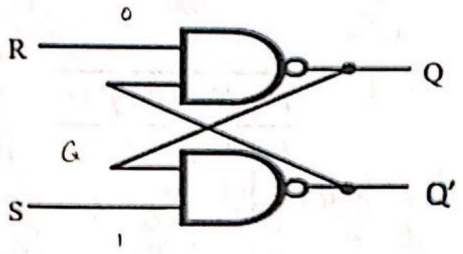

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R=1, S=0

(c) (4 Points) What setting of R and S sets Q to Q and Q' to Q'?

R=1, S=1

3.3 C **4 / 4**

✓ **- 0 pts** **Correct $$S=1,R=1$$**

- 2 pts Error in S

- 2 pts Error in R

4. A PN flip-flop has four operations: 0(reset), 1(set), no change (output remains unchanged) and toggle (output changes to its complement), when inputs P and N are 00, 01, 10, 11, respectively.

(a) (4 Points) If we use $Q(t)$ to represent the output of a PN flip-flop at time t, fill in the following table:

P	N	$Q(t+1)$
0	0	0
0	1	1
1	0	$Q(t)$
1	1	$Q(t)'$

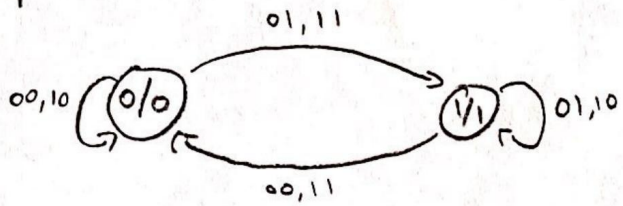
(b) (4 Points) Write the expression for $Q(t+1)$ in terms of present input (P and N) and state $Q(t)$.

P	N	Q(t)	Q(t+1)
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	0

$Q(t+1) = P'N + PN'Q(t) + PNQ(t)'$

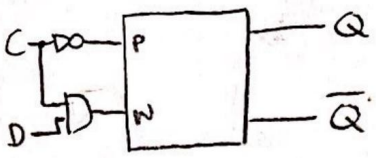
(c) (14 Points) Show the state transition table and state diagram of a PN flip-flop with input($P \in \{0,1\}$ and $N \in \{0,1\}$), output ($z = Q(t)$) and state ($Q(t) \in 0, 1$).

	Input (PN)				
PS: Q(t)	PN=00	PN=01	PN=10	PN=11	z
0	0	1	0	1	0
1	0	1	1	0	1
	NS, Q(t+1)				



(d) (4 Points) Show how a PN flip-flop can be converted to a D flip-flop.

C	D	Q(t+1)	P	N
0	0	Q(t)	1	0
0	1	Q(t)	1	0
1	0	0	0	0
1	1	1	0	1



4.1 a **4 / 4**

✓ **- 0 pts** **Correct**

![4a.PNG](/files/93a78af4-4d53-417f-99ec-21e1bb3cceab)

- 1 pts Error in first row

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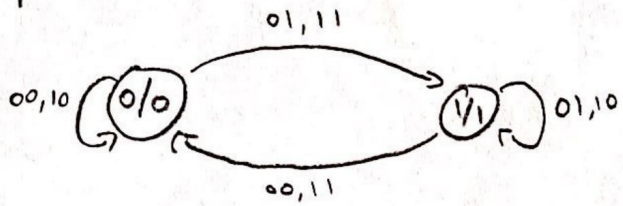

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C	D	Q(t+1)	P	N
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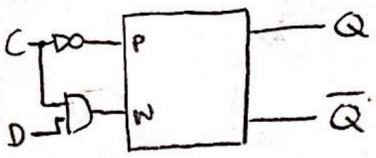
0	1	Q(t)	1	0
1	0	0	0	0
1	1	1	0	1



4.2 b **4 / 4**

✓ **- 0 pts** **Correct**

![4b.PNG](/files/04b7a363-406f-4817-9c6e-6ff8221bbe2e)

- 0.5 pts Contains constant 0 and 1 in expression

- 1 pts Single error (missing / extra P or N or negation in a term)

- 3 pts Incorrect expression

- 4 pts Blank

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0	0	1	1
0	1	0	0
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(c) (14 Points) Show the state transition table and state diagram of a PN flip-flop with input($P \in \{0,1\}$ and $N \in \{0,1\}$), output ($z = Q(t)$) and state ($Q(t) \in 0, 1$).

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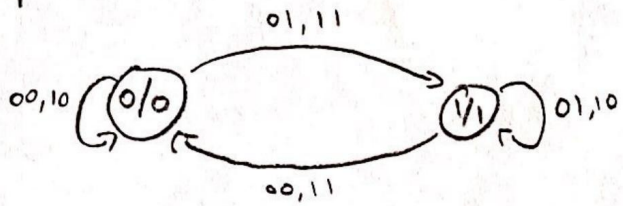

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C	D	Q(t+1)	P	N
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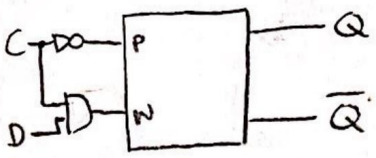
0	1	Q(t)	1	0
1	0	0	0	0
1	1	1	0	1



4.3 C **14 / 14**

✓ **- 0 pts** **Correct**

![4c.PNG](/files/ae238b0a-577f-4d5e-a92c-7f94e3d0f591)

- **- 8 pts** More/less than 2 states
- **- 2 pts** Transition table: first row incorrect
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(a) (4 Points) If we use $Q(t)$ to represent the output of a PN flip-flop at time t, fill in the following table:

P	N	$Q(t+1)$
0	0	0
0	1	1
1	0	$Q(t)$
1	1	$Q(t)'$

(b) (4 Points) Write the expression for $Q(t+1)$ in terms of present input (P and N) and state $Q(t)$.

P	N	Q(t)	Q(t+1)
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	0
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$Q(t+1) = P'N + PN'Q(t) + PNQ(t)'$

(c) (14 Points) Show the state transition table and state diagram of a PN flip-flop with input($P \in \{0,1\}$ and $N \in \{0,1\}$), output ($z = Q(t)$) and state ($Q(t) \in 0, 1$).

	Input (PN)				
PS: Q(t)	PN=00	PN=01	PN=10	PN=11	z
0	0	1	0	1	0
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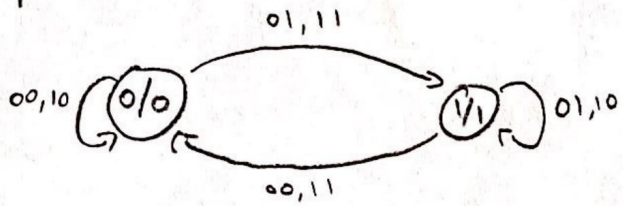
	NS, Q(t+1)				



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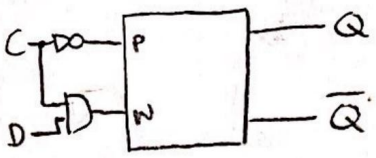


4.4 d 4 / 4

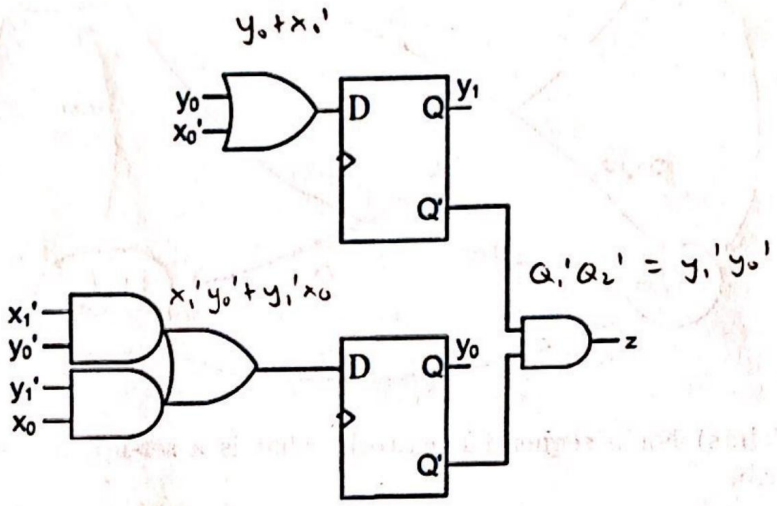
✓ **- 0 pts** **Either is correct:**

![4d.PNG](/files/e1efabf0-94aa-40fc-a18b-2ff476c0ff5e)

![qq.png](/files/46e2d4e9-fbf6-4d44-9a29-2fd64894b9a4)

- **1 pts** Minor error (eg: used constant 1 instead of 0, or switched the two inputs, etc.)
- **2.5 pts** Incorrect
- **4 pts** Used D as input to P and D' as input to N
- **4 pts** Blank

5. We would like to analyze the following sequential network. It has two input bits x_1 and x_0, with a single output bit z. Note, both D Flip-flops connect to the same CLK, not shown in the figure for simplicity.



(a) (4 Points) Write expressions for z, $y_1(t+1)$ and $y_0(t+1)$ in terms of inputs (x_1 and x_0) and present states (y_1 and y_0).

$z = y_1'y_0'$

$y_1(t+1) = x_0' + y_0$

$y_0(t+1) = x_1'y_0' + x_0y_1'$

(b) (8 Points) Using the expressions, fill in the table below.

PS	Input $x_1(t)x_0(t)$				Output
$y_1(t)y_0(t)$	00	01	10	11	z
00	11	01	10	01	1
01	10	11	10	11	0
10	11	01	10	00	0
11	10	10	10	10	0
	$y_1(t+1)y_0(t+1)$				
	NS				

(c) (4 Points) Is this a Moore or Mealy machine?

Moore

5.1 a **4 / 4**

✓ **- 0 pts** **Correct**

![5a.PNG](/files/4af03f1e-c54e-40a2-b978-ad7759742382)

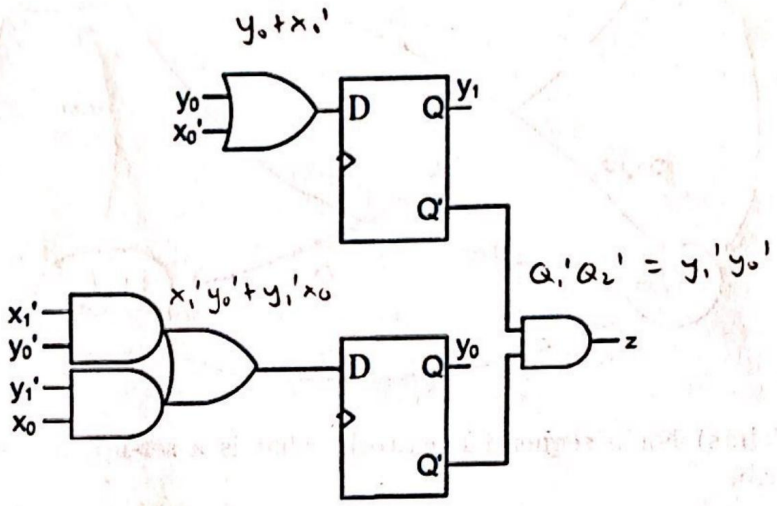
- 1 pts z incorrect

- 1 pts $$y_{0}(t+1)$$ incorrect

- 1 pts $$y_{1}(t+1)$$ incorrect

- 4 pts Blank

5. We would like to analyze the following sequential network. It has two input bits x_1 and x_0, with a single output bit z. Note, both D Flip-flops connect to the same CLK, not shown in the figure for simplicity.



(a) (4 Points) Write expressions for z, $y_1(t+1)$ and $y_0(t+1)$ in terms of inputs (x_1 and x_0) and present states (y_1 and y_0).

$z = y_1'y_0'$

$y_1(t+1) = x_0' + y_0$

$y_0(t+1) = x_1'y_0' + x_0y_1'$

(b) (8 Points) Using the expressions, fill in the table below.

PS	Input $x_1(t)x_0(t)$				Output
$y_1(t)y_0(t)$	00	01	10	11	z
00	11	01	10	01	1
01	10	11	10	11	0
10	11	01	10	00	0
11	10	10	10	10	0
	$y_1(t+1)y_0(t+1)$				
	NS				

(c) (4 Points) Is this a Moore or Mealy machine?

Moore

5.2 b **8 / 8**

✓ **- 0 pts** **Correct**

![5b.PNG](/files/a9025a63-5864-4852-892c-aa2ac55fc934)

- 1.5 pts Error in first row next states

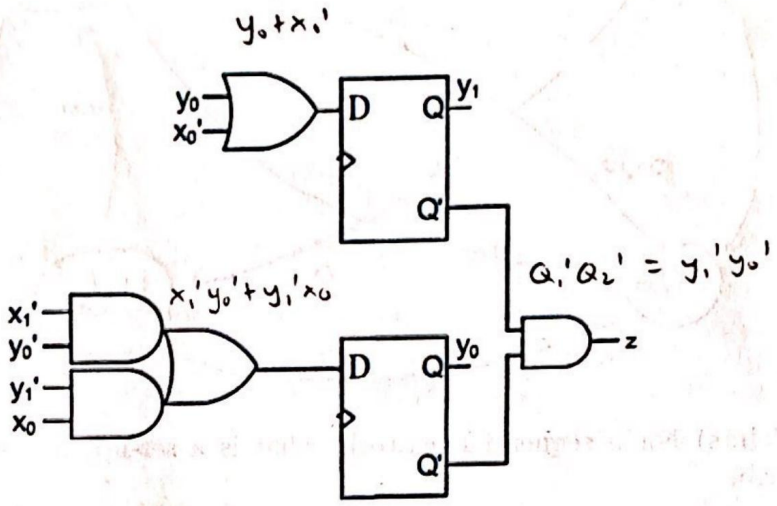
- 1.5 pts Error in second row next states

- 1.5 pts Error in third row next states

- 1.5 pts Error in forth row next states

- 2 pts Error in output

5. We would like to analyze the following sequential network. It has two input bits x_1 and x_0, with a single output bit z. Note, both D Flip-flops connect to the same CLK, not shown in the figure for simplicity.



(a) (4 Points) Write expressions for z, $y_1(t+1)$ and $y_0(t+1)$ in terms of inputs (x_1 and x_0) and present states (y_1 and y_0).

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PS	Input $x_1(t)x_0(t)$				Output
$y_1(t)y_0(t)$	00	01	10	11	z
00	11	01	10	01	1
01	10	11	10	11	0
10	11	01	10	00	0
11	10	10	10	10	0
	$y_1(t+1)y_0(t+1)$				
	NS				

(c) (4 Points) Is this a Moore or Mealy machine?

Moore

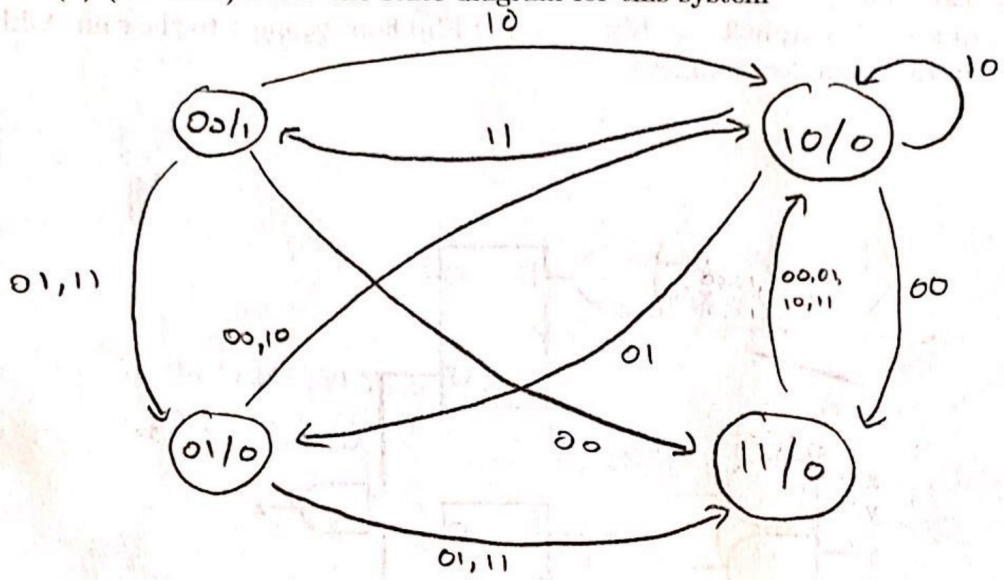
5.3 C **4 / 4**

✓ **- 0 pts Correct: Moore**

- 3.5 pts Incorrect: Mealy

- 4 pts Blank

(d) (8 Points) Draw the state diagram for this system

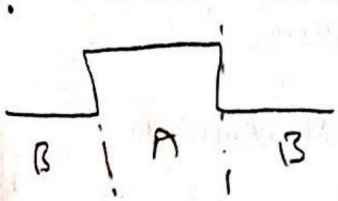


6. (4 Points) For a sequential network, what is a set-up time and hold time? Please describe.

Set-up time is the amount of time before a clock pulse (rising/falling edge) that you hold your input constant in order to account for the propagation delay of the preceding combinational network.
Hold time is the amount of time after a clock pulse that you hold your input constant in order to account for the propagation delay of the sequential network.

7. (4 Points) Explain how does the Master-slave architecture realize the edge-triggering mechanism. You may use the Master-slave D Flip-flip as an example.

By putting 2 D-latches in series and inverting the clock on one of them, one D-latch can change state when the clock is 1, and the other can change state when the clock is 0:



This filters out the original input so that any changes to the Q of the second D-latch only occur at the edges of the clock input.

5.4 d **8 / 8**

✓ **- 0 pts** **Correct**

- 0.5 pts State 00 incorrect output

- 1.5 pts State 00 incorrect transitions

- 0.5 pts State 01 incorrect output

- 1.5 pts State 01 incorrect transitions

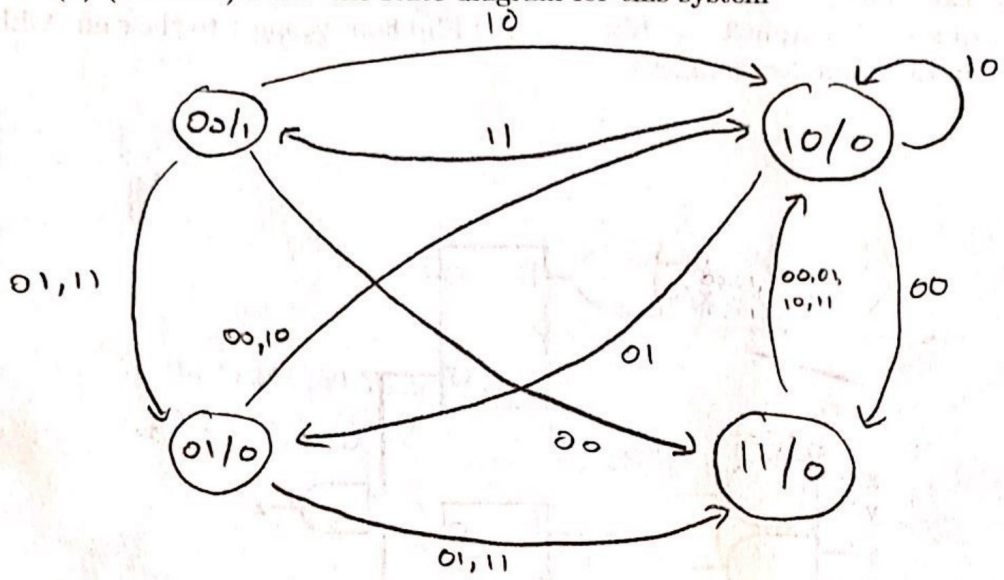
- 0.5 pts State 10 incorrect output

- 1.5 pts State 10 incorrect transitions

- 0.5 pts State 11 incorrect output

- 1.5 pts State 11 incorrect transitions

(d) (8 Points) Draw the state diagram for this system



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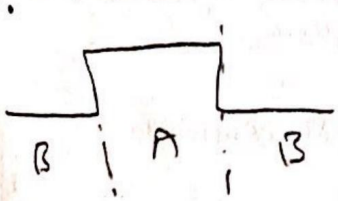


This filters out the original input so that any changes to the Q of the second D-latch only occur at the edges of the clock input.

6 6 **4 / 4**

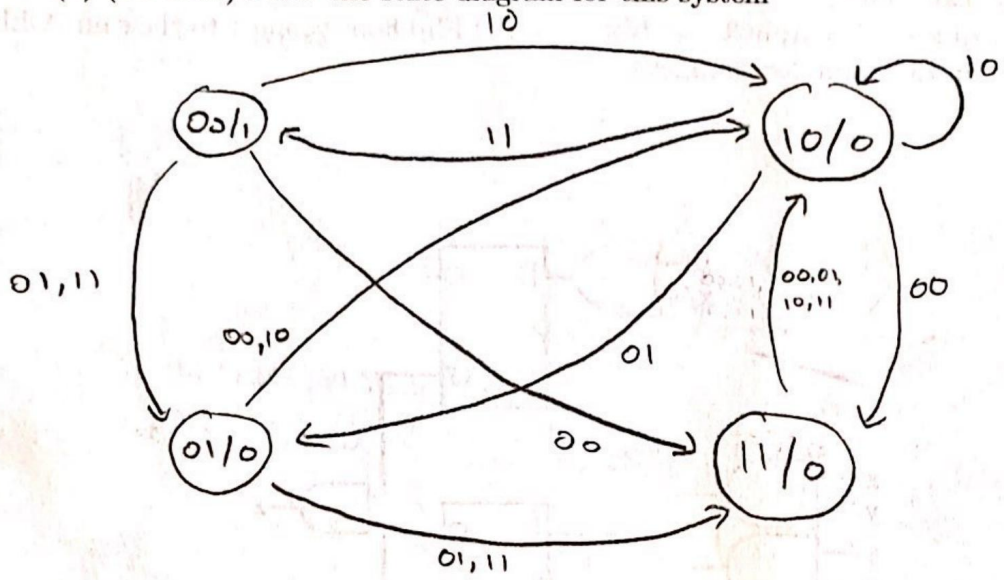
✓ **- 0 pts** **Correct; Example answer: `setup time`: minimal interval between the (stable) _input_ and the _triggering edge_ (_clock pulse_); `hold time`: minimal interval that the input should be _kept unchanged_(_hold_) after the _triggering edge_(_clock pulse_)**

- 1 pts Minor error in set-up time

- 1 pts Minor error in hold time

- 4 pts Blank

(d) (8 Points) Draw the state diagram for this system



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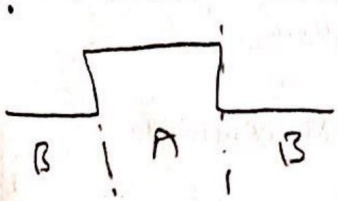

This filters out the original input so that any changes to the Q of the second D-latch only occur at the edges of the clock input.

7 7 **4 / 4**

✓ **- 0 pts** **Correct; Key statement: master and slave latch works on different but consecutive phases of a single clock pulse.**

- 1 pts Minor error

- 4 pts Blank