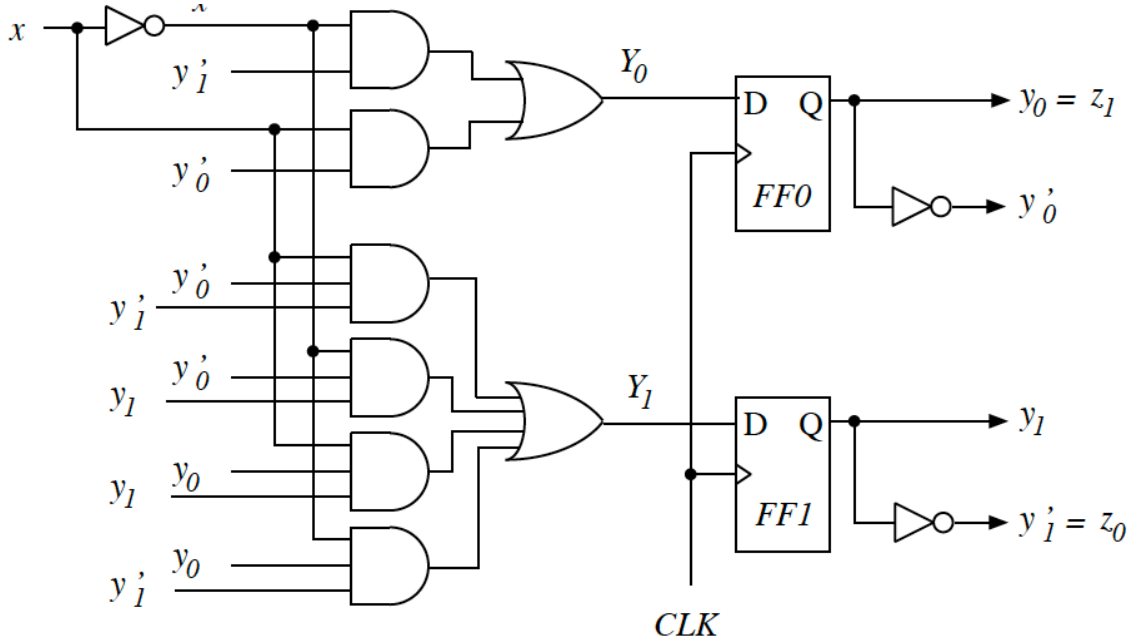
CS M51A
Logic Design of Digital Systems
Winter 2021

Some slides borrowed and modified from:
M.D. Ercegovac, T. Lang and J. Moreno, Introduction to Digital Systems.

ANALYSIS OF CANONICAL SEQUENTIAL NETWORKS



State transition

$$Y_0 = x'y_1' + xy_0'$$
$$Y_1 = xy_0'y_1' + x'y_0'y_1 + xy_0y_1 + x'y_0y_1'$$

Output

$$z_0 = y_1'$$
$$z_1 = y_0$$

- STATE-TRANSITION AND OUTPUT FUNCTIONS:

PS	Input		
y_1y_0	$x=0$	$x=1$	
00	01	11	01
01	11	00	11
10	10	01	00
11	00	10	10
	Y_1Y_0		z_1z_0
	NS		Output

- CODES:

x	x
0	a
1	b

z_1z_0	z
00	c
01	d
10	e
11	f

y_1y_0	s
00	S_0
01	S_1
10	S_2
11	S_3

- HIGH-LEVEL SPECIFICATION:

  Input: $x(t) \in \{a, b\}$
  Output: $z(t) \in \{c, d, e, f\}$
  State: $s(t) \in \{S_0, S_1, S_2, S_3\}$
  Initial state: $s(0) = S_2$

  Functions: The state-transition and output functions

PS	$x(t) = a$	$x(t) = b$	
S_0	S_1	S_3	d
S_1	S_3	S_0	f
S_2	S_2	S_1	c
S_3	S_0	S_2	e
	NS		$z(t)$

State Diagram

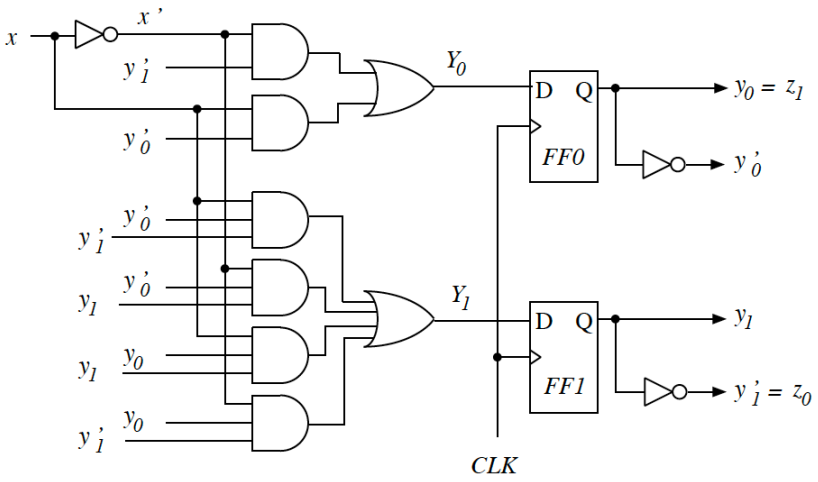
PS	$x(t)=a$	$x(t)=b$	
S_0	S_1	S_3	d
S_1	S_3	S_0	f
S_2	S_2	S_1	c
S_3	S_0	S_2	e
	NS		$z(t)$

$x(t)$	a	a	b	a	b	b	a	b	a	a	b	b	b	a	
$s(t)$	S_2	S_2	S_2	S_1	S_3	S_2	S_1	S_3	S_2	S_2	S_2	S_1	S_0	S_3	S_0
$z(t)$	c	c	c	f	e	c	f	e	c	c	c	f	d	e	d

PROPAGATION DELAY x to z_0:

For x changes 0→1 and z_0 changes 1→ 0

SET-UP TIME:	$t_{su}(net)$	$=$	$t_{pHL}(\text{NOT}) + t_{pHL}(\text{AND3})$
			$+t_{pHL}(\text{OR4}) + t_{su}$
		$=$	$(0.05 + 0.017 \times 3) + (0.18 + 0.018)$
			$+(0.45 + 0.025) + 0.3$
		$=$	1.07 [ns]
HOLD TIME:	$t_h(net)$	$=$	0.14 [ns]
PROPAGATION DELAY:	$t_p(z_0)$	$=$	$t_{pLH}(\text{FF}) + t_{pHL}(\text{NOT})$
		$=$	$(0.49 + 0.038 \times 3)$
			$+(0.05 + 0.017 \times (L + 3))$
		$=$	$0.70 + 0.017L$ [ns]
			(load of NOT is $L + 3$, load of FF is 3)



EXAMPLE: DESIGN

Input: $x(t) \in \{a, b, c\}$
Output: $z(t) \in \{0, 1\}$
State: $s(t) \in \{A, B, C, D\}$
Initial state: $s(0) = A$

Functions: The state-transition and output functions

PS	Input		
	$x = a$	$x = b$	$x = c$
A	C,0	B,1	B,0
B	D,0	B,0	A,1
C	A,0	D,1	D,0
D	B,0	A,0	D,1
	$NS,\ z$		

EXAMPLE (cont.)

- CODING:

Input code

x	x_1	x_0
a	0	1
b	1	0
c	1	1

State code

s	y_1	y_0
A	0	0
B	1	0
C	0	1
D	1	1

EXAMPLE (cont.)

- STATE-TRANSITION AND OUTPUT FUNCTIONS

PS	Input		
	$x = a$	$x = b$	$x = c$
A	C,0	B,1	B,0
B	D,0	B,0	A,1
C	A,0	D,1	D,0
D	B,0	A,0	D,1
	$NS,\ z$		

Input code

x	x_1	x_0
a	0	1
b	1	0
c	1	1

State code

s	y_1	y_0
A	0	0
B	1	0
C	0	1
D	1	1

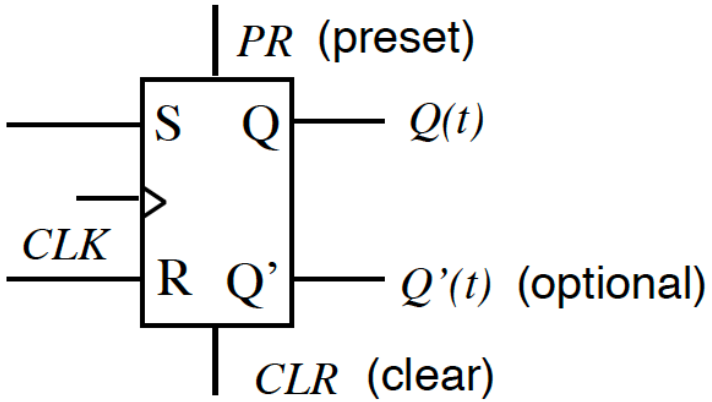
PS	x_1x_0		
y_1y_0	01	10	11
00	01,0	10,1	10,0
10	11,0	10,0	00,1
01	00,0	11,1	11,0
11	10,0	00,0	11,1
	$Y_1Y_0,\ z$		
	NS, Output		

$$Y_1 =$$
$$Y_0 =$$
$$z =$$

EXAMPLE(cont.)

Gate level design of the system:

SR FLIP-FLOP



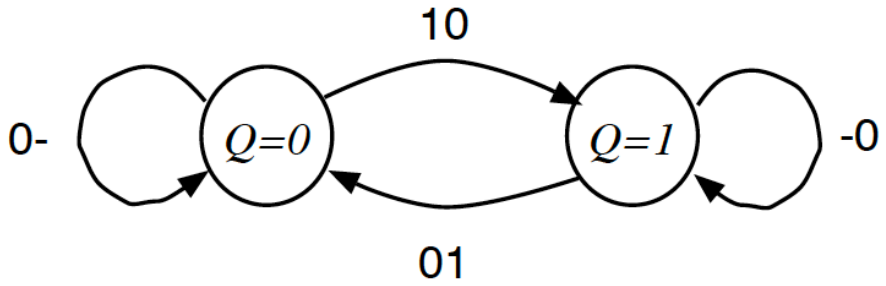
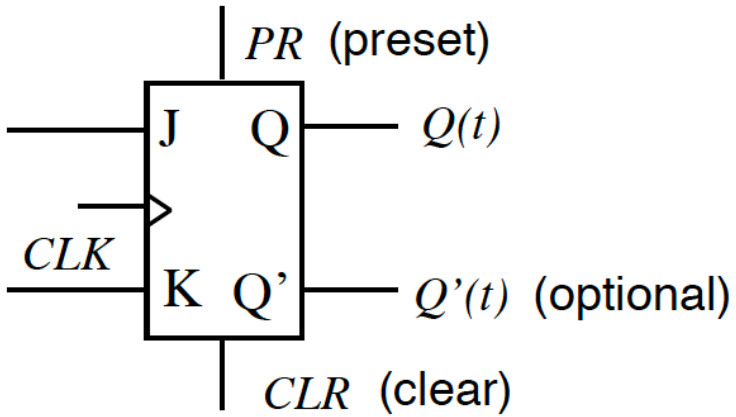


Figure 8.20: SR FLIP-FLOP AND ITS STATE DIAGRAM.

$PS = Q(t)$	$S(t)R(t)$			
	00	01	10	11
0	0	0	1	-
1	1	0	1	-
	$NS = Q(t+1)$			

$$Q(t+1) = Q(t)R'(t) + S(t) \quad \text{restriction: } R(t) \cdot S(t) = 0$$

JK FLIP-FLOP



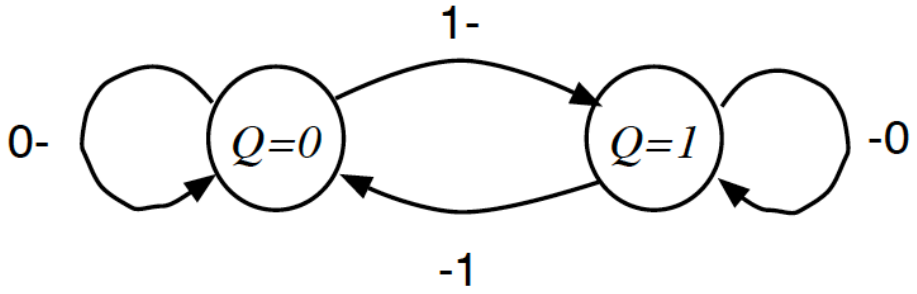


Figure 8.21: JK FLIP-FLOP AND ITS STATE DIAGRAM.

$PS = Q(t)$	$J(t)K(t)$			
	00	01	10	11
0	0	0	1	1
1	1	0	1	0
	$NS = Q(t+1)$			

$$Q(t+1) = Q(t)K'(t) + Q'(t)J(t)$$

T (Toggle) FLIP-FLOP

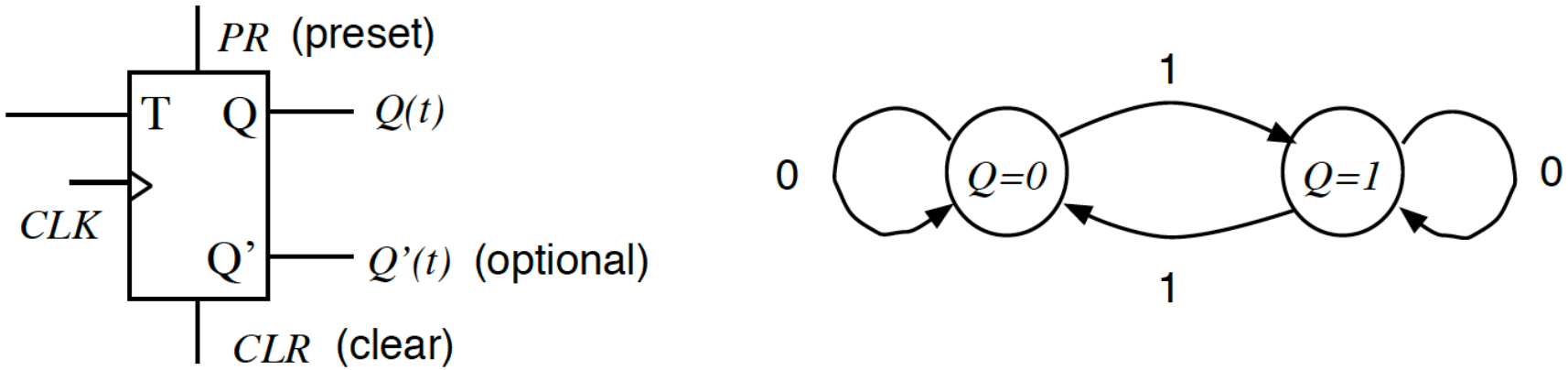


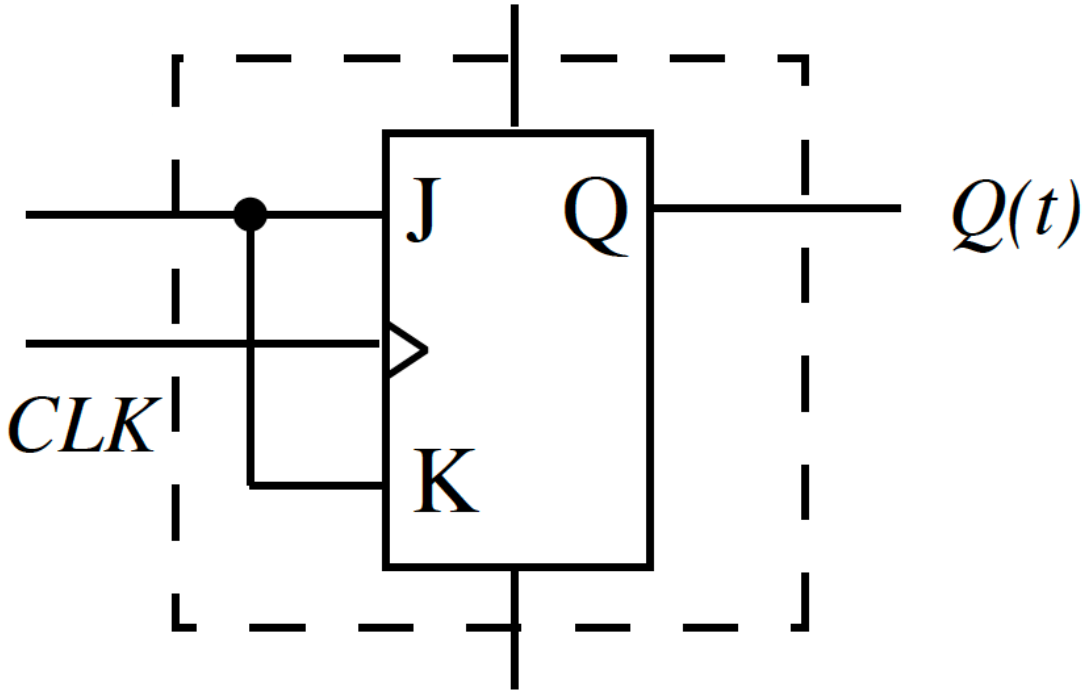
Figure 8.22: T FLIP-FLOP AND ITS STATE DIAGRAM.

$PS = Q(t)$	$T(t)$	
	0	1
0	0	1
1	1	0
	$NS = Q(t+1)$	

$$Q(t+1) = Q(t) \oplus T(t)$$

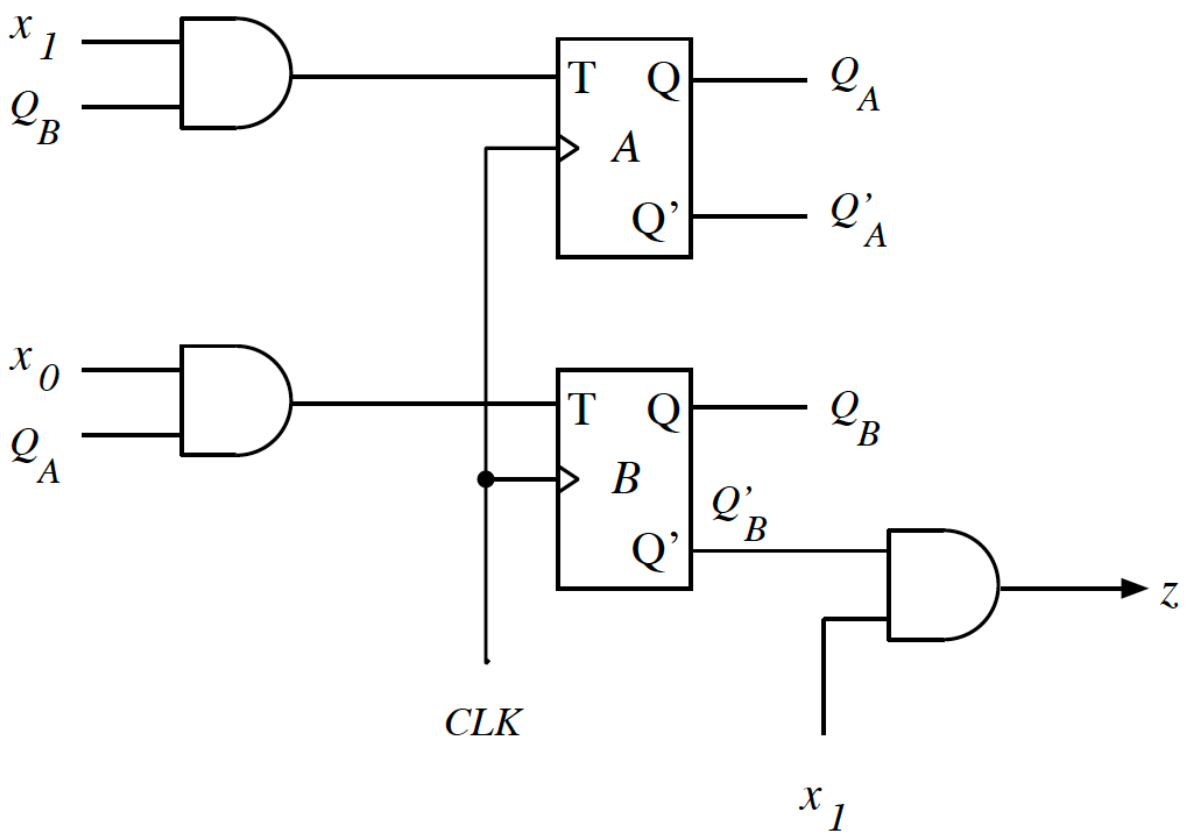
Clicker Question

What does the whole circuit do?



a) It works as a T FlipFlop
b) It works as a D Flip Flop
c) It works as a combinational invertor
d) It is not a valid circuit
e) It works as a combinational buffer

EXAMPLE: ANALYSIS



$$T_A =$$
$$T_B =$$
$$z(t) =$$

EXAMPLE (cont.)

- STATE-TRANSITION AND OUTPUT FUNCTIONS

PS	Input							
Q_AQ_B	x_1x_0				x_1x_0			
	00	01	10	11	00	01	10	11
00	00	00	00	00	0	0	1	1
01	01	01	11	11	0	0	0	0
10	10	11	10	11	0	0	1	1
11	11	10	01	00	0	0	0	0
	Q_AQ_B				z			
	NS				Output			

- CODING:

Q_A	Q_B	s
0	0	S_0
0	1	S_1
1	0	S_2
1	1	S_3

x_1	x_0	x
0	0	a
0	1	b
1	0	c
1	1	d

EXAMPLE (cont.)

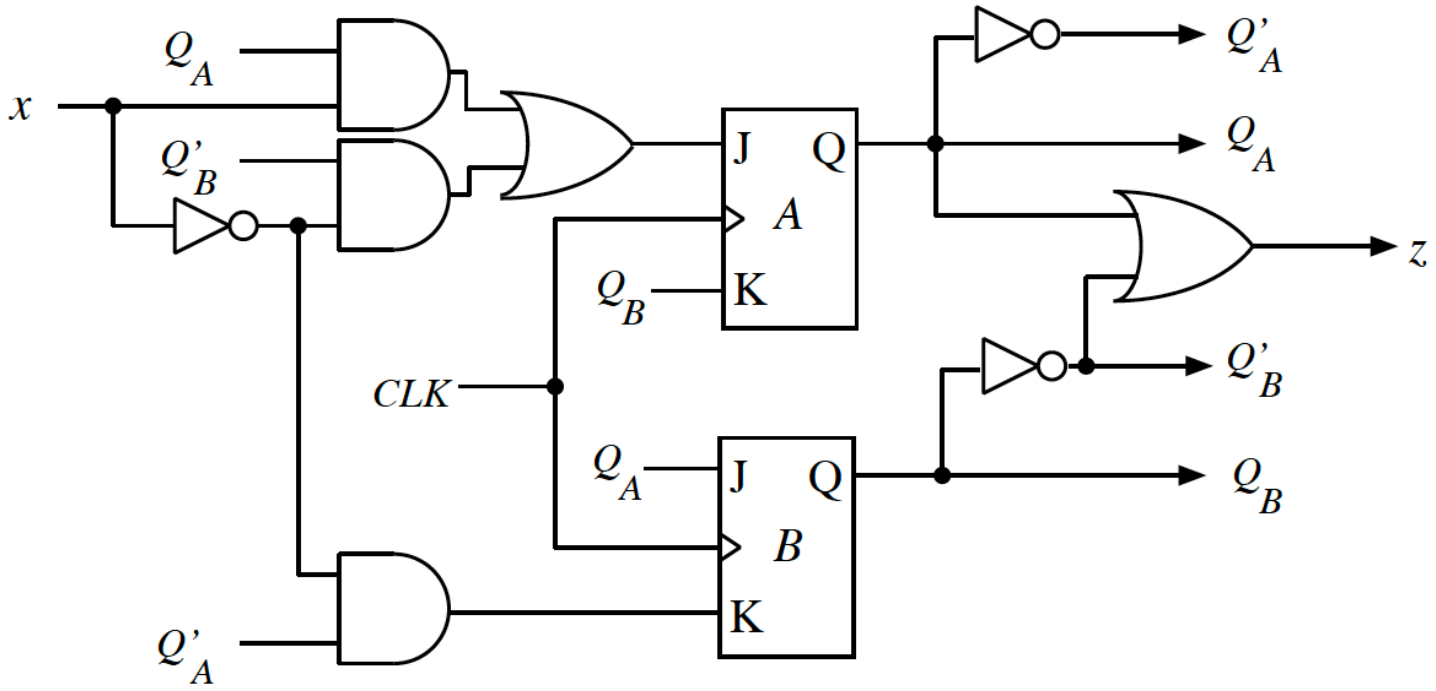
- HIGH-LEVEL DESCRIPTION:

  Input: $x(t) \in \{a, b, c, d\}$
  Output: $z(t) \in \{0, 1\}$
  State: $s(t) \in \{S_0, S_1, S_2, S_3\}$
  Initial state: $s(0) = S_0$

  Functions: The state-transition and output functions

PS	x				x			
	a	b	c	d	a	b	c	d
S_0	S_0	S_0	S_0	S_0	0	0	1	1
S_1	S_1	S_1	S_3	S_3	0	0	0	0
S_2	S_2	S_3	S_2	S_3	0	0	1	1
S_3	S_3	S_2	S_1	S_0	0	0	0	0
	NS				z			

EXAMPLE: ANALYSIS



EXAMPLE(cont.)

$$J_A = \qquad K_A =$$
$$J_B = \qquad K_B =$$

$$z =$$

$$Q_A(t+1) =$$

$$Q_B(t+1) =$$

EXAMPLE (cont.)

- STATE-TRANSITION AND OUTPUT FUNCTIONS

PS	NS		Output
	$x = 0$	$x = 1$	z
$Q_A Q_B$	$Q_A Q_B$	$Q_A Q_B$	
00	10	00	1
01	00	01	0
10	11	11	1
11	01	01	1

- STATE CODING

Q_A	Q_B	S
0	0	S_0
0	1	S_1
1	0	S_2
1	1	S_3

EXAMPLE (cont.)

- HIGH-LEVEL DESCRIPTION

  Input: $x(t) \in \{0, 1\}$
  Output: $z(t) \in \{0, 1\}$
  State: $s(t) \in \{S_0, S_1, S_2, S_3\}$
  Initial state: $s(0) = S_0$

  Functions: The state-transition and output functions

PS	Input		
	$x = 0$	$x = 1$	
S_0	S_2	S_0	1
S_1	S_0	S_1	0
S_2	S_3	S_3	1
S_3	S_1	S_1	1
	NS		z

State Diagram

EXAMPLE: DESIGN MODULO-5 COUNTER

- USE T FLIP-FLOPS

Input:	$x(t) \in \{0, 1\}$
Output:	$z(t) \in \{0, 1, 2, 3, 4\}$
State:	$s(t) \in \{S_0, S_1, S_2, S_3, S_4\}$
Initial state:	$s(0) = S_0$
Functions:	Counts modulo-5, i.e., (0,1,2,3,4,0,1,2,3,4,0...),

State Diagram:

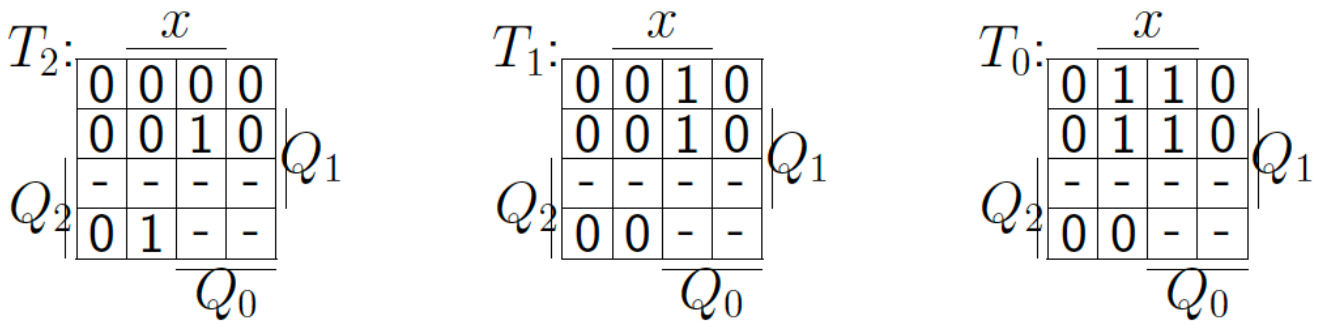
EXAMPLE (cont.)

z	z_2	z_1	z_0
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0

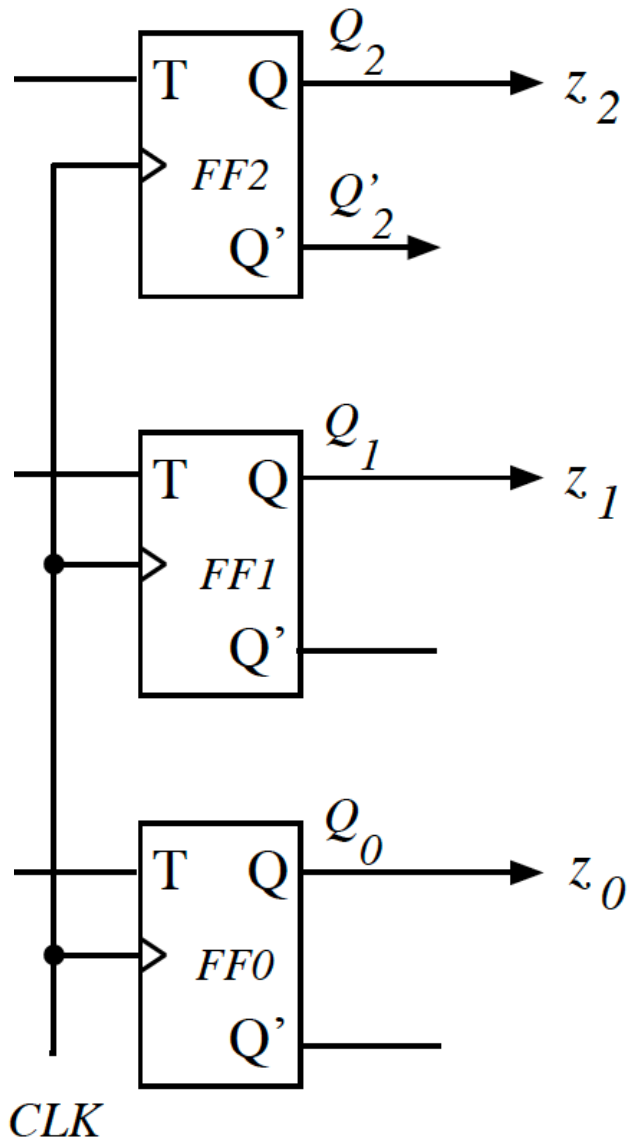
PS	Input		Input	
$Q_2Q_1Q_0$	$x=0$	$x=1$	$x=0$	$x=1$
000	000	001	000	001
001	001	010	000	011
010	010	011	000	001
011	011	100	000	111
100	100	000	000	100
	NS		$T_2T_1T_0$	

EXAMPLE (cont.)

sm – STATE MAP



$$T_2 = xQ_2 + xQ_1Q_0$$
$$T_1 = xQ_0$$
$$T_0 = xQ_2'$$


T
Q
FF2
Q'
Q2
Q'2
z2
T
Q
FF1
Q'
Q1
z1
T
Q
FF0
Q'
Q0
z0
CLK