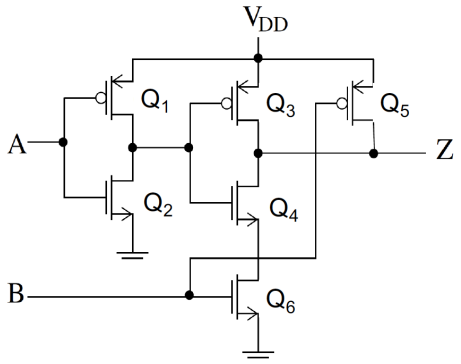
CS M51A, Winter 2021, Assignment 4
(Total Mark: 90 points, 9%)

Due: Wed Feb 3rd, 10:00 AM Pacific Time
Student Name:
Student ID:
Note: You must complete the assignments entirely on your own, without discussing with others.

1. (a) (14 Points) Given the circuit below, complete the table below, determining the resistances for Q_1 to Q_6 and the final output Z. The transistors Q_1 to Q_6 should be High or Low (show by 'H' or 'L') resistance. The output Z may be 0, 1, float (show by –) or short (show by *).



A	B	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Z
0	0							
0	1							
1	0							
1	1							

(b) (6 Points) Write sum of MINTERMS and product of MAXTERMS for Z.

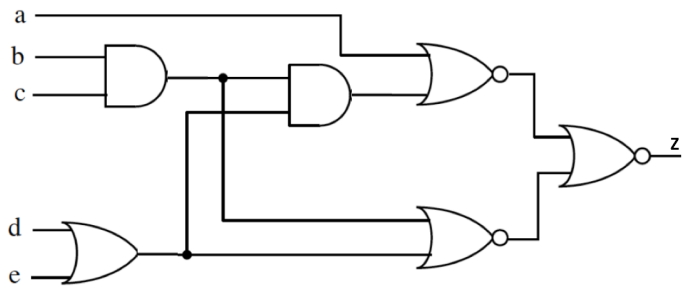
2. (a) (4 Points) Write the sum of minterms and product of maxterms function for the following table.

A	B	F
0	0	0
0	1	1
1	0	0
1	1	0

(b) (6 Points) Implement F using PMOS and NMOS transistors. Use at most 6 transistors in total; only the signal itself can be used as input.

(c) (6 Points) Implement F using inverters and transmission gates; you may use logic 0, logic 1 or the signal itself as input.

3. Consider the following system where the output Z has a load (L) of 4.

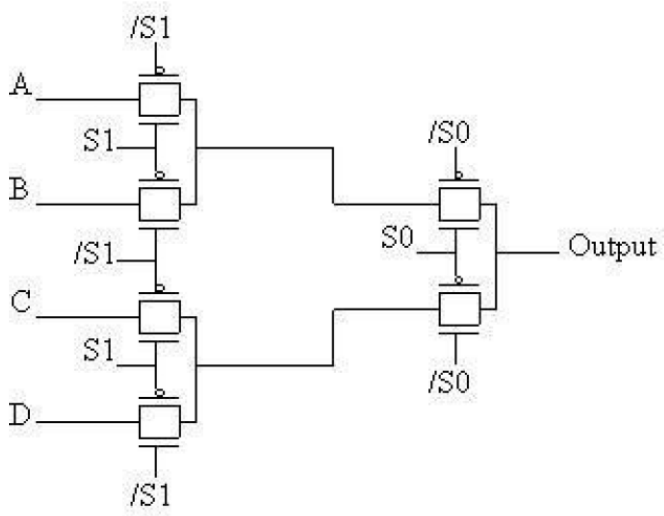


Gate Type	Fan-in	Propagation Delays (ns)	
		t_{pLH}	t_{pHL}
NOT	1	$0.02 + 0.038L$	$0.05 + 0.017L$
NAND	2	$0.05 + 0.038L$	$0.08 + 0.027L$
NOR	2	$0.06 + 0.075L$	$0.07 + 0.016L$
AND	2	$0.08 + 0.038L$	$0.09 + 0.027L$
OR	2	$0.08 + 0.075L$	$0.09 + 0.016L$

(a) (8 Points) determine the low to high propagation delay $t_{pLH}(d, z)$ of the output z.

(b) (8 Points) determine the high to low propagation delay $t_{pHL}(b, z)$ of the output z.

4. Consider the following circuit, where /S1 and /S0 present complement (NOT) of S1 and S0, respectively.



(a) (2 Points) What is the value of output when S0=1, S1=0.

(b) (2 Points) What is the value of output when S0=1, S1=1.

(c) (8 Points) Write a sum of product expression for the output in terms of A,B,C,D,S0,S1.

5. Use transmission gates to implement the following logical expressions; you may use logic 0, logic 1, the signal itself or its complement as input, e.g. A, A', 0, 1 are all valid input of your design):

   (a) (6 Points) F = A + B (OR gate)

   (b) (6 Points) F = (ABC)' (3-input NAND gate)

   (c) (6 Points) F = ABC (3-input AND gate)

(d) (6 Points) F = ABC + DE

6. (2 Points) For a transmission gate, why are both PMOS and NMOS used?