Grading Rubric for Lab 3: Stopwatch

This is the grading rubric for the Stopwatch Project. You will need to explain the purpose behind ALL states and their simulation result in your report; try to make your FSM design as concise as possible.

Demo

	Points
Overall Design	**20**
- Explain FSM Design and Show Diagram	4
- Show and Explain Implementation of Counter	4
- Show and Explain Implementation of 4 Clocks	4
- Show and Explain Button Debouncing	4
- Show and Explain Implementation of Seven-Segment Display	4
Simulation	**8**
- Explain Testbench Design	3
- Explain Simulation Result	5
Implementation	**32**
- Show and Explain UCF Design	2
- Demonstrate counter value on the Seven segment display for 1Hz rate under normal mode	5
- Demonstrate that when SEL is set to 1, the “second” portion should increment at 2 Hz rate under adjustment mode	5
- Demonstrate that when SEL is set to 0, the “minute” portion should increment at 2 Hz rate under adjustment mode	5
- Demonstrate that the timer should continue to count at 1Hz rate from the adjusted value when ADJ is set to 0 again.	5
- Demonstrate that Pause is working	5
- Demonstrate that Reset is working	5

Report

	Points
Introduction and Requirements	**10**
- Overview of the lab and your design	5
- Summarize general reason and implementation of button debounce	5
- Summary the detail of how to use the seven-segment display	5
Design Descriptions	**15**
- Include a diagram of your FSM (hand-drawn or computer generated)	2
- Explain each state of your FSM -2 points per missing state diagram Explain each module in your code	6
- Purposes of each Module	5
- Input and Output of each Module	2
Simulation	**10**
- Waveform diagram for each of the states and counter result under that state -1 point per missing waveform diagram (up to 5 waveforms)	5
- Explain why each waveform is correct -1 point per missing explanation (up to 5 explanations)	5
Conclusion	**5**
- Summary of your design	2
- Challenges and how to overcome them	2
- Perceived team contribution	1

Team Contribution

We expect each and all students to contribute to their group. Those who do not contribute will be docked 40% of their assignment grade.

Deliverables

When you finish, you should submit the following parts of your design to CCLE:

1. **Project Code:** the Xilinx ISE project folder should be cleaned up (*Project* > *Cleanup Project Files*), zipped and uploaded in the corresponding assignment page on the course website
2. **Lab Report (Electronic Version):** The lab report should also be uploaded in the assignment page on the course website