# CS M51A
# Logic Design of Digital Systems
# Winter 2021

Some slides borrowed and modified from:
M.D. Ercegovac, T. Lang and J. Moreno, Introduction to Digital Systems.
D. Patterson and J. Hennessy, Computer Organization and Design

# Review

- Truth table
- Switching Expression and Boolean Algebra
- Sum of Minterms and Product of Maxterms
- Symbols and Gate level design

# Clicker Question

Which one is equal to ABC + A'B + A' + B' + C'

a) A'
b) B'
c) 1
d) 0
e) none

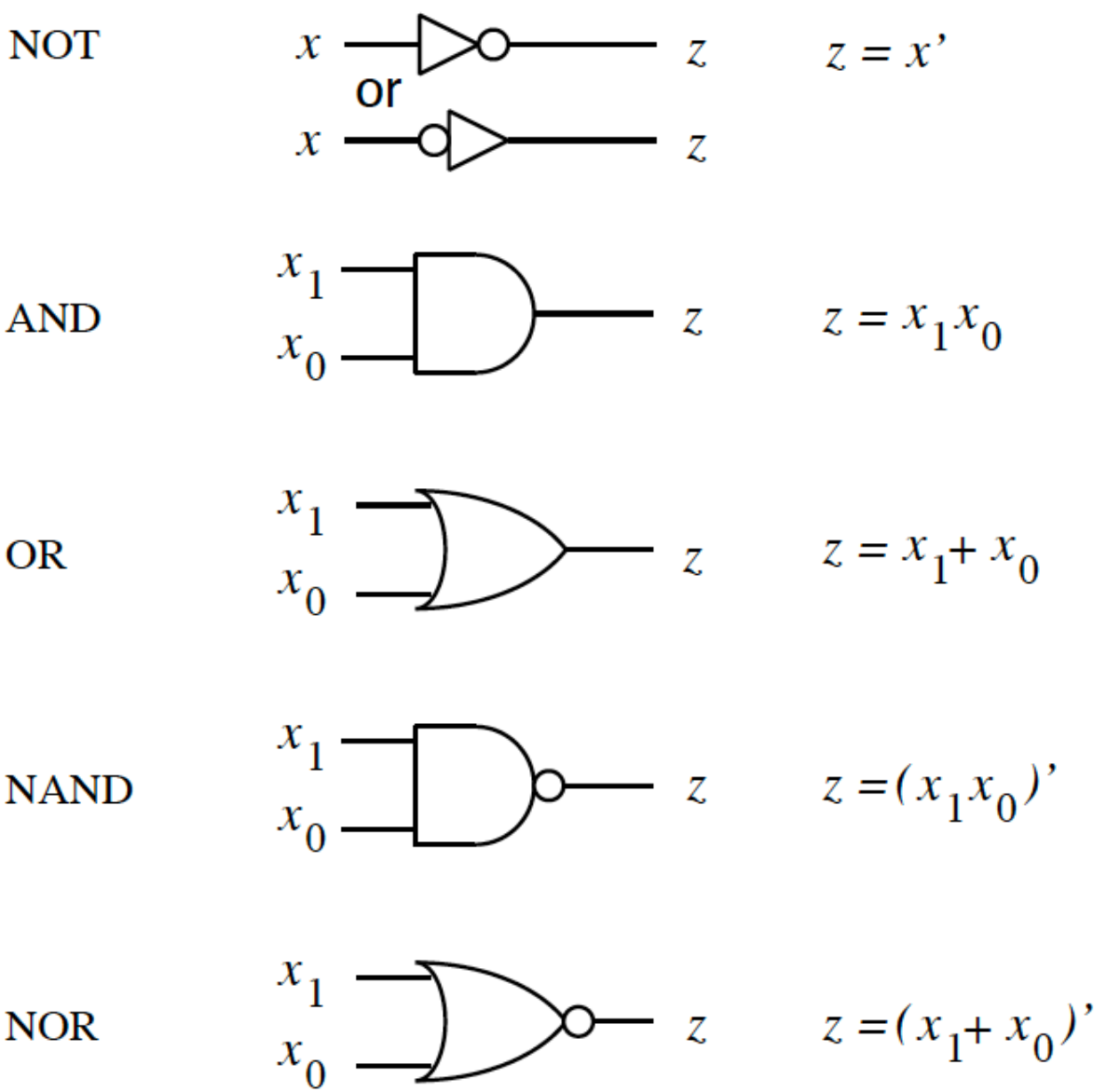
# Design a 1-bit adder

Truth table → Expression → Symbols

# Design a 1-bit adder

Truth table → Expression → Symbols

# How can we build these gates?



# Transistors

## complementary metal oxide semiconductor(CMOS)

# REPRESENTATION OF BINARY VARIABLES

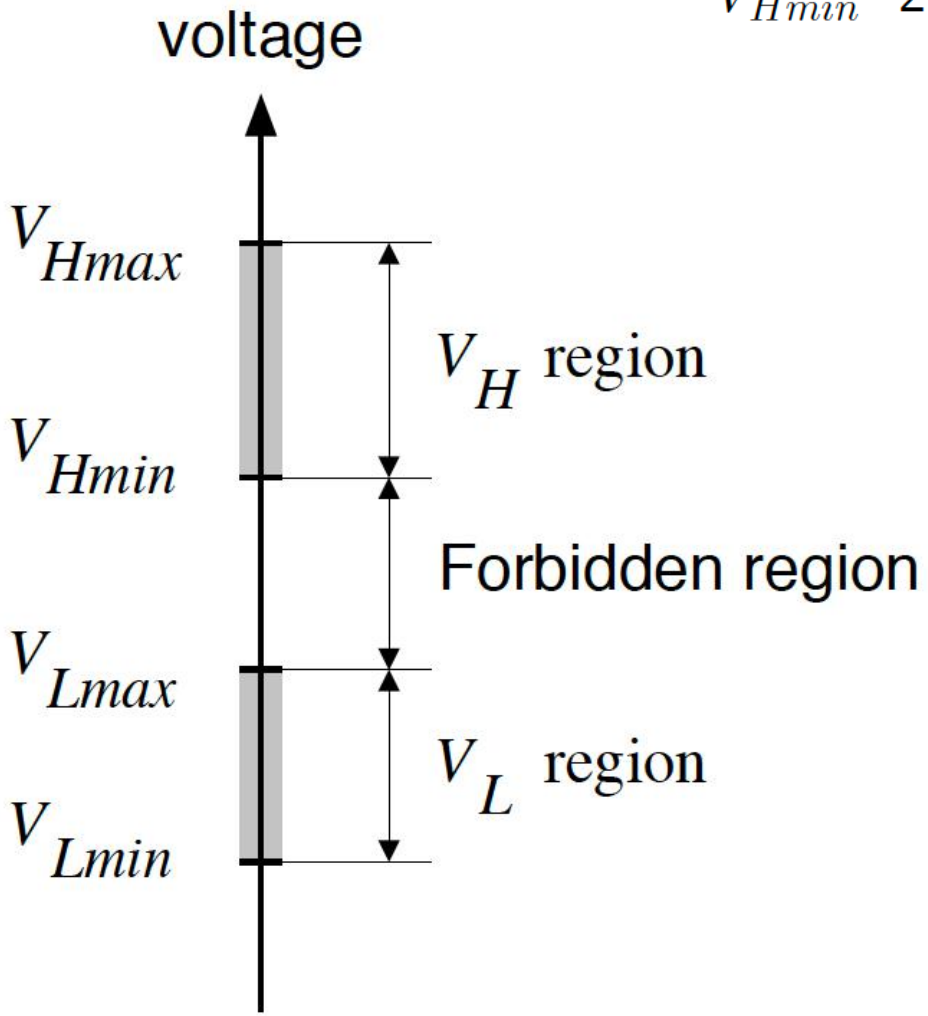
- REPRESENTATION OF 0 AND 1 BY ELECTRICAL SIGNALS
  - VOLTAGES
  - CURRENTS
  - ELECTRICAL CHARGES
- REALIZATION OF CIRCUITS THAT OPERATE ON THESE SIGNALS TO IMPLEMENT DESIRED SWITCHING FUNCTIONS

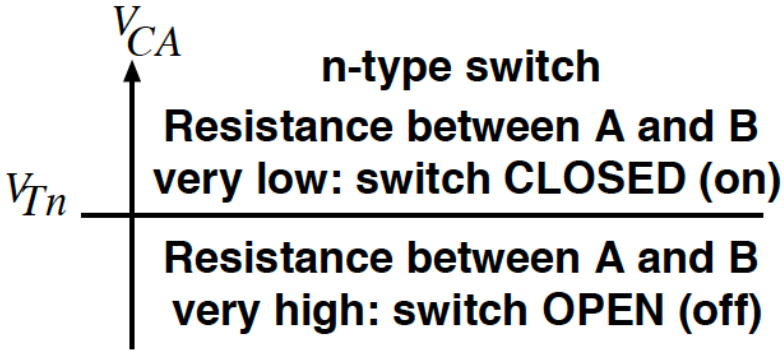
TYPICAL VALUES FOR A 3.3V CMOS TECHNOLOGY

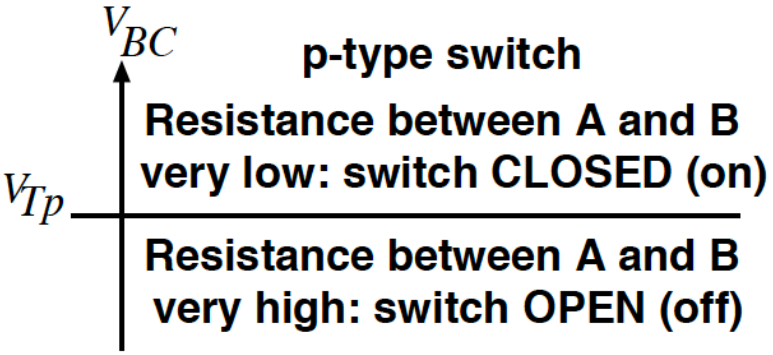
| | | | |
|---|---|---|---|
| $V_{Hmax}$ | 3.3V | $V_{Lmax}$ | 0.8V |
| $V_{Hmin}$ | 2.0V | $V_{Lmin}$ | 0.0V |

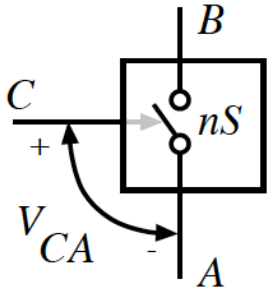
# VOLTAGE REGIONS

| | | | |
|---|---|---|---|
| $V_{Hmax}$ | 3.3V | $V_{Lmax}$ | 0.8V |
| $V_{Hmin}$ | 2.0V | $V_{Lmin}$ | 0.0V |

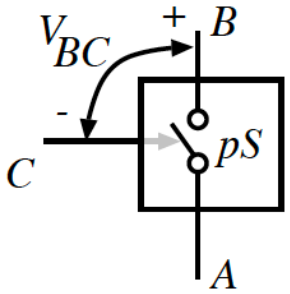



$V_{CA}$
n-type switch
Resistance between A and B
very low: switch CLOSED (on)
$V_{Tn}$
Resistance between A and B
very high: switch OPEN (off)

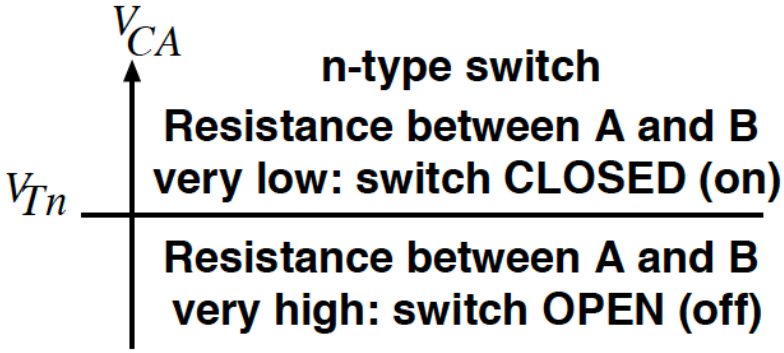

$V_{BC}$
p-type switch
Resistance between A and B
very low: switch CLOSED (on)
$V_{Tp}$
Resistance between A and B
very high: switch OPEN (off)

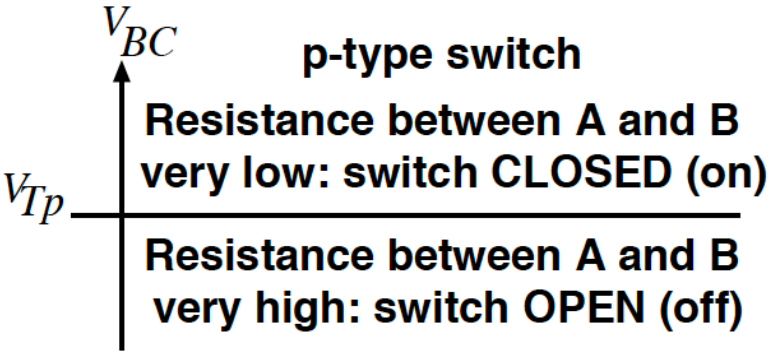

B
C
nS
+
$V_{CA}$
-
A

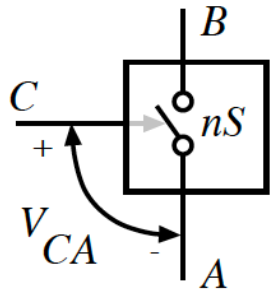
(a)


$V_{BC}$
+
B
-
pS
C
A

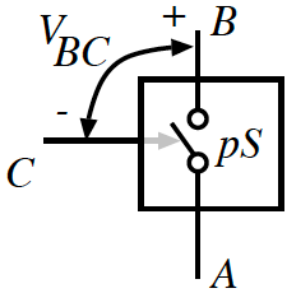
# STRUCTURE AND OPERATION OF TRANSISTORS



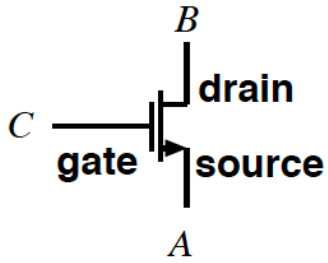



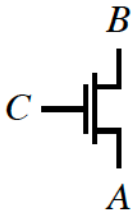

(a)



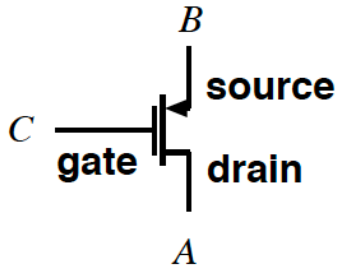

NMOS transistor



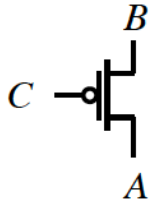

logical symbol




PMOS transistor



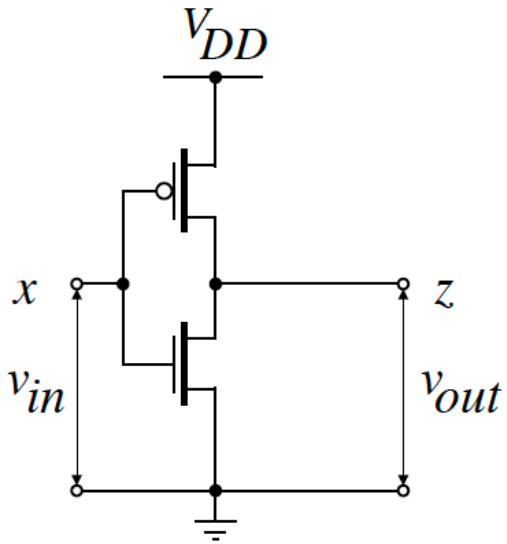

logical symbol

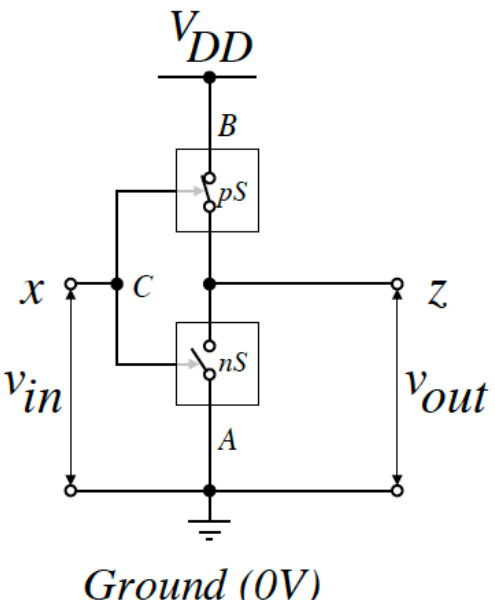



(b)

# CMOS NOT GATE

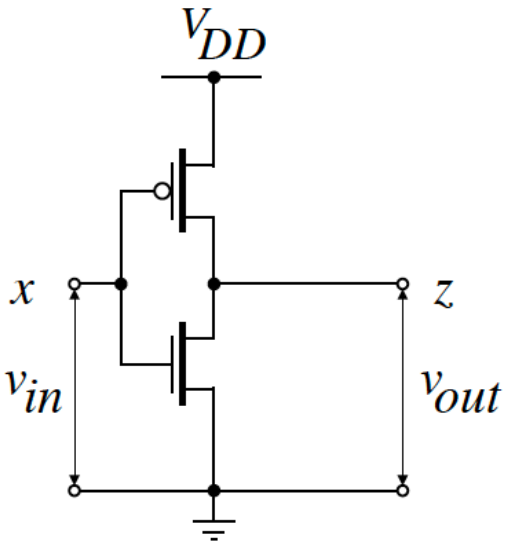
- COMPLEMENTARY MOS CIRCUIT

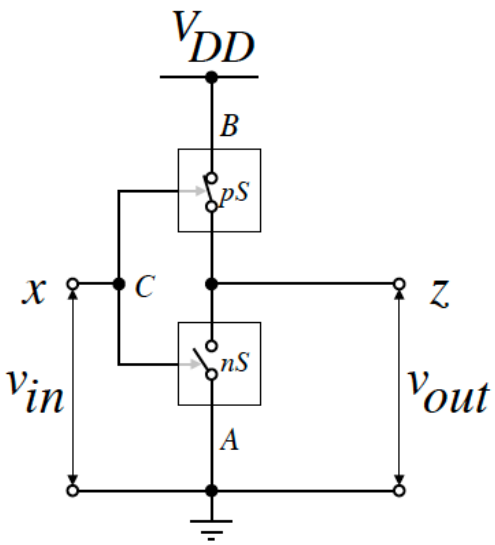


# CMOS NOT GATE

- COMPLEMENTARY MOS CIRCUIT

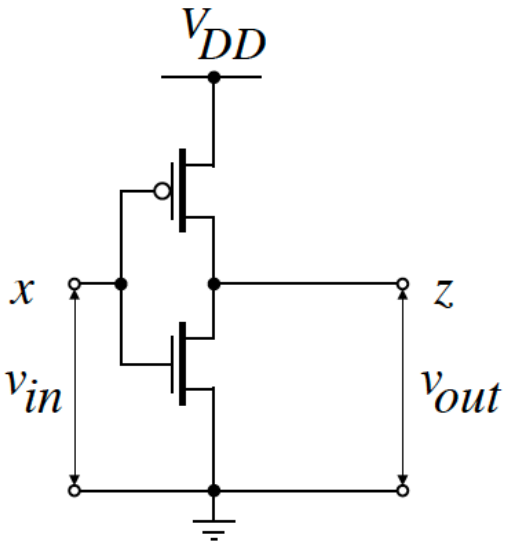


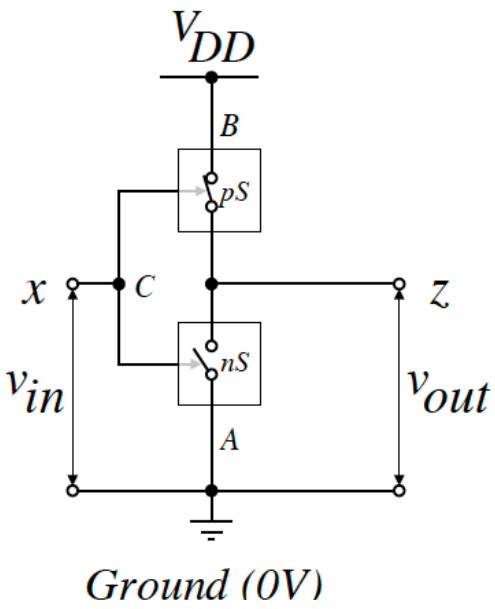




| $v_{in}$ | $v_{out}$ |
|---|---|
| $V_H$ | $V_L$ |
| $V_L$ | $V_H$ |

# CMOS NOT GATE

- COMPLEMENTARY MOS CIRCUIT



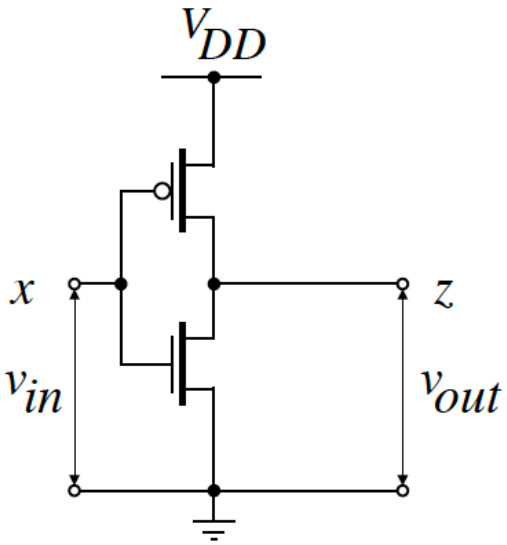



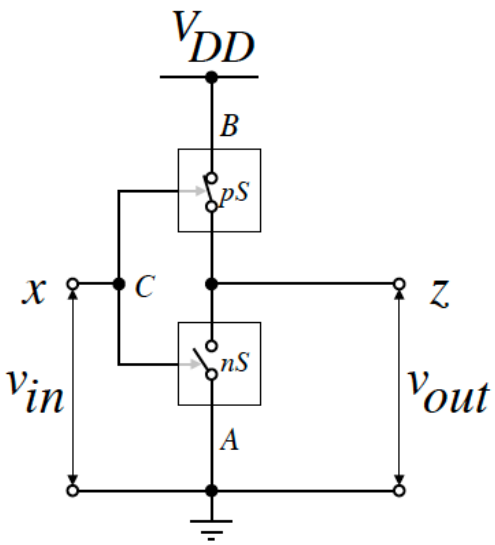

| $v_{in}$ | $v_{out}$ |
|---|---|
| $V_H$ | $V_L$ |
| $V_L$ | $V_H$ |

Which gate is this?

# CMOS NOT GATE

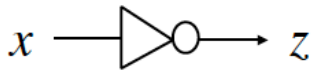
- COMPLEMENTARY MOS CIRCUIT



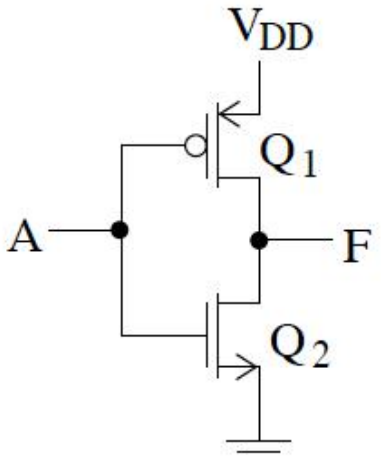




*Ground (0V)*

| $v_{in}$ | $v_{out}$ |
|---|---|
| $V_H$ | $V_L$ |
| $V_L$ | $V_H$ |



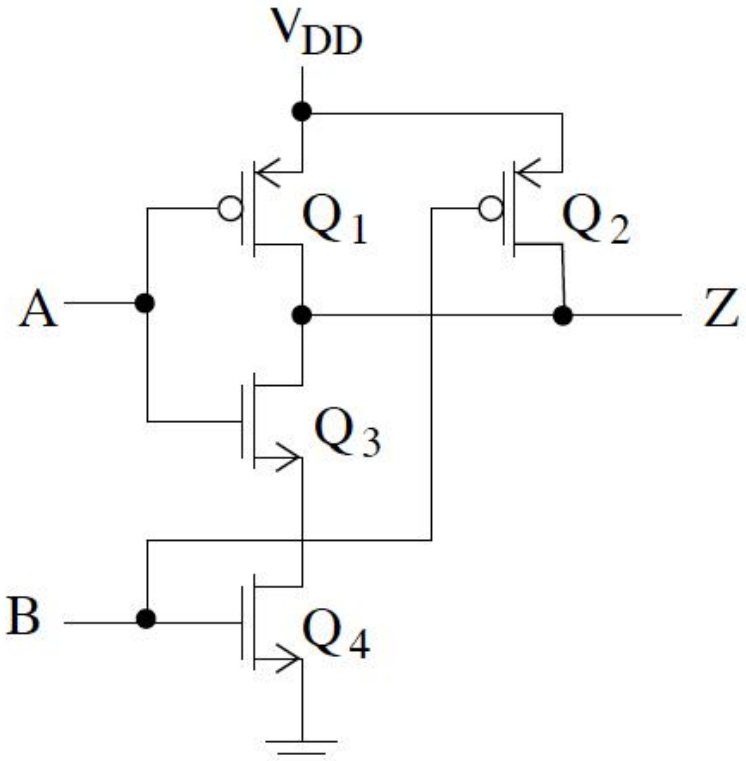

| x | z |
|---|---|
| 1 | 0 |
| 0 | 1 |




| A | $Q_1$ | $Q_2$ | F |
|---|---|---|---|
| 0 | Low | High | 1 ($V_H$) |
| 1 | High | Low | 0 ($V_L$) |

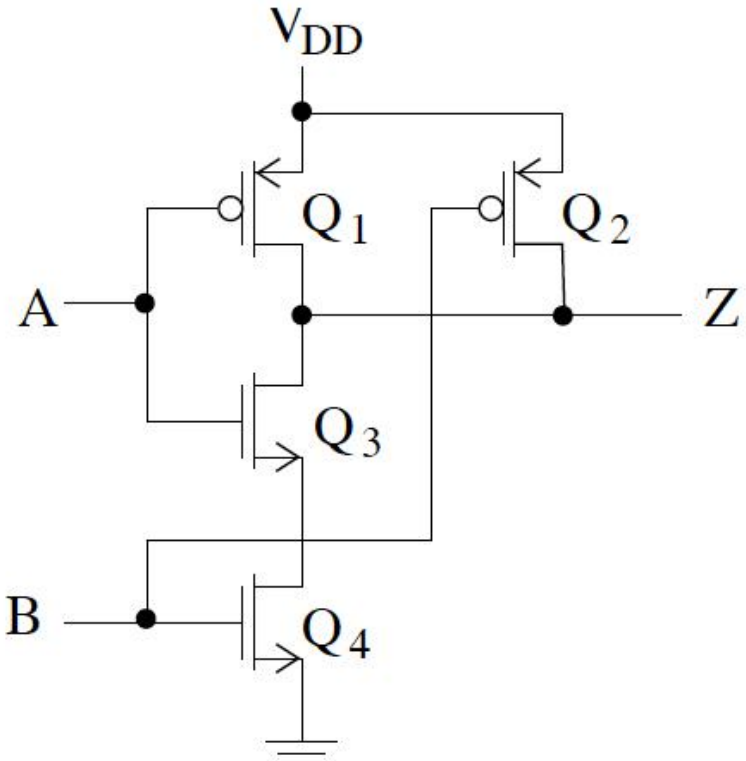
- To analyze CMOS circuit:
  - Make table with inputs, transistors, and output(s)
  - For each row of table (setting of inputs), check whether transistor resistance is High,Low
  - For each row of table, check if output has clean path to power (1) ground (0)

# CMOS




| A | B | $Q_1$ | $Q_2$ | $Q_3$ | $Q_4$ | Z |
|---|---|---|---|---|---|---|
| 0 | 0 | Low | Low | High | High | 1 |
| 0 | 1 | | | | | |
| 1 | 0 | | | | | |
| 1 | 1 | | | | | |

**CMOS**

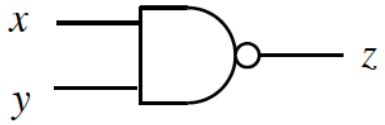


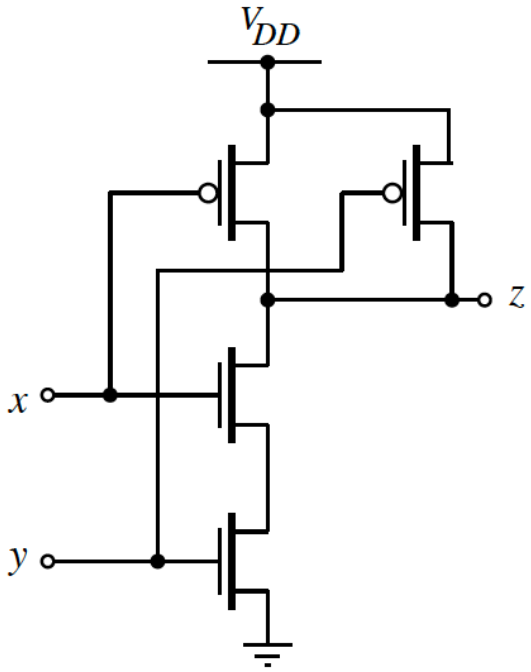

| A | B | $Q_1$ | $Q_2$ | $Q_3$ | $Q_4$ | Z |
|---|---|---|---|---|---|---|
| 0 | 0 | Low | Low | High | High | 1 |
| 0 | 1 | | | | | |
| 1 | 0 | | | | | |
| 1 | 1 | | | | | |

Which Gate is this?

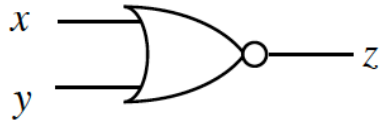
# NAND and NOR GATES

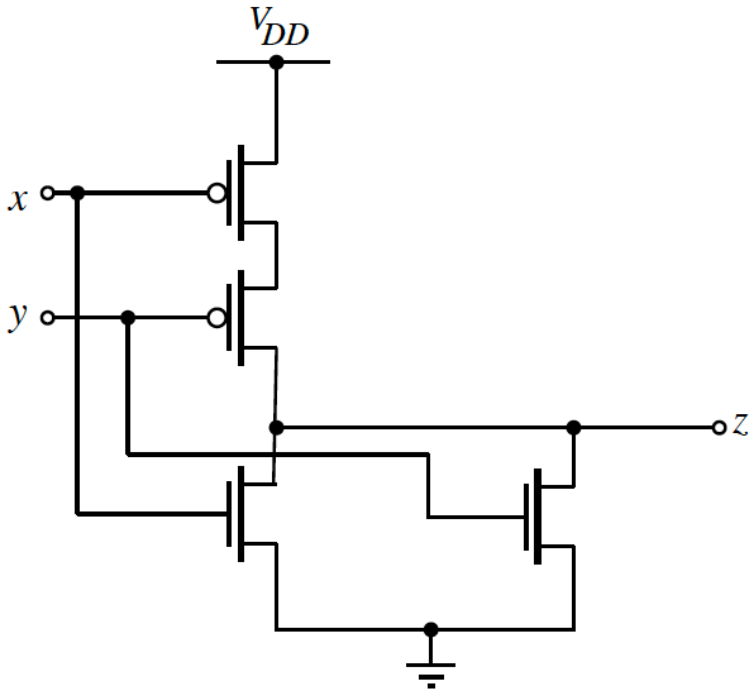
Circuit 1: NAND



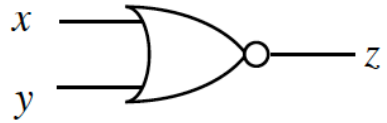

Circuit 2: NOR

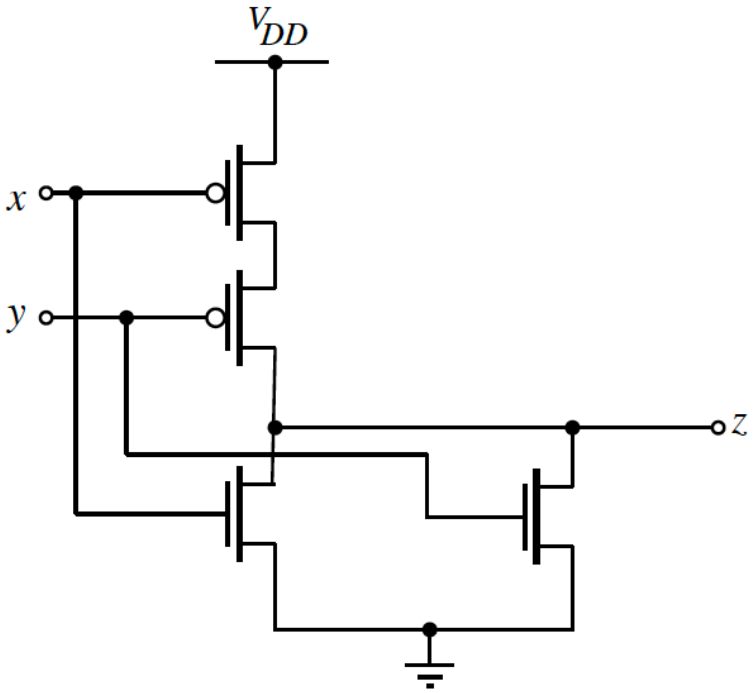


# NAND and NOR GATES

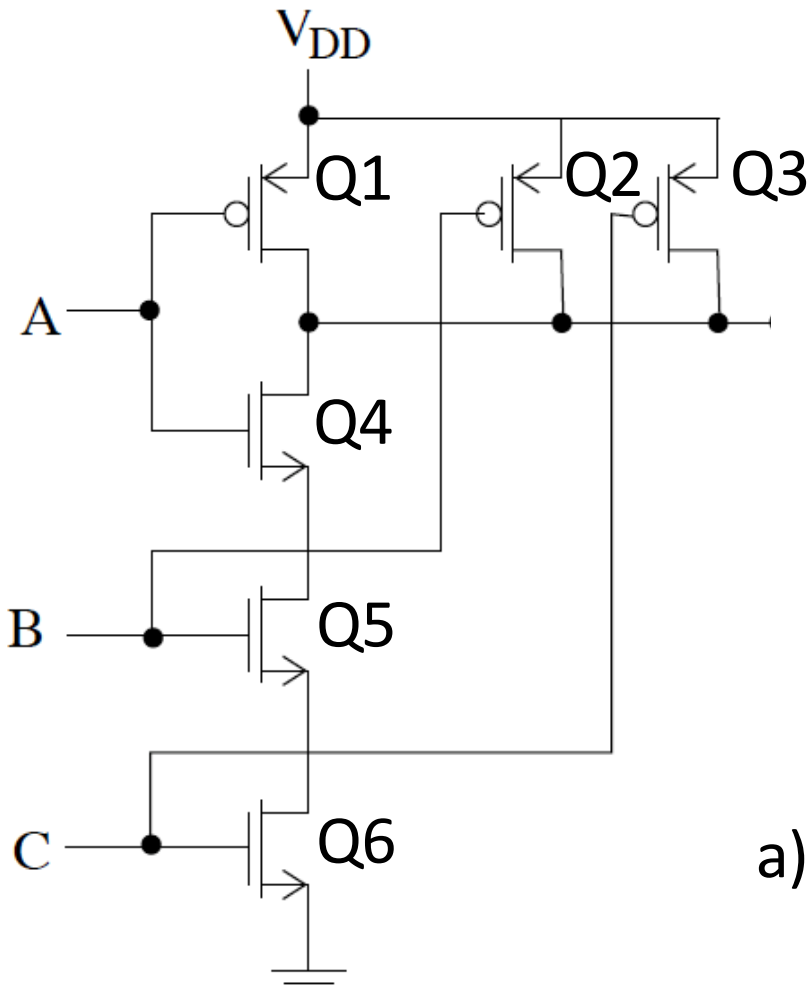
Circuit 2: NOR




| x | y | Q1 | Q2 | Q3 | Q4 | z |
|---|---|---|---|---|---|---|
| | | | | | | |

# Clicker Question




| A B C | Q1 | Q2 | Q3 | Q4 | Q5 | Q6 |
|---|---|---|---|---|---|---|
| 0 0 0 | ? | ? | ? | ? | ? | ? |

a) H, H, H, L, L, L

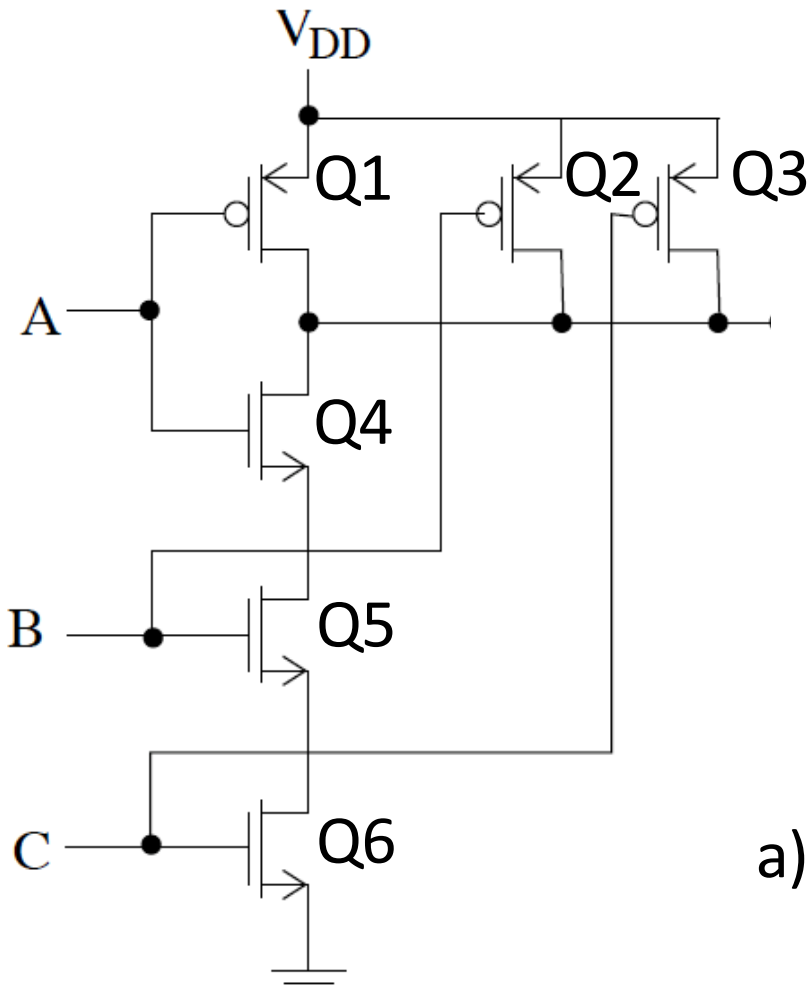
b) L, H, L, H, L, H

c) L, L, L, H, H, H

d) H, L, H, L, H, L

e) none

# Clicker Question




| A | B | C | Q1 | Q2 | Q3 | Q4 | Q5 | Q6 |
|---|---|---|---|---|---|---|---|---|
| 0 | 1 | 0 | ? | ? | ? | ? | ? | ? |

a) H, H, H, L, L, L

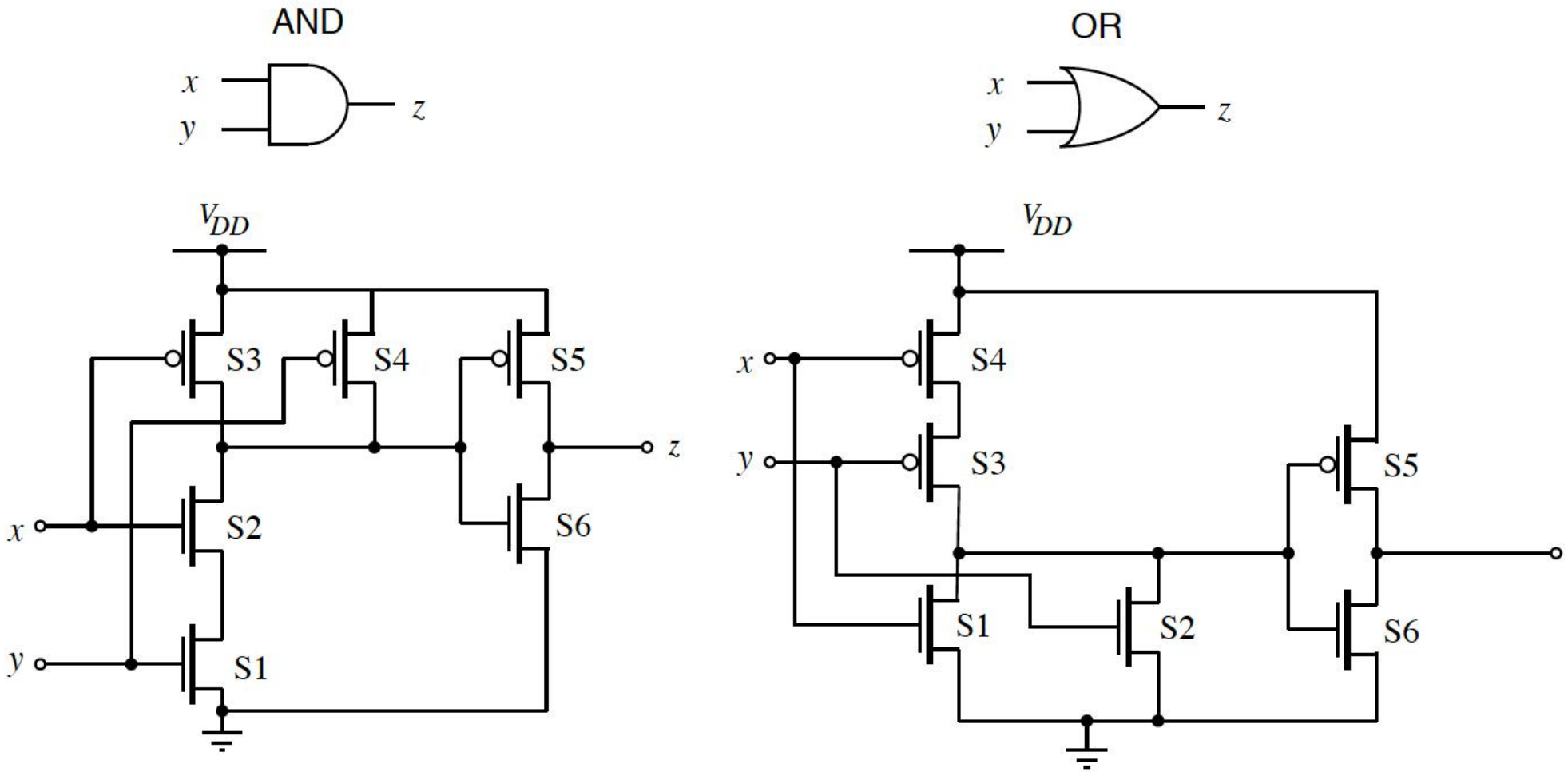
b) L, H, L, H, L, H

c) L, L, L, H, H, H

d) H, L, H, L, H, L

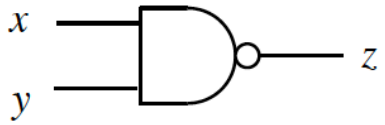
e) none

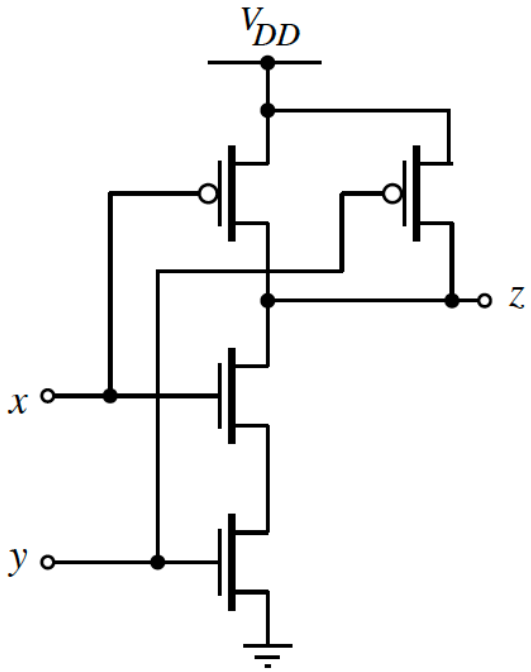
# AND and OR GATES



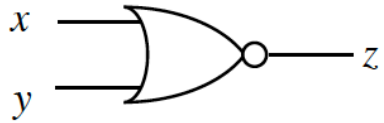
# NAND and NOR GATES

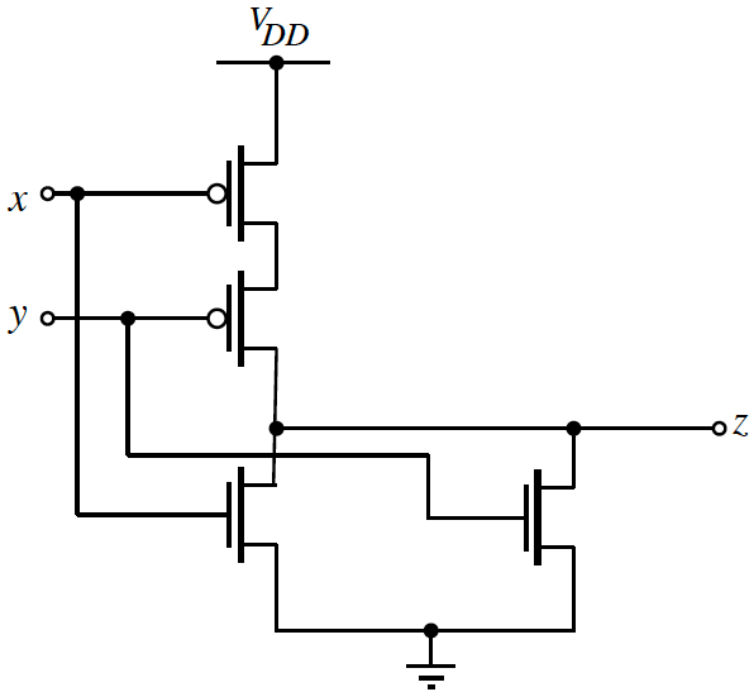
Circuit 1: NAND



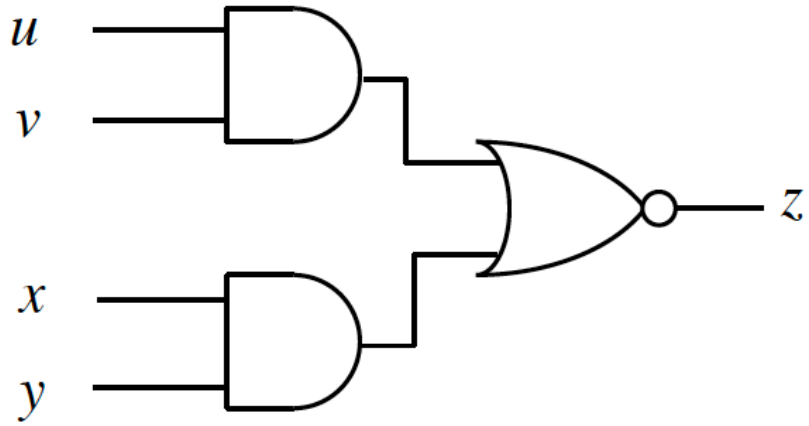

Circuit 2: NOR



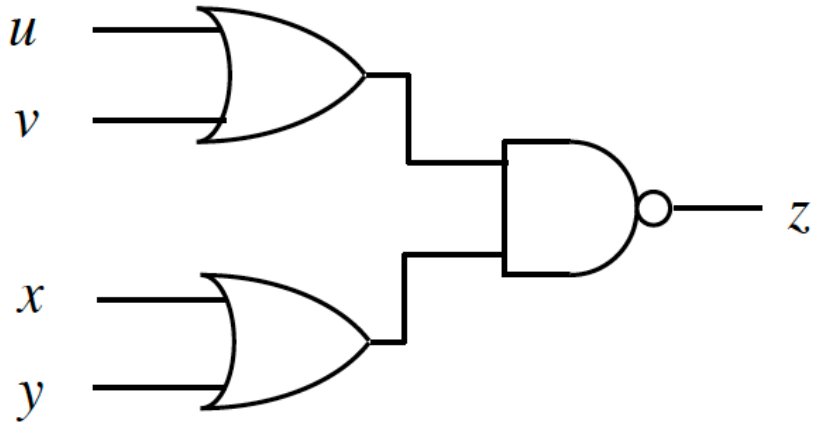
# COMPLEX GATES

## AND-OR-INVERT (AOI)

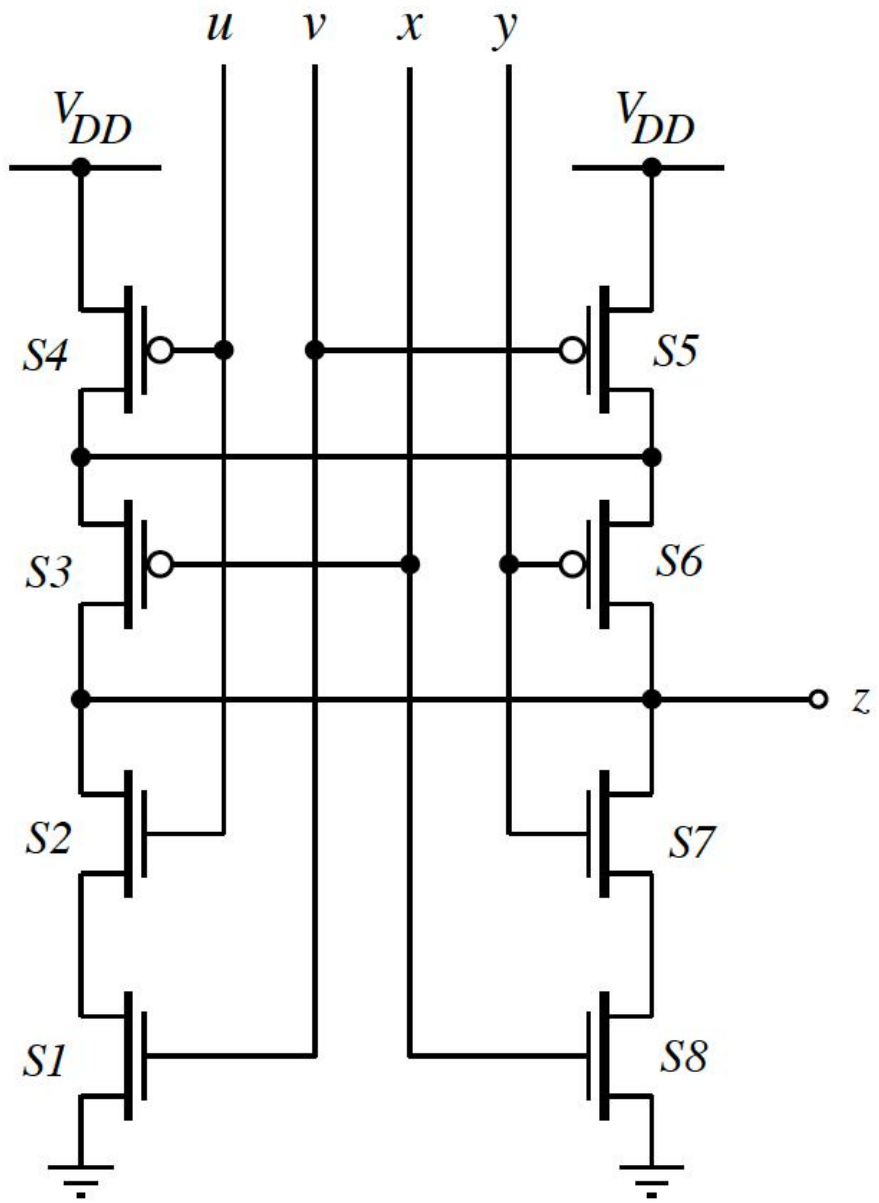


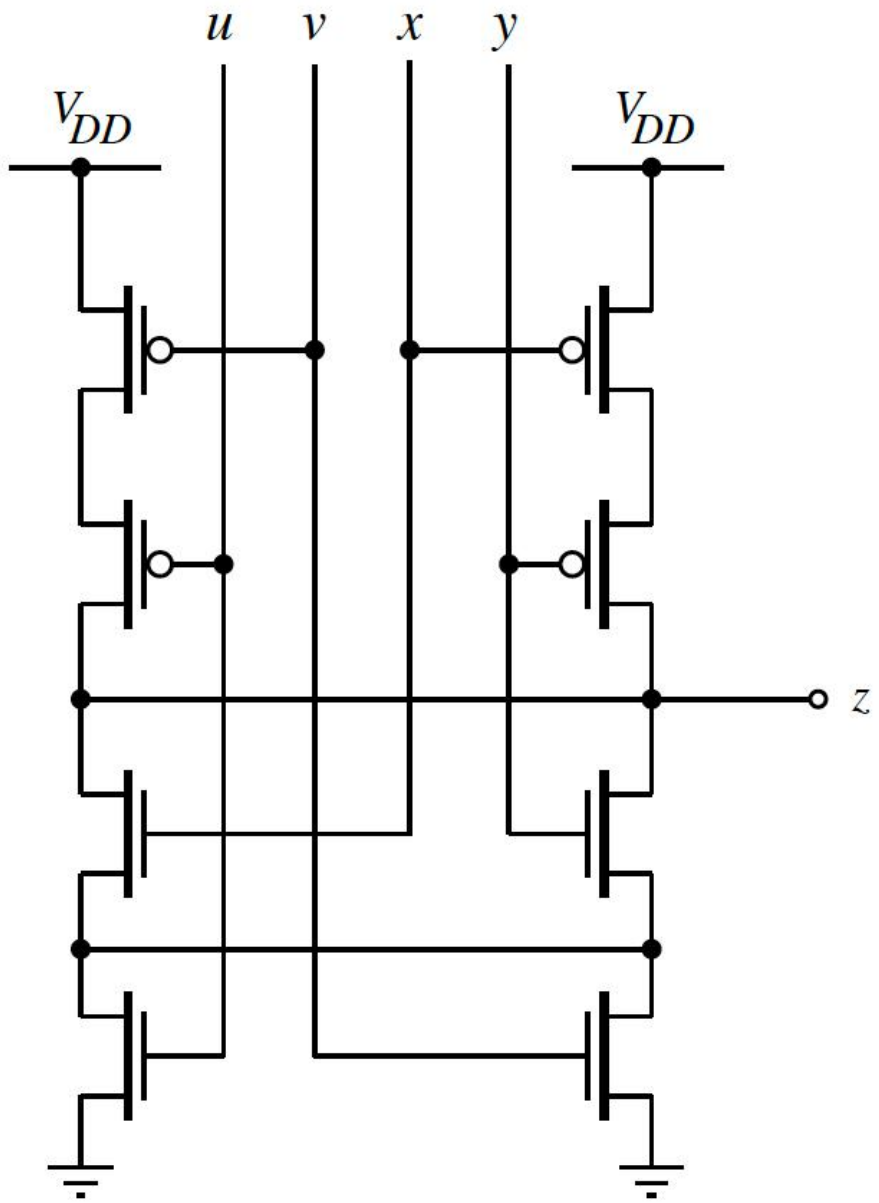

$z = (uv + xy)'$

## OR-AND-INVERT (OAI)

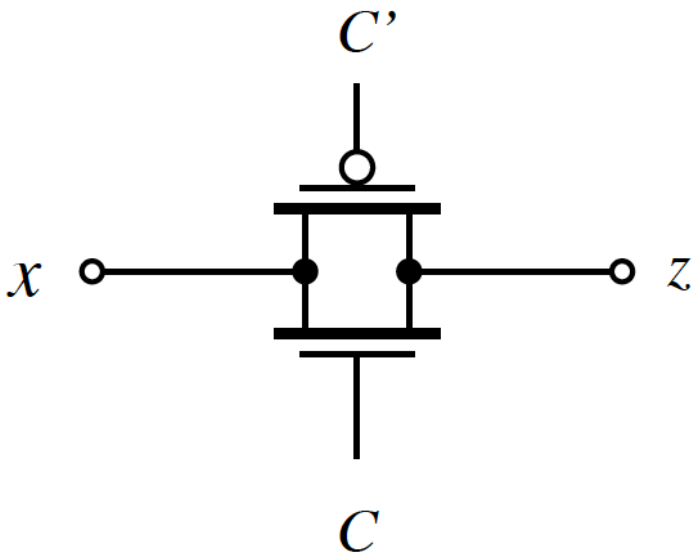



$z = [(u+v)(x+y)]'$


u
v
x
y
$V_{DD}$
$V_{DD}$
S4
S5
S3
S6
z
S2
S7
S1
S8


u
v
x
y
$V_{DD}$
$V_{DD}$
z

# TRANSMISSION GATE




| C | n-switch | p-switch | z |
|---|---|---|---|
| 0 | off | off | Z |
| 1 | on | on | x |

*Z - high impedance state*