

# CS M51A, Winter 2021, Assignment 9

(Total Mark: 120 points, 12% )

Due: Wed Mar 10rd, 10:00 AM Pacific Time

Student Name:

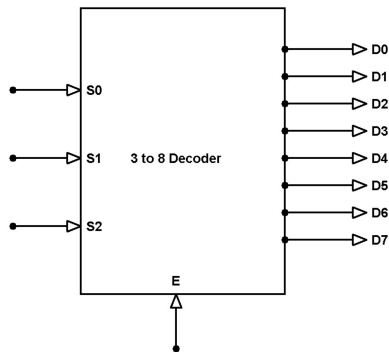
Student ID:

**Note:** You must complete the assignments entirely on your own,  
without discussing with others.

1. (10 Points) Using the following decoder, AND and OR Gates, implement the following function. Please show which decoder's input must be connected to x, y and z.

$$z_1 = xyz + x'y'z' + x'yz$$

$$z_2 = xy'z' + x'yz' + x'y'z$$



- (10 Points) Using 3-to-8 Decoders and a few other gates (such as OR, AND, or Inverters), design a full-adder. First, draw the truth table for full-adder. Then draw your design.
- (10 Points) Design a 3-to-8 decoder (without the enable input) using only inverters and 2-input ANDs. Your design must use the minimum number of gates possible.

4. (10 Points) Design a 4-to-1 MUX using three 2-to-1 MUXes. Label your inputs as  $x_0$ ,  $x_1$ ,  $x_2$ ,  $x_3$ , output as  $y$ , and the select bits as  $s_1$ ,  $s_0$ .

5. (10 Points) Design a 1-to-4 DEMUX using two 1-to-2 DEMUXes. Label your input as  $x$ , outputs as  $y_0$ ,  $y_1$ ,  $y_2$ ,  $y_3$  and the select bits as  $s_1$ ,  $s_0$ .

6. Assume we have three binary input  $(x_2, x_1, x_0)$ , draw a design that computes the following logic expressions using 8-to-1 MUX respectively (**one** MUX for each expression). You may use "0", "1",  $x_2$ ,  $x_1$  or  $x_0$  as your inputs.

(a) (10 Points)  $\Sigma m(0, 3, 5, 6)$

(b) (10 Points)  $\Pi M(1, 3, 5, 7)$

7. (a) (10 Points) Draw the truth table for the following function:  $Z(A,B,C,D) = ABCD + A'D + ABC'$

(b) (10 Points) Given the truth table of part (a), implement Z using **one** 16-to-1 MUX. (You may use "0", "1", A, B, C or D as your inputs)

(c) (10 Points) Given the truth table of part (a), implement Z using only inverters and **one** 8-to-1 MUX. (You may use "0", "1", A, B, C or D as your inputs)

8. (a) (10 Points) Draw the truth table of a 3-input XOR function. (i.e.  $F = \text{XOR}(A, B, C)$ )

(b) (10 Points) Draw a design which computes F using only inverters and **one** 4-to-1 MUX. (You may use "0", "1", A, B, or C as your inputs)