21W-COMSCIM51A-1 Homework 4

CHARLES ZHANG

TOTAL POINTS

87 / 90

QUESTION 1

1 20 pts

1.1 a **14 / 14**

✓ **+ 14 pts** **Correct**

![Screen_Shot_2021-01-30_at_12.32.42_AM.png](/files/0aaaea84-e1e1-40c0-b9bf-4868b22aa514)

+ 0 pts Placeholder: use point adjustment, 0.5 for each.

1.2 b **6 / 6**

✓ **- 0 pts** **Correct**

- 3 pts Should be $$\Sigma m(0, 2, 3)$$ or $$A'B' + AB' + AB$$

- 3 pts Should be $$\Pi M(1)$$ or $$A + B'$$

QUESTION 2

2 16 pts

2.1 a **4 / 4**

✓ **- 0 pts** **Correct:**

Sum of Products:

A'B

$$\Sigma$$m(1)

Product of Sums:

(A+B)(A'+B)(A'+B')

$$\prod$$M(0, 2, 3)

- 2 pts Incorrect / missing sum of minterms

- 2 pts Incorrect / missing product of maxterms

- 4 pts Blank

2.2 b **3 / 6**

- 0 pts Correct

- 2 pts Minor error

✓ **- 3 pts** **Used NAND instead of NOR**

- 3 pts Did not negate B

- 3 pts NPN is attached to VDD / PNP attached to GND

- 3 pts Used more than 6 transistors

- 4.5 pts F can float or short

- 6 pts Blank

2.3 c **6 / 6**

✓ **- 0 pts** **Correct**

- 1 pts Used variable complements as inputs

- 1 pts Minor error

- 3 pts Error

- 4 pts Major error

- 6 pts Blank

QUESTION 3

3 16 pts

3.1 a **8 / 8**

✓ **- 0 pts** **Correct: $$0.794 = (0.08 + 0.075\times 2) + (0.08 + 0.038)+(0.07 + 0.016)+(0.06 + 0.075\times 4)$$**

- 2 pts Missing $$0.08 + 0.075\times 2$$

- 2 pts Missing $$0.08 + 0.038$$

- 2 pts Missing $$0.07 + 0.016$$

- 2 pts Missing $$0.06 + 0.075\times 4$$

3.2 b **8 / 8**

✓ **- 0 pts** **Correct: $$0.53 = (0.09 + 0.027\times 2) + (0.09 + 0.027)+(0.06 + 0.075)+(0.07 + 0.016\times 4)$$**

- 2 pts Missing $$0.09 + 0.027\times 2$$

- 2 pts Missing $$0.09 + 0.027$$

- 2 pts Missing $$0.06 + 0.075$$

- 2 pts Missing $$0.07 + 0.016\times 4$$

QUESTION 4

4 12 pts

4.1 a 2 / 2

✓ **- 0 pts** **Correct: B**

- 2 pts Incorrect

- 2 pts Blank

4.2 b 2 / 2

✓ **- 0 pts** **Correct: A**

- 2 pts Incorrect

- 2 pts Blank

4.3 c 8 / 8

✓ **- 0 pts** **Correct: S0'S1'D + S0'S1C + S0S1'B + S0S1A**

- 2 pts 1 term incorrect

- 4 pts 2 terms incorrect

- 6 pts 3 terms incorrect

- 8 pts 4 terms incorrect

- 4 pts Not a sum of product

- 4 pts Not in terms of A, B, C, D, S0, S1

- 8 pts Blank

QUESTION 5

5 24 pts

5.1 a 6 / 6

✓ **- 0 pts** **Correct; example answers (note: it is ok to use inverters for inverting the input):**
![Screen_Shot_2021-01-30_at_12.40.48_AM.png](/files/db490e20-52fd-41cf-a553-0f0c04ef56bb)

- 0.5 pts Used not gate for inputs

- 0.5 pts Used VDD and/or GND instead of 0 and 1

- 0.5 pts Must draw out transmission gates

- 2 pts Single error

- 4 pts Major error

- 6 pts Blank

5.2 b 6 / 6

✓ **- 0 pts** **Correct; example answers (note: it is ok to use inverters for inverting the input):**
![Screen_Shot_2021-01-30_at_12.42.55_AM.png](/files/bab94c00-4f34-409f-8ae2-e158eb0aaabf)

- 2 pts Minor error

- 4 pts Major error

- 6 pts Blank

5.3 c 6 / 6

✓ **- 0 pts** **Correct; example answers (note: it is ok to use inverters for inverting the input):**
![Screen_Shot_2021-01-30_at_12.43.53_AM.png](/files/09ce0723-1114-42b8-b802-810e8fceea40)

- 2 pts Minor error

- 3 pts Error

- 4 pts Major error

- 6 pts Blank

5.4 d 6 / 6

✓ **- 0 pts** **Correct; example answers (note: it is ok to use inverters for inverting the input):**
![Screen_Shot_2021-01-30_at_12.44.46_AM.png](/files/0c05c6e3-adac-4c3a-ae54-7f667d6446a5)

- 2 pts Functionally correct, but including gates other than transmission gates, e.g. inverter, *MOS.

- 2 pts Minor error

- 3 pts Error

- 4 pts Major error

QUESTION 6

6 6 2 / 2

✓ **- 0 pts** **Correct:**
Something related to PMOS passing a 1, and NMOS passing a 0.
Or something related to PMOS passing a weak 0 and NMOS passing a weak 1.

- 1 pts Minor error

- 2 pts Blank / incorrect

- 1 pts Needs to be more specific

Charles Zhang
305413659
Academic Integrity:

CS M51A HW#4

1a)

A	B	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Z
0	0	L	H	H	L	L	H	1
0	1	L	H	H	L	H	L	0
1	0	H	L	L	H	L	H	1
1	1	H	L	L	H	H	L	1

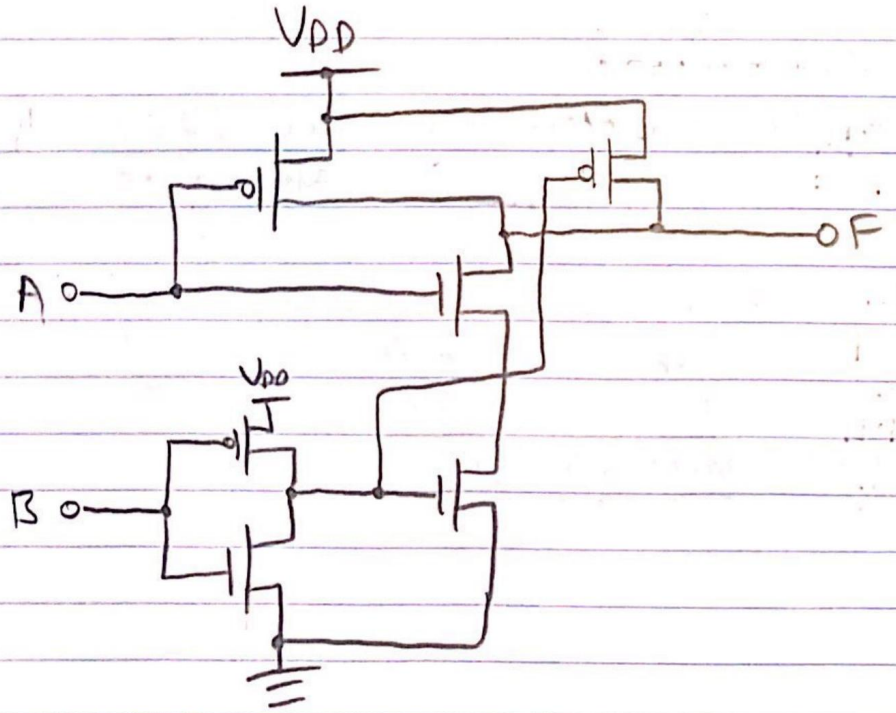
1b) $\Sigma m(0,2,3)$, $\Pi M(1)$

2a)

A	B	F
0	0	0
0	1	1
1	0	0
1	1	0

$\Sigma m(1) = \Pi M(0,2,3)$

2b) $F = A'B = (A+B')'$ → NOR gate



1.1 a **14 / 14**

✓ **+ 14 pts** **Correct**

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+ 0 pts Placeholder: use point adjustment, 0.5 for each.

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1a)

A	B	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Z
0	0	L	H	H	L	L	H	1
0	1	L	H	H	L	H	L	0
1	0	H	L	L	H	L	H	1
1	1	H	L	L	H	H	L	1

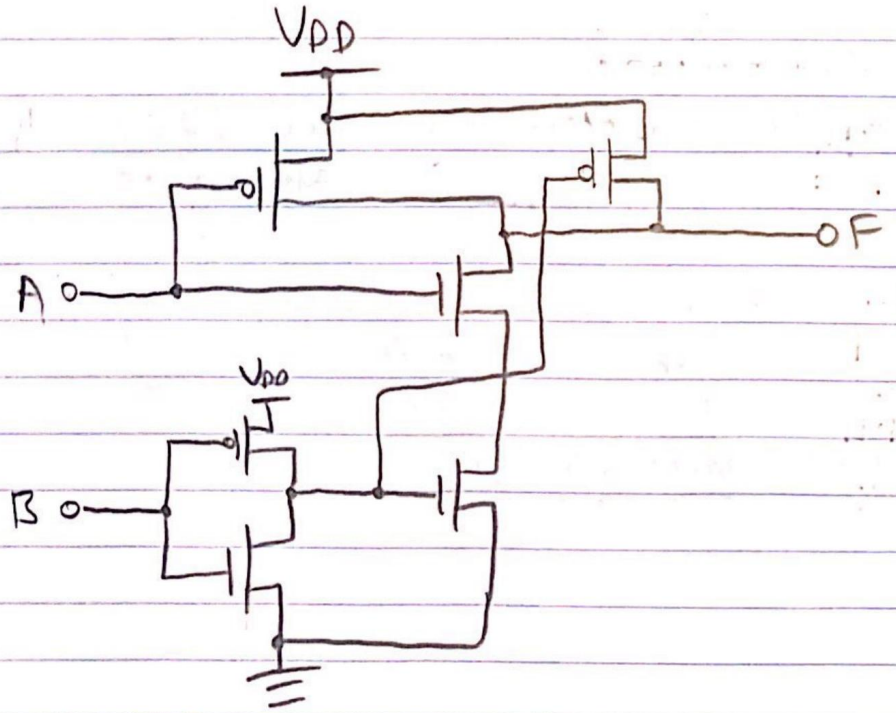
1b) $\Sigma m(0,2,3)$, $\Pi M(1)$

2a)

A	B	F
0	0	0
0	1	1
1	0	0
1	1	0

$\Sigma m(1) = \Pi M(0,2,3)$

2b) $F = A'B = (A+B')'$ → NOR gate



1.2 b 6 / 6

✓ **- 0 pts** Correct

- 3 pts Should be $$\Sigma m(0, 2, 3)$$ or $$A'B' + AB' + AB$$

- 3 pts Should be $$\Pi M(1)$$ or $$A + B'$$

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1a)

A	B	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Z
0	0	L	H	H	L	L	H	1
0	1	L	H	H	L	H	L	0
1	0	H	L	L	H	L	H	1
1	1	H	L	L	H	H	L	1

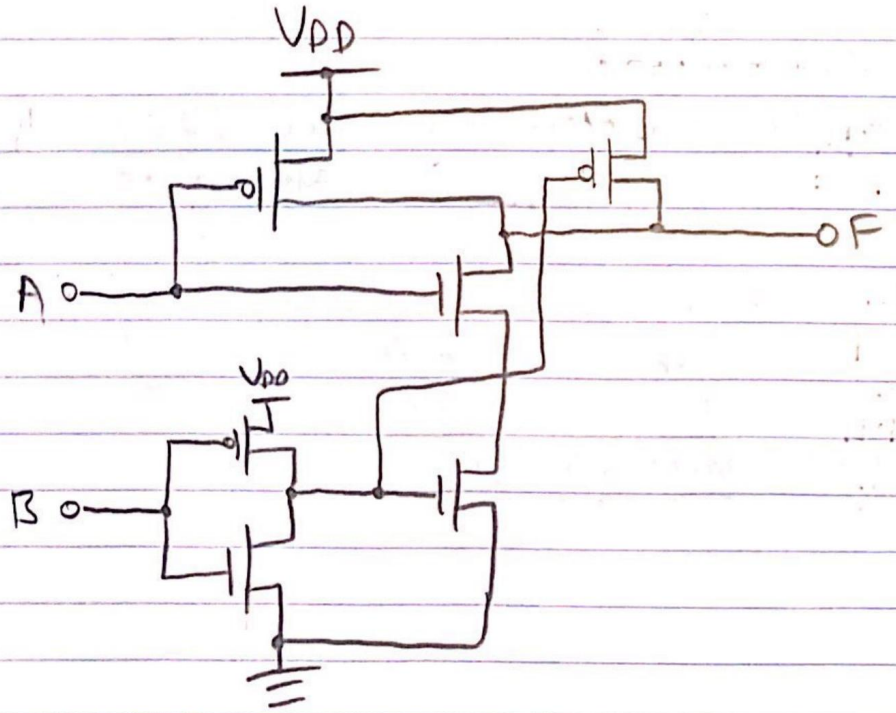
1b) $\Sigma m(0,2,3)$, $\Pi M(1)$

2a)

A	B	F
0	0	0
0	1	1
1	0	0
1	1	0

$\Sigma m(1) = \Pi M(0,2,3)$

2b) $F = A'B = (A+B')'$ → NOR gate



2.1 a **4 / 4**

✓ **- 0 pts** **Correct:**

Sum of Products:

A'B

$$\Sigma$$m(1)

Product of Sums:

(A+B)(A'+B)(A'+B')

$$\prod$$M(0, 2, 3)

- 2 pts Incorrect / missing sum of minterms

- 2 pts Incorrect / missing product of maxterms

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1a)

A	B	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Z
0	0	L	H	H	L	L	H	1
0	1	L	H	H	L	H	L	0
1	0	H	L	L	H	L	H	1
1	1	H	L	L	H	H	L	1

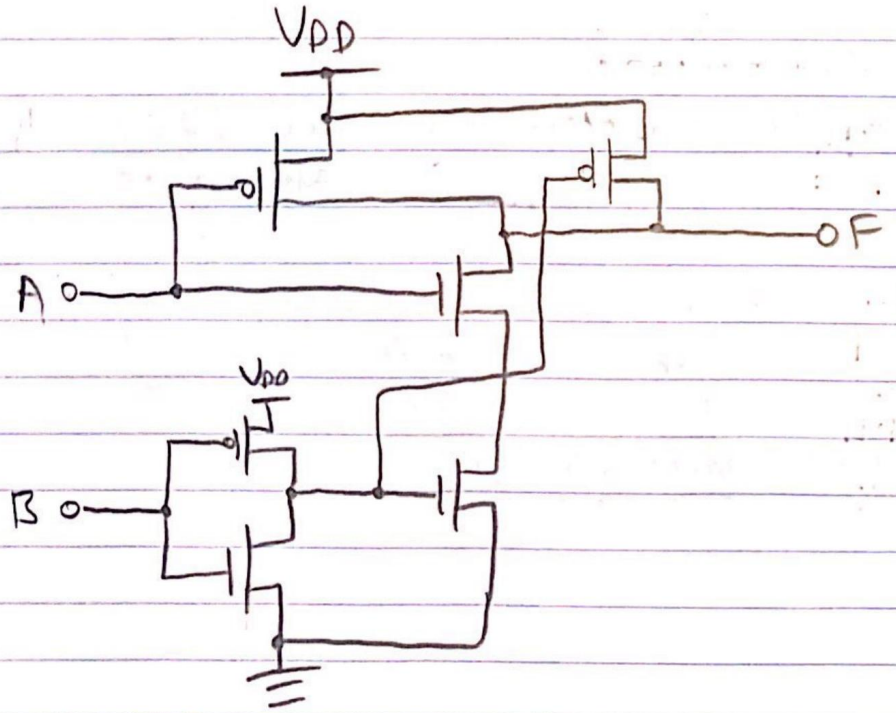
1b) $\Sigma m(0,2,3)$, $\Pi M(1)$

2a)

A	B	F
0	0	0
0	1	1
1	0	0
1	1	0

$\Sigma m(1) = \Pi M(0,2,3)$

2b) $F = A'B = (A+B')'$ → NOR gate



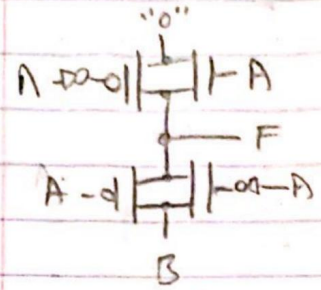
2.2 b **3 / 6**

- **0 pts** Correct
- **2 pts** Minor error

✓ **- 3 pts** **Used NAND instead of NOR**

- **3 pts** Did not negate B
- **3 pts** NPN is attached to VDD / PNP attached to GND
- **3 pts** Used more than 6 transistors
- **4.5 pts** F can float or short
- **6 pts** Blank

✓ 2c) $F = A'B = (A + B')'$ → AND gate



A	B	G_1	G_2	F
0	0	on	off	0 ✓
0	1	off	on	1 ✓
1	0	on	off	0 ✓
1	1	off	on	0 ✓

3a) $L = 4$, find $t_{pLH}(0,2)$

$x = t_{pLH}(OR) + t_{pLH}(AND) + t_{pHL}(NOR) + t_{pLH}(NOR)$

$x = (0.08 + 0.075(2)) + (0.08 + 0.038) + (0.07 + 0.016) + (0.06 + 0.075(4))$

$x = 0.23 + 0.118 + 0.086 \quad 0.36 = 0.794\,ns$

$y = t_{pLH}(OR) + t_{pHL}(NOR) + t_{pLH}(NOR)$

$y = (0.08 + 0.075(2)) + (0.07 + 0.016) + (0.06 + 0.075(4))$

$y = 0.23 + 0.086 + 0.36 = 0.676\,ns$

$\boxed{t_{pLH}(0,2) = \max(x,y) = 0.794\,ns}$

3b) $L = 4$, find $t_{pHL}(b,z)$

$x = t_{pHL}(AND) + t_{pHL}(AND) + t_{pLH}(NOR) + t_{pHL}(NOR)$

$x = (0.09 + 0.027(2)) + (0.09 + 0.027) + (0.06 + 0.075) + (0.07 + 0.016(4))$

$x = 0.144 + 0.117 + 0.135 + 0.134 = 0.53\,ns$

$y = t_{pHL}(AND) + t_{pLH}(NOR) + t_{pHL}(NOR)$

$y = 0.144 + 0.135 + 0.134 = 0.413\,ns$

$\boxed{t_{pHL}(b,z) = \max(x,y) = 0.53\,ns}$

2.3 C **6 / 6**

✓ **- 0 pts** **Correct**

- 1 pts Used variable complements as inputs

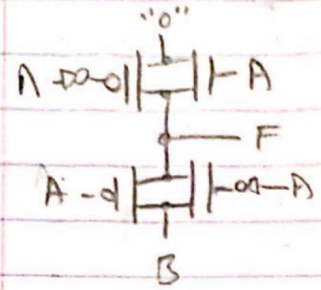
- 1 pts Minor error

- 3 pts Error

- 4 pts Major error

- 6 pts Blank

✓ 2c) $F = A'B = (A + B')'$ → AND gate



A	B	G_1	G_2	F
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3.1 a **8 / 8**

✓ **- 0 pts** **Correct: $$0.794 = (0.08 + 0.075\times 2) + (0.08 + 0.038)+(0.07 + 0.016)+(0.06 + 0.075\times 4)$$**

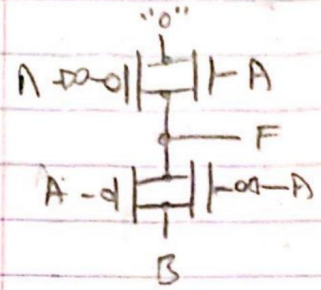
- 2 pts Missing $$0.08 + 0.075\times 2$$

- 2 pts Missing $$0.08 + 0.038$$

- 2 pts Missing $$0.07 + 0.016$$

- 2 pts Missing $$0.06 + 0.075\times 4$$

✓ 2c) $F = A'B = (A + B')'$ → AND gate



A	B	G_1	G_2	F
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$\boxed{t_{pLH}(0,2) = \max(x,y) = 0.794\,ns}$

3b) $L = 4$, find $t_{pHL}(b,z)$

$x = t_{pHL}(AND) + t_{pHL}(AND) + t_{pLH}(NOR) + t_{pHL}(NOR)$

$x = (0.09 + 0.027(2)) + (0.09 + 0.027) + (0.06 + 0.075) + (0.07 + 0.016(4))$

$x = 0.144 + 0.117 + 0.135 + 0.134 = 0.53\,ns$

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$y = 0.144 + 0.135 + 0.134 = 0.413\,ns$

$\boxed{t_{pHL}(b,z) = \max(x,y) = 0.53\,ns}$

3.2 b **8 / 8**

✓ **- 0 pts** **Correct: $$0.53 = (0.09 + 0.027\times 2) + (0.09 + 0.027)+(0.06 + 0.075)+(0.07 + 0.016\times 4)$$**

- 2 pts Missing $$0.09 + 0.027\times 2$$

- 2 pts Missing $$0.09 + 0.027$$

- 2 pts Missing $$0.06 + 0.075$$

- 2 pts Missing $$0.07 + 0.016\times 4$$

4a) $S_0 = 1, S_1 = 0$

A → Z
B → B
C → Z
D → D
B → B
D → Z

→ $S_1 = 0$

→ $S_0 = 1$

Output = B

4b) $S_0 = 1, S_1 = 1$

A → A
B → Z
C → C
D → Z
A → A
C → Z

→ $S_1 = 1$

→ $S_0 = 1$

Output = A

4c)

S_1	S_0	F
0	0	D
0	1	B
1	0	C
1	1	A

$$(S_1' S_0' D) + (S_1' S_0 B) + (S_1 S_0' C) + (S_1 S_0 A)$$

4.1 a **2 / 2**

✓ **- 0 pts Correct: B**

- 2 pts Incorrect

- 2 pts Blank

4a) $S_0 = 1, S_1 = 0$

A → Z
B → B
C → Z
D → D
B → B
D → Z

→ $S_1 = 0$

→ $S_0 = 1$

Output = B

4b) $S_0 = 1, S_1 = 1$

A → A
B → Z
C → C
D → Z
A → A
C → Z

→ $S_1 = 1$

→ $S_0 = 1$

Output = A

4c)

S_1	S_0	F
0	0	D
0	1	B
1	0	C
1	1	A

$$(S_1' S_0' D) + (S_1' S_0 B) + (S_1 S_0' C) + (S_1 S_0 A)$$

4.2 b **2 / 2**

✓ **- 0 pts Correct: A**

- 2 pts Incorrect

- 2 pts Blank

4a) $S_0 = 1, S_1 = 0$

A → Z
B → B
C → Z
D → D
B → B
D → Z

→ $S_1 = 0$

→ $S_0 = 1$

Output = B

4b) $S_0 = 1, S_1 = 1$

A → A
B → Z
C → C
D → Z
A → A
C → Z

→ $S_1 = 1$

→ $S_0 = 1$

Output = A

4c)

S_1	S_0	F
0	0	D
0	1	B
1	0	C
1	1	A

$$(S_1' S_0' D) + (S_1' S_0 B) + (S_1 S_0' C) + (S_1 S_0 A)$$

4.3 C **8 / 8**

✓ **- 0 pts** **Correct: S0'S1'D + S0'S1C + S0S1'B + S0S1A**

- 2 pts 1 term incorrect

- 4 pts 2 terms incorrect

- 6 pts 3 terms incorrect

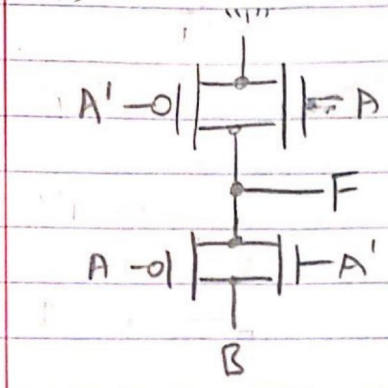
- 8 pts 4 terms incorrect

- 4 pts Not a sum of product

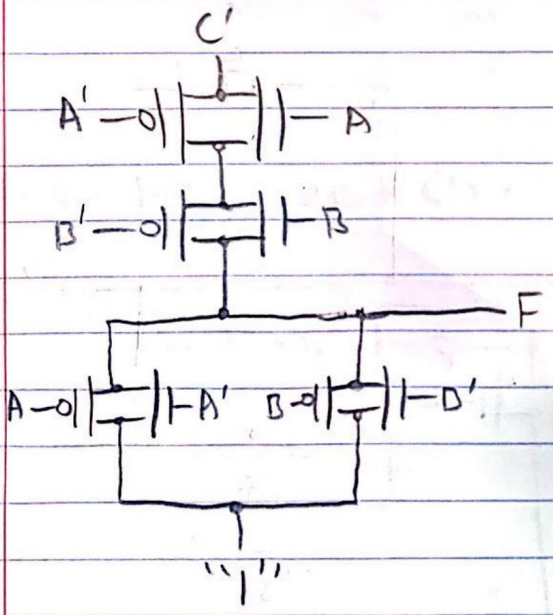
- 4 pts Not in terms of A, B, C, D, S0, S1

- 8 pts Blank

5a) $F = A + B \rightarrow$ OR gate $= (A'B')'$



5b) $F = (ABC)' = A' + B' + C' \rightarrow$ OR gate



5.1 a **6 / 6**

✓ **- 0 pts Correct; example answers (note: it is ok to use inverters for inverting the input):**

![Screen_Shot_2021-01-30_at_12.40.48_AM.png](/files/db490e20-52fd-41cf-a553-0f0c04ef56bb)

- 0.5 pts Used not gate for inputs

- 0.5 pts Used VDD and/or GND instead of 0 and 1

- 0.5 pts Must draw out transmission gates

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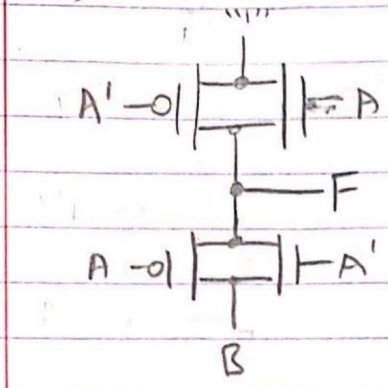

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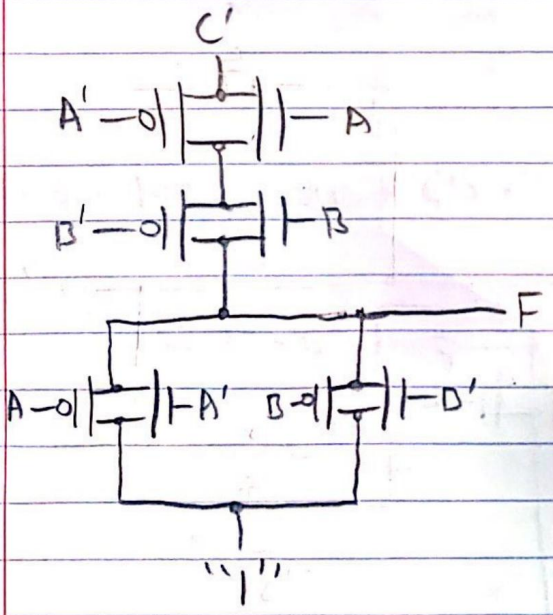

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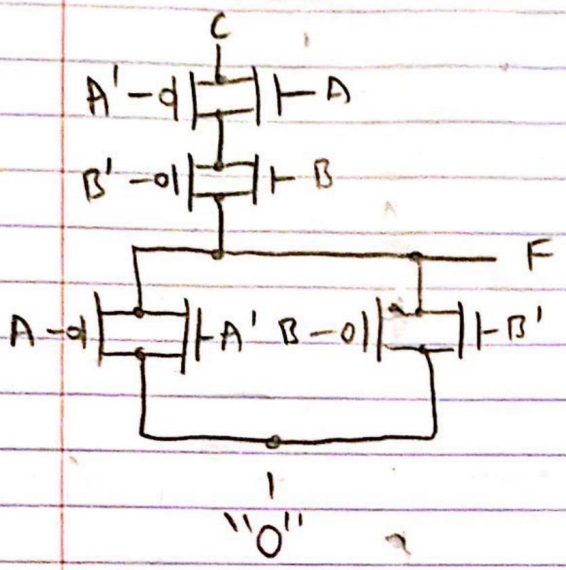
- 2 pts Minor error

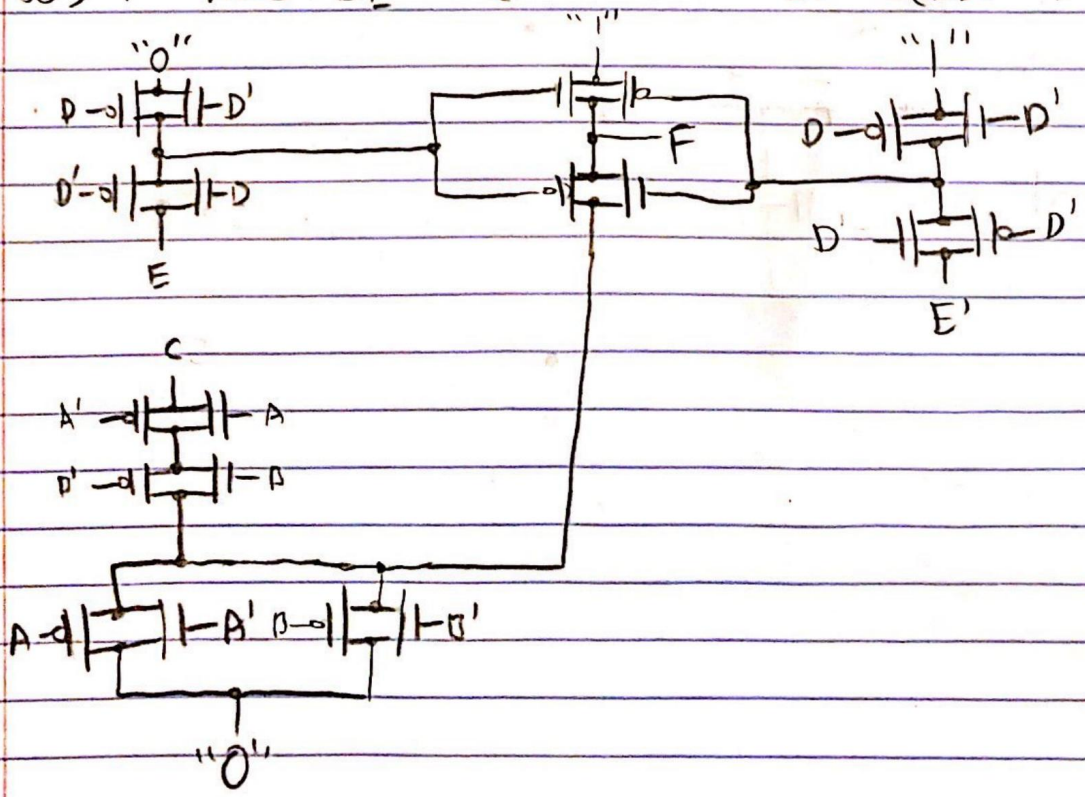
- 4 pts Major error

- 6 pts Blank

5c) F = ABC



5d) F = ABC + DE = (A'+B'+C')' + DE (DE)' = D'+E'



5.3 C **6 / 6**

✓ **- 0 pts** **Correct; example answers (note: it is ok to use inverters for inverting the input):**

![Screen_Shot_2021-01-30_at_12.43.53_AM.png](/files/09ce0723-1114-42b8-b802-810e8fceea40)

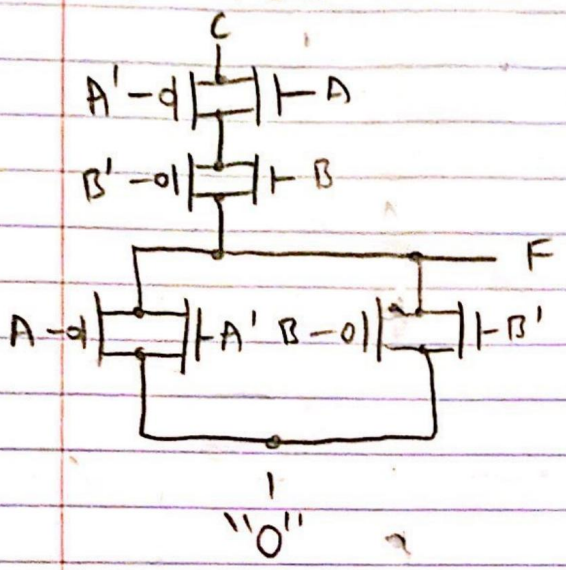
- 2 pts Minor error

- 3 pts Error

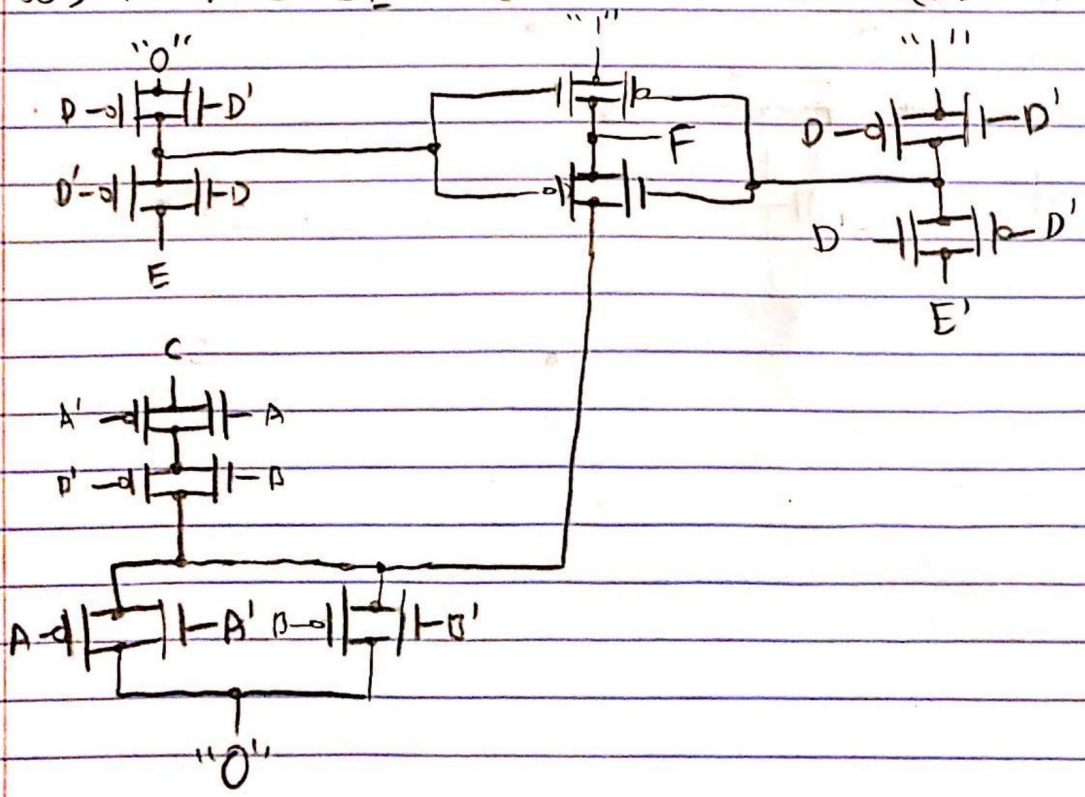
- 4 pts Major error

- 6 pts Blank

5c) F = ABC



5d) F = ABC + DE = (A'+B'+C')' + DE (DE)' = D'+E'



5.4 d **6 / 6**

✓ **- 0 pts Correct; example answers (note: it is ok to use inverters for inverting the input):**

![Screen_Shot_2021-01-30_at_12.44.46_AM.png](/files/0c05c6e3-adac-4c3a-ae54-7f667d6446a5)

- 2 pts Functionally correct, but including gates other than transmission gates, e.g. inverter, *MOS.

- 2 pts Minor error

- 3 pts Error

- 4 pts Major error

6) Both PMOS and NMOS must be used to account for both high and low signals coming in. PMOS gates are only effective switches when connected to high voltage sources. Meanwhile, NMOS gates are only effective switches when connected to a low voltage source. Since the source of the transmission gate can be either high or low voltage, both PMOS and NMOS must be used to account for all possibilities.

6 6 **2 / 2**

✓ **- 0 pts** **Correct:**

Something related to PMOS passing a 1, and NMOS passing a 0.

Or something related to PMOS passing a weak 0 and NMOS passing a weak 1.

- 1 pts Minor error

- 2 pts Blank / incorrect

- 1 pts Needs to be more specific