UCLA Computer Science Department

CS M51A: Logic Design of Digital Systems, Winter 2021

Instructor: Prof. Omid Abari (omid@cs.ucla.edu), http://www.cs.ucla.edu/~omid

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Teaching Assistants: Sicheng Jia (jsicheng@cs.ucla.edu), Xiaojian Ma (xm@cs.ucla.edu)

Lectures: MW 10:00 am - 11:50 am, Zoom (link is posted on CCLE)
Discussions: F 10:00 am - 11:50 am, Zoom (link is posted on CCLE)

Office hours (Sicheng Jia**):** Tue 8:45-9:45am, and Thu 12:00-1:00pm, Zoom (link is posted on CCLE)
Office hours (Xiaojian Ma**):** Tue 4:00 pm - 6:00 pm, Zoom (link is posted on CCLE)
Office hours (Prof. Omid Abari**):** Mon 12:00 pm - 1:00 pm, Zoom (link is posted on CCLE)

Textbook (Optional): M.D. Ercegovac, T. Lang and J. Moreno, Introduction to Digital Systems, John Wiley & Sons, New York, 1999. Available as reader at UCLA Bookstore and on the Web.

Course material: Lectures, assignments and solutions will be posted on CCLE or/and Gradescope.

Class Communication: Important class announcements will be done through online class forum on Piazza. If you have any questions regarding class materials, they also need to be asked on Piazza. Please make sure to sign up for CSM51A Piazza forum at http://piazza.com/ucla/winter2021/csM51A

Grading: 10 assignments, each is roughly 10% of your final grade. (No midterm, No Final Exam)

Assignments: Assignments are due on **Wednesdays 10 am PT**. Late work will not be accepted. In exceptional circumstances, arrangements must be made in advance of the due date for an extension. You must complete the assignments **entirely on your own**. You are NOT allowed to discuss your solutions with others or see another student's solutions. Gradescope is used to submit assignments.

Academic Honesty: I expect all students to follow the UCLA Student Conduct Code. This code prohibits cheating, fabrication, multiple submissions, and facilitating academic dishonesty. You can find further information about this code at the Student Guide to Academic Integrity. The Office of the Dean of Students offers a workshop on academic integrity if you wish to understand UCLA's policies on this issue more thoroughly.

Schedule:

Date	Topics	Assignment	Reading (optional)
Week 1			
Jan 4th	Introduction		Ch1
Jan 6th	Data Representation		Ch2
Jan 8th	Discussion	HW1 Posted	
Week 2			
Jan 11th	Boolean Algebra, Truth tables, etc		Ch2
Jan 13th	Sum of products and product of sums, etc	HW1 Due	Ch2
Jan 15th	Discussion	HW2 Posted	
Week 3			
Jan 18th	Martin Luther King, Jr. holiday		
Jan 20th	Sum of minterms and product of maxterms	HW2 Due	Ch2
Jan 22nd	Discussion	HW3 Posted	
Week 4			
Jan 25th	Gate implementation, transmission gates		Ch3
Jan 27th	Functional and Timing Analysis	HW3 Due	Ch4
Jan 29th	Discussion	HW4 Posted	
Week 5			
Feb 1st	minimal two-level networks, Karnaugh Maps		Ch5
Feb 3rd	NAND and NOR networks	HW4 Due	Ch5
Feb 5th	Discussion	HW5 Posted	
Week 6			
Feb 8th	Finite state machines		Ch7
Feb 10th	Reduction of the state set.	HW5 Due	Ch7
Feb 12th	Discussion	HW6 Posted	
Week 7			
Feb 15th	Presidents' Day holiday		
Feb 17th	SR Latch, D Latch, D Flip-Flop	HW6 Due	Ch8
Feb 19th	Discussion	HW7 Posted	
Week 8			
Feb 22nd	Analysis and design of canonical networks.		Ch8
Feb 24th	Design of sequential networks with flip-flops	HW7 Due	Ch8
Feb 26th	Discussion	HW8 Posted	
Week 9			
Mar 1st	Decoders and Encoders		Ch9
Mar 3rd	Multiplexers and Demultiplexers	HW8 Due	Ch9
Mar 5th	Discussion	HW9 Posted	
Week 10			
March 8th	Full adder and half adder		Ch10
March 10th	Shift registers, and counters	HW9 Due	Ch11
March 12th	Discussion	HW10 Posted	
Week Final			
March 17th		HW10 Due	