

# CS M51A, Winter 2021, Assignment 8

(Total Mark: 120 points, 12% )

Due: Wed Mar 3rd, 10:00 AM Pacific Time

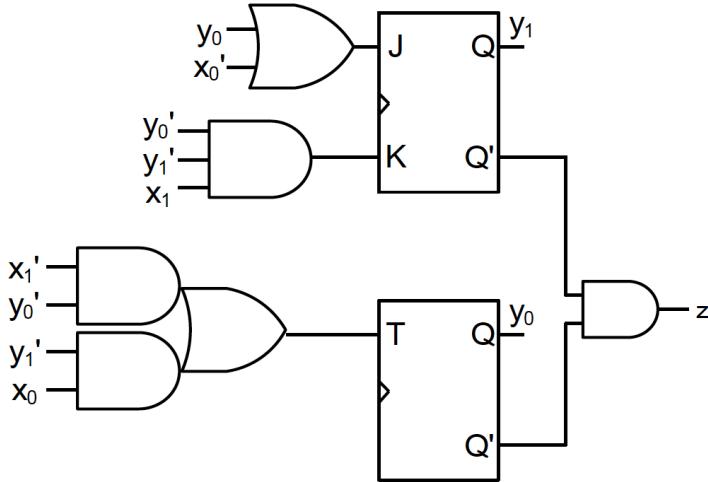
Student Name:

Student ID:

**Note:** You must complete the assignments entirely on your own,  
without discussing with others.

1. We would like to analyze the following sequential network. It has two input bits  $x_1$  and  $x_0$ , with a single output bit  $z$ . Note, both Flip-flops connect to the same CLK, not shown in the figure for simplicity.

$$\begin{aligned} J &= x_0' + y_0 \\ K &= x_1 y_0' y_1' \\ Q(t+1) &= J Q' + K' Q \\ T &= x_1' y_0' + x_0 y_1' \\ Q(t+1) &= T' Q + T Q' \end{aligned}$$



- (6 Points) Write expressions for  $z$ ,  $y_1(t+1)$  and  $y_0(t+1)$  in terms of inputs ( $x_1$  and  $x_0$ ) and present states ( $y_1$  and  $y_0$ ).

$$z = y_1' y_0'$$

$$y_1(t+1) = (x_0' + y_0)y_1' + (x_1 y_0' y_1')' y_0 = x_0' y_1' + y_1' y_0 + x_1 y_1'$$

$$y_0(t+1) = (x_1' y_0' + x_0 y_1')' y_0 + (x_1' y_0' + x_0 y_1') y_0' = x_1' y_0' + x_0 y_1' y_0'$$

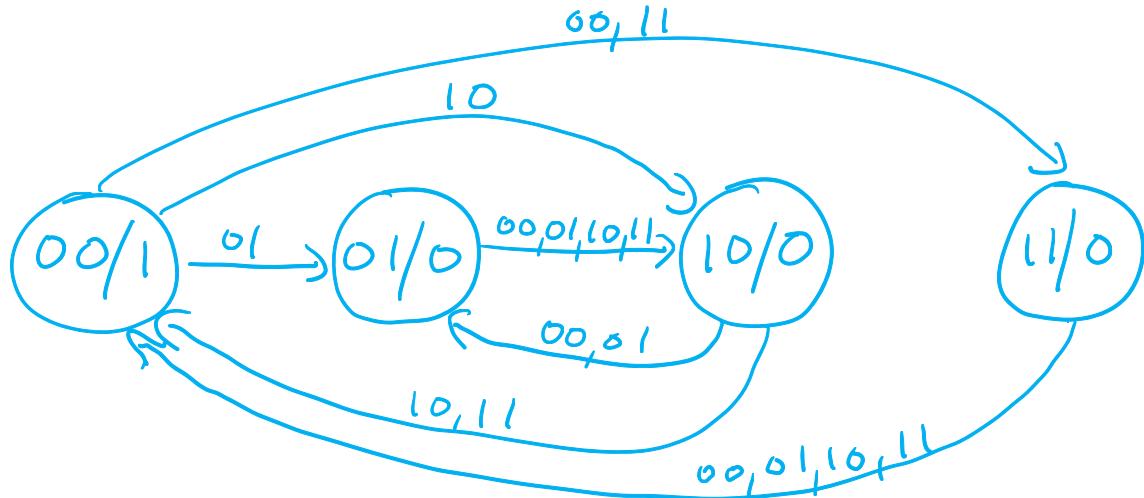
(b) (8 Points) Using the expressions, fill in the table below.

$PS$	Input $x_1(t)x_0(t)$				Output
$y_1(t)y_0(t)$	00	01	10	11	$z$
00	11	01	10	11	1
01	10	10	10	10	0
10	01	01	00	00	0
11	00	00	00	00	0
	$y_1(t+1)y_0(t+1)$				
	NS				

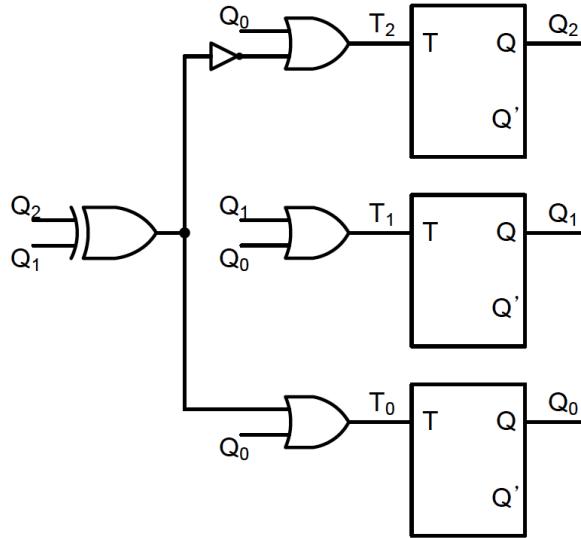
(c) (4 Points) Is this a Moore or Mealy machine?

Moore

(d) (8 Points) Draw the state diagram for this system



2. We would like to analyze the sequential system shown below. It is a autonomous counter which outputs a fixed string of numbers. The system does not have any input and the output changes at every clock cycle.



a) (6 Points) Write the expressions for  $T_2$ ,  $T_1$ , and  $T_0$ .

$$T_2 = Q_0 + (Q_2 \oplus Q_1)' = Q_0 + Q_2'Q_1' + Q_2Q_1$$

$$T_1 = Q_1 + Q_0$$

$$T_0 = Q_0 + Q_2 \oplus Q_1 = Q_0 + Q_2'Q_1 + Q_2Q_1'$$

b) (10 points) Show the state transition table for the system, indicating the next states for each present state.

$$Q_2(t+1) = T_2(t) \oplus Q_2(t) \quad Q_1(t+1) = T_1(t) \oplus Q_1(t)$$

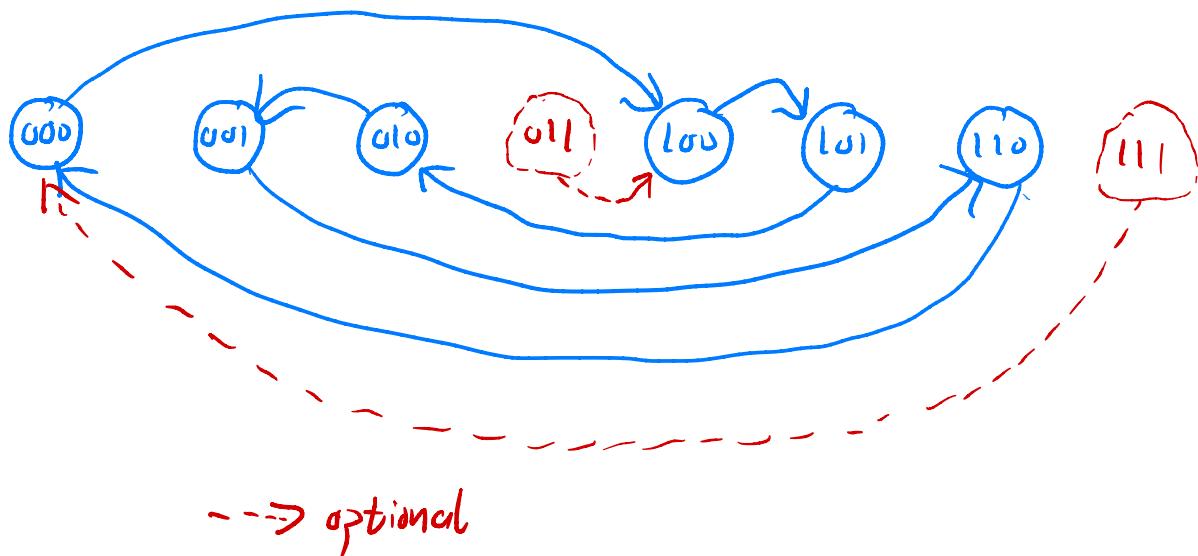
$$Q_0(t+1) = T_0(t) \oplus Q_0(t)$$

PS	NS
<u><math>Q_2Q_1Q_0(t)</math></u>	<u><math>Q_2Q_1Q_0(t+1)</math></u>
000	100
001	110
010	001
011	— or 100

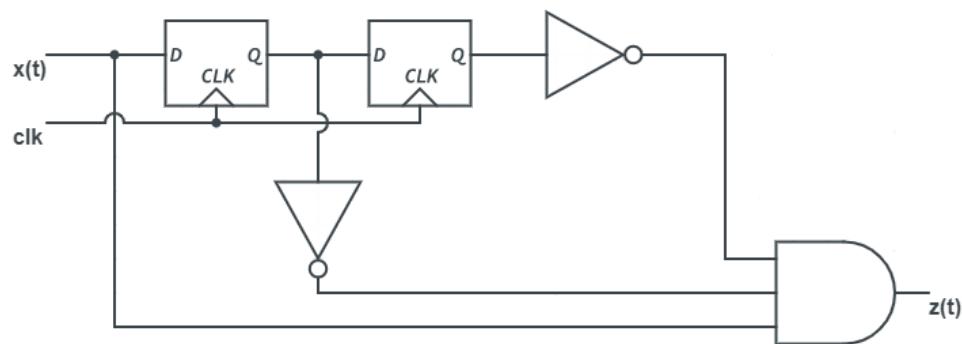
(cont'd)

PS	NS
<u><math>Q_2Q_1Q_0(t)</math></u>	<u><math>Q_2Q_1Q_0(t+1)</math></u>
100	101
101	010
110	000
111	— or 000

c) (4 points) Draw the state transition diagram of the system.



3. The following sequential system implements a pattern detector.

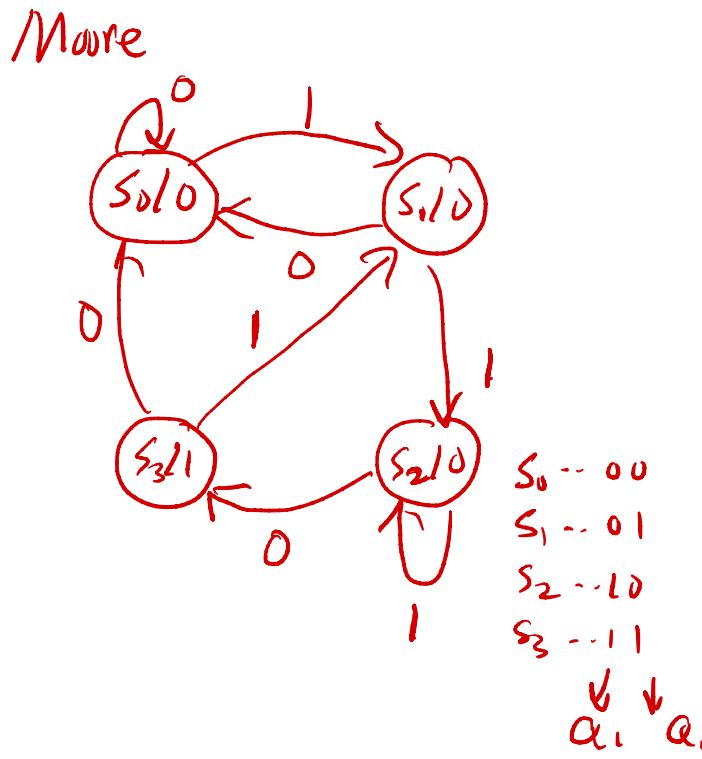
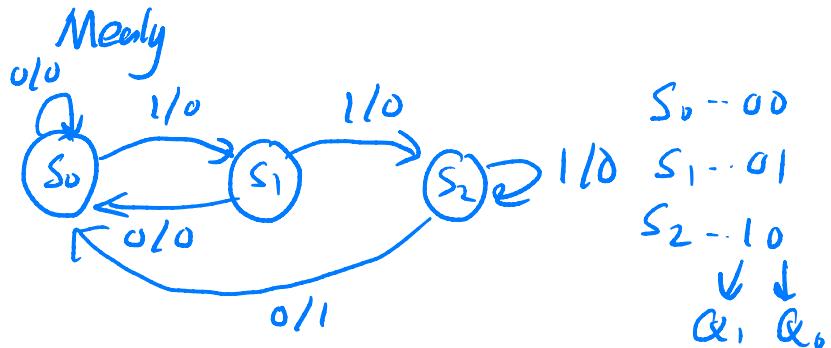


(4 Points) What pattern does this system detect?

001

4. Using D flip-flops, design a sequential system with one binary input  $x(t)$  and one binary output  $z(t)$ . The output is 1 whenever pattern 110 are observed; otherwise the output is 0.

a) (4 Points) Draw the state diagram for this system



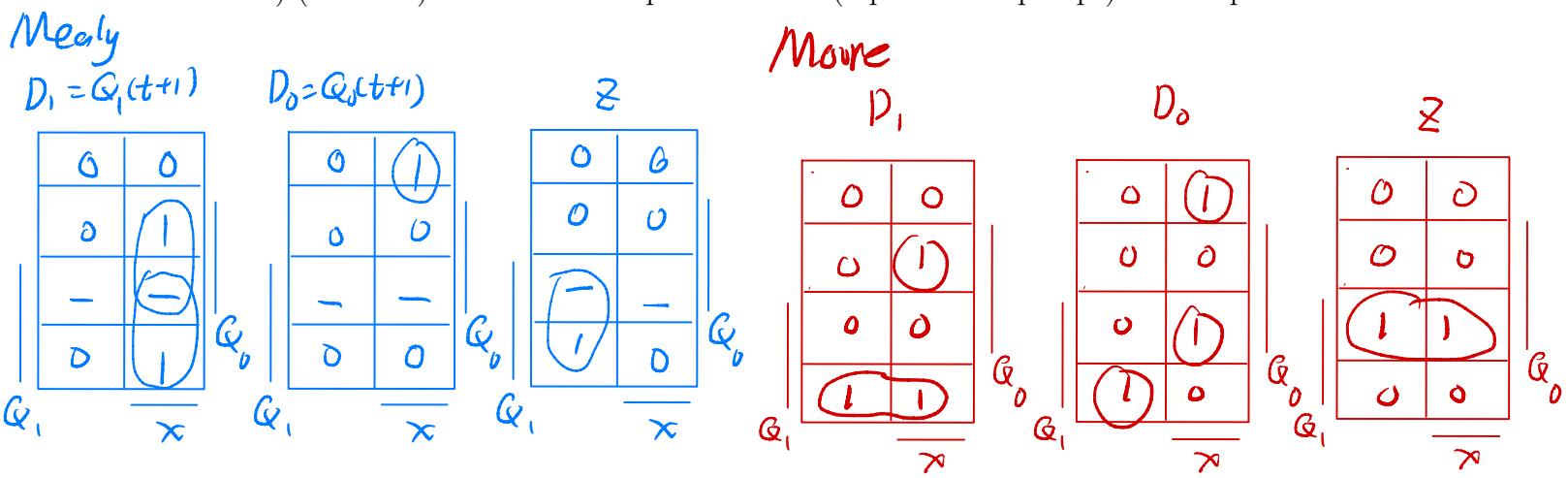
*Mealy*

		$x(t)$	
PS		$x=0$	$x=1$
$Q, Q_o$			
00		00, 0	01, 0
01		00, 0	10, 0
10		00, 1	10, 0
11		—	—
		$NS/z(t)$	

*Moore*

PS		$x(t)$		$z(t)$
		$x=0$	$x=1$	
$Q, Q_o$				
00		00	01	0
01		00	10	0
10		11	10	0
11		00	01	1
		$NS$		

c) (6 Points) Draw the K-maps for each D (input of D flip-flops) and output z



d) (6 Points) Write switching expressions for each D (input of D flip-flops) and output z

*Mealy*

$$D_1 = xQ_1 + xQ_0$$

$$D_0 = xQ_1'Q_0'$$

$$Z = x'Q_1'$$

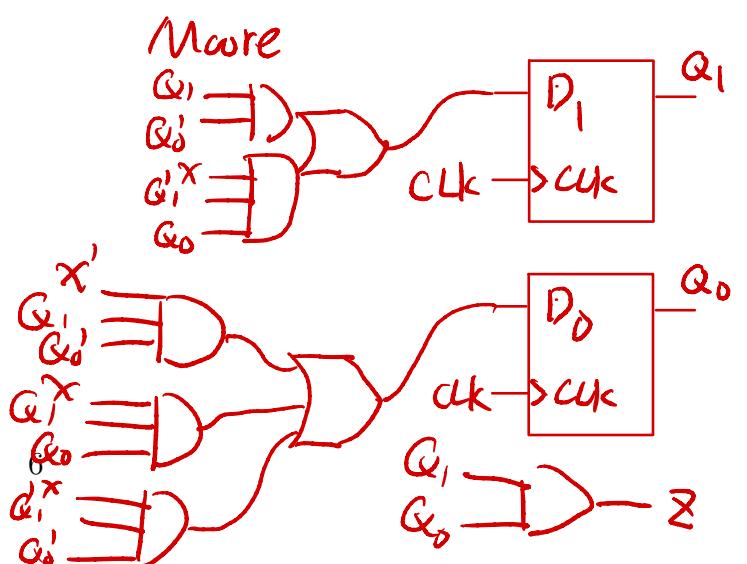
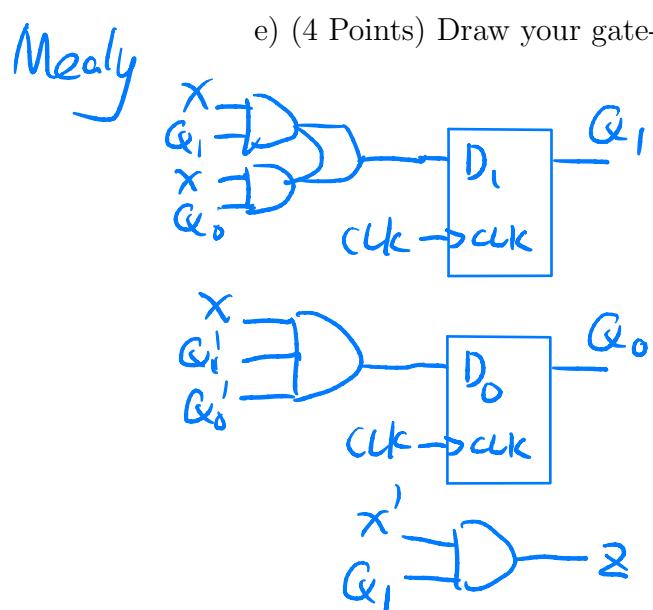
*Moore*

$$D_1 = Q_1Q_0' + xQ_1'Q_0$$

$$D_0 = x'Q_1Q_0' + xQ_1Q_0 + xQ_1'Q_0'$$

$$Z = Q_1Q_0$$

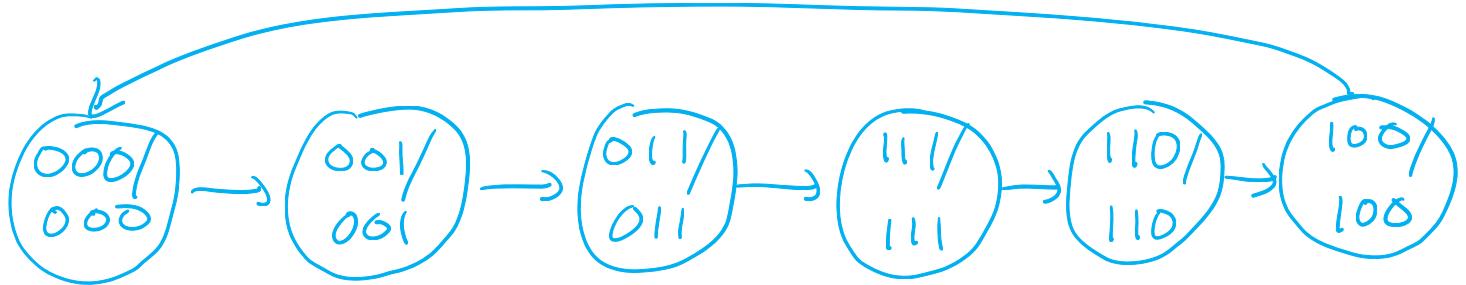
e) (4 Points) Draw your gate-level design (using gates and D flip-flops)



5. Using T flip flops, we want to design a cyclic counter which has an output sequence of period 6 as shown:  $000 \rightarrow 001 \rightarrow 011 \rightarrow 111 \rightarrow 110 \rightarrow 100 \rightarrow 000 \rightarrow 001 \rightarrow \dots$

The counter does not have an input signal, but moves to the appropriate next state at every clock. Code the states so that the output at each state will be the same as the state assignment, in other words,  $z(t) = s(t)$  ( $z(t)$ ,  $s(t)$  are output and state assignment at time  $t$  respectively). Assume that the counter will always start at 000 and will never enter an unused state.

- a) (4 Points) Draw the state diagram for this system



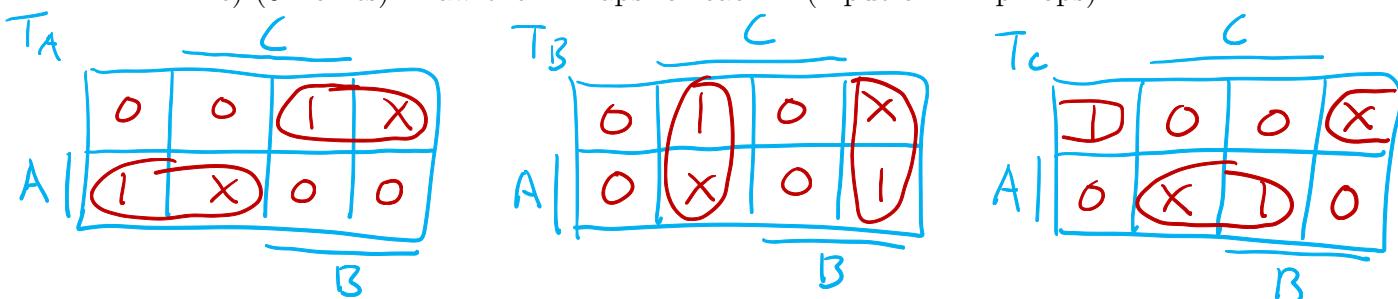
- b) (6 Points) Show the state transition table

PS	NS	Output	TA	TB	TC
000	001	000	0	0	1
001	011	001	0	1	0
011	111	011	1	0	0
111	110	111	0	0	1
110	100	110	0	1	0
100	000	100	1	0	0

PS	TA	TB	TC
000	0	0	1
001	0	1	0
010	x	x	x
011	1	0	0
100	1	0	0
101	x	x	x
110	0	1	0
111	0	0	1

ABC

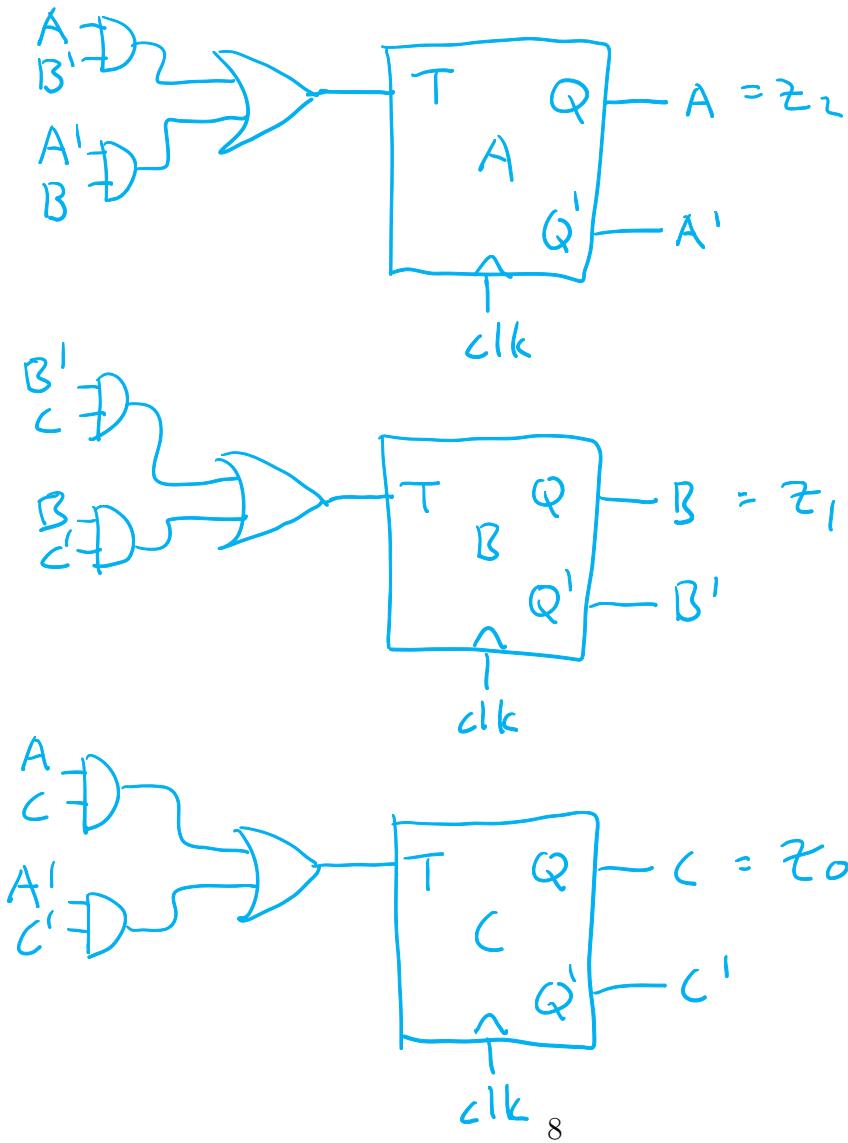
- c) (6 Points) Draw the K-maps for each T (input of T flip-flops)



d) (6 Points) Write switching expressions for each T (input of T flip-flops)

$$T_A = AB' + A'B \quad T_B = B'C + BC' \quad T_C = AC + A'C'$$

e) (6 Points) Draw your gate level design (using gates and T flip-flops)



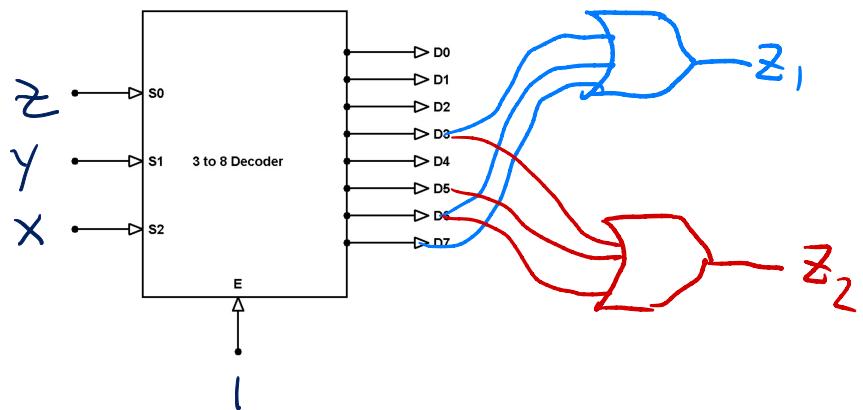
6. (6 Points) Using the following decoder, AND and OR Gates, implement the following function. Please show which decoder's input must be connected to x, y and z.

$$z_1 = xyz + xyz' + x'y'z$$

$$z_2 = xy'z + xyz' + x'y'z'$$

$$z_1 = xyz + xyz' + x'y'z$$

$$\begin{array}{ccc} 111 & 110 & 011 \\ \downarrow & \downarrow & \downarrow \\ 7 & 6 & 3 \end{array}$$



$$z_2 = xy'z + xyz' + x'y'z'$$

$$\begin{array}{ccc} 101 & 110 & 011 \\ \downarrow & \downarrow & \downarrow \\ 5 & 6 & 3 \end{array}$$

7. (10 Points) Design a 4-to-16 decoder using only 3-to-8 decoders and NOT gates. Draw your design below. For decoder, please use the same symbol as question 6.

