

CS M51A

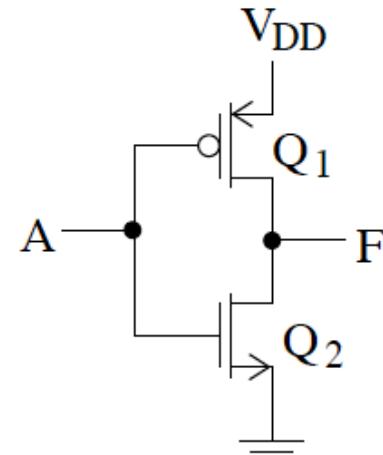
Logic Design of Digital Systems

Winter 2021

Some slides borrowed and modified from:

M.D. Ercegovac, T. Lang and J. Moreno, Introduction to Digital Systems.

D. Patterson and J. Hennessy, Computer Organization and Design

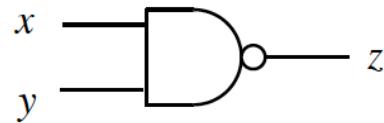


A	Q_1	Q_2	F
0	Low	High	1 (V_H)
1	High	Low	0 (V_L)

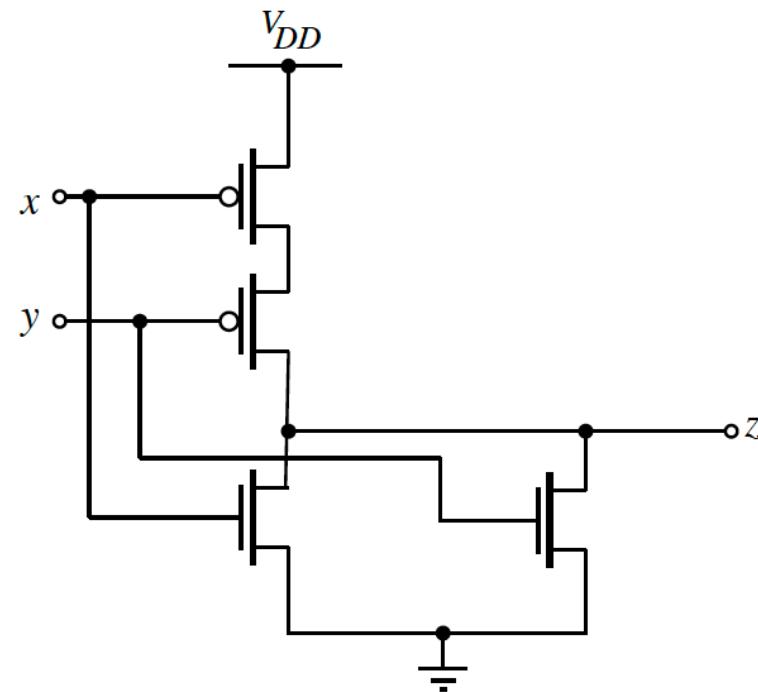
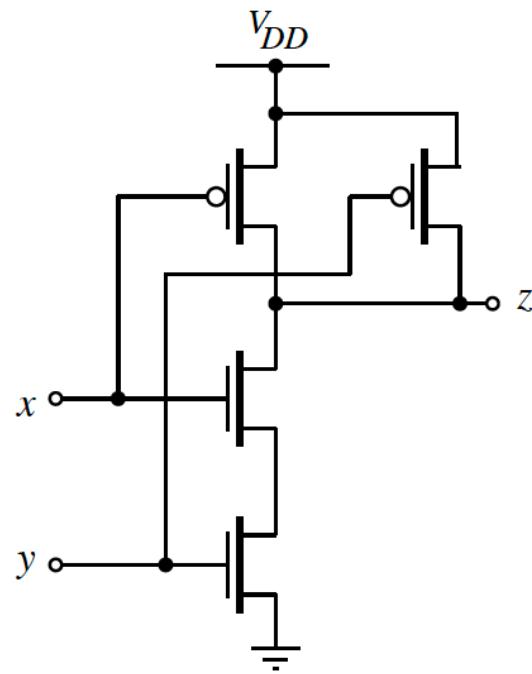
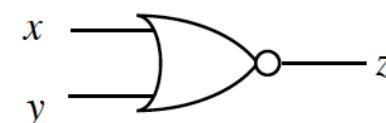
- To analyze CMOS circuit:
 - Make table with inputs, transistors, and output(s)
 - For each row of table (setting of inputs), check whether transistor resistance is High,Low
 - For each row of table, check if output has clean path to power (1)
ground (0)

NAND and NOR GATES

Circuit 1: NAND

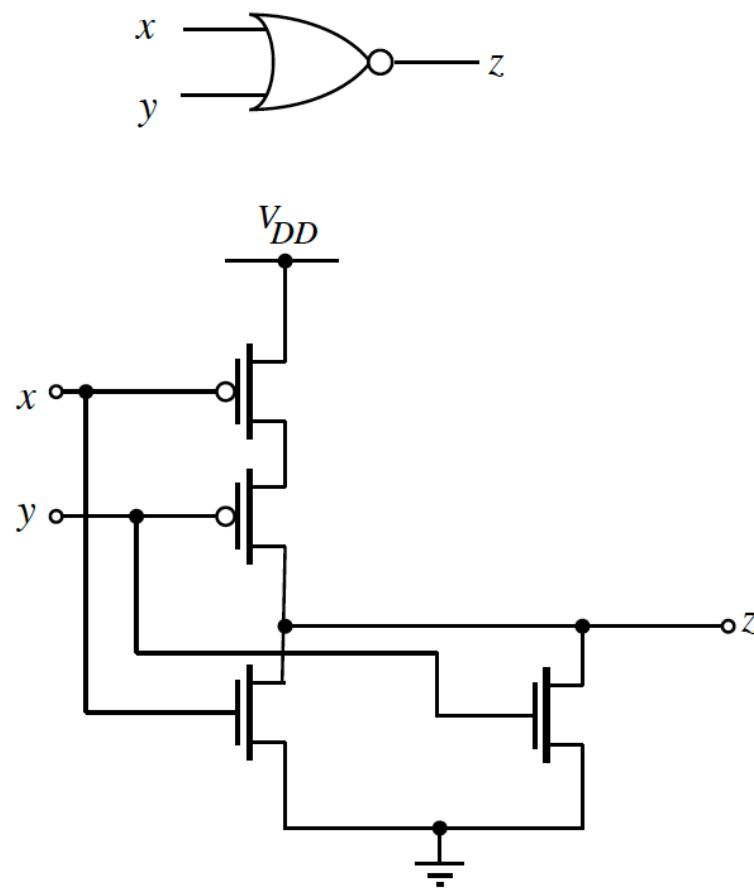


Circuit 2: NOR



NAND and NOR GATES

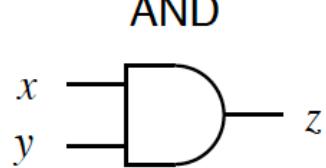
Circuit 2: NOR



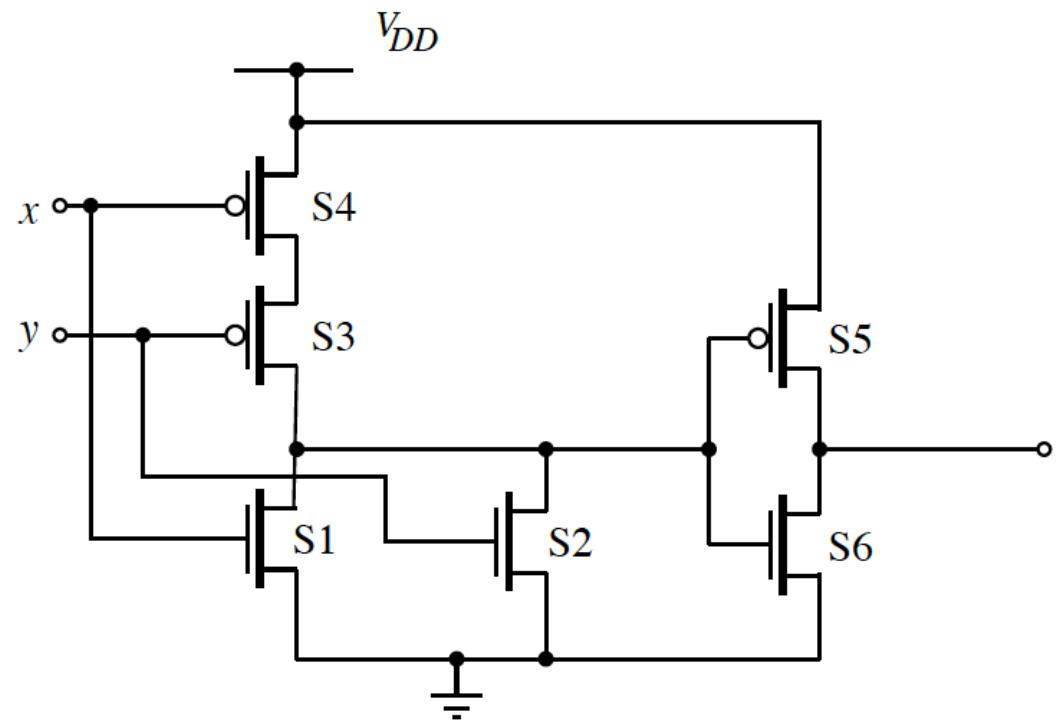
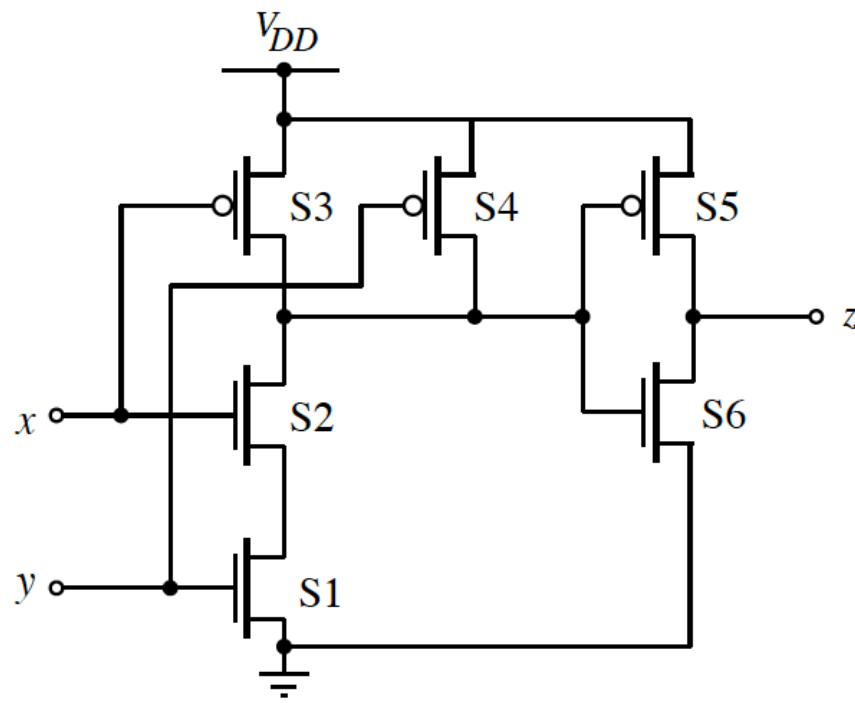
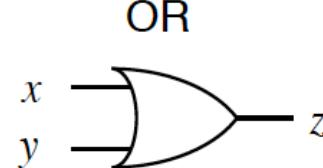
x	y	Q1	Q2	Q3	Q4	z
0	0	1	1	1	1	1

AND and OR GATES

AND

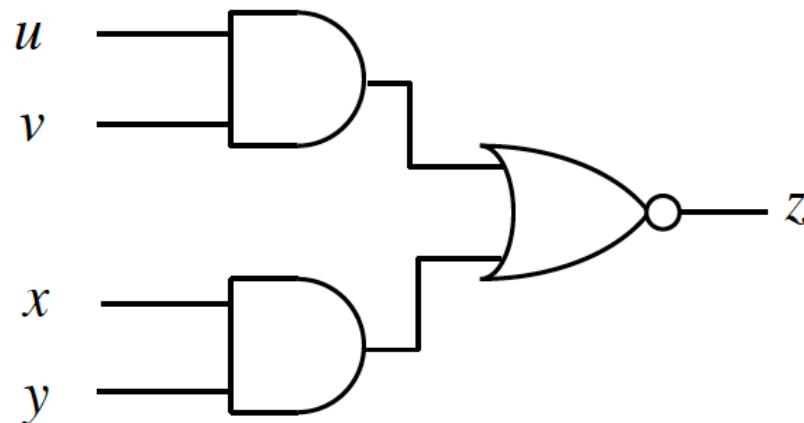


OR



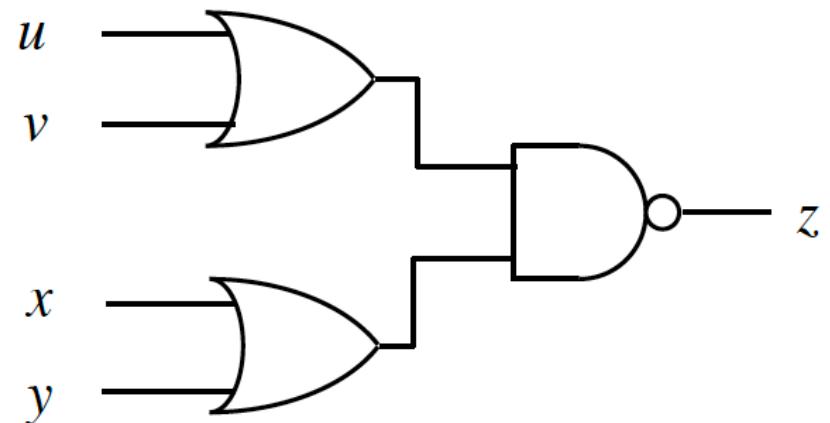
COMPLEX GATES

AND-OR-INVERT (AOI)

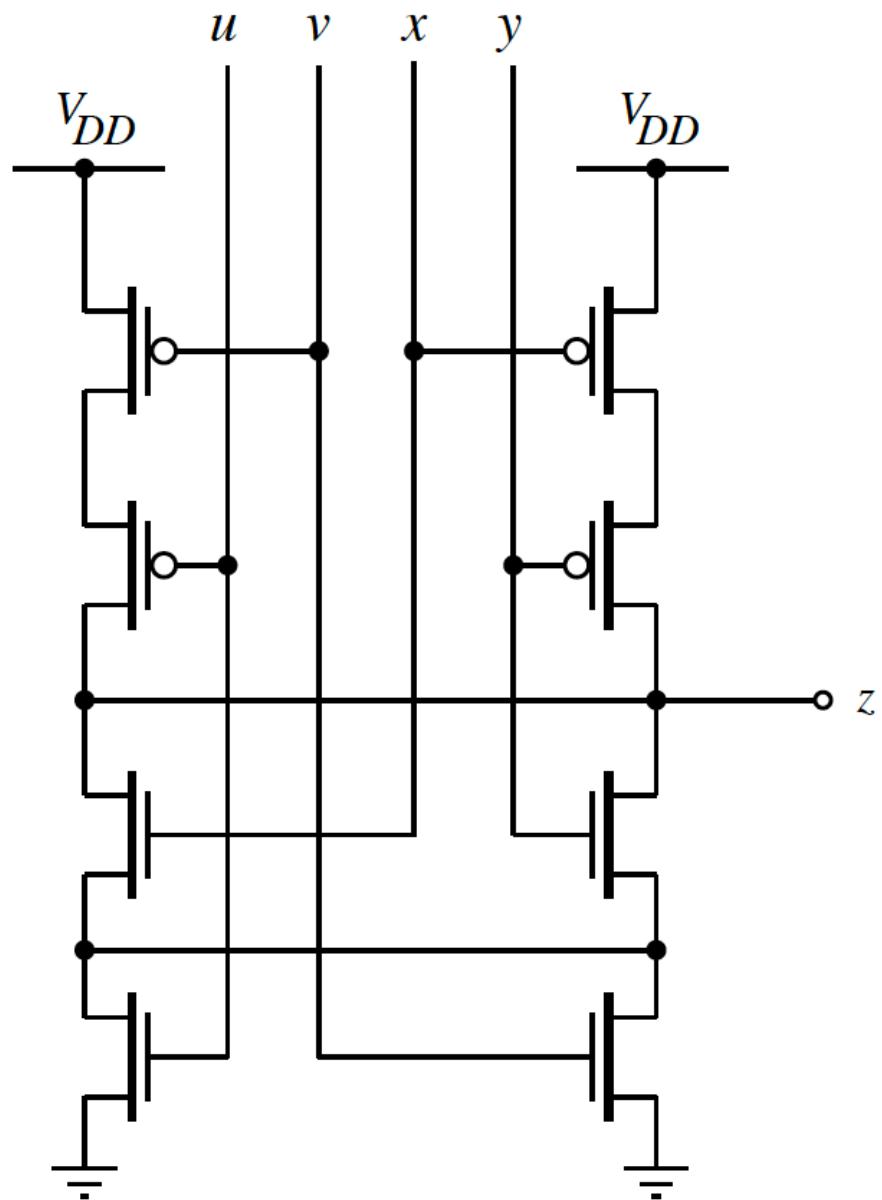
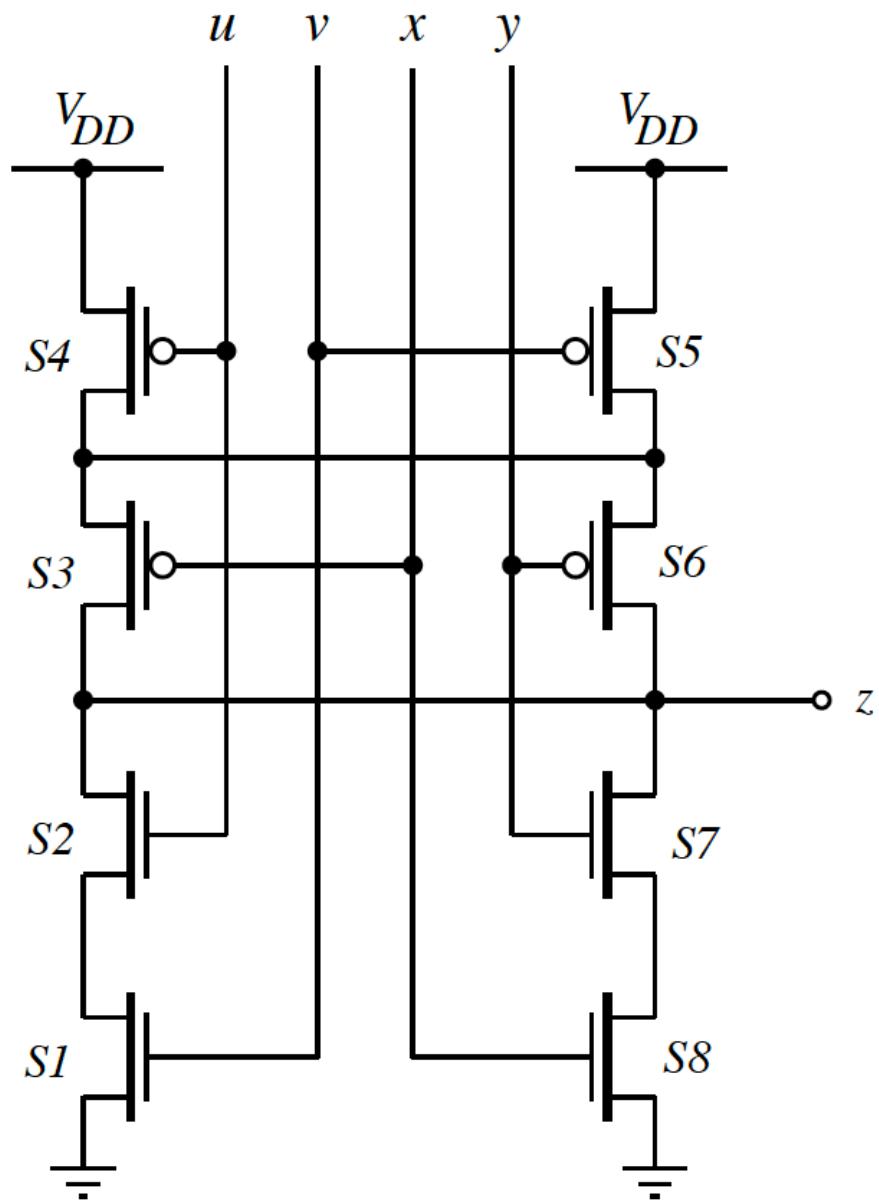


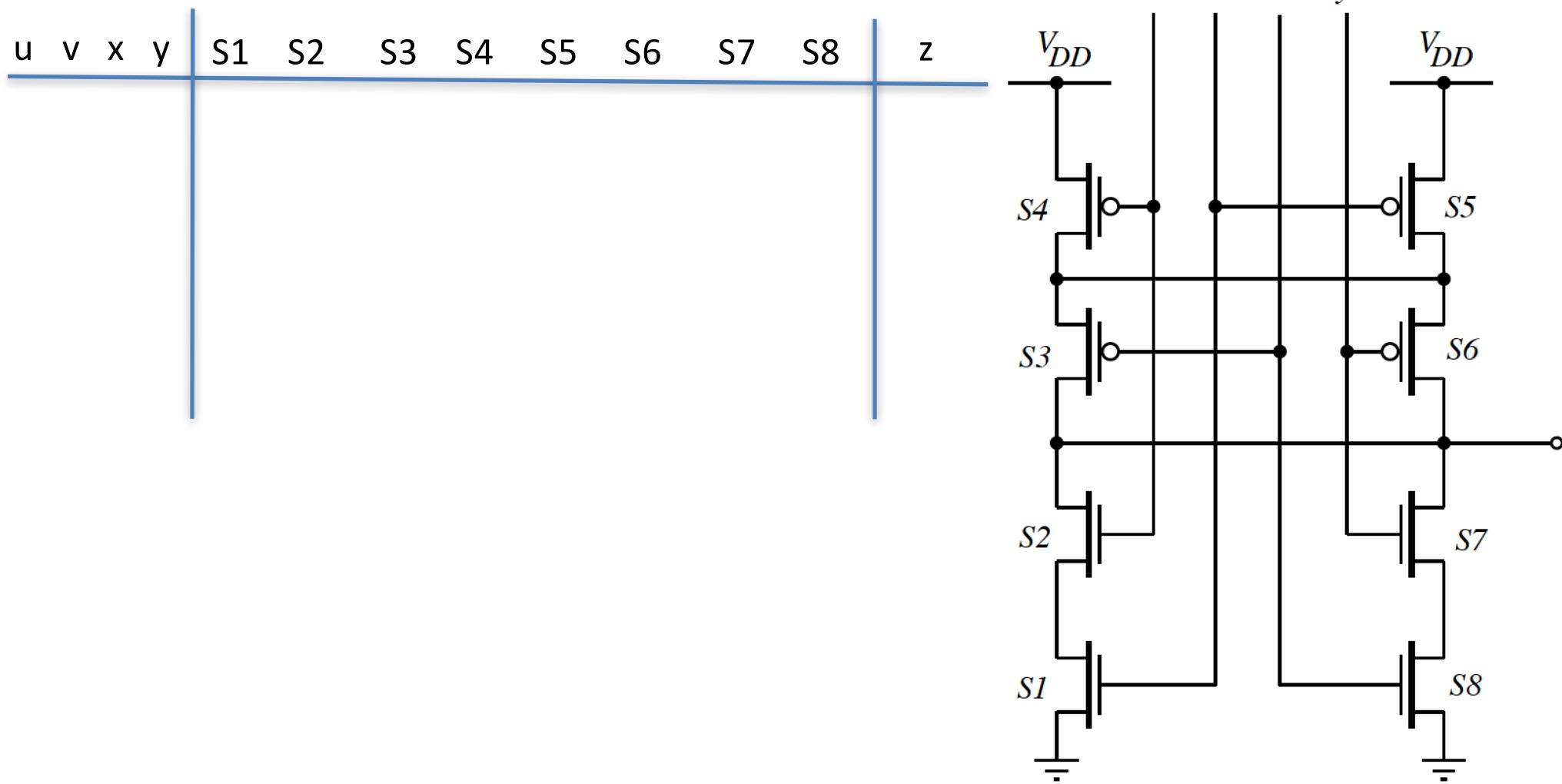
$$z = (uv + xy)'$$

OR-AND-INVERT (OAI)



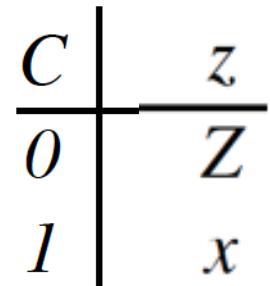
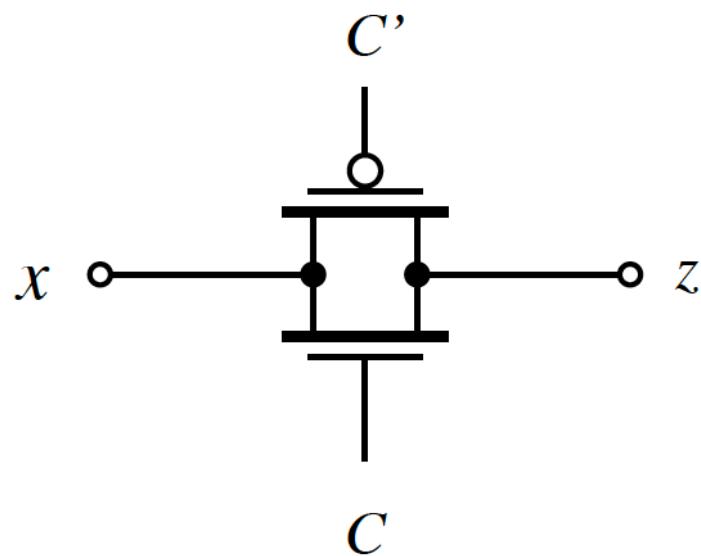
$$z = [(u+v)(x+y)]'$$





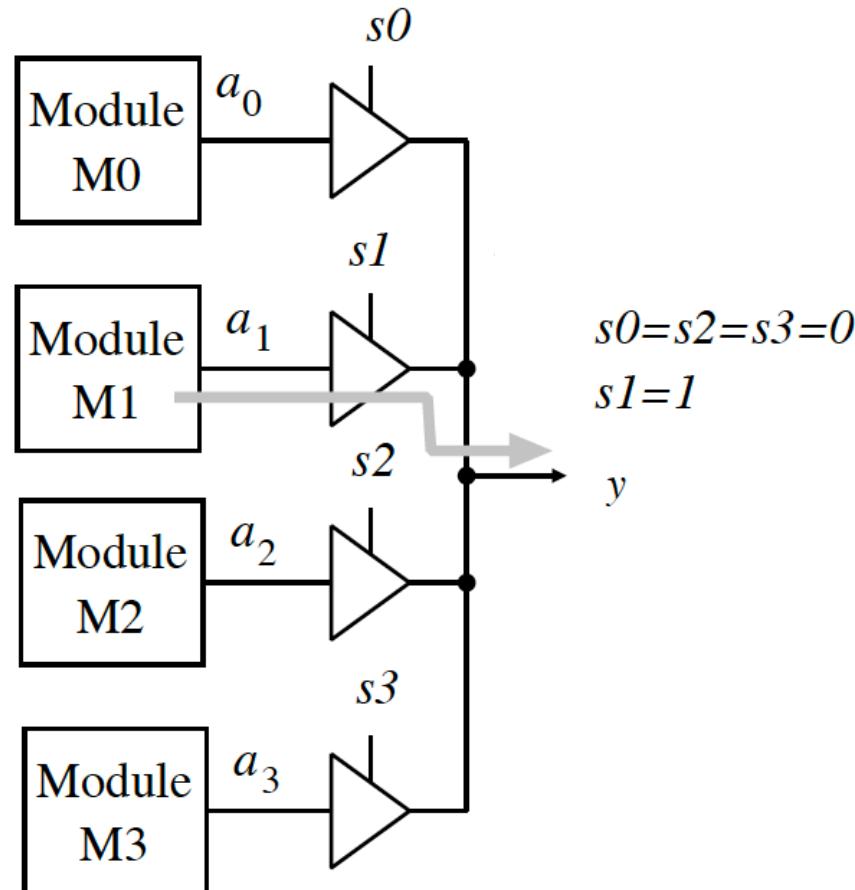
TRANSMISSION GATE

Also known as Three-state Buffer

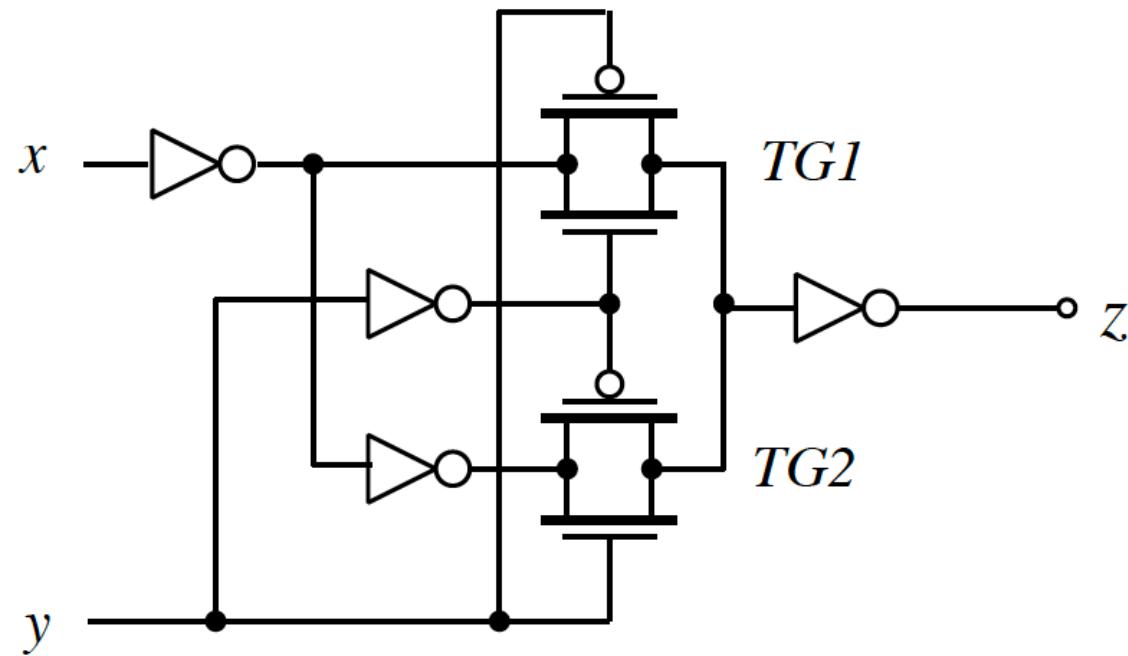


Z - *high impedance state*

THREE-STATE DRIVER (BUFFER)

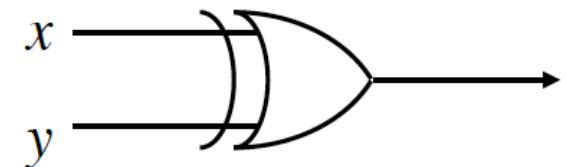
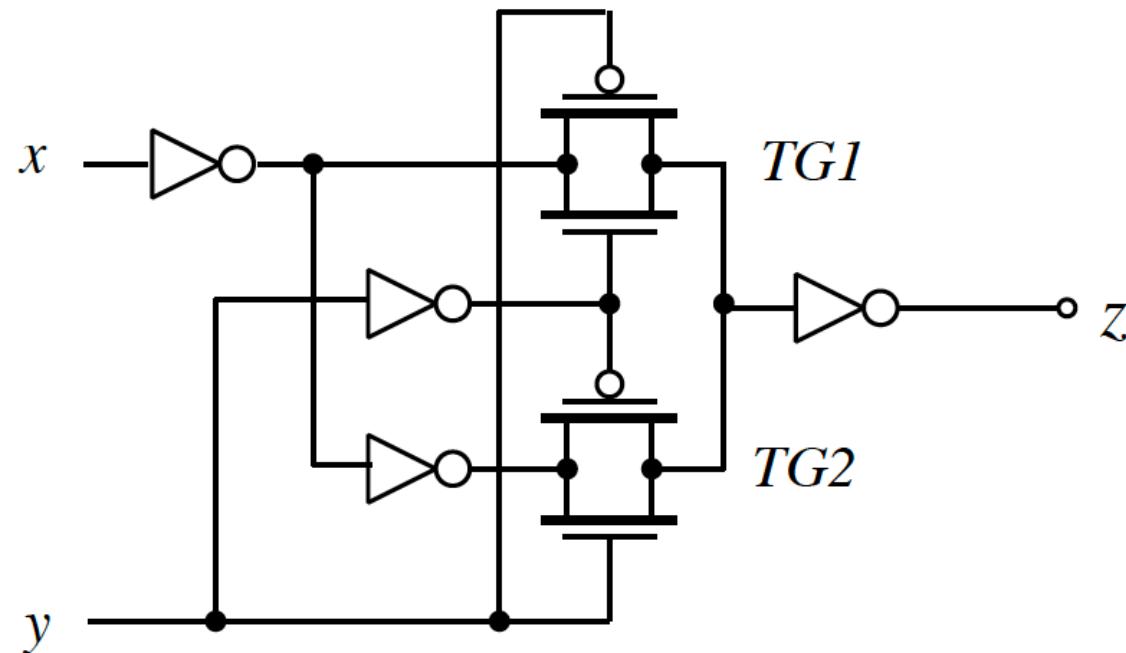


XOR WITH TRANSMISSION GATES



y	$TG1$	$TG2$	z
0			
1			

XOR WITH TRANSMISSION GATES



y	$TG1$	$TG2$	z
0			
1			

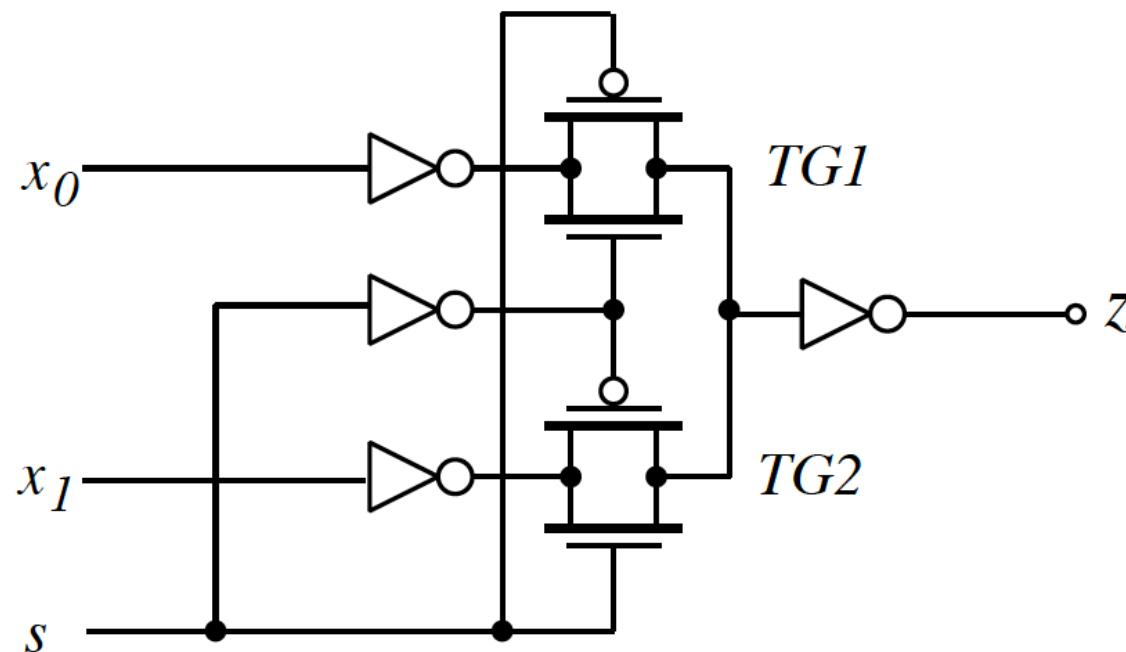
Clicker Question

What is the state of TG1, TG2, and Z for:

S=1

X0=1

X1=0



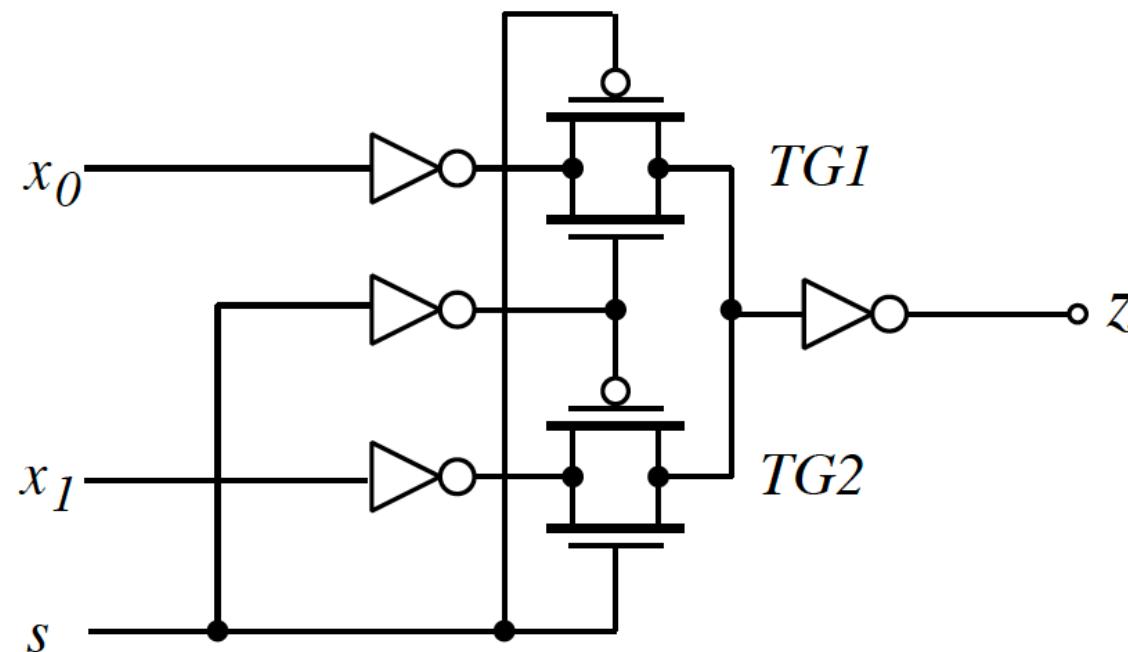
- a) TG1= on TG2=on Z=0
- b) TG1= on TG2=off Z=1
- c) TG1= off TG2=on Z=0
- d) TG1= off TG2=on Z=0
- e) none

What is the state of TG1, TG2, and Z for:

S=0

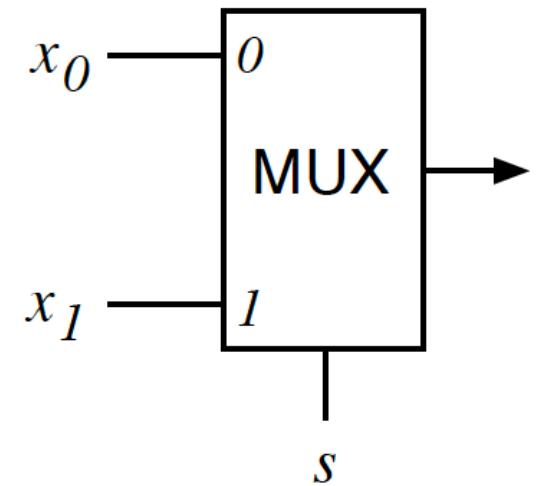
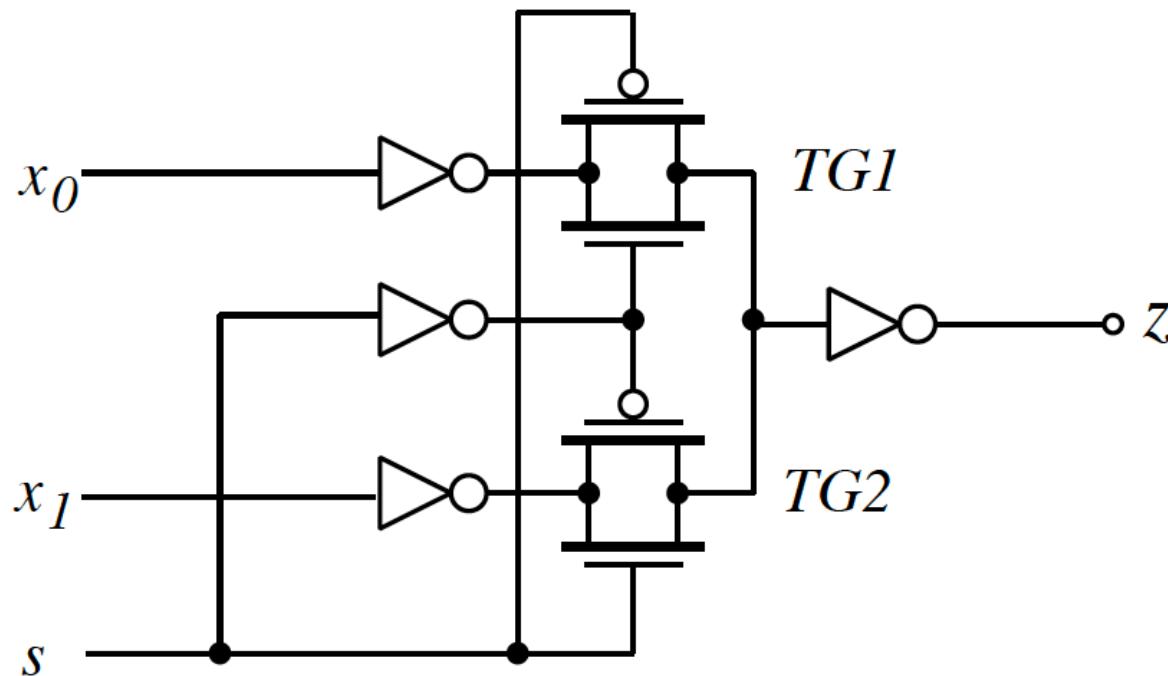
X0=1

X1=0



- a) TG1= on TG2=on Z=0
- b) TG1= on TG2=off Z=1
- c) TG1= off TG2=on Z=0
- d) TG1= off TG2=on Z=0
- e) none

MUX WITH TRANSMISSION GATES



s	$TG1$	$TG2$	z
0	1	0	0
1	0	1	1

Process of Designing a Hardware

Design Implementation

VHDL

```
library IEEE;
use IEEE.STD_Logic_1164.all;

entity LATCH_IF_ELSIF is
    port (En1, En2, En3, A1, A2, A3: in std_logic;
          Y: out std_logic);
end entity LATCH_IF_ELSIF;

architecture RTL of LATCH_IF_ELSIF is
begin
    process(En1, En2, En3, A1, A2, A3)
    begin
        if(En1 = '1') then
            Y <= A1;
        elsif(En2 = '1') then
            Y <= A2;
        elsif(En3 = '1') then
            Y <= A3;
        end if;
    end process;

end architecture RTL;
```

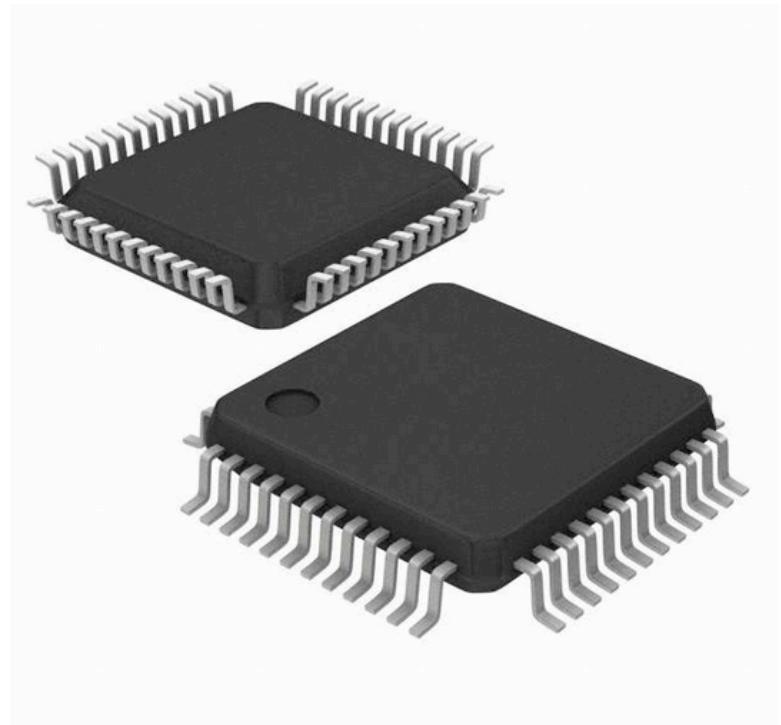
Verilog

```
module LATCH_IF_ELSIF (En1, En2, En3, A1, A2, A3,Y);
    input En1, En2, En3, A1, A2, A3;
    output Y;
    reg Y;

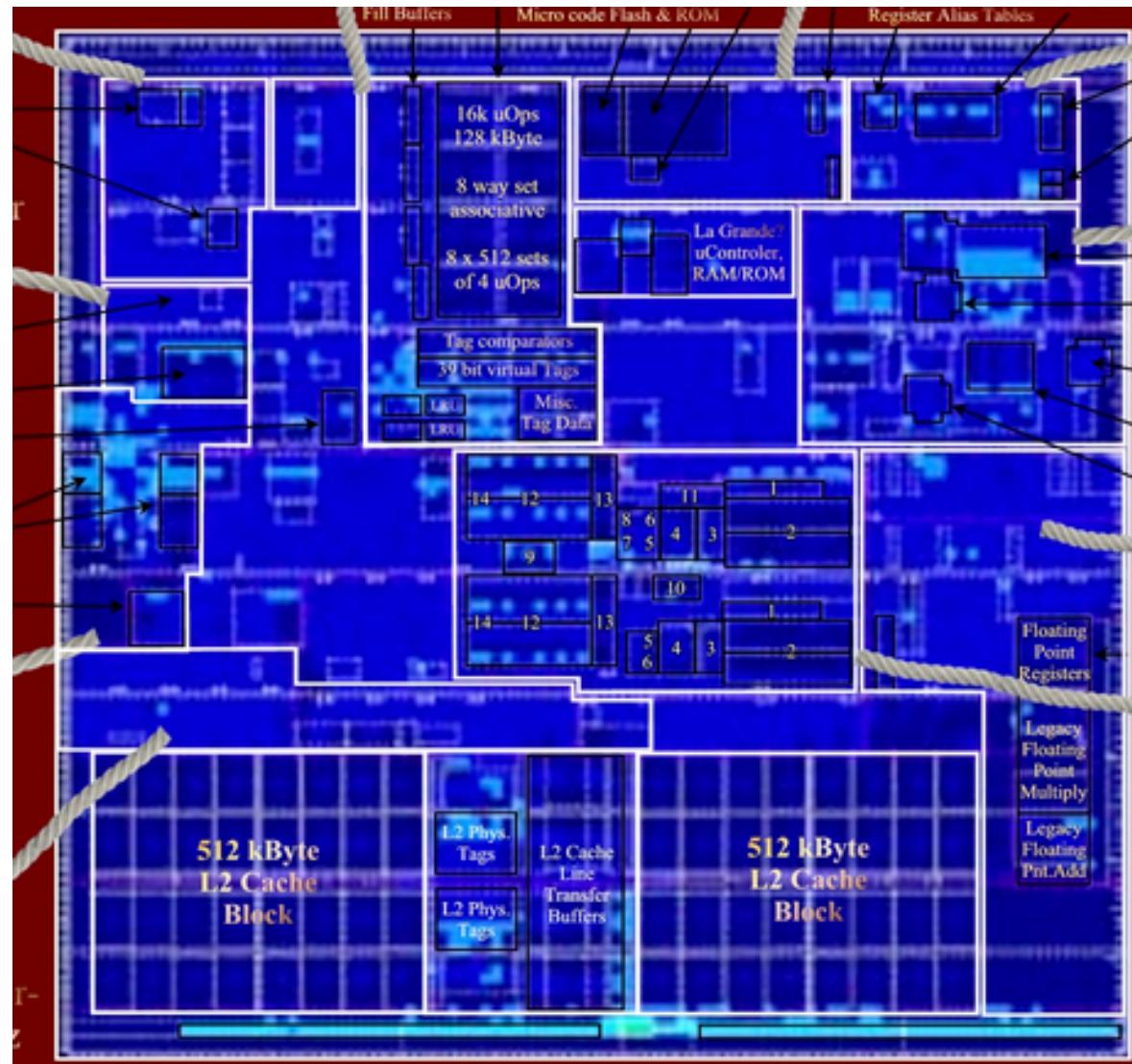
    always @(En1 or En2 or En3 or A1 or A2 or A3)
        if(En1 == 1)
            Y =A1;
        else if (En2 == 1)
            Y = A2;
        else if (En3 == 1)
            Y = A3;

end module
```

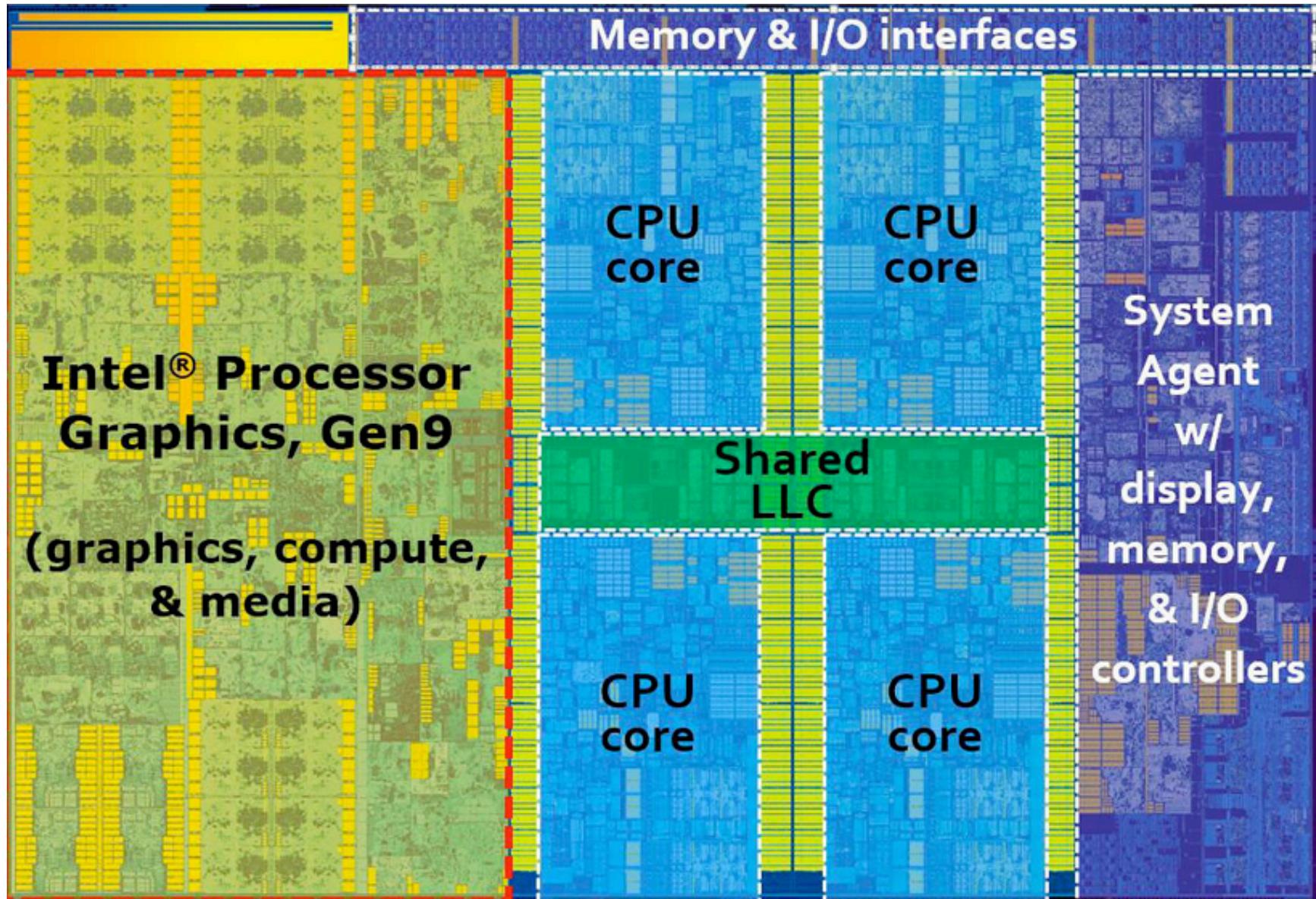
FPGA versus ASIC



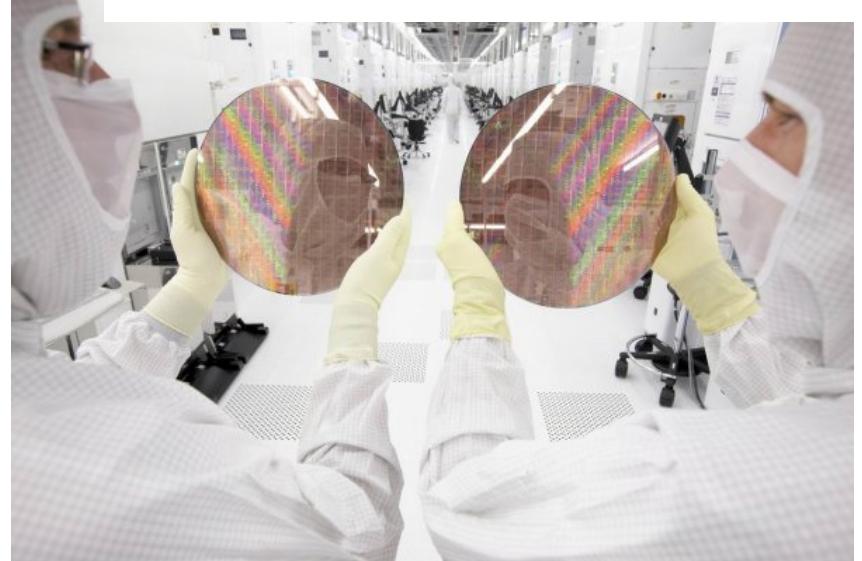
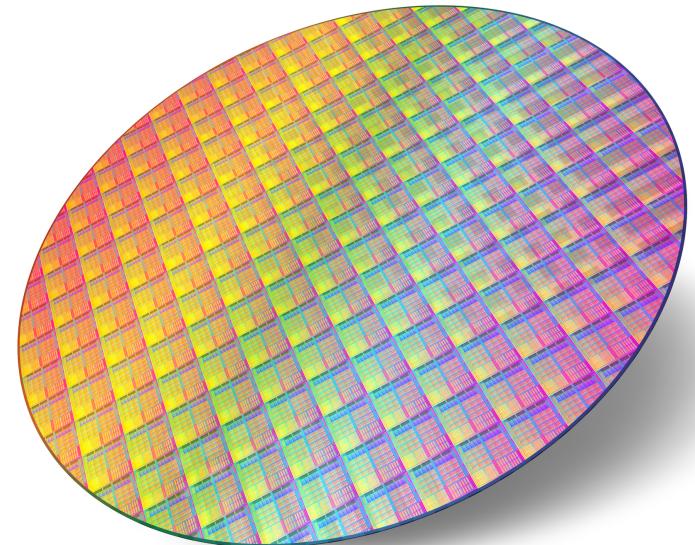
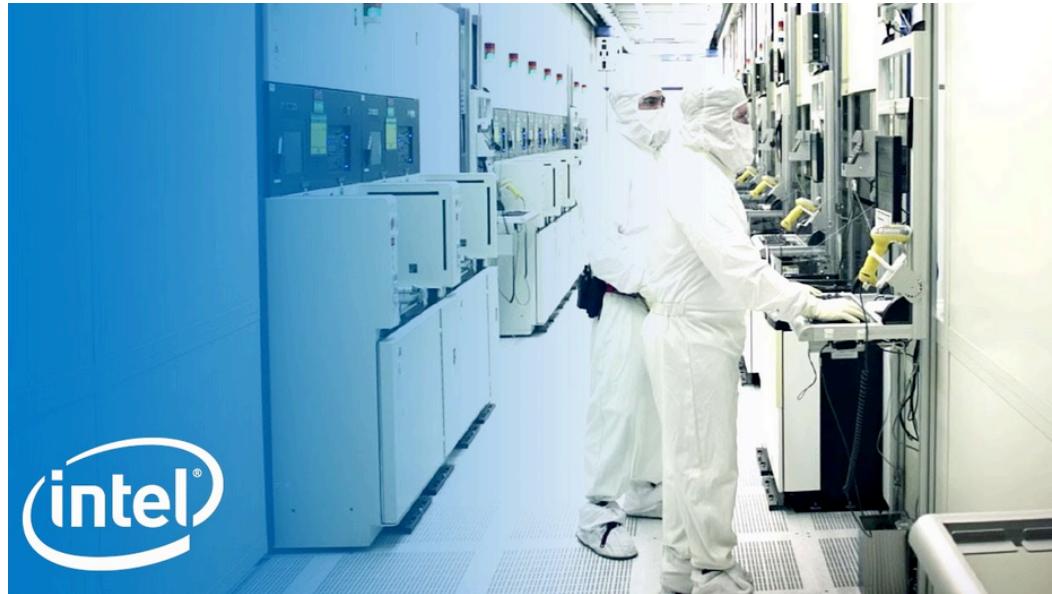
Intel Pentium Chip



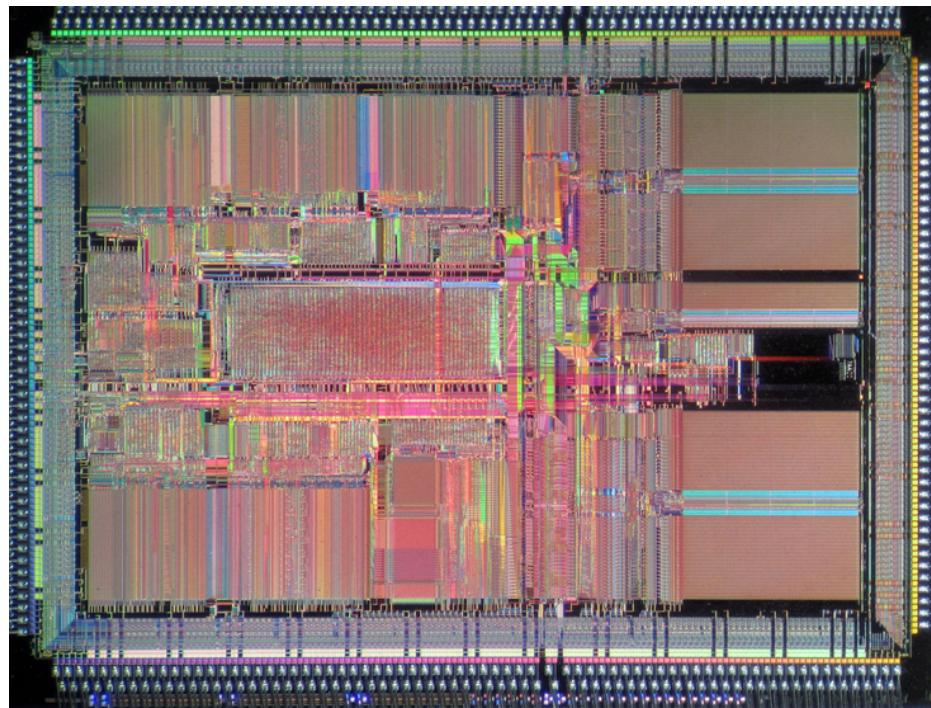
Another CPU



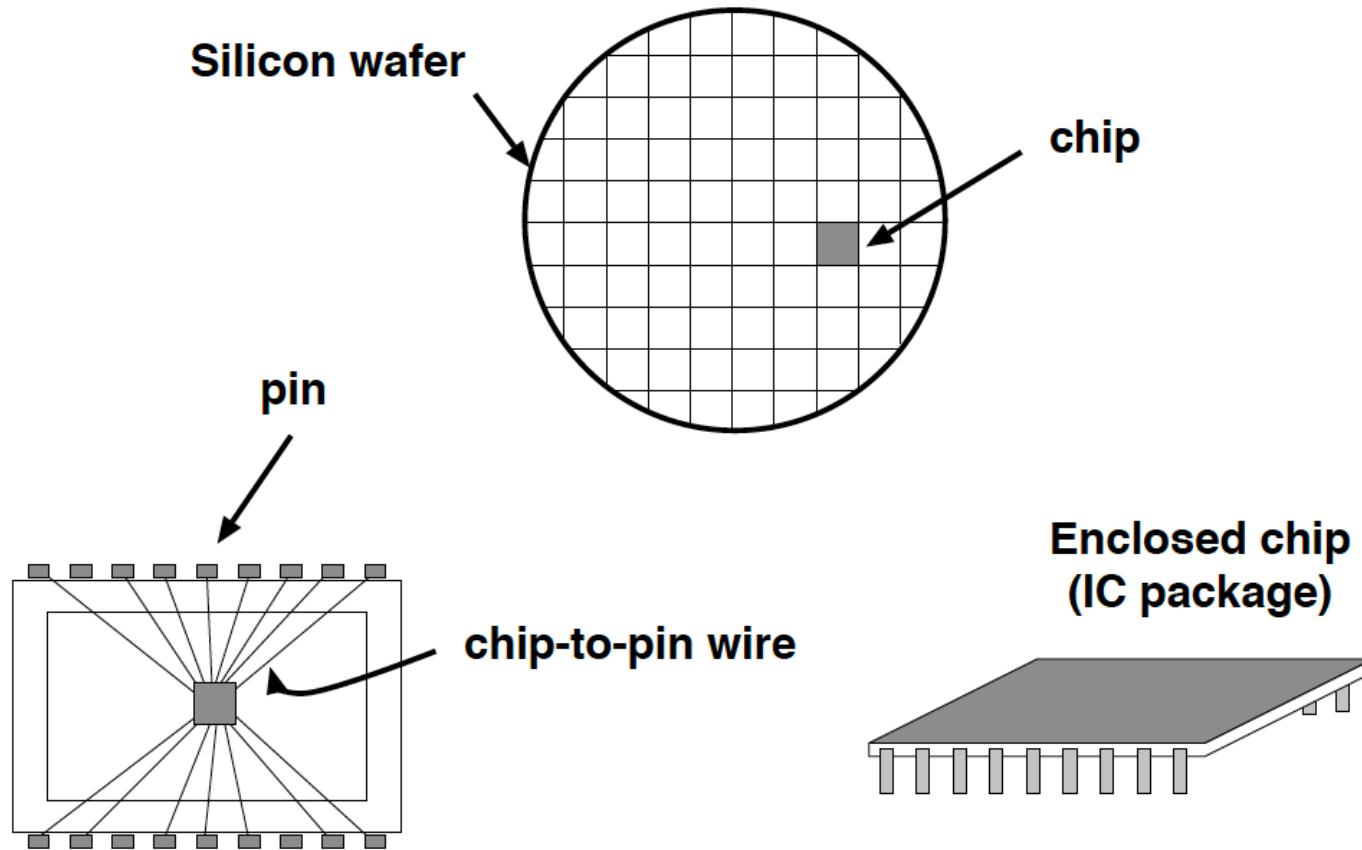
Fabrication



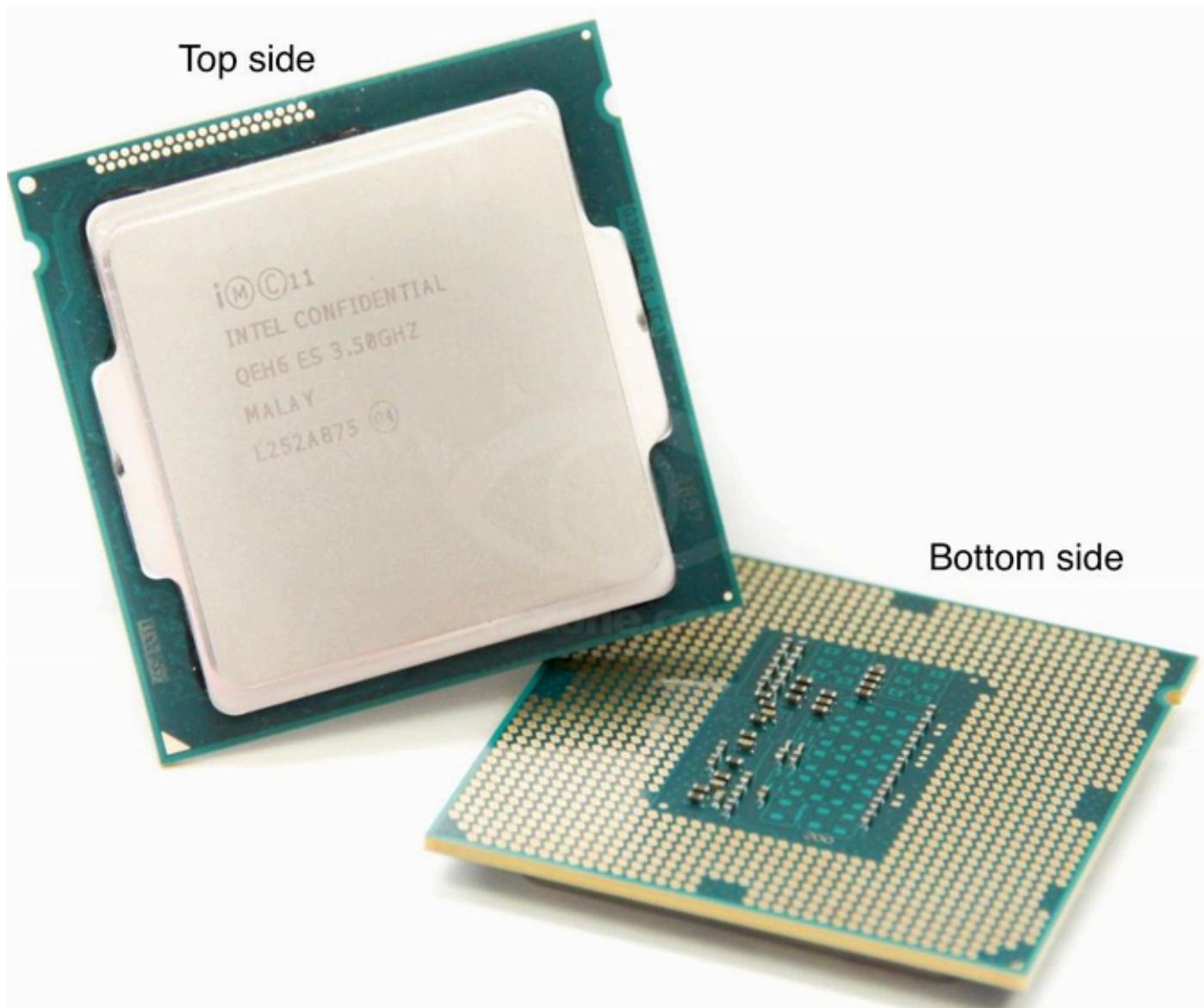
Die



Packaging



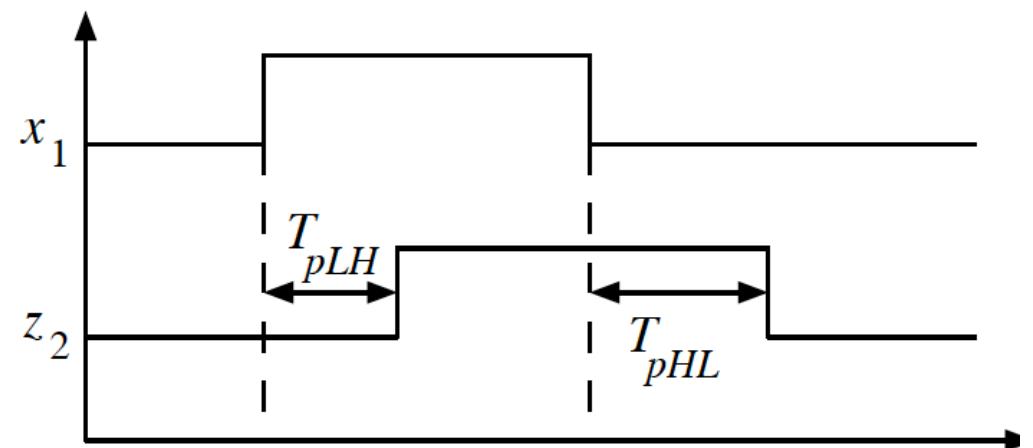
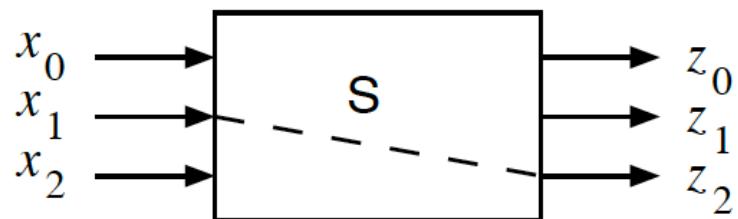
Packaging



Board design



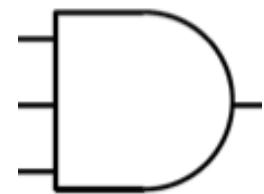
Timing Analysis



Gate type	Fan-in	Propagation delays	
		t_{pLH} [ns]	t_{pHL} [ns]
AND	2	$0.15 + 0.037L$	$0.16 + 0.017L$
AND	3	$0.20 + 0.038L$	$0.18 + 0.018L$
OR	2	$0.12 + 0.037L$	$0.20 + 0.019L$
OR	3	$0.12 + 0.038L$	$0.34 + 0.022L$
NOT	1	$0.02 + 0.038L$	$0.05 + 0.017L$

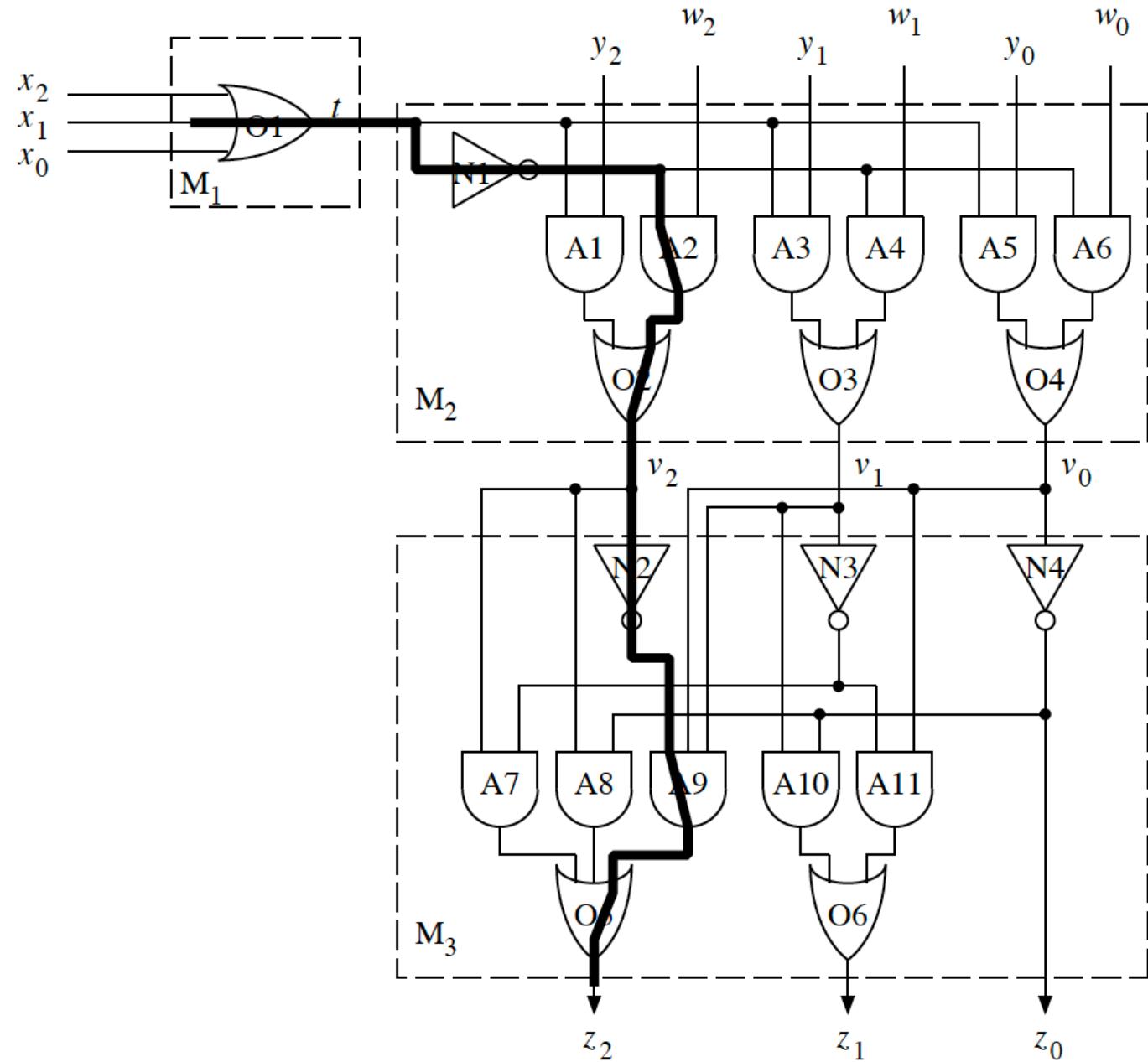
Clicker Question

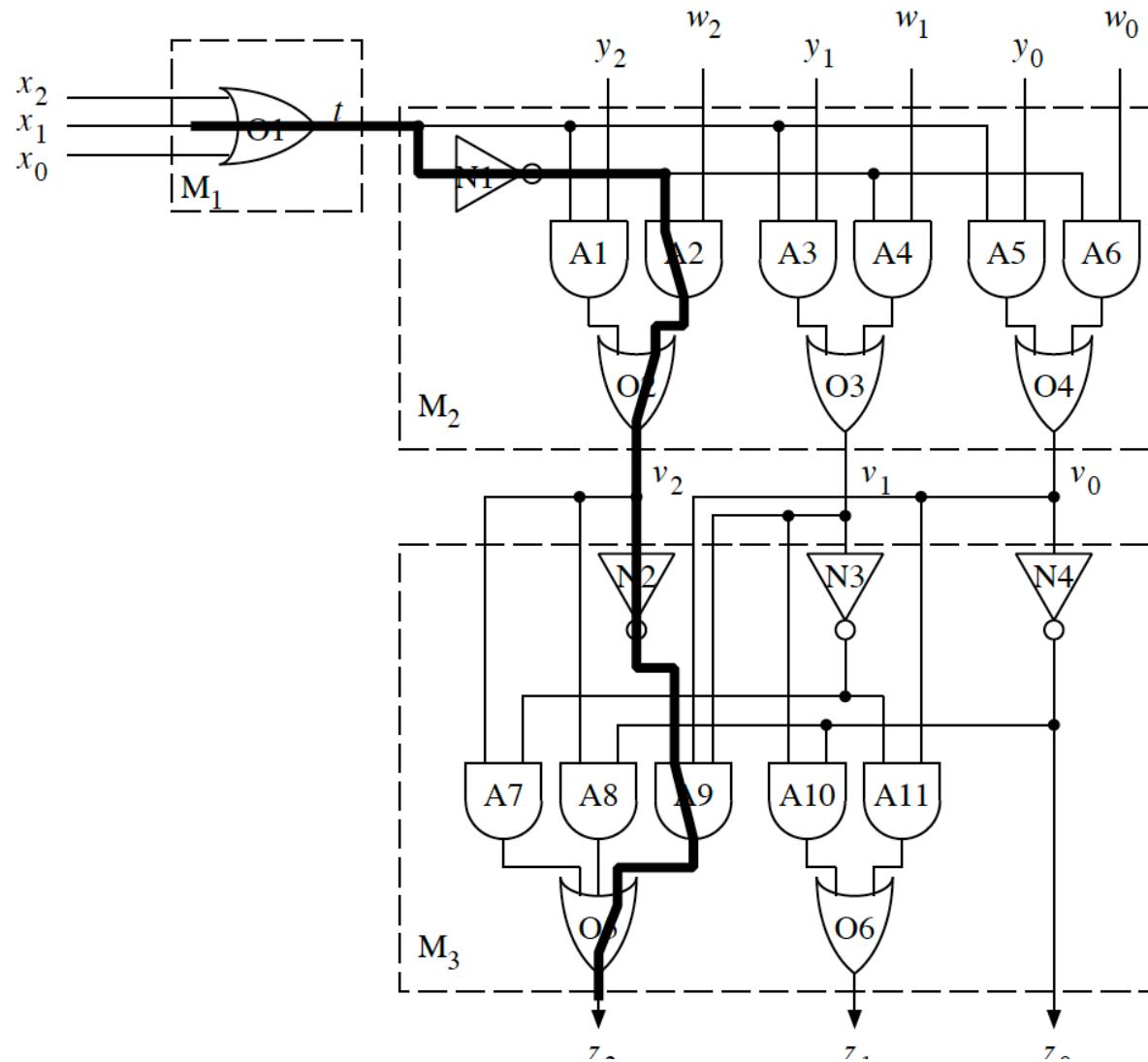
Using the gate characteristics given below,
determine equation for the propagation delay
 t_{pHL} for this circuit



- a) 0.20+0.038
- b) 0.18+0.018
- c) 0.12+0.038
- d) 0.34+0.022
- e) Not clear

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OR	3	$0.12 + 0.038L$	$0.34 + 0.022L$
NOT	1	$0.02 + 0.038L$	$0.05 + 0.017L$





NETWORK DELAY Example of path delay calculation:

$$O_1 \rightarrow N_1 \rightarrow A_2 \rightarrow O_2 \rightarrow N_2 \rightarrow A_9 \rightarrow O_5$$

NETWORK DELAY Example of path delay calculation:

$$O_1 \rightarrow N_1 \rightarrow A_2 \rightarrow O_2 \rightarrow N_2 \rightarrow A_9 \rightarrow O_5$$

$$\begin{aligned} T_{pLH}(x_1, z_2) &= t_{pLH}(O_1) + t_{pHL}(N_1) + t_{pHL}(A_2) + t_{pHL}(O_2) \\ &\quad + t_{pLH}(N_2) + t_{pLH}(A_9) + t_{pLH}(O_5) \end{aligned}$$

$$\begin{aligned} T_{pHL}(x_1, z_2) &= t_{pHL}(O_1) + t_{pLH}(N_1) + t_{pLH}(A_2) + t_{pLH}(O_2) \\ &\quad + t_{pHL}(N_2) + t_{pHL}(A_9) + t_{pHL}(O_5) \end{aligned}$$

Gate	Identifier	Output load	t_{pLH} [ns]	t_{pHL} [ns]
OR3	O_1	4	0.27	0.43
NOT	N_1	3	0.13	0.10
AND2	A_2	1	0.19	0.18
OR2	O_2	3	0.23	0.26
NOT	N_2	1	0.06	0.07
AND3	A_9	1	0.24	0.20
OR3	O_5	L	$0.12 + 0.038L$	$0.34 + 0.022L$

$$\begin{aligned} T_{pLH}(x_1, z_2) &= 0.27 + 0.10 + 0.18 + 0.26 + 0.06 \\ &\quad + 0.24 + 0.12 + 0.038L = 1.23 + 0.038L \text{ [ns]} \end{aligned}$$

$$\begin{aligned} T_{pHL}(x_1, z_2) &= 0.43 + 0.13 + 0.19 + 0.23 + 0.07 \\ &\quad + 0.20 + 0.34 + 0.022L = 1.59 + 0.022L \text{ [ns]} \end{aligned}$$