

DM74LS73A

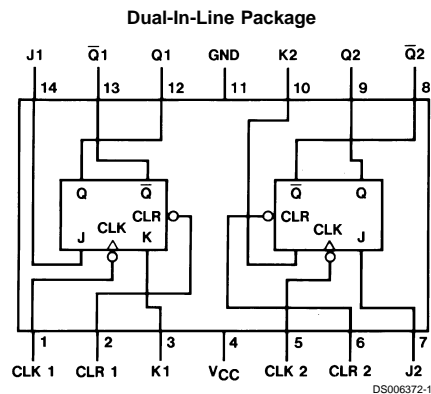
Dual Negative-Edge-Triggered Master-Slave J-K Flip-Flops with Clear and Complementary Outputs

General Description

This device contains two independent negative-edge-triggered J-K flip-flops with complementary outputs. The J and K data is processed by the flip-flops on the falling edge of the clock pulse. The clock triggering occurs at a voltage level and is not directly related to the tran-

sition time of the negative going edge of the clock pulse. The data on the J and K inputs is allowed to change while the clock is high or low without affecting the outputs as long as setup and hold times are not violated. A low logic level on the clear input will reset the outputs regardless of the levels of the other inputs.

Connection Diagram



Order Number DM54LS73AJ, DM54LS73AW, DM74LS73AM or DM74LS73AN
See Package Number J14A, M14A, N14A or W14B

Function Table

Inputs				Outputs	
CLR	CLK	J	K	Q	\bar{Q}
L	X	X	X	L	H
H	↓	L	L	Q_0	\bar{Q}_0
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	Toggle	Toggle
H	H	X	X	Q_0	\bar{Q}_0

H = High Logic Level

L = Low Logic Level

X = Either Low or High Logic Level

↓ = Negative going edge of pulse.

Q_0 = The output logic level before the indicated input conditions were established.

Toggle = Each output changes to the complement of its previous level on each falling edge of the clock pulse.

DM74LS73A Dual Negative-Edge-Triggered Master-Slave J-K Flip-Flops with Clear and Complementary Outputs

Absolute Maximum Ratings (Note 1)

Supply Voltage

7V

Input Voltage

7V

Operating Free Air Temperature Range

DM54LS

DM74LS

Storage Temperature Range

–55°C to +125°C

0°C to +70°C

–65°C to +150°C

Recommended Operating Conditions

Symbol	Parameter		DM54LS73A			DM74LS73A			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.8	V
I_{OH}	High Level Output Current				–0.4			–0.4	mA
I_{OL}	Low Level Output Current				4			8	mA
f_{CLK}	Clock Frequency (Note 3)		0		30	0		30	MHz
f_{CLK}	Clock Frequency (Note 4)		0		25	0		25	MHz
t_W	Pulse Width (Note 3)	Clock High	20			20			ns
		Preset Low	25			25			
		Clear Low	25			25			
t_W	Pulse Width (Note 4)	Clock High	25			25			ns
		Preset Low	30			30			
		Clear Low	30			30			
t_{SU}	Setup Time (Notes 2, 3)		20↓			20↓			ns
t_{SU}	Setup Time (Notes 2, 4)		25↓			25↓			ns
t_H	Hold Time (Notes 2, 3)		0↓			0↓			ns
t_H	Hold Time (Notes 2, 4)		5↓			5↓			ns
T_A	Free Air Operating Temperature		–55		125	0		70	°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: The symbol (↓) indicates the falling edge of the clock pulse is used for reference.

Note 3: $C_L = 15$ pF, $R_L = 2$ k Ω , $T_A = 25^\circ\text{C}$ and $V_{CC} = 5\text{V}$.

Note 4: $C_L = 50$ pF, $R_L = 2$ k Ω , $T_A = 25^\circ\text{C}$ and $V_{CC} = 5\text{V}$.

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 5)	Max	Units
V_I	Input Clamp Voltage	$V_{CC} = \text{Min}$, $I_I = -18$ mA			–1.5	V
V_{OH}	High Level Output Voltage	$V_{CC} = \text{Min}$, $I_{OH} = \text{Max}$	DM54	2.5	3.4	V
		$V_{IL} = \text{Max}$, $V_{IH} = \text{Min}$	DM74	2.7	3.4	
V_{OL}	Low Level Output Voltage	$V_{CC} = \text{Min}$, $I_{OL} = \text{Max}$	DM54		0.25	V
		$V_{IL} = \text{Max}$, $V_{IH} = \text{Min}$	DM74		0.35	
		$I_{OL} = 4$ mA, $V_{CC} = \text{Min}$	DM74		0.25	
I_I	Input Current @ Max Input Voltage	$V_{CC} = \text{Max}$	J, K		0.1	mA
		$V_I = 7\text{V}$	Clear		0.3	
			Clock		0.4	
I_{IH}	High Level Input Current	$V_{CC} = \text{Max}$	J, K		20	μA
		$V_I = 2.7\text{V}$	Clear		60	
			Clock		80	

Electrical Characteristics (Continued)

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 5)	Max	Units
I_{IL}	Low Level Input Current	$V_{CC} = \text{Max}$ $V_I = 0.4V$	J, K		-0.4	mA
			Clear		-0.8	
			Clock		-0.8	
I_{OS}	Short Circuit Output Current	$V_{CC} = \text{Max}$ (Note 6)	DM54	-20	-100	mA
			DM74	-20	-100	
I_{CC}	Supply Current	$V_{CC} = \text{Max}$ (Note 7)		4	6	mA

Switching Characteristics

at $V_{CC} = 5V$ and $T_A = 25^\circ C$

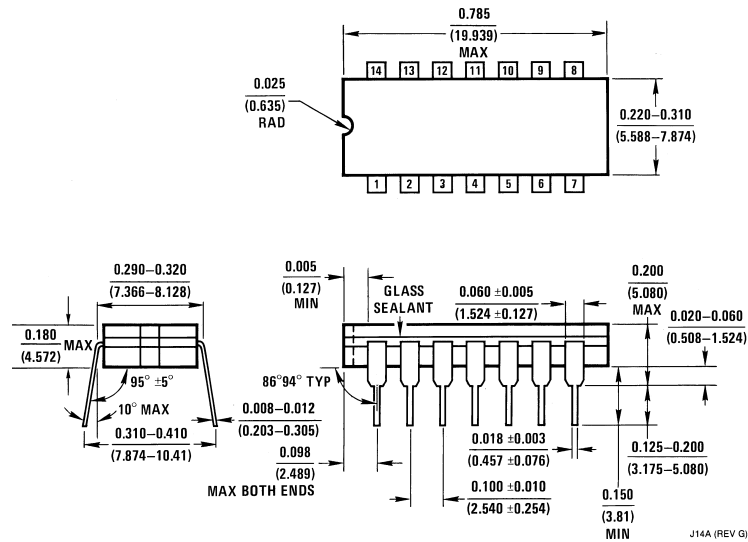
Symbol	Parameter	From (Input) To (Output)	R _L = 2 kΩ				Units
			C _L = 15 pF		C _L = 50 pF		
			Min	Max	Min	Max	
f _{MAX}	Maximum Clock Frequency		30		25		MHz
t _{PHL}	Propagation Delay Time High to Low Level Output	Clear to Q		20		28	ns
t _{PLH}	Propagation Delay Time Low to High Level Output	Clear to \overline{Q}		20		24	ns
t _{PLH}	Propagation Delay Time Low to High Level Output	Clock to Q or \overline{Q}		20		24	ns
t _{PHL}	Propagation Delay Time High to Low Level Output	Clock to Q or \overline{Q}		20		28	ns

Note 5: All typicals are at $V_{CC} = 5V$, $T_A = 25^\circ C$.

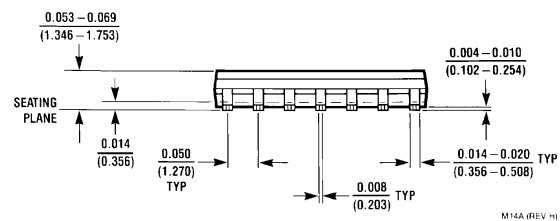
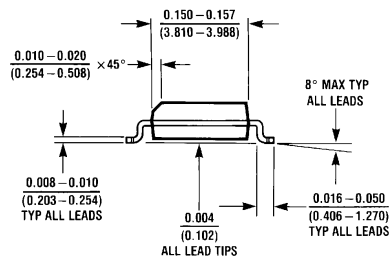
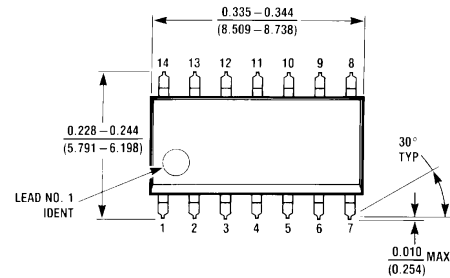
Note 6: Not more than one output should be shorted at a time, and the duration should not exceed one second. For devices, with feedback from the outputs, where shorting the outputs to ground may cause the outputs to change logic state, an equivalent test may be performed where $V_O = 2.25V$ and $2.125V$ for DM54 and DM74 series, respectively, with the minimum and maximum limits reduced by one half from their stated values. This is very useful when using automatic test equipment.

Note 7: With all outputs open, I_{CC} is measured with the Q and \bar{Q} outputs high in turn. At the time of measurement, the clock is grounded.

Physical Dimensions inches (millimeters) unless otherwise noted

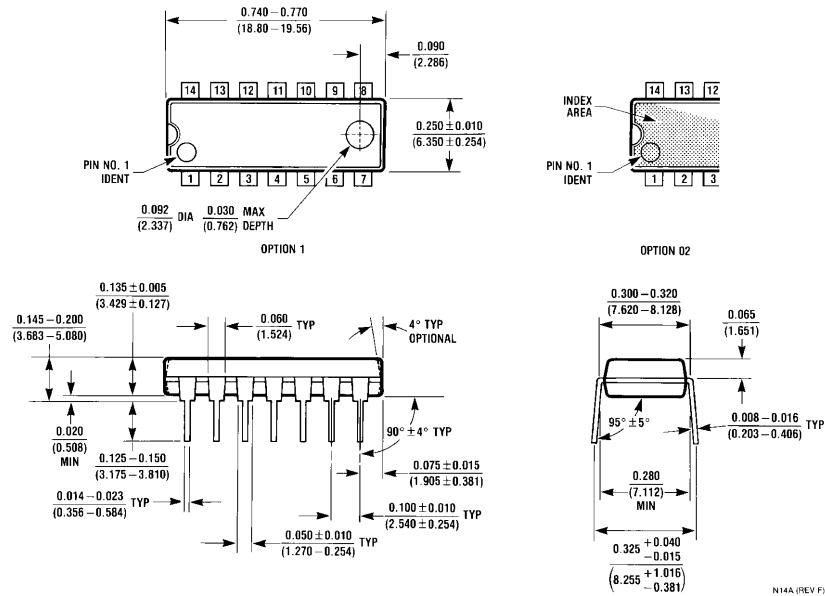


14-Lead Ceramic Dual-In-Line Package (J)
Order Number DM54LS73AJ
Package Number J14A

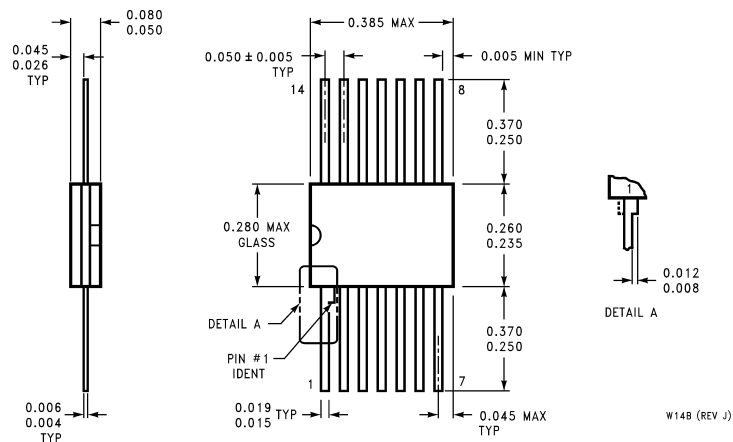


14-Lead Small Outline Molded Package (M)
Order Number DM74LS73AM
Package Number M14A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



14-Lead Molded Dual-In-Line Package (N)
Order Number DM74LS73AN
Package Number N14A



14-Lead Ceramic Flat Package (W)
Order Number DM54LS73AW
Package Number W14B

DM74LS73A Dual Negative-Edge-Triggered Master-Slave J-K Flip-Flops with Clear and Complementary Outputs

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

Fairchild Semiconductor Corporation Americas
Customer Response Center
Tel: 1-888-522-5372

www.fairchildsemi.com

Fairchild Semiconductor Europe
Fax: +49 (0) 1 80-530 85 86
Email: europe.support@nsc.com
Deutsch Tel: +49 (0) 8 141-35-0
English Tel: +44 (0) 1 793-85-68-56
Italy Tel: +39 (0) 2 57 5631

Fairchild Semiconductor Hong Kong Ltd.
13th Floor, Straight Block,
Ocean Centre, 5 Canton Rd.
Tsimshatsui, Kowloon
Hong Kong
Tel: +852 2737-7200
Fax: +852 2314-0061

National Semiconductor Japan Ltd.
Tel: 81-3-5620-6175
Fax: 81-3-5620-6179