DCS Lab 4
Sequential circuit

Sequential circuit

- Different from combinational circuit, a sequence circuit has memory elements that allow it to store information about previous data.

O

```
always @(posedge clk or negedge rst_n) begin
    if(!rst_n)
        a <= 0;
    else
        a <= a + 1;
end
```

← Sequential circuit

X

```
assign a = a + 1;

always @(*) begin
  a = a + 1;
end

always @(*) begin
  if(a > b) a = b;
  else a = a;
end
```

← Combinational circuit

Waveform different

- Combinational circuit

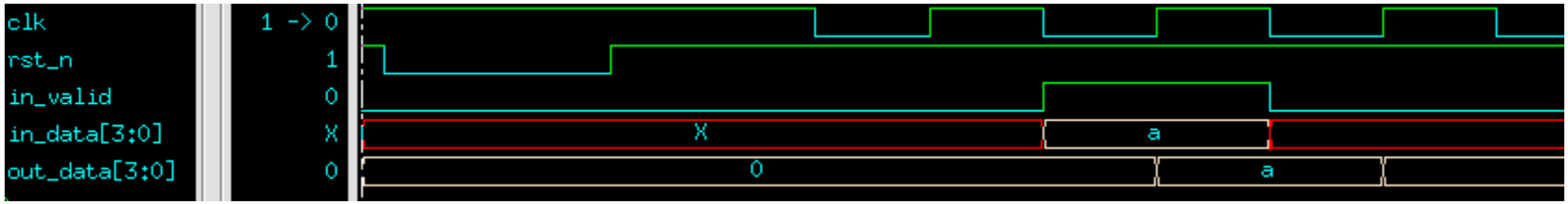
```
always@(*)begin
    if(in_valid) out_data = in_data;
    else out_data = 0;
end

assign out_data = (in_valid) ? in_data : 0;
```

Waveform different

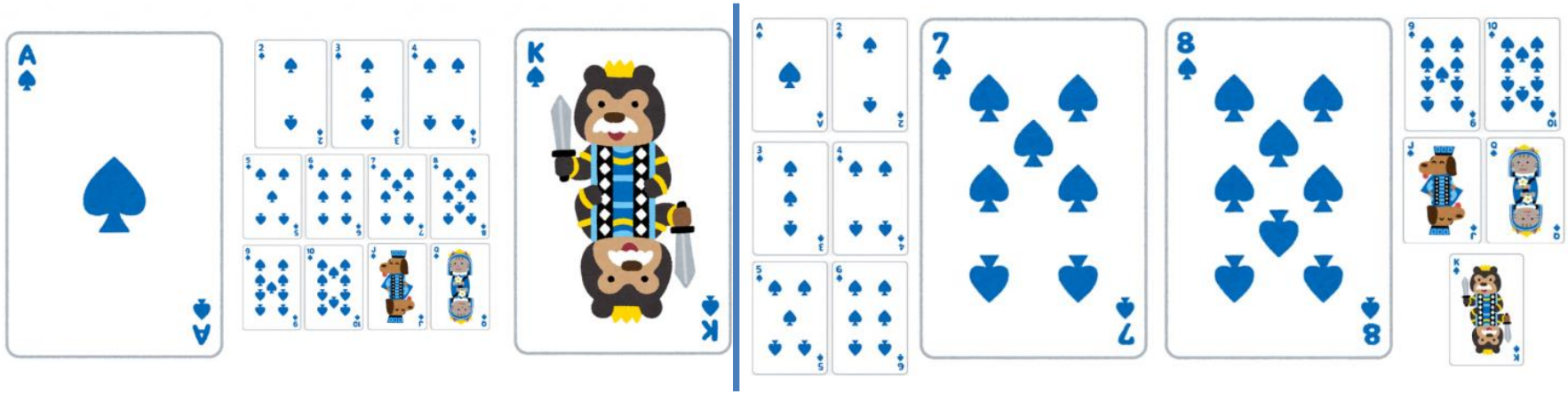
- Sequence circuit

```
always@(posedge clk or negedge rst_n)begin
    if(!rst_n)
        out_data <= 0;
    else begin
        if(in_valid) out_data <= in_data;
        else out_data <= 0;
    end
end
```



The design of the detection sequence

- 射龍門 is a type of poker game where players are dealt two cards. If the third card falls within the range, the player wins; otherwise, they lose.



If the first two cards are A and K (1 and 13), the third card can be 2~Q(2~12) to win the game while A or K can not.

If the first two cards are 7 and 8, no matter what the third card is, it cannot satisfy the winning condition.

Output condition

- TA will provide a random series of numbers as data.
- If three adjacent data points satisfy the condition that the first and third numbers are doors and the second number is a ball.
- Output 1 if the conditions for scoring a goal are met, and 0 otherwise.
- EX: input data: 13 9 2 4 6
  output data should be: 1 0 1

  (13>9 9>2) (9>2 2<4) (2<4 4<6)
- Output length = input length - 2

Seq.sv

Input Signal	Bit Width	Definition
clk	1	Clock
rst_n	1	Asynchronous active-low reset
in_valid	1	High when input is valid

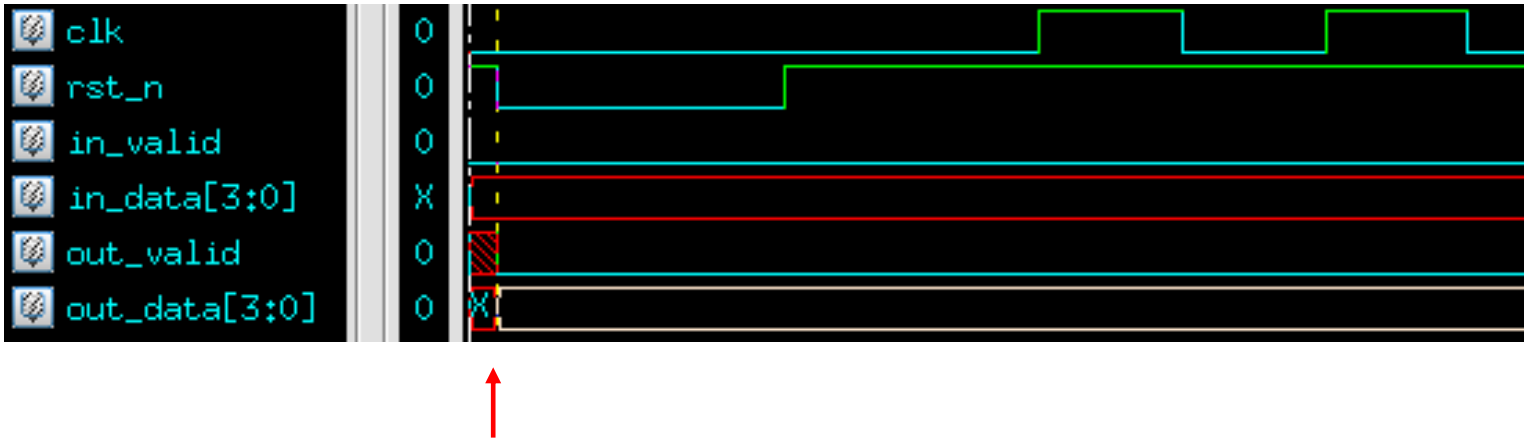
Output Signal	Bit Width	Definition
out_data	1	If satisfy the winning condition output 1, otherwise output 0.
out_valid	1	High when output is valid

Spec

- All outputs must have asynchronous negative-edge reset.
- 01_RTL needs to pass.
- 02_SYN should have no errors or latches.
- 02_SYN's timing slack must be met.
- 03_GATE needs to pass.

Waveform rst_n

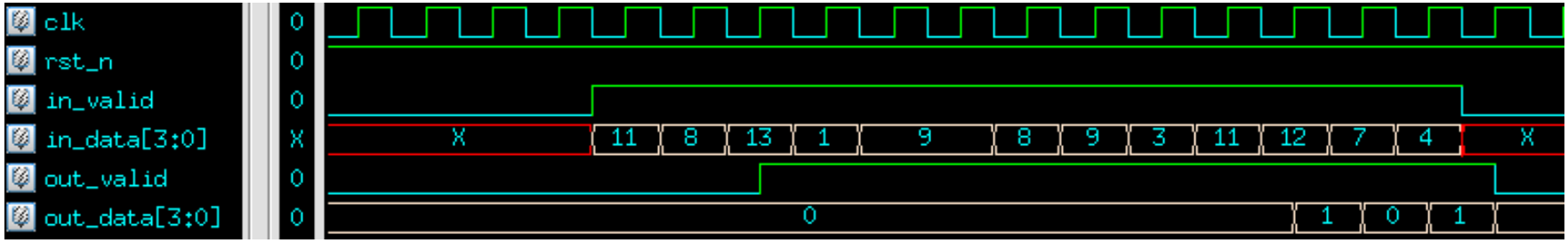
- Waveform



negative trigger asynchronous reset

Waveform in_data

- Waveform



Command

- tar -xvf ~dcsta01/Lab04.tar
- cd Lab04/01_RTL/
- Need 02_SYN
  - No Latch
  - No error
  - No timing violation (MET)
- Need 03_GATE
- Separate combinational and sequential blocks

Demo1: 3/24(Thursday), 16:20:00

Demo2: 3/24(Thursday), 23:59:59