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ABSTRACT

Reducing the energy inefficiency of conventional CMOS-based computing devices—which rely on logically irreversible gates to process information—remains both a fundamental engineering challenge and a practical social challenge of increasing importance. We extend an alternative computing paradigm that manipulates microstate distributions to store information in the metastable minima determined by an effective potential energy landscape. These minima serve as mesoscopic memories that are manipulated by a dynamic landscape to perform information processing. Central to our results is the *control erase* protocol, which controls the landscape's metastable minima to determine whether information is preserved or erased. Importantly, successive protocol executions can implement a NAND gate—a logically irreversible universal logic gate. We show how to practically implement CEs in a device created by two inductively coupled superconducting quantum interference devices (SQUIDs). We identify circuit parameter ranges that give rise to effective CEs and establish the device's robustness against thermally induced errors. These SQUID-based logical devices are capable of operating above GHz frequencies and at the $k_B T$ energy scale. Due to this, optimized devices and associated protocols provide a universal-computation substrate that is both computationally fast and energy efficient.

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The controlled-erasure computing paradigm manipulates microstate distributions to store information in metastable mesoscopic memories. We implement this by inductively coupling superconducting quantum interference devices (SQUIDs) that operate above GHz frequencies and at the $k_B T$ energy scale. We show how bifurcation theory provides a workable and robust design strategy for performing universal classical computations in an energy landscape.

I. INTRODUCTION

Conventional classical computing systems harness irreversible logic gates—e.g., NAND gates—to process information. Irreversibility arises from erasing input information to create desired output states, coming at a minimum theoretical heat dissipation cost of

$k_B T \ln 2$ per erasure¹. During their operation, current conventional CMOS-based computational devices generate $\mathcal{O}(10^4)$ times more heat than this minimum cost.^{2–5} On the social scale, energy consumption for computational purposes is projected to reach 20% of global energy demand by 2030.⁶ In light of this, it is time to investigate alternative strategies and substrates that give rise to markedly more energy-efficient universal computation.

One strategy implied in Landauer's seminal 1961 result^{1,7–14} focuses on manipulating metastable energy minima in an effective potential energy landscape. Coarse-graining the microstate phase-space surrounding the minima yields long-lived mesoscopic memory states that correspond to the logical 0s and 1s of binary computation. From this perspective, a computation is implemented by controlling memory-state dynamics through changes in the landscape to implement a map between initial and final memory states. This “energy first” perspective of computation allows for the careful

analysis and prediction of a given logic gate's performance and efficiency.^{1,7,11,14}

Elaborating on this framework, Sec. II first describes a family of potential energy landscapes capable of storing two bits of information. Section III introduces a family of *control erase* (CE) protocols—two-dimensional generalizations of single-bit erasure protocols. Section IV then presents a device constructed from two inductively coupled superconducting quantum interference devices (SQUIDs).^{15–20} We demonstrate that this device implements an appropriate potential energy landscape and executes CE protocols by changing its circuit parameters. Sections V A–V C explore the effectiveness of the SQUID CE implementation as a function of circuit parameters. Notably, serial executions of CEs produce a robust NAND gate, as detailed in Sec. V D. Executing robust NAND gates with this device supports extremely low-energy universal computation.

II. PHYSICAL COMPUTING VIA METASTABLE LANDSCAPES

Consider a potential energy landscape that exhibits several energy minima supported via an underlying physical substrate, which is connected to a thermal environment that introduces damping and noise into its dynamics. The minima are separated by energy barriers, whose heights are substantially larger than the thermal energy $k_B T$. The thermal environment quickly induces distributions of microstates to settle into local equilibria in the phase-space regions surrounding these wells. Noise perturbs the microstates within their respective regions; however, it is unlikely to drive the microstates between these regions on a timescale that scales exponentially with the energy barrier height. The energy barriers prevent mixing between these regions except on these very long timescales. As a result, the minima serve to support long-lived mesoscopic system states—metastable memory states. Manipulating them with the potential's dynamics corresponds to information processing.

The following details physically embedded computations via landscape control in this setting.^{1,13,21–24} Specifically, these computations are stochastic mappings from the set of initial to final memory states \mathcal{M} . Here, we introduce the *control erase* (CE) protocol over two input bits. One way of embedding 2-bit computations is to control a two-dimensional potential with a minimum in each quadrant. The memory states are distinguished using the x and y axes,

$$\text{first [second] bit} = \begin{cases} 0 & \text{if } x[y] < 0, \\ 1 & \text{if } x[y] > 0. \end{cases} \quad (1)$$

Figure 1 illustrates a quadruple well potential with an example memory-state instantiation chosen by the locations of the minima according to Eq. (1). The computational operations to be performed on the potential—i.e., the deterministic transformation of the potential that maps information from initial to final metastable memory states—is referred to as a *physical protocol*.

Last, we formally define metastable memory states in the x - y plane and how they evolve under a computational protocol. Over the time interval $t \in [t_i, t_f]$ and given an initial two-bit metastable memory state $(X, Y) := (m_x(t = t_i), m_y(t = t_i)) \in \mathcal{M}$,

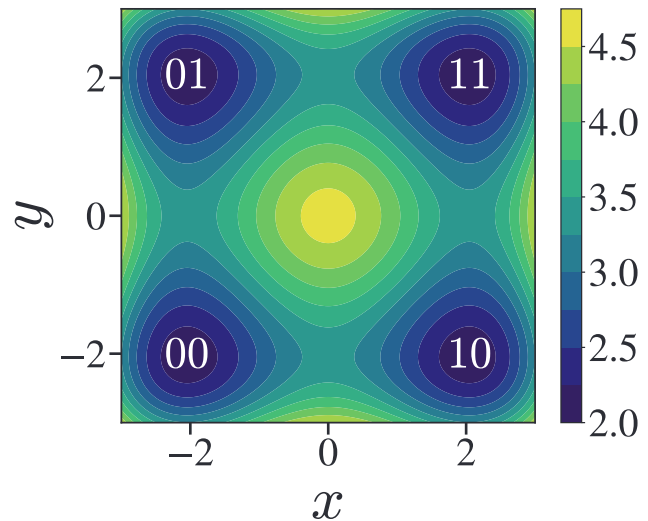


FIG. 1. Example 2-bit memory mesoscopic-state instantiation in a four well potential. Regions surrounding energy minima provide metastable information storage, whose bit value is assigned according to Eq. (1). Controlling this energy landscape manipulates the memory state's dynamics, thereby implementing information processing.

the final memory state $(X', Y') := (m_x(t = t_f), m_y(t = t_f))$ is determined by the conditional probability $\mathbf{p} = \Pr((X', Y')|(X, Y))$. With this, the final microstate distribution $\tilde{p}(t = t_f)$ is updated through $\tilde{p}(t = t_f) = \mathbf{p} \tilde{p}(t = t_i)$. A deterministic logic gate is successfully performed when these conditional probabilities are very close to either 0 or 1.

III. CONTROL ERASE PROTOCOL

The NAND gate is a binary logical gate that takes in two input bits, meaning that there are four possible input states—00, 01, 10, and 11—and one output bit—either 0 or 1. Specifically, the output state is 1 for all input states except if both input bits are 1, in which case the output is 0.

Consider reading the output state to be 1 with no knowledge of a NAND gate's input state. Since there are three possible inputs that can produce this single output state, inferring which specific two-bit input state led to the output bit 1 is impossible. The logical impossibility manifests as a physically irreversible erasure of information associated with phase-space contraction at the microscopic scale. In contrast, if the output was 0, then the input is trivially known to be 11 and no phase-space contraction is entailed.

The above illustrates the NAND's underlying information processing task: Preserve some input information, while erasing the rest. In this way, performing a NAND gate requires the ability to carry out controlled erasure protocols over the space of memory states.

Erasure protocols in one-dimensional systems have been studied previously.^{1,11,13,25–29} The following extends this to an erasure protocol via the two-dimensional potential shown in Fig. 1. The additional freedom given by the second dimension permits control

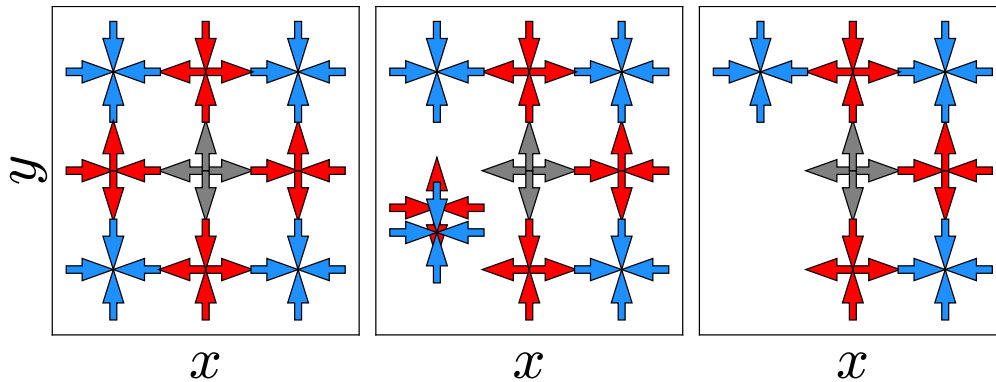


FIG. 2. Control erase (CE) protocol illustrated via the dynamical skeleton of the potential energy landscape in Fig. 1, showing only the potential's fixed points and corresponding local flow fields. Stable minima (unstable saddle) fixed points are colored blue (red), while gray indicates a local maximum. This CE is executed with respect to the y axis: The states contained on the negative x half-plane undergo an erasure of Y to the 1 state, while those on the positive x half-plane do not change. This results in the third quadrant's stored information being erased into the second quadrant. (Left) Initial potential energy landscape configuration. (Center) The stable and unstable fixed points in the third quadrant (lower left of panel) approach each other just before annihilation. (Right) Immediately after fixed point annihilation in the third quadrant. If this landscape is held long enough, all information initially stored in quadrant III will be erased to quadrant II. Importantly, all other fixed points are maintained during this time. One completes the CE protocol cycle by bringing the potential back to its starting configuration. Note that the saddle node bifurcation in this particular CE is designed with our choice of the physical substrate in mind; a CE operation can also be accomplished with a pitchfork bifurcation.

over what information is preserved and erased. Via that control, a NAND operation can be performed. To accomplish this, we introduce the *control erase* (CE) protocol. Figure 2 illustrates a CE protocol via the potential's skeleton, viewing the potential from a dynamical systems perspective—i.e., via its fixed points and local flow fields in the microscopic state space. In this example, the negative x half-plane executes an erasure protocol, while the positive x half-plane remains unchanged.

Executing a given CE protocol requires three binary choices, illustrated via examples:

1. First, choose which of the two input bits to operate on. For example, erasing information along the y axis requires operating only on the second bit so that $Y' \neq Y$. This implies that the first input bit is preserved, i.e., $X' = X$. However, this does not fully specify the pair of states involved in the CE: 00 and 01, or 10 and 11 are both candidate pairs for a $Y' \neq Y$ operation.

2. Next, specify which pair of two-bit memory states are involved in the erasure. Suppose we select the states 10 and 11: Doing this controls the erasure operation on X such that information is erased in Y only if $X = 1$. Otherwise, if $X = 0$, the information stored in Y is preserved. We denote this choice as a function $CE(X, Y)$ that is an identity on Y if $X = 0$ and an erasure of Y if $X = 1$.
3. However, we also need to choose whether Y is erased to the 0 or the 1 state. For example, if we erase to state 1, we augment our notation to be $CE_1(X, Y)$.

These three binary choices produce the eight CE protocols of interest shown in Fig. 8. All said, the choices above give us $(X', Y') = (I(X), CE_1(X, Y))$, where $I(X)$ indicates an identity operation on the X input bit. For legibility, we introduce a condensed notation that suppresses the functional dependencies: $(X', Y') = (I_X, C_{\bar{X}}E_1)$. The following relies on this notation.

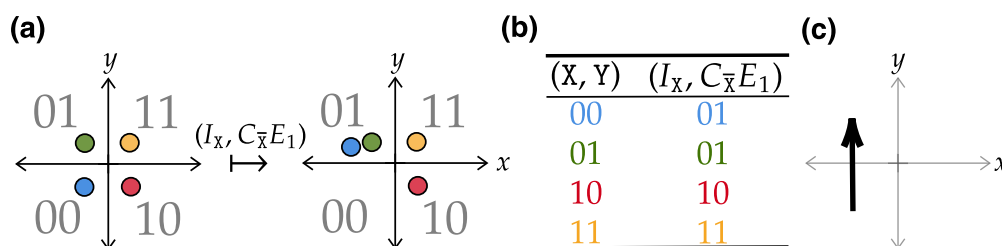


FIG. 3. (a) State mapping executed by the control erase $(X', Y') = (I_X, C_{\bar{X}}E_1)$. Each quadrant contains a coarse-grained metastable memory state, defined by Eq. (1). Every circle represents a distribution of microstates, i.e., information, and is colored based on its original memory-state instantiation. (b) CE truth table. The overline above state X , in the symbol $C_{\bar{X}}$, indicates controlling on the negation of X , erasing Y to 1 only when $X = 0$. (c) Arrow-based notation illustrating the $(I_X, C_{\bar{X}}E_1)$ CE protocol. This depiction is also used in Sec. V D. Figure 8 shows all CEs of interest.

Figure 3 shows multiple representations of another CE: $(I_X, C_{\bar{X}}E_I)$. This also erases information stored in Y , but instead of erasing the information if $X = 1$, the erasure happens if $X = 0$. In other words, our control is \bar{X} (NOT X), rather than X . Of particular importance is the arrow-based notation in Fig. 3, which is employed when detailing the NAND gate in Sec. V D.

To generalize the CE notation, first we know that one of the two output states $\rho' \in \{X', Y'\}$ is created by the identity operation $\rho' = I_\rho$, where $\rho \in \{X, Y\}$. The other output state is created by $C_\sigma E_A$. Here, $\sigma \in \{\rho, \bar{\rho}\}$ indicates the control state for an erasure to the $A \in \{0, 1\}$ state. Note that the overline $\bar{\rho}$ above ρ indicates a negation of the ρ state. The eight CEs of interest are shown in Fig. 8 in Appendix C.

IV. DEVICE IMPLEMENTATION

Sufficient control of a quadruple well potential that takes the form of Fig. 1 can perform a CE. Here, superconducting quantum interference devices (SQUIDs) are employed as an example physical platform for performing CE protocols. To emphasize, other than zero-resistance supercurrents and the Josephson nonlinearity, no quantum-mechanical phenomena are used for information processing. In addition, low-temperature operation is relied on only insofar as it is necessary to establish the supercurrent. We first briefly review related superconducting device physics. Then, we specify the device of interest—two inductively coupled SQUIDs, shown in Fig. 4—whose potential energy landscape can dynamically execute CE protocols.

Historically, the *quantum flux parametron* (QFP) was invented by Goto in 1985^{15,30} for classical computing applications on an energy-efficient superconducting platform. With the incentive of optimizing circuit parameters and operating on slower computational timescales to aid energy efficiency, Takeuchi *et al.* introduced the *adiabatic QFP* (AQFP).^{4,31} In contrast to our focus here, their circuit parameters were not optimized for thermodynamic performance but instead were determined via bifurcation theory. With a similar design construction as the QFP, and having the same equations of motion as the QFP, in 1989 Han *et al.* introduced the *variable β radio frequency SQUID*.^{16–18} This device was later named the *compound Josephson junction radio frequency SQUID* (CJJ rf SQUID).^{19,32,33} Its principal use was for investigating macroscopic quantum phenomenon (MQP), not classical information processing. As such, our present goal—demonstrating universal classical information and storage—is not shared with the CJJ rf SQUID literature.

This said, the circuit parameter values used in these earlier devices happen to be useful in Sec. V C for evaluating the performance of our device of interest when performing CE protocols. Since QFPs and CJJ rf SQUIDs are both SQUIDs, we refer to the device in Fig. 4 as two inductively coupled SQUIDs. Reference 20 introduced and detailed the device in Fig. 4. Importantly, it supports a potential equivalent to that of Fig. 1. To understand how it executes computations, the following gives a synopsis of the device's potential energy surface. Physically grounded approximations and assumptions for executing a CE protocol are then detailed.

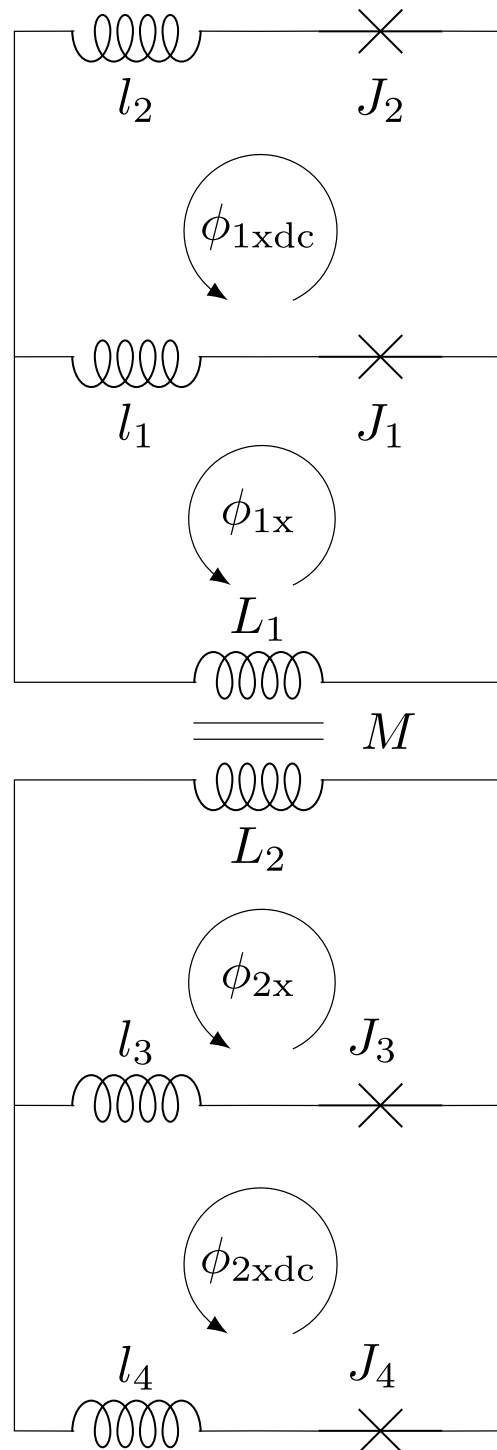


FIG. 4. Two inductively coupled SQUIDs interacting via mutual inductance coupling constant M .

Figure 4 illustrates a device consisting of two inductively coupled SQUIDs. In this circuit, L_i (l_i) indicate the radio frequency (direct current) SQUID inductances, while J_j indicates the Josephson junctions, all for which $i = 1, 2$, and $j = 1, 2, 3, 4$. Up to a constant, this device generates the following potential energy surface:

$$\begin{aligned} U' = U/U_0 = & \frac{1}{2}(\varphi_1 - \varphi_{1x})^2 + \frac{1}{2}(\varphi_2 - \varphi_{2x})^2 \\ & + \frac{\gamma_1}{2}(\varphi_{1dc} - \varphi_{1xdc})^2 + \frac{\gamma_2}{2}(\varphi_{2dc} - \varphi_{2xdc})^2 \\ & - \beta_1 \cos \frac{\varphi_{1dc}}{2} \cos \varphi_1 - \beta_2 \cos \frac{\varphi_{2dc}}{2} \cos \varphi_2 \\ & + \delta\beta_1 \sin \frac{\varphi_{1dc}}{2} \sin \varphi_1 + \delta\beta_2 \sin \frac{\varphi_{2dc}}{2} \sin \varphi_2 \\ & + \mu(\varphi_1 - \varphi_{1x})(\varphi_2 - \varphi_{2x}). \end{aligned} \quad (2)$$

Here, $\varphi_r = (2\pi\phi_r)/\Phi_0$ is the reduced flux variable of the r th flux variable, while Φ_0 is the flux quantum. We subsequently take $L := L_1 = L_2$ and $l_{1(2)} := l_{1(3)} = l_{2(4)}$. Next, we define $L_\alpha = \alpha L$ for which $\alpha = 1 - \mu^2$ such that $\mu = M/L$. M is a tunable mutual inductance constant: While its experimental implementation—a SQUID coupler between the two SQUIDs—is discussed in Refs. 32–34, the coupler's dynamics will not be addressed here. With this, $U_0 = (\Phi_0/2\pi)^2/L_\alpha$ and $\gamma_{1(2)} = L_\alpha/2l_{1(2)}$. Last, $\beta_{1(2)} = 2\pi L_\alpha(I_{c2(4)} + I_{c1(3)})/\Phi_0$, and $\delta\beta_{1(2)} = 2\pi L_\alpha(I_{c2(4)} - I_{c1(3)})/\Phi_0$, where each I_{cj} corresponds to the critical current I_c of the j th Josephson junction.

Note that Eq. (2) contains four degrees of freedom, namely, φ_i and φ_{idc} , where $i = 1, 2$. This type of compound SQUID is generally constructed with $\gamma_i \gg 1$.^{18,35} This implies that any changes in φ_{idc} are rapidly observed in φ_{idc} , so we assume $\varphi_{idc} = \varphi_{ixdc}$. Applying this approximation to Eq. (2) projects the potential onto two dimensions, providing the potential energy surface shown in Fig. 1 in the φ_1 – φ_2 plane.

Next, we assume that the fabrication consistency of the JJ elements is such that $\delta\beta_1 = \delta\beta_2 = 0$: This assumption is fairly common, as it streamlines the process of analyzing the device's equation of motion. In practice, $\delta\beta_1 \neq \delta\beta_2 \neq 0$, which results in a slight offset in the wells' locations.²⁷ This induced asymmetry in a real device can be at least partially compensated by external flux parameters if necessary. Along similar lines, we let $\beta := \beta_1 = \beta_2$ as well as $I_c := I_{c1} = I_{c2} = I_{c3} = I_{c4}$. Finally, assuming small-valued coupling ratios, we drop terms that are quadratic in μ , which sends $\alpha \rightarrow 1$ and $L_\alpha \rightarrow L$.

All this done, rewriting Eq. (2) then gives

$$\begin{aligned} U' = & \frac{1}{2}(\varphi_1 - \varphi_{1x})^2 + \frac{1}{2}(\varphi_2 - \varphi_{2x})^2 \\ & - \beta \cos \frac{\varphi_{1xdc}}{2} \cos \varphi_1 - \beta \cos \frac{\varphi_{2xdc}}{2} \cos \varphi_2 \\ & + \mu(\varphi_1 - \varphi_{1x})(\varphi_2 - \varphi_{2x}). \end{aligned} \quad (3)$$

Equation (3) describes a dimensionless potential U' with two degrees of freedom; this will be frequently referred to in the remainder. We manipulate the potential energy landscape with the following circuit parameters for $i = 1, 2$: (i) φ_{ix} tilts the potential with respect to the i th axis, (ii) φ_{ixdc} provides an *in situ* barrier control on the i th axis, and (iii) μ supplies a coupling interaction between the two circuits,

which biases the potential to favor wells that lie on one of the two diagonals in the φ_1 – φ_2 plane.

V. CONTROL ERASE PROTOCOL IMPLEMENTATION

The approximations in Sec. IV yield the potential given in Eq. (3) and displayed in Fig. 1. Manipulating the aforementioned external circuit parameters implements any of the eight possible control erase (CE) protocols shown in Fig. 8. Using the CE (I_x , $C_{\overline{x}}E_1$) from Figs. 2 and 3 as an example, we detail how to find circuit parameter values that give rise to “effective” protocols in Sec. V A. We qualitatively show this by exploring circuit parameter values that give rise to ranges for which this particular CE can be executed. Furthermore, we quantify this protocol's effectiveness—i.e., if it is highly robust—in Sec. V C. Section V B generalizes to determine which circuit parameters will be used to carry out any CE protocol in Fig. 8. With this, Sec. V D demonstrates the physical execution of an effective NAND gate. As a final practical note, we do not detail how inputs are given, or how outputs are read, from the circuit. We assume only that the circuit begins in a particular logical state and undertake the task of implementing a control protocol for which it ends in the logical state dictated by the CE operation

A. Effective CE protocol

Figure 5(a) highlights the important fixed points on the potential immediately before and after the stable (red) and unstable (green) fixed points annihilate in the negative- x half-plane. After the annihilation, a CE is possible since the orange, blue, and purple fixed points on the positive- x half-plane are preserved. From the perspective detailed in Sec. III, the information stored in the Υ state on the negative- x half-plane is erased, while all other information in the potential's memory states is preserved. In this example, $\Delta U'_{00}$ denotes the potential barrier that must vanish for the CE to be carried out. Once this barrier vanishes, $\Delta U'_{01}$, $\Delta U'_{10}$, and $\Delta U'_{11}$ denote the barriers that need to be maintained. The goal is to find the circuit parameter values that give these barriers sufficiently large heights, as this further contributes to a robust CE.

Figure 5(b) illustrates bifurcation diagrams of the φ_2 coordinate over a given circuit parameter range, while all other parameters are held constant. Note that the coordinate φ_2 is solely illustrated because φ_1 varies negligibly in comparison. Additionally, if fixed points annihilate within a parameter value range, they are displayed in Fig. 5(b). Otherwise, the fixed points do not annihilate within this selected range, and their φ_2 trajectory is not shown.

To guide the exploration of viable parameter values, a general view of the relationship between the dimensionless barrier heights illustrated in Fig. 5(b) and the energy scale of thermal fluctuations $k_B T$ is useful. Understanding this aids in determining whether a barrier height is energetically large enough to store microstates within a metastable memory state.

For example, suppose the barrier should be no smaller than $50k_B T$. Using common values from the SQUID literature,^{17,36} $T = 100$ mK and $L = 230$ pH, this corresponds to a dimensionless barrier height of $\Delta U' = 50k_B T/U_0 = 0.15$. We indicate this barrier height with the dashed horizontal line in the insets of Fig. 5(b); it represents a proxy for characterizing dimensionless barrier heights.

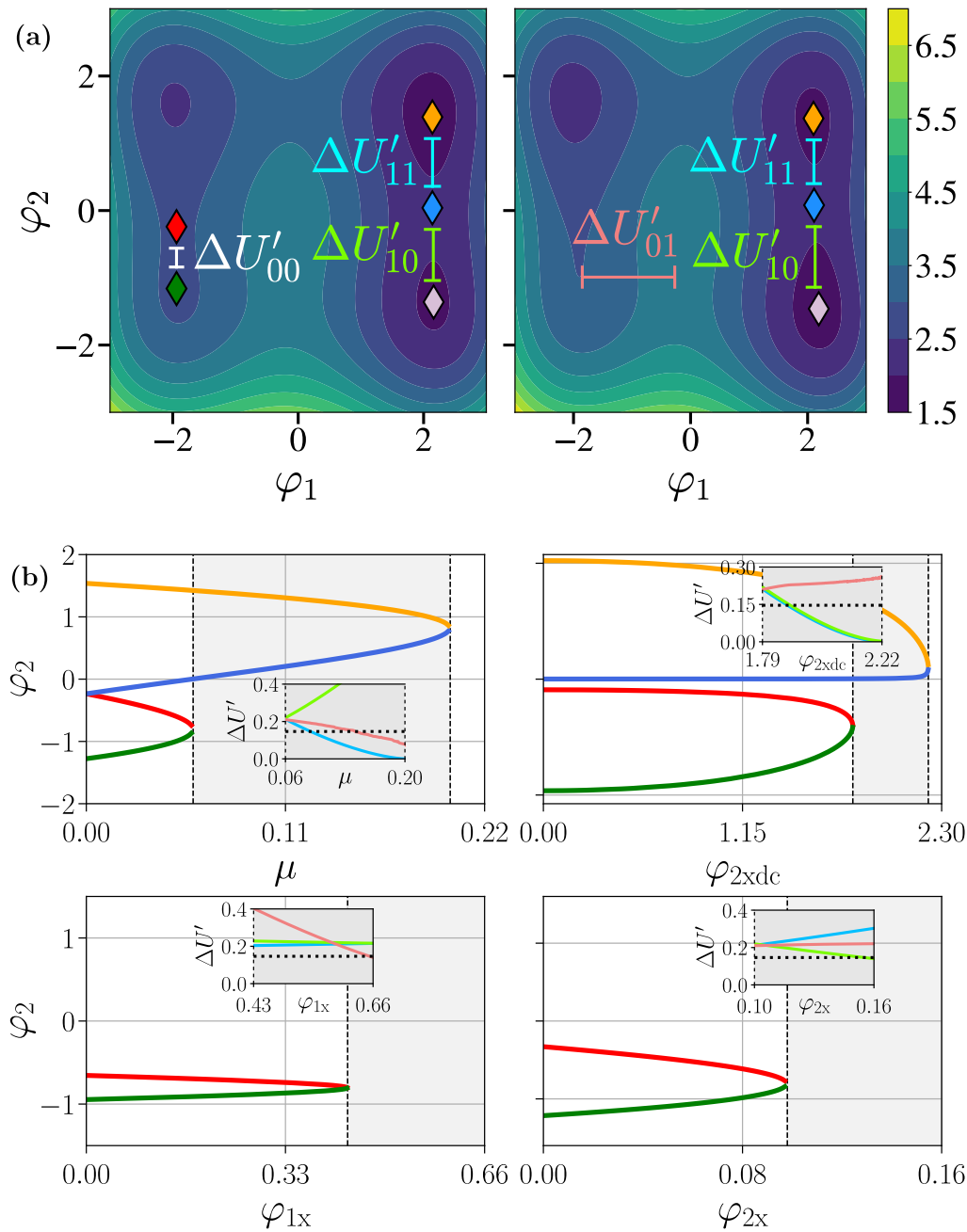


FIG. 5. Circuit parameter ranges that eliminate the dimensionless potential barriers $\Delta U'_{00}$ and maintain $\Delta U'_{11}$ and $\Delta U'_{10}$. In the insets, light blue, light green, and light red correspond to the barriers $\Delta U'_{11}$, $\Delta U'_{10}$, and $\Delta U'_{01}$, respectively. The dotted line corresponds to a thermal energy barrier of $50 k_B T$ at $T = 100$ mK with $L = 230$ pH. For exemplary purposes, $\beta = 2.3$. (a) Specific fixed points (colored diamonds) within the potential energy landscape, as well as corresponding energy barriers, are utilized to investigate the CE in Fig. 2. (Left) Prior to the fixed point annihilation in the third quadrant. (Right) After fixed point annihilation that causes $\Delta U'_{00}$ to vanish. Once all information stored in the 00 state is erased into the 01 state and the potential is subsequently brought back to its original configuration, the CE is completed. (b) Circuit parameter ranges for achieving the CE in Fig. 2, which can be accomplished by the annihilation of the green and red fixed points while maintaining the yellow and blue fixed points. Each circuit parameter range holds all other nonzero circuit parameters at the respective constant values: $\mu = 0.06$, $\varphi_{2xdc} = 1.79$, $\varphi_{1x} = 0.61$, and $\varphi_{2x} = 0.10$. These circuit parameters lead to effective CE protocols and, therefore, robust NAND gates.

That is, if a circuit parameter's value results in either $\Delta U'_{01}$, $\Delta U'_{10}$, or $\Delta U'_{11}$ falling below this line, then we say it is no longer able to reliably store information in the relevant well. Of course, this all varies depending on the device's operating temperature and parameter values. For instance, if we wanted to continue using $U' = 0.15$ as a with other standard values from the QFP literature^{4,31,37,38}— $T = 4.2$ K and $L = 10$ pH—this corresponds to a dimension-full barrier height of $\Delta U = 0.15U_0 = 28 k_B T$. As a final note, motivated by Ozfidan *et al.*,³⁶ we let $\beta = 2.3$.

The following now describes the qualitative consequences of changing each circuit parameter and the resulting potential in Fig. 5(a). First, as μ increases, the depth of the minima representing the states 01 and 10 increases. Meanwhile, the minimum's depth in the 11 state decreases, leading to $\Delta U'_{11}$ decreasing. This indicates that μ should not take on too large of a value in order to avoid fluctuations over the $\Delta U'_{11}$ barrier. Next, if the magnitude of $\varphi_{2\text{xdc}}$ increases, then both $\Delta U'_{11}$ and $\Delta U'_{10}$ decrease. Consequently, its value should be large enough only to ensure that $\Delta U'_{00}$ is eliminated while $\Delta U'_{11}$ and $\Delta U'_{10}$ are maintained. Changing $\varphi_{1\text{x}}$ adjusts the potential's tilt with respect to the φ_1 axis. If $\varphi_{1\text{x}}$ takes on too large of a value, then the barrier $\Delta U'_{01}$ will be undesirably eliminated. However, its value must be large enough to ensure that $\Delta U'_{00}$ is eliminated. Similarly, tuning $\varphi_{2\text{x}}$ changes the tilt of the potential with respect to the φ_2 axis. If $\varphi_{2\text{x}}$ is too large, then the blue (purple) stable (unstable) fixed points can annihilate, which causes information to be erased in the region where it should be preserved.

Obtaining effective circuit parameter ranges involves determining two particular values: (i) the value resulting in $\Delta U'_{01}$, $\Delta U'_{10}$, and $\Delta U'_{11}$ having the same height, and (ii) the value that results in one barrier falling below the proxy line. The first (second) criterion serves as the lower (upper) end of the range. Ultimately, there are clear trade-offs that depend on the value of a given circuit parameter. Finding the set of parameters permitting control over which information is erased and preserved requires a balancing act: A careful process of selecting parameter values that are large enough to erase the desired information but not so large that the information originally planned to be preserved ends up being erased.

For μ , since $\Delta U'_{11}$ is most susceptible to information leakage, its effective range corresponds to $[0.06, 0.09]$. Similarly, to maintain as large $\Delta U'_{11}$ and $\Delta U'_{10}$ as possible, the value of $\varphi_{2\text{xdc}}$ should also lie at the lower end of the range $[1.79, 1.88]$. Then, to aid the effect of μ and $\varphi_{2\text{xdc}}$ on the potential and to maintain $\Delta U'_{01}$, $\varphi_{1\text{x}}$ would ideally take on a value within the range of $[0.59, 0.65]$. At the same time, to strike a balance between the increase of $\Delta U'_{11}$ and the decrease of $\Delta U'_{10}$, $\varphi_{2\text{x}}$ ideally lies within the range $[0.1, 0.15]$. Within these ranges, a reliable CE can be performed.

B. Control erase parameter selection

We now detail which circuit parameters—including their respective signs and magnitudes—are deployed for any of the eight CE protocols of interest. By leveraging the relationship between the potential's dynamics and employing the CE notation introduced in Sec. III, all eight CE protocols in Fig. 8 can be implemented in a systematic way. The following explains this approach, summarizing the results in Table II.

To begin, define a sign-based Iverson bracket,

$$[[P]] := \begin{cases} > 0, & \text{if } [P] = 1, \\ < 0, & \text{if } [P] = 0. \end{cases} \quad (4)$$

Here, $[P]$ is the Iverson bracket of the statement P and $[P]$ evaluates to 1 if P is true or 0 if P is false. This notation is useful when discussing how the sign of a circuit parameter is determined. Let's now review the four parameters involved in each CE protocol:

- φ_{ixdc} lowers the barrier between specific pairs of states to be erased;
- φ_{jx} compensates for the unwanted effects of φ_{ixdc} ;
- μ biases the target erasure state to be more energetically favorable; and
- φ_{ix} compensates for the unwanted effects of μ .

For these parameters, $i, j \in \{1, 2\}$ with $i \neq j$. To determine which φ_{ixdc} to use for a given CE, recall that we specify a CE with three parameters: ρ , σ , and A . If $\rho = \times$ (\forall), then $i, j = 2, 1$ (1, 2). As seen from Eq. (3), φ_{ixdc} appears only in the cosine function: Since this function is even, the sign of φ_{ixdc} is not relevant. Recall from Secs. IV and V A that φ_{ixdc} lowers energy barriers on both sides of the i th axis. However, the CE requires one barrier to be maintained. Thus, we need a control parameter to offset this barrier drop so that it applies to only one half of the φ_1 - φ_2 plane, while maintaining the other barrier. The parameter deploying this barrier offset is φ_{jx} , and its sign is given by $[[\sigma \neq \rho]]$.

Next, μ biases the potential such that the minima along one of the diagonals of the φ_1 - φ_2 plane are more energetically favorable compared to those on the other diagonal. Its sign determines which well becomes the target for the erasure and is given by $[[[\sigma = \rho] \text{ XOR } A]]$. Since μ acts along the diagonals of the φ_1 - φ_2 plane, it causes asymmetry between two wells that are supposed to be storing information, resulting in unwanted information leakage. Fortunately, the parameter φ_{ix} can be used to compensate for this effect by tilting the potential to offset this unintentional information leakage. The sign of this parameter is found through $[[A]]$.

For all CEs of interest in Fig. 8, Table II compactly shows the signs of the relevant circuit parameters.

C. CE robustness

During our example CE in Fig. 5, once $\Delta U'_{00}$ vanishes, the information needs to propagate from the 00 state to the 01 state. The time this takes is denoted as t_{CE} ; it serves as a proxy for the CE timescale.

As this information is erased, other information is being stored in the 01, 10, and 11 states due to the barriers $\Delta U'_{01}$, $\Delta U'_{10}$, and $\Delta U'_{11}$ being maintained. However, we see in Fig. 5(b) that as a circuit parameter increases, at least one barrier's height decreases. The microstates stored in these decreasing barriers are most susceptible to fluctuating out of their respective memory states. Due to this, the timescale that characterizes how long these states reliably store information is in competition with t_{CE} . This type of timescale is known as a dwell time,^{16,18,39} which is denoted as t_d . Implicitly from Fig. 5(a), there are three dwell times that contribute to CE performance—those being the dwell times corresponding to the states

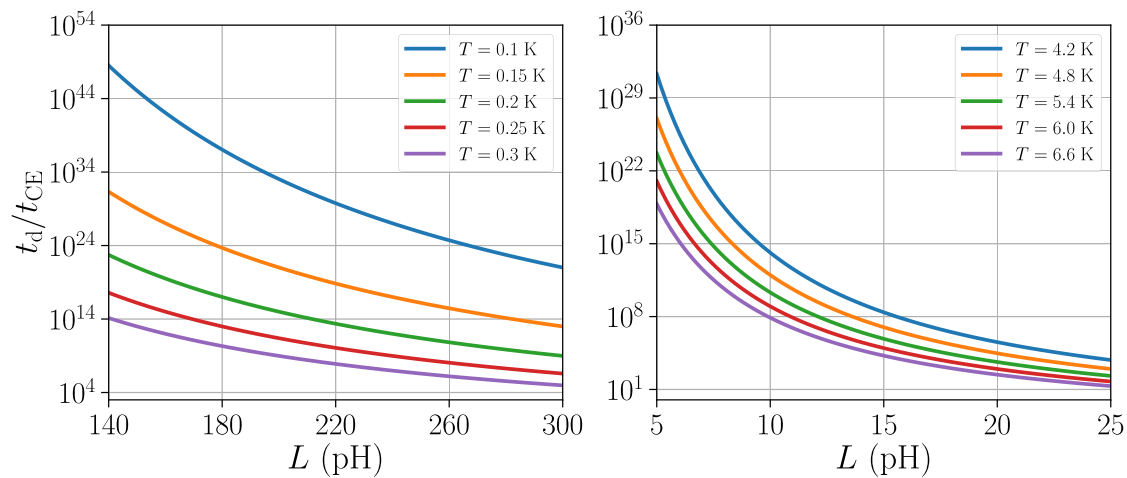


FIG. 6. The ratio t_d/t_{CE} characterizes the robustness of a particular device's construction as an order of magnitude estimate. (Left) MQP literature inductance values and temperatures.^{16–19,27,29,32,33,35,40} To demonstrate the behavior of the robustness at colder temperatures, the temperature range [100–300] mK is only displayed. Note that $R = 1 \Omega$, $C = 500$ fF, and $I_c = 5 \mu A$. (Right) QFP literature inductance and temperature values.^{4,31,37,38} Note that the values $5 \leq L \leq 10$ pH are exercised to demonstrate the performance of a QFP if obtainable, while typical QFP inductances are greater than or equal to 10 pH. For this figure, $R = 1 \Omega$, $C = 1$ pF, and $I_c = 25 \mu A$.

01, 10, and 11. The minimum of these three dwell times ultimately dictates CE failure.

If the length of time that information can be reliably stored is much longer than the timescale of a CE protocol, then the probability of an error resulting from an unwanted thermally activated transition is low. To quantify this, we take the ratio t_d/t_{CE} as a measure of robustness.

To calculate t_{CE} , we approximate the information in the 00 state as a single damped particle traveling down a quadratic potential from the point where the fixed points initially annihilate; the derivation is included in [Appendix A](#). For t_d , since there are three dwell times that affect CE performance, we choose the minimum of these dwell times to characterize CE robustness. This provides a more conservative estimate of a particular CE's performance; refer to [Appendix B](#) for details. Of particular relevance, t_d is exponentially proportional to $1/L$ and $1/T$; this has a dominant effect on the robustness t_d/t_{CE} . Studying the robustness as a function of L and T allows for interpreting the performance of a CE across the MQP and QFP literature.

From [Sec. V A](#), selecting parameter values at the lower end of the effective parameter range yields a more robust CE: We found that $\mu = 0.06$, $\varphi_{ixdc} = 1.79$, $\varphi_{jx} = 0.61$, and $\varphi_{ix} = 0.10$. These will be known as the *effective parameter values*. With these, [Fig. 6](#) displays an order of magnitude estimate of the CE robustness for different values of L and T . Since the MQP (QFP) literature employs SQUIDs for different purposes—thereby leading to differing ranges of L and T —we separate the possible value ranges into the left (right) figures. The relevant MQP literature^{16–19,27,29,32,33,35,40} corresponds to the left figure, which has a general temperature range of [100, 500] mK, while the inductance values range from [140, 300] pH. An upper value of $\mathcal{O}(10^{48})$ CEs per device is obtained with the inductance value of $L = 140$ pH found from Saira *et al.*²⁷ at $T = 100$ mK.

On the right—following the QFP literature^{4,31,37,38}—the operating temperatures are no colder than 4.2 K, in addition to $L \geq 10$ pH. To demonstrate robustness with a broader scope than constructed thus far, we use a range that begins at a theoretical value of $L = 5$ pH to obtain an upper value of $\mathcal{O}(10^{31})$ CEs per device at 4.2 K. For both areas of the literature, we identify that lower temperature and inductance values correspond to a greater expected number of successful CEs per device. The values of R , C , and I_c are chosen as typical values found in the respective literature studies. As a final point, note that from [Fig. 6](#) the ratio t_d/t_{CE} was calculated with the effective parameter values. We further assumed that the information traveling from the 00 state to the 01 state begins at the location determined from nonzero circuit parameters for the CE.

Now, suppose all circuit parameters were initialized to zero so that the potential matches [Fig. 1](#). Then, tune all circuit parameters infinitely fast to their respective final values. Due to this, the information stored in the 00 state is now traveling from the location determined by zero-valued circuit parameters, as opposed to the point of annihilation. This means that the information must now travel a greater distance to the 01 state, thereby resulting in a larger t_{CE} . Considering this scenario provides a more conservative estimate for the ratio t_d/t_{CE} . That said, we found that this larger t_{CE} will be no more than twice the value of the most conservative estimate of t_{CE} , leading to a reduction of the robustness of order one compared to that shown in [Fig. 6](#).

D. NAND gate application

Executing successive CE protocols allows for performing a NAND gate. The CE has two input bits and two output bits as seen from [Fig. 3](#), while the NAND gate has two inputs but only one output bit. When the number of logical output bits is less

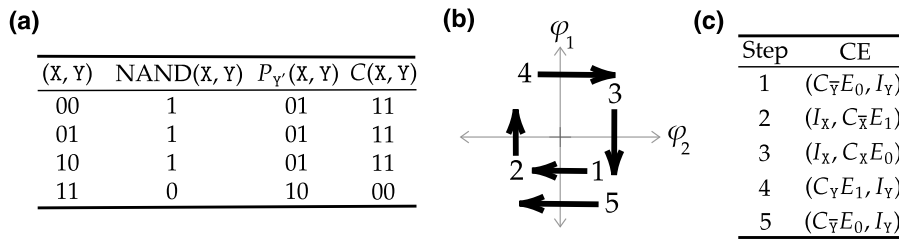


FIG. 7. NAND computations carried out on a coarse-grained potential of Fig. 1, which is reproducible by Eq. (3). (a) Tabulated computations of the NAND gate. Steps (1)–(3) execute the partial computation $P_Y(X, Y)$. Additionally, steps (1)–(5) accomplish the complete computation $C(X, Y)$. (b) Arrow-based schematic for performing partial and complete NAND gates. (c) Tabulated step numbers and CE protocols corresponding to Fig. (b).

than the number of embedded output bits in a computational system, there is added flexibility when choosing which bit to read as the output for a computation. For example, we can specify that $X' = \text{NAND}(X, Y)$ without prescribing the Y' computation. Thus, we define two kinds of NAND gates: a *partial* NAND, written as $P_{\rho'}(X, Y)$, which only requires the state ρ' to yield the desired output, and a *complete* NAND, denoted as $C(X, Y)$, which requires that $X' = Y' = \text{NAND}(X, Y)$. Figure 7(a) tabulates these choices.

From here, Fig. 7(b) illustrates both kinds of computations, and Fig. 7(c) tabulates the computations. Recall from Fig. 1 that the first, second, third, and fourth quadrants correspond to the memory states 11, 01, 00, and 10, respectively. In this example, carrying out only steps (1)–(3) executes the partial computation P_Y . This can be seen by tracking the arrows through the included protocol steps: In step (1), the information in state 10 is erased into the 00 state; in step (2), the combined information—comprising of the information from the initial 00 and 10 states—is erased into the 01 state; in step (3), the information in 11 state is translated into 10 state using the dynamics of the CE protocol. Note that in this step, there is no logical erasure since quadrant III was already vacated in step (1). At this point, the Y' output bit represents a NAND gate of X and Y . Continuing to track the arrows for steps (4)–(5) executes the computation C .

Partial NAND gates built from CEs require fewer successive CE protocol executions than complete NAND gates. However, performing complete NAND gates provides more redundancy regarding from which states the computations can be read.

VI. FABRICATION CONSIDERATIONS AND FUTURE WORK

Herein, we demonstrated that the circuit in Fig. 4 is sufficiently controllable to perform the universal 2-bit CE operation. To get here, we made a number of implicit assumptions in our analyses, along with the explicit assumptions laid out in Sec. IV. This leaves several important practical consideration unanswered when considering how this elementary logic gate is best incorporated into a fully fledged computational device. That said, our goal is to demonstrate a new approach to 2-bit universal computation by leveraging bifurcation theory and present an early proof of concept implementation that utilizes SQUIDs.

It is still worth noting, however, that the field of superconducting logic has been around for decades and so we can lean on practical scaling and fabrication advances already established in the field. For example, while we do not discuss how inputs are given to, or how outputs are read from, our device, we can infer from,

e.g., the QFP and AQFP literature that other SQUID circuits will serve as input currents and outputs will be read off by external SQUIDs.^{4,15,30,31,38} Similarly, we do not investigate scaling to many gates or methods for correcting errors that may arise when performing multiple operations sequentially. That being said, using SQUIDs for classical computation has shown promise for achieving larger scale computational capabilities. In Ref. 41, a microprocessor was constructed out of 21 460 Josephson junctions that can function as a full adder; error correction has also been addressed in the context of superconducting logic.⁴² However, these types of superconducting chips are not yet capable of surpassing modern day conventional computing capabilities, although they have been decades in the making.¹⁵ Finally, while we did give an estimate of how thermal noise will affect our device fidelity, we did not specify other kinds of noise or perform detailed analyses for how noise affects the device's dynamics. Again, we can turn to work like that found in Refs. 43–45 for these answers.

Future goals involve combining the insights gained from microscopic simulations of the phase-space dynamics, similar to that of Refs. 24 and 35, with device level SPICE simulations, further optimizing the CE within the possible SQUID logical design space.

VII. CONCLUSION

We presented the family of control erase (CE) protocols in Fig. 8 and introduced notation in Sec. III that allows them to be concisely enumerated. We introduced a device in Fig. 4 that performs CE protocols by tuning circuit parameter values to access the desired bifurcations. Characterizing a measure of a protocol's robustness involved associating a storage length time with the protocol's duration. We conducted an order of magnitude estimate of the robustness for an example CE protocol in Fig. 6, yielding a high robustness for protocols that employ realistic parameter values spanning different areas of superconducting circuit literature.

Section V B established a connection between the device's circuit parameters and the CE notation. Linking various CE protocols together by leveraging this relationship allowed for universal computations. Section V D demonstrated a NAND gate that employs only CEs. Due to its superconducting operation, the device can perform CE-based universal computations at extremely low energy cost. Keep in mind that any quadruple well potential that has sufficient enough control could implement a CE, but we choose this specific substrate in this work for, e.g., its potential energy-efficient properties. It is worth noting that the CE operation does theoretically support an adiabatic, or thermodynamically reversible, implementation. This implementation was ruled out for the circuit we

analyzed by control restrictions and parameter ranges. An intriguing avenue for further study is an adiabatic version of the CE and whether it can also be implemented in a superconducting substrate. In addition, there is added flexibility when performing NAND gates via the potential in Fig. 1. Partial computations permit fewer executions of erasure protocols, which implies that computations can be performed with even lower energetic costs. Conversely, executing complete computations gives rise to reading the same computation regardless of which axis is chosen to be the output, thereby providing an added layer of redundancy.

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AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

Author Contributions

Christian Z. Pratt: Conceptualization (equal); Data curation (equal); Formal analysis (equal); Investigation (equal); Methodology (equal); Software (equal); Validation (equal); Visualization (equal); Writing – original draft (equal); Writing – review & editing (equal). **Kyle J. Ray:** Conceptualization (equal); Data curation (equal); Formal analysis (equal); Investigation (equal); Methodology (equal); Software (equal); Validation (equal); Visualization (equal); Writing – original draft (equal); Writing – review & editing (equal). **James P. Crutchfield:** Conceptualization (equal); Formal analysis (equal); Funding acquisition (equal); Investigation (equal); Methodology (equal); Project administration (equal); Supervision (equal); Validation (equal); Visualization (equal); Writing – original draft (equal); Writing – review & editing (equal).

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

APPENDIX A: CONTROL ERASE TIMESCALE APPROXIMATION SCHEME

The following details an approximation scheme for the potential in Eq. (3) during the control erase (CE) protocol described in Sec. III. Specifically, to represent the distribution of microstates being erased into 01 state, we approximate this situation as a particle sliding down a quadratic slope. From this, we calculate t_{CE} —the time it takes for the particle to travel to the bottom of the slope.

TABLE I. Relevant circuit quantity scaling.

Circuit quantity	$z'(z_c)$ Identifications
m	$m'(C)$
γ	$\gamma'(1/R)$
ϕ	$\varphi(\phi_c)$
U	$U'(\phi_c^2/L)$
t	$t'(\sqrt{LC})$

First, note that in Fig. 3, the coordinate ϕ_1 has negligible change in comparison with the change in ϕ_2 . With this in mind, we will consider the potential to be dependent only on ϕ_2 . Next, the height of the potential U that the particle travels down is on the order of $U_0 \sim 10^{-22}$. Essentially, the particle's motion can be described in terms of ϕ_2 without the loss of generality. Then, there are two forces acting on the particle: (i) the force due to the potential $-dU/d\phi_2$ and (ii) the classical damping force $-\gamma d\phi_2/dt$. This means that the particle's motion is described by Newtonian mechanics due to the influence of a dimension-full potential U and damping coefficient γ , written as

$$\frac{d^2\phi_2}{dt^2} + \frac{\gamma}{m} \frac{d\phi_2}{dt} + \frac{1}{m} \frac{dU}{d\phi_2} = 0. \quad (\text{A1})$$

Observe that Eq. (3) is dimensionless, while Eq. (A1) describes a particle's motion under the influence of a potential with units of energy. To reconcile this, we must rewrite Eq. (A1) in terms of dimensionless quantities. Reference 35 detailed a strategy for converting dimension-full equations of motion—such as Eq. (A1)—into dimensionless equations of motion. To do this, we write a dimensional quantity z as $z = z'z_c$ in which z' is the dimensionless representation of the quantity, while z_c represents a dimensional scaling factor. Table I summarizes the circuit quantity scaling parameters z_c .

Now, after appropriately making substitutions and further simplifying, we write the dimensionless Eq. (A1) as

$$\frac{d^2\varphi_2}{dt'^2} + \Lambda \frac{d\varphi_2}{dt'} + \theta \frac{dU'}{d\varphi_2} = 0, \quad (\text{A2})$$

where $\Lambda = \gamma'\sqrt{LC}/m'RC$ and $\theta = 1/m'$. The approximation scheme of the potential will now be detailed. First, we write the dimension-full potential as $U(\phi_2) = k\phi_2^2/2$, where k serves as the spring constant of the dimension-full potential. The goal is to write the potential in the dimensionless form: $U'(\varphi_2) = k'\varphi_2^2/2$, with k' being the spring constant of the dimensionless potential. This can be done by setting $k_c = U_c/2\phi_c^2$, in order to obtain $k' = U'/(k_c\varphi_2^2)$. Now, the particle's motion is written as

$$\frac{d^2\varphi_2}{dt'^2} + 2\lambda \frac{d\varphi_2}{dt'} + \omega^2\varphi_2 = 0, \quad (\text{A3})$$

which is analogous to the differential equation modeling a damped harmonic oscillator that oscillates at frequency $\omega^2 = k'\theta$ under damping coefficient $\lambda = \Lambda/2$. We deploy the ansatz: $\varphi_2(t') = Ae^{\alpha t'}$ in which $\alpha = -\lambda \pm \sqrt{\lambda^2 - \omega^2} = -\lambda \pm \Omega$. We will focus on two possible situations, which involve $\Omega^2 > 0$ or $\Omega^2 < 0$. Subsequently, these will be categorized as *overdamped* and *underdamped*, respectively.

1. Overdamped

When $\Omega^2 > 0$, the solution to Eq. (A3) is⁴⁶

$$\varphi_2(t') = A \exp(-(\lambda - \Omega)t') + B \exp(-(\lambda + \Omega)t'), \quad (\text{A4})$$

which describes an overdamped oscillator with initial conditions A and B . To understand them, we first detail the consequences of the particle-like representation of the distribution of microstates. The average position of this distribution localizes to a position at any given time—represented by a particle in this case—while its average initial velocity will be zero. With this, the initial conditions are (i) $\varphi_2(t' = 0) = \varphi_2^o$ and (ii) $d\varphi_2(t' = 0)/dt' = 0$. Solving for these two initial conditions, and substituting the results back into Eq. (A4), gives

$$\varphi_2(t') = \frac{\varphi_2^o}{\Omega} (\lambda + \Omega) e^{-\lambda t'} \sinh(\Omega t') + \varphi_2^o e^{-(\lambda + \Omega)t'}. \quad (\text{A5})$$

Numerically solving Eq. (A5) for a final time $t' = t'_f$ and multiplying the result by \sqrt{LC} yield $t_{\text{CE}} = t'_f \sqrt{LC}$.

2. Underdamped

If $\Omega^2 < 0$, we must define $\tilde{\omega} = \sqrt{\omega^2 - \lambda^2}$ in order for the general solution to be written as⁴⁶

$$\varphi_2(t') = D \exp(-\lambda t') \cos(\tilde{\omega} t' + \theta). \quad (\text{A6})$$

Equation (A6) describes an underdamped harmonic oscillator for which the coefficient D and phase θ are solved using initial conditions. Subsequently, solving for them in the same manner as before and substituting the results into Eq. (A6) produce

$$\varphi_2(t') = \varphi_2^o \sqrt{1 + \left(\frac{\lambda}{\tilde{\omega}}\right)^2} \exp(-\lambda t') \cos(\tilde{\omega} t' + \Theta),$$

for which $\Theta = \arctan(\lambda/\tilde{\omega})$.

APPENDIX B: DWELL TIME

The escape rate^{27,47,48} in the $l = 1, 2$ direction is

$$\Gamma_l = \frac{\omega_{p,l}}{2\pi} \exp\left(-\frac{\Delta U_b}{k_B T}\right). \quad (\text{B1})$$

First, $\omega_{p,l}$ is the plasma frequency in the l th flux direction. It serves as the characteristic frequency of oscillations that are parallel to the escape direction, i.e., how frequently the particle approaches the barrier. To find it, we consider the dimension-full potential $U(\phi_1, \phi_2)$ and identify that we can perform a Taylor expansion in the l th coordinate around a minimum ($\phi_1 = \phi_1^*, \phi_2 = \phi_2^*$). Of particular interest, and up to a constant, we look to the following second-order terms of the potential:

$$U(\phi_1, \phi_2) \approx \frac{1}{2} \frac{\partial^2 U}{\partial \phi_1^2} \Big|_{(\phi_1^*, \phi_2^*)} (\phi_1 - \phi_1^*)^2, \quad (\text{B2})$$

as well as

$$U(\phi_1, \phi_2) \approx \frac{1}{2} \frac{\partial^2 U}{\partial \phi_2^2} \Big|_{(\phi_1^*, \phi_2^*)} (\phi_2 - \phi_2^*)^2. \quad (\text{B3})$$

We identify the second partial derivative taken with respect to ϕ_l evaluated at the minimum to be the spring constant k_l . From here, we take the corresponding plasma frequency to be $\omega_{p,l} = \sqrt{k_l/m}$ for which the dimension-full mass $m = C$.

Furthermore, ΔU_b indicates the barrier height between a local minimum and a local maximum, k_B is the Boltzmann constant, and T is the circuit's operating temperature. The escape rate is exponentially damped by the energy barrier because the thermal environment guarantees particles are exponentially unlikely to have energies that exceed the thermal energy scale. Γ_l characterizes how many escape events are expected out of the minima per second. Finally, the dwell time is the reciprocal of Eq. (B1): $t_{d,l} = 1/\Gamma_l$. Explicitly, the plasma frequencies of interest for the dimensionless barriers $\Delta U'_{01}$ ($\Delta U'_{11}$ and $\Delta U'_{10}$) correspond to the flux direction

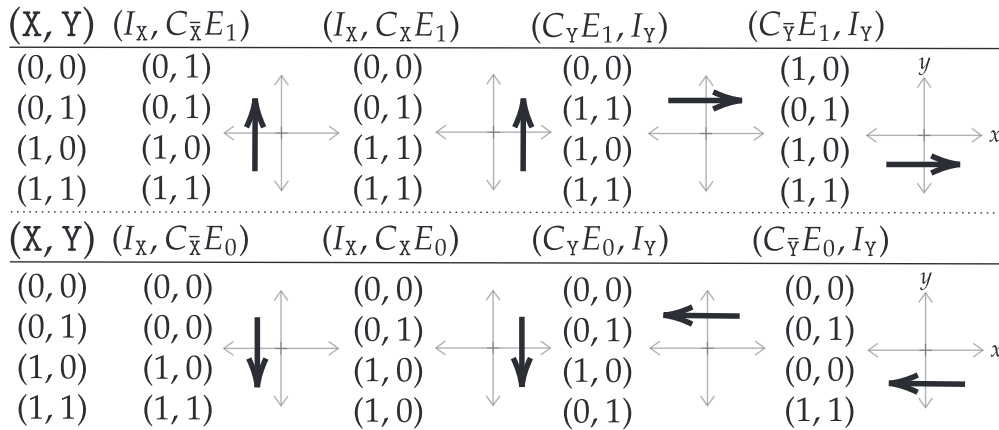


FIG. 8. All control erasure protocols of interest here, displayed with arrow-based notation first shown in Fig. 3.

TABLE II. Tabulated relationships between experimental circuit parameters—including their indices and signs—and the CE notation introduced in Sec. III. + (−) corresponds to a positive (negative) sign of a particular circuit parameter.

	$(I_x, C_{\bar{x}}E_1)$	(I_x, C_xE_1)	$(C_{\bar{y}}E_1, I_y)$	$(C_{\bar{y}}E_1, I_y)$	$(I_x, C_{\bar{x}}E_0)$	(I_x, C_xE_0)	$(C_{\bar{y}}E_0, I_y)$	$(C_{\bar{y}}E_0, I_y)$
i	2	2	1	1	2	2	1	1
j	1	1	2	2	1	1	2	2
$\text{sgn}(\varphi_{1x})$	+	−	+	+	+	−	−	−
$\text{sgn}(\varphi_{2x})$	+	+	−	+	−	−	−	+
$\text{sgn}(\mu)$	+	−	−	+	−	+	+	−

$l = 1$ ($l = 2$). We utilize the minimum dwell time to calculate the robustness t_d/t_{CE} .

APPENDIX C: CONTROL ERASURES OF INTEREST

Figure 8 exhibits all control erasure protocols of interest. Appropriate successive executions of a subset of these protocols lead to performing a NAND gate. Note that this is not an exhaustive illustration of possible control erasure protocols but only represents those of current interest. Table II shows the indices, signs, and relationships of the relevant circuit parameters for a particular CE. The nonzero barrier-control parameter is determined by i . Meanwhile, the magnitudes of the tilt parameters that offset the bias and barrier changes to the potential are related by $|\varphi_{jx}| > |\varphi_{ix}|$, respectively. By using the effective magnitudes of the circuit parameters detailed in Sec. V C and successively executing effective CE protocols, a robust NAND gate can be performed.

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