

FIR manual

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Overview

1.1 Functional Features

- 1) Data bit width configurable
- 2) pipeline input/output
- 3) All data output precision
- 4) Filter order number can be configured
- 5) Filter coefficients can be dynamic configuration
- 6) Support filter coefficients pre-storage

Module principle

FIR Principle:

$$y[k] = \sum_{n=0}^{N-1} a[n]x(k-n), k = 0,1,...,N-1$$

The user can choose the implementation architecture according to whether the filter coefficients are symmetric or not. FIR with symmetric coefficients can save half of the multipliers and lower output delay.

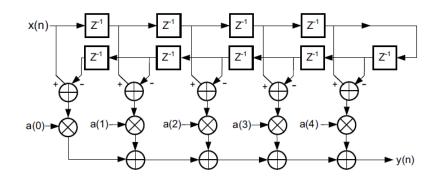


Figure 1 1 coefficient of symmetric structure (10)

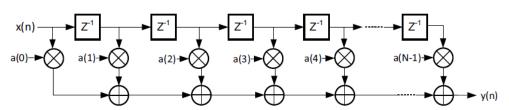


Figure 2 2Coefficient asymmetric architecture (nth-order)

Parameters are defined

Table 1 Definition of parameters 1

Parameter names	Default	Instructions	
SPEED_FAST	1	Depending on the fir clock frequency setting, this	
		value can be set to 1 when the timing is tight.	
		1-multiply-accumulate is completed in two beats	
		O- Multiply and accumulate in one beat	
DATA_IN_WIDTH	16	Data input bit width	
DATA_OUT_WIDTH	16 + 16 + 2	Data output bit width,	
		Calculation method:	
		DATA_IN_WIDTH + COE_WIDTH + ceil(log2(COE_TAPS))	
COE_WIDTH	16	Filter coefficient bit width	
COE_TAPS	3	Filter order	
COE_SYMMETRY	0	Whether the filter coefficients are symmetrical or	
		not, FIR with symmetrical coefficient structure can	
		save half of the multipliers and lower output	
		delay.	
		1- Symmetrical structure	
		0- Asymmetric structures	
COE_LOCAL_NUM	2	Number of filter coefficient prememory banks	
COE_SEL_WIDTH	2	Choose the bit width for the filter coefficient	
		bank	
		Calculation:	
		ceil(log2(COE_LOCAL_NUM + 1))	
COE_FILE	{16'd11, 16'd12,	Filter coefficient prestored values, format:	
	16'd13, 16'd21,	{index0_1, index0_2,, index0_COE_TAPS,	
	16'd22, 16'd33}	<pre>index1_1, index1_2, , index1_COE_TAPS,</pre>	
		}	

Interface definition

Table 2 Interface Signal Definition2

Signal Name	Directi	Clock	Description
	ons	domain	
clk	Input		Master clock
rst_n	Input	clk	Reset signal
coe_sel_vld_i	Input	clk	Filter coefficient selection enabled.
coe_sel_index_i[COE_SEL_W	Input	clk	Filter coefficients select index.
IDTH-1:0]			Choose a value of 0 - (COE_LOCAL_NUM-1), which
			corresponds to the prestored coefficients.
			Choose the value COE_LOCAL_NUM, which
			corresponds to the dynamic configuration
			factor.
			Other values, invalid
coe_reload_vld_i	Input	clk	Filter coefficients dynamic configuration
			enabled
coe_reload_data_i[COE_WID	Input	clk	滤波器系数动态数据,滤波器系数需要以流的形式
TH-1:0]			持续输入 COE_TAPS 个数据。
data_vld_i	The	clk	Data input can make
	input		
data_i[DATA_IN_WIDTH-1:0]	Input	clk	Data entry

data_vld_o	Output	clk	Filtered data output enabled
data_o[DATA_IN_WIDTH-1:0]	The	clk	Filtered data output
	output		

Interface timing

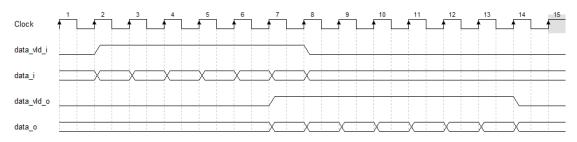


FIG. 3 3Data input and output timing

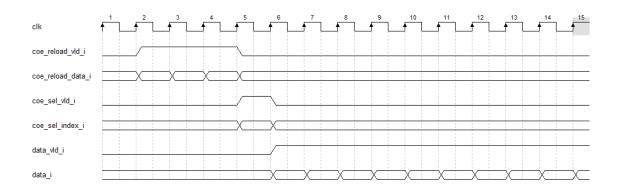


Figure 4 4dynamic configuration and coefficient of gravity separation sequence Note 1: When reselection of filter coefficients is performed

0 ≤ coe_sel_index_i < COE_LOCAL_NUM	The group of prestored coefficients	
U ≪ COE_SET_INDEX_I \ COE_EOCAL_NUM	for the index value	
and all index i == COE LOCAL NUM	Corresponding to dynamically	
<pre>coe_sel_index_i == COE_LOCAL_NUM</pre>	configured coefficient groups	
coe_sel_index_i == others	Invalid	

Note 2: the filter coefficients re-election, need to make sure that FIR module for data processing, otherwise the output data is wrong. (because the filter coefficients are changed in the process of calculation)