FFT Manual

File update records

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Overview

1.1 Functional Features

1) Support data bit width up to 16bit

2) fft/ifft transform types are supported

3) Support 4-16384 transform points

4) Support dynamic configuration transformation points, transformation type

5) Support pipeline input/output

6) Module internal each level of butterfly operation cut one bit

7) Support fixed point only

8) Only reverse output is supported

9) Support overflow prevention processing

Module principle

Principle of FFT:

$X[k] = \sum_{n=0}^{N-1} x[n] W_N^{nk}, k = 0,1,\ldots,N-1,$ where$W_N^{nk} = e^{-j\frac{2\pi}{N}nk}$

The FFT module uses SDF (serial delay feedback) architecture to realize pipeline control, and the butterfly operation uses cordic algorithm to complete the rotation.

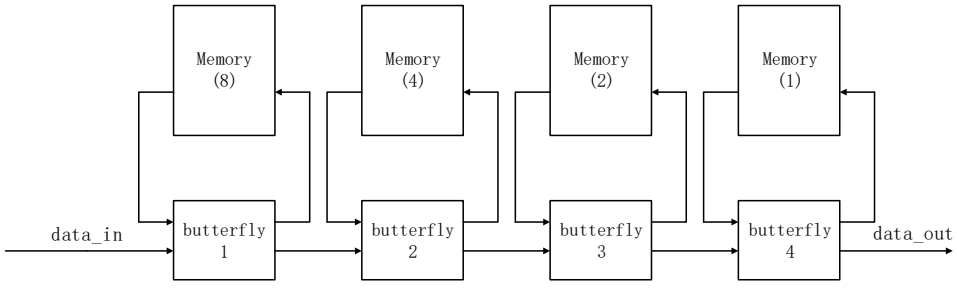

FIG. 1 SDF data architecture (16 points)

The following figure shows the data structure diagram of the 16-point FFT:

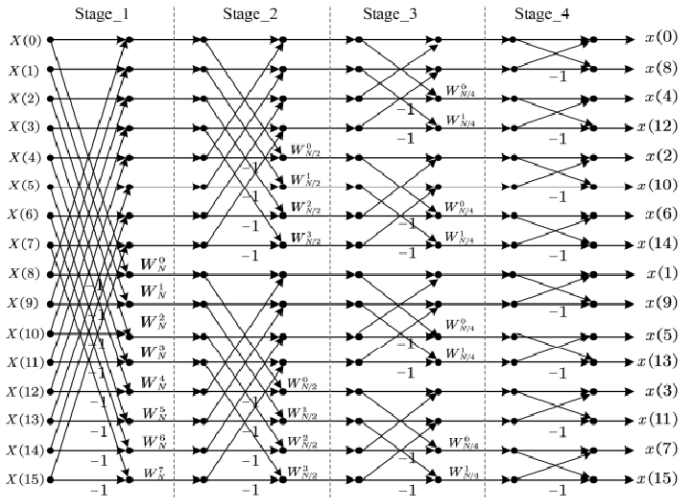

Figure 2 16-point 2FFT data structure

Taking the 16-point FFT as an example, the first level 0 data and 8 data realize the butterfly shape, so 8 data are stored. The calculation method is shown in Figure 3. FIG. 3 3Part A is completely input (0~7). When input 8, and 0 data are calculated to produce 0 and 8 of the second level. At this time, 0 is directly sent to the next stage, and 8 is fed back to the input buffer. When all is finished, 0 ~ 7 to 8 to 15 data output. Then different levels are calculated from this.

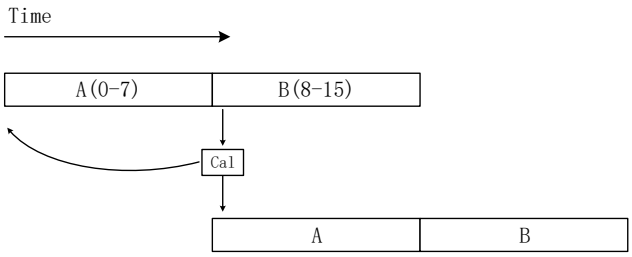

FIG. 3 3Principle of single-level control of SDF architecture

Parameter Definition

Table 1 Definition of parameters1

Parameter names	Default	Instructions
DATA_WIDTH	16	Data bit width, maximum support 16 bits
RAM_RD_LATENCY	2	RAM read latency, the user configures the value according to their RAM
FFT_IFFT	0	Default transformation type 0-fft 1-ifft
MAX_STAGE	12	The biggest change points, support 4-16384 points

		Calculation method MAX_STAGE = log2(N), where N is the maximum number of transformation points That is, MAX_STAGE ranges from 2-14
OVERFLOW_PRO	1	Anti-overflow treatment 0- Do no overflow handling 1- Do no overflow handling If the modulus of the input IQ data is less than or equal to 2^(DATA_WIDTH-1), you can set this value to 0, then the scaling factor is N, and the quantization signal to noise is better. If the modulus of the input IQ data is greater than 2^(DATA_WIDTH-1), the value **must be** set to 1 to prevent data overflow after butterfly operation. At this time, the input data is shifted one bit to the right inside the module, the scaling factor is changed to 2*N, and the quantization signal-to-noise ratio (SNR) has about 6dB loss.

Interface Definition

Table 2 Interface Signal Definition2

Signal Name	direction	Clock domain	Description
clk	Input	--	Master clock All signals are sampled at the rising edge of this signal
rst_n	Input	clk	Reset signal Effective level: low;
cfg_vld	Enter	clk	Dynamic update transformation type, transformation points enable. Note: After dynamically updating the transformation type and transformation points, it is necessary to wait for sig_start_receive_ready_o signal to be high before entering new data. Valid level: high level;
cfg_fft_ifft	Input	clk	Transformation type 0-fft 1-ifft
cfg_N [3:0]	The input	clk	Change points, support 4-16384 points, this value can not be set greater than the maximum number of points due to MAX_STAGE pair The calculation method is cfg_N = log2(N), where N is the maximum number of transformation points That is, the cfg_N range is 2-MAX_STAGE
sig_start_receive_ready_o	The output	clk	数据帧头输入指示使能，在动态更改变换类型、变换点数后，需要等待该信号拉高才能输入新数据
sig_start_i	Input	clk	Data frame header Input indication to indicate the beginning of a frame of data
sig_vld_i	Input	clk	Data entry enabled
sig_real_i[x:0]	Input	clk	Real part data input
sig_imag_i[x:0]	Input	clk	The imaginary part of the data input
sig_start_o	Output	clk	Transform dataframe header output instructions
sig_vld_o	Output	clk	Transform data output enabled

sig_real_o[x:0]	Output	clk	Transform the real part of the data output
sig_imag_o[x:0]	Output	clk	Transform data imaginary part output
N_index_o[x:0]	Output	clk	Transform the data corresponding to the serial number indication, output in reverse order

Interface timing

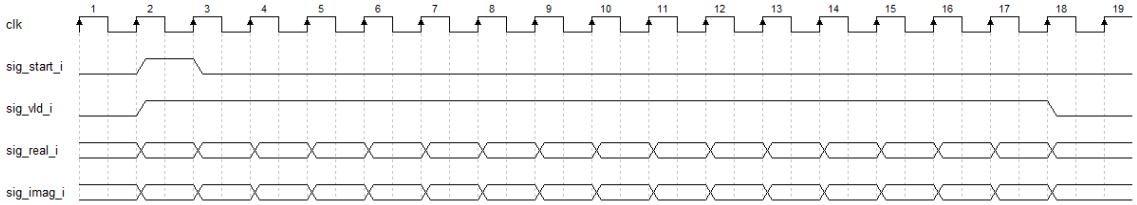

Figure 4 4Data entry timing (16 points)

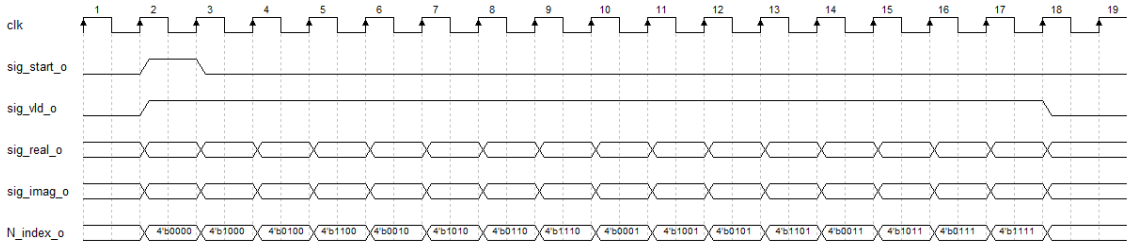

Figure 5 5Data output time series (16 points)

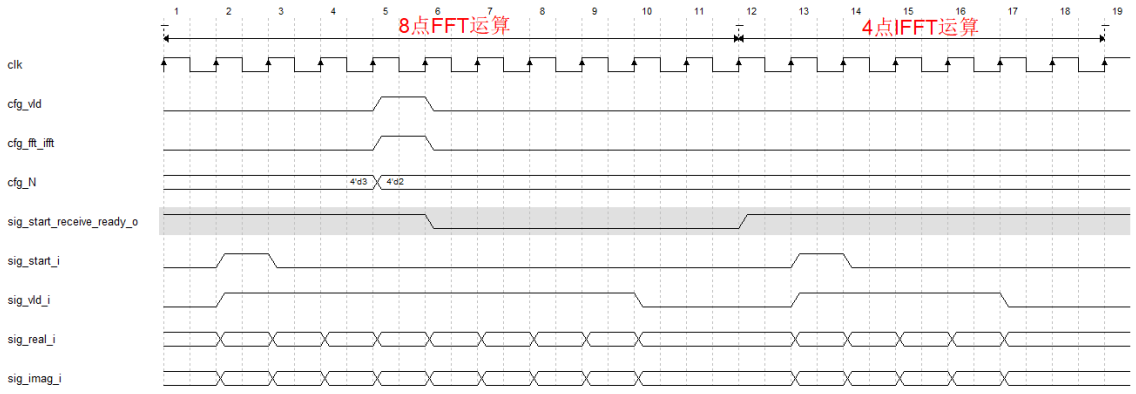

Figure 6 6Dynamic configuration timing

Note: After dynamic configuration change points, change type. It is necessary to wait for the sig_start_receive_ready_o signal to be raised before entering new data packets.

Take Figure 6 as an example, if the dynamic configuration is carried out during the 8-point FFT conversion (change to 4-point, IFFT), the 8-

point FFT operation will continue, and the sig_start_receive_ready_o signal will be set as high inside the module after the operation is completed. Figure 6 6At this time, the 4-point IFFT data can be input.