Supplementary Material

1 Proof of Theorem 5.1

We give the detailed definition of the transformation from $\overline{\text{AD}}$ to $\overline{\text{MWIS}}$ by replacing directed edges E_I with undirected edges $E_{I\to C}$.

Predicate 1.1 (R)**.** *$R(n_i, n_j)$ denotes if n_j is reachable from n_i by E_I. An inductive definition of predicate R is as follows,*

1. $\forall n_i \in N, R(n_i, n_i)$.
2. $\forall n_i, n_j, n_k \in N,\ R(n_i, n_j) \wedge \langle n_j, n_k\rangle \in E_I \to R(n_i, n_k)$

Predicate R is reflexive and transitive by its definition. That is, $\forall n_i, n_j, n_k \in N$ it must satisfy:

- **Reflexivity**: $R(n_i, n_i)$, i.e., every node is reachable from itself.
- **Transitivity**: if $R(n_i, n_j) \wedge R(n_j, n_k)$, then $R(n_i, n_k)$.

Definition 1.1 (T)**.** *$T : G_{\overline{AD}} \to G_{\overline{MWIS}}$, denoting the transformation from $G_{\overline{AD}} = (N, E_I, E_C)$ to $G_{\overline{MWIS}} = (N, \varnothing, E_C \cup E_{I\to C})$ by replacing directed edges E_I with undirected edges $E_{I\to C}$. Specifically, $\forall n_{a_s}, n_{a_t}, n_{b_s}, n_{b_t} \in N$, s.t. $(n_{a_t}, n_{b_t}) \in E_C \wedge R(n_{a_s}, n_{a_t}) \wedge R(n_{b_s}, n_{b_t}), (n_{a_s}, n_{b_s}) \in E_{I\to C}$.*

Then Theorem VI.1 can also be defined as follows.

Theorem. *Assuming the optimal solution of $\overline{AD}$ in $G_{\overline{AD}}$ is $N'_{\overline{AD}}$, and the one of $\overline{MWIS}$ in $G_{\overline{MWIS}} = T(G_{\overline{AD}})$ is $N'_{\overline{MWIS}}$, $N'_{\overline{AD}} = N'_{\overline{MWIS}}$.*

The proof of the Theorem is given as follows.

Proof.

1) First, we prove $N'_{\overline{\text{AD}}}$ is also an independent set of $G_{\overline{\text{MWIS}}}$. $\forall n_i, n_j \in N'_{\overline{\text{AD}}}$,
   a) According to the definition of $\overline{\text{AD}}$, as $n_i, n_j \in N'_{\overline{\text{AD}}}$, we have $(n_i, n_j) \notin E_C$.
   b) Assume $(n_i, n_j) \in E_{I\to C}$. According to the definition of T, $\exists n_{a_t}, n_{b_t}$, s.t. $(n_{a_t}, n_{b_t}) \in E_C \wedge R(n_i, n_{a_t}) \wedge R(n_j, n_{b_t})$.
   As $n_i \in N'_{\overline{\text{AD}}}$ and $R(n_i, n_{a_t})$, n_{a_t} must be in $N'_{\overline{\text{AD}}}$. Similarly, n_{b_t} is also in $N'_{\overline{\text{AD}}}$.
   Thus, both n_{a_t} and n_{b_t} are in $N'_{\overline{\text{AD}}}$. We can have $(n_{a_t}, n_{b_t}) \notin E_C$. Contradiction.
   Therefore, $(n_i, n_j) \notin E_{I\to C}$
   c) According to a) and b), $\forall n_i, n_j \in N'_{\overline{\text{AD}}}$, $(n_i, n_j) \notin E_C$ and $(n_i, n_j) \notin E_{I\to C}$. Thus, $N'_{\overline{\text{AD}}}$ is also an independent set of $G_{\overline{\text{MWIS}}}$.
2) Second, we prove $N'_{\overline{\text{MWIS}}}$ is also a solution of $\overline{\text{AD}}$ in $G_{\overline{\text{AD}}}$.
   a) $\forall n_i, n_j \in N'_{\overline{\text{MWIS}}}$, according to the definition of $\overline{\text{MWIS}}$, $(n_i, n_j) \notin E_C$.
   b) $\forall n_i \in N'_{\overline{\text{MWIS}}}$, we are going to prove that $\forall n_j \in N$ s.t. $\langle n_i, n_j\rangle \in E_I$, $n_j \in N'_{\overline{\text{MWIS}}}$ by contradiction. We assume $\exists n_j$ s.t. $\langle n_i, n_j\rangle \in E_I$ and $n_j \notin N'_{\overline{\text{MWIS}}}$.

i) $\forall n_k$ s.t. $(n_j, n_k) \in E_C$, as $R(n_i, n_j)$ and $R(n_k, n_k)$, according to the definition of T, we can have $(n_i, n_k) \in E_{I \to C}$. Thus, $n_k \notin N'_{\overline{\text{MWIS}}}$.

ii) $\forall n_k$ s.t. $(n_j, n_k) \in E_{I \to C}$, according to the definition of T, $\exists n_{j_t}, n_{k_t} \in N$, s.t. $(n_{j_t}, n_{k_t}) \in E_C \wedge R(n_j, n_{j_t}) \wedge R(n_k, n_{k_t})$. As $R(n_i, n_j) \wedge R(n_j, n_{j_t})$, we can also have $R(n_i, n_{j_t})$ (i.e., transitivity of R), which implies $\exists n_{j_t}, n_{k_t} \in N$, s.t. $(n_{j_t}, n_{k_t}) \in E_C \wedge R(n_i, n_{j_t}) \wedge R(n_k, n_{k_t})$. Thus, $(n_i, n_k) \in E_{I \to C}$ by the definition of T, and $n_k \notin N'_{\overline{\text{MWIS}}}$.

Therefore, $\forall n_k$ s.t. $(n_j, n_k) \in E_C \cup E_{I \to C}, n_k \notin N'_{\overline{\text{MWIS}}}$. $N''_{\overline{\text{MWIS}}} = N'_{\overline{\text{MWIS}}} + \{n_j\}$ is also an independent set.

As $w : N \to \mathbb{R}_{\geq 0}$, $w(N''_{\overline{\text{MWIS}}}) \geq w(N'_{\overline{\text{MWIS}}})$, $N'_{\overline{\text{MWIS}}}$ is not guaranteed to be the optimal solution. Contradiction.

Therefore, $\forall n_i \in N'_{\overline{\text{MWIS}}}$, if $\langle n_i, n_j \rangle \in E_I$, we must have $n_j \in N'_{\overline{\text{MWIS}}}$.

c) According to a) and b) and the definition of $\overline{\text{AD}}$, $N'_{\overline{\text{MWIS}}}$ is also a solution of $\overline{\text{AD}}$ in $G_{\overline{\text{AD}}}$.

3) According to 1) and 2), we can have $N'_{\text{AD}} = N'_{\overline{\text{MWIS}}}$.

□

2 Granularity of Data Inlining and Instruction Set Interleaving

The binaries in SPEC-Inter contain coarse-grained ARM/Thumb interleaving. In our evaluation, we do not introduce more fine-grained ARM/Thumb interleavings (e.g., within functions) considering the following reasons.

First, in stripped binaries, function entries are unknown such that our disassembler and the baselines have to deal with the code blob as a whole.

Second, instruction mode changes happening at function calls are similar to those within functions and do not degrade the difficulty for disassembly. As described in Section 2.2 in the paper, the instruction mode can be changed by some branch instructions, e.g., blx. Unlike the call instruction in x86/x64, there is no specific function call instruction in ARM binariesA function call in ARM is also considered as a branch, using the `bl`/`blx` instruction. Thus, the mode changes at different positions are similar. Note that the ARM/Thumb interleaving shown in the motivation example (Figure 1 in the paper) is a tail call instead of being in the middle of a function.

In addition, we build SPEC-Inter by compiling different files/modules with different instruction sets, which is a common process when building real ARM applications. Crafting binaries with a lot of ARM/Thumb interleavings within functions can be achieved at the assembly code level, but hard at the compilation level.

As for SPEC-Data, we do not embed data into the middle of functions. However, we do this for the obfuscation dataset.

3 Failure Rate of P-Disasm and Spedi

As discussed in Section 3.2 in the paper, P-Disasm is based on an assumption that the occluded instruction sequences tend to quickly converge on true instructions. However, this is only true for x86/x64 binaries. For ARM binaries, as there are two instruction sets, the occlusion of instruction sets exists in the entire code sections. Without the help of the converged instructions, there is no local propagation within the occlusion space, and the propagation algorithm becomes quite slow and consumes a huge amount of memory. As shown in Table 1, P-Disasm terminates for more than half of binaries on all datasets due to memory explosion.

Spedi also has issues with disassembling large binaries, especially the complex obfuscated binaries. Note that Spedi only supports Thumb instructions and are only evaluated on binaries compiled with Thumb instructions, i.e., the half of SPEC-Basic, SPEC-Data, and the binaries built with obfuscation.

Table 1: Failure Rate (%) for P-Disasm and Spedi

Dataset		P-Disasm	Spedi
Basic	SPEC2000	54.58	5.42
	SPEC2006	57.29	13.33
Data	SPEC2000	51.67	9.58
	SPEC2006	58.54	12.92
Inter	SPEC2000	60.63	N/A
	SPEC2006	65.83	N/A
$r = 0$	SPEC2000	57.08	77.50
	SPEC2006	60.67	72.27
$r = 50$	SPEC2000	64.58	84.17
	SPEC2006	63.60	81.51
$r = 100$	SPEC2000	75.83	89.17
	SPEC2006	67.36	81.51

4 More Details of Efficiency

XDA. Although XDA is quick in disassembly, it requires additional time for model training.In our evaluation, the XDA model trained on SPEC CPU2006 takes 21 hours for pretraining and 15.6 hours for finetuning, following the default settings of 10 epochs and 30 epochs, respectively.

D-ARM. Figure 1 plots the relation between the time cost of D-ARM and the binary sizes (on the AOSP dataset). The relation tends to be linear, which implies that D-ARM can scale gracefully in practice.

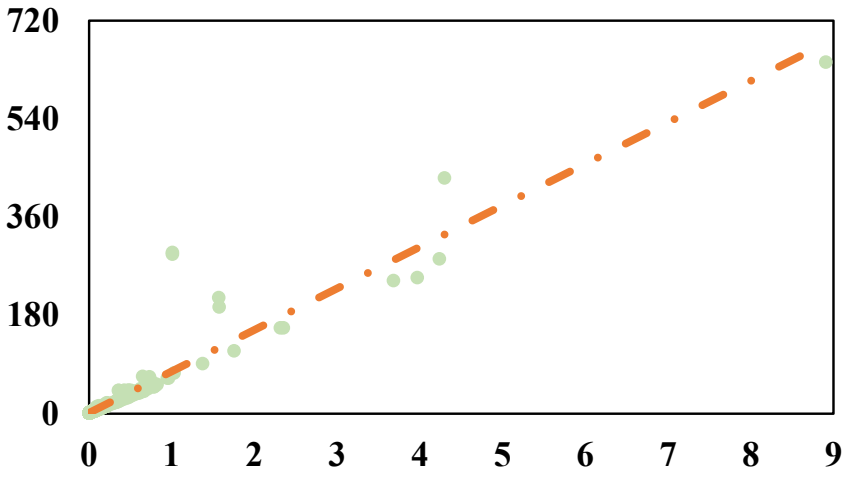

Figure 1: Time cost (Y-axis, seconds) taken by D-ARM exhibits a linear complexity in binary size (X-axis, MB).