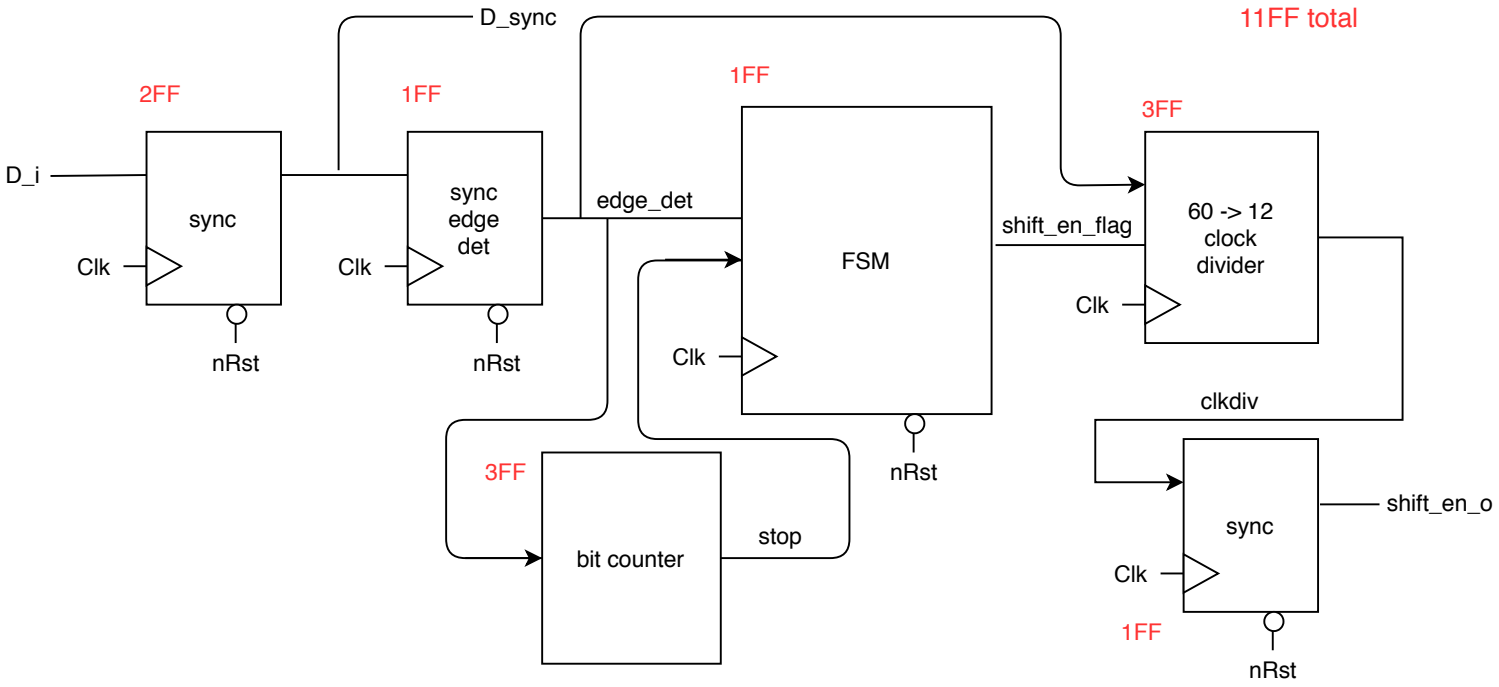
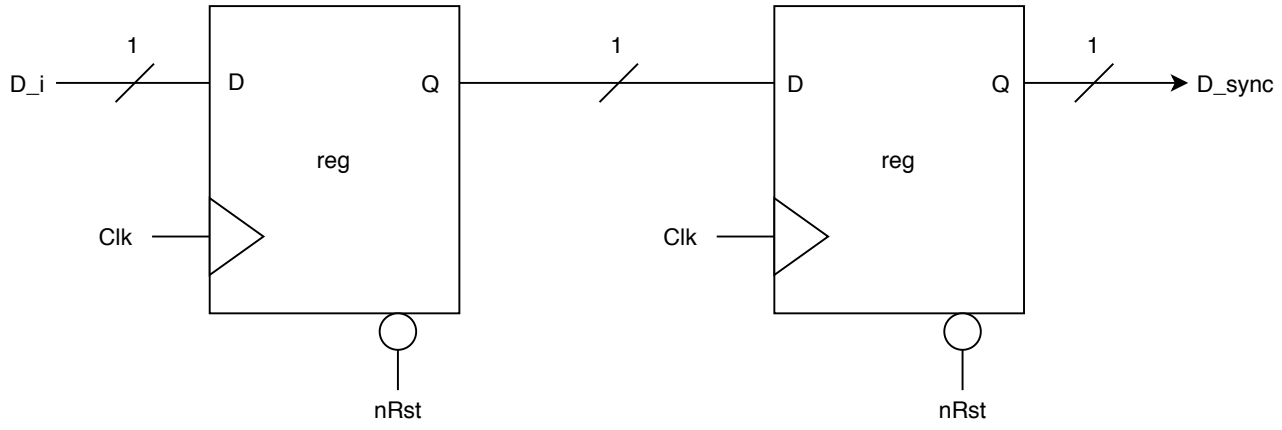
**ECE337 hw-1**
**Name: Ti-Wei Chen**
**mg account: mg35**
**Date: 09/11/2020**
**Collaborator: None**

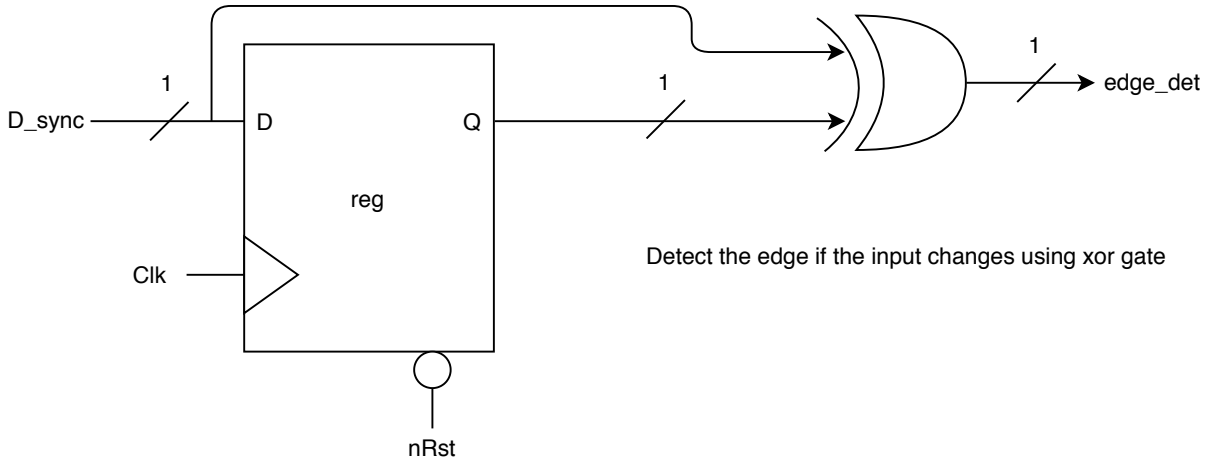
## Top Level Diagram for Timing Recover Circuit




## Sync

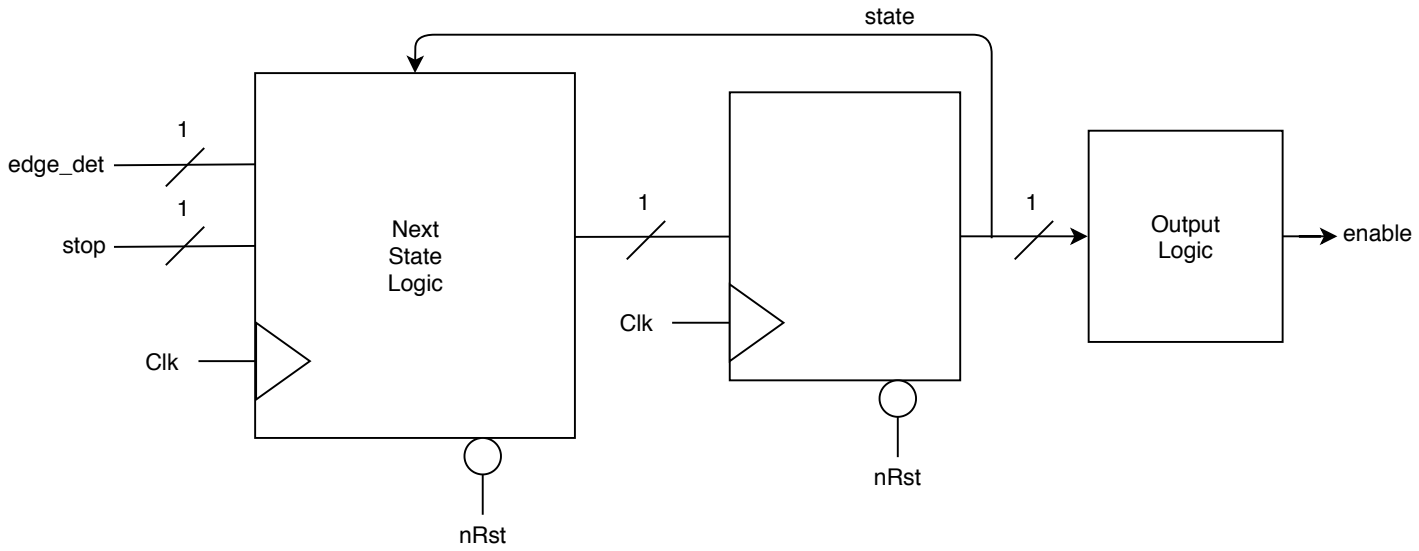



## Sync Edge Detector

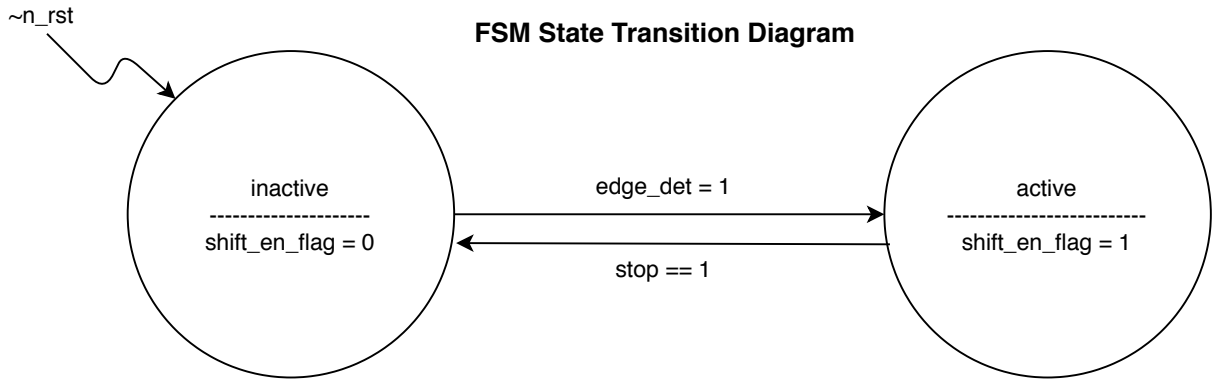



Detect the edge if the input changes using xor gate

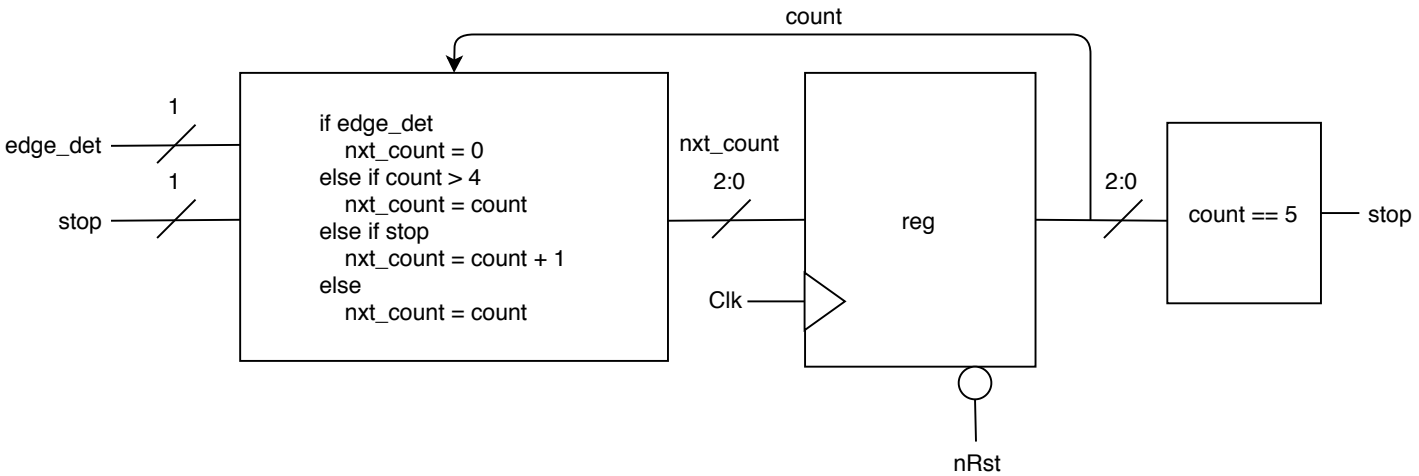
**FSM**




**FSM State Transition Diagram**

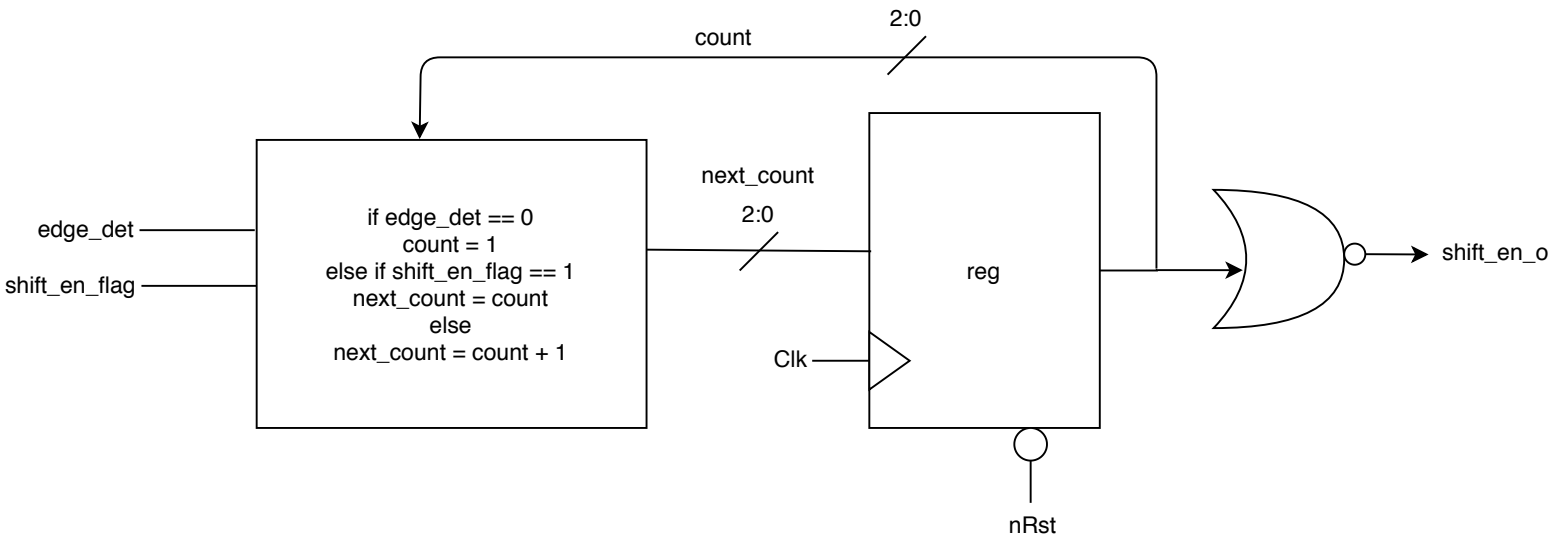



**Counter**




When count = 5 bits period, stop = 1. There's no next count, the count updates on inputs clock period.

**60 -> 12 Clock Divider**




60MHz to 12 MHz. Count to 5 every clock cycle while the flag == 1, then generate pulse when count == 0.