Laboratory 1, Total Points: 30

Due Date: January 22, 2019 (Tuesday), 11:59 PM CST

In this lab, we will review the basic building blocks of digital systems and VHDL programming.
Textbook Sections: Digital Design and Computer Architecture: **2.1- 2.5, 2.7, 4.1-4.3**
Students may refer the above-mentioned textbook sections and Quartus tutorial to complete the lab exercises.

Exercises

1. (7 pts) A digital circuit has four inputs and two outputs. The inputs $A_{3:0}$ represent a number from 0 to 15. Output P should be TRUE if the number is prime (0 and 1) are not prime, but 2, 3, 5, and so on, are prime). Output D should be TRUE if the number is divisible by 2. Give Boolean equations for Output P and D using the truth table, sketch the digital circuit, implement the circuit as a VHDL module and simulate it. Submit the truth table, circuit diagrams for P and D, VHDL code, and simulation graph in your report. Also, upload your VHDL file in Blackboard.

2. (7 pts) A priority encoder has 2^N inputs. It produces an N-bit binary output indicating the most significant bit of the input that is TRUE, or 0 if none of the inputs are TRUE. It also produces an output NONE that is TRUE if none of the inputs are TRUE. Design an eight-input priority encoder with inputs $A_{7:0}$ and outputs $Y_{2:0}$ and NONE. For example, if the input is 00101000, the output Y should be 101 and NONE should be 0. Give a Boolean equation for each output, and sketch a schematic. For example, if the input is 00101000, the output Y should be 101 and NONE should be 0. Submit the truth table, circuit diagrams for Y and NONE, VHDL code, and simulation graph in your report. Also, upload your VHDL file in Blackboard.

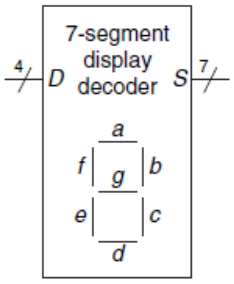

Figure 1: Seven-segment display

3. (8 pts) A hexadecimal seven-segment display decoder takes a 4-bit data input $D_{3:0}$ and produces seven outputs to control light-emitting diodes to display the hexadecimal digits A, B, C, D, E, and F as well as 0–9. The seven outputs are often called segments **a** through **g**, or S_a–S_g, as defined in Figure 1. Write a truth table for the outputs and find Boolean equations for them. Write a VHDL module for the display decoder. Submit the truth table, circuit diagrams for S_a and S_b, VHDL code, and simulation graph in your report. Also, upload your VHDL file in Blackboard.

4. (8 pts) Multiplexers (**mux**) are commonly used combinational circuits. They choose an output from among several possible inputs based on the value of a select (control) signal. Figure 2 shows the schematic of 2:1 mux with two data inputs D_0 and D_1, a select input S, and one output Y. The multiplexer chooses between the two data inputs based on the select: if S = 0, Y =D_0, and if S = 1, Y =D_1. Implement a VHDL module mux2_1 for 2:1 multiplexer. Then, implement a structure VHDL module mux4_1 using mux2_1 module. Finally, implement a structure VHDL module mux8_1 using mux4_1 and mux2_1 modules. Submit the block diagram for mux8_1, VHDL code for mux2_1, mux4_1, and mux8_1, and simulation graph in your report. Also, upload your VHDL files in Blackboard.

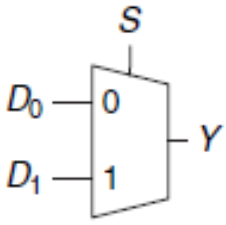

Figure 2: 2:1 Multiplexer