Dustin James Kendall

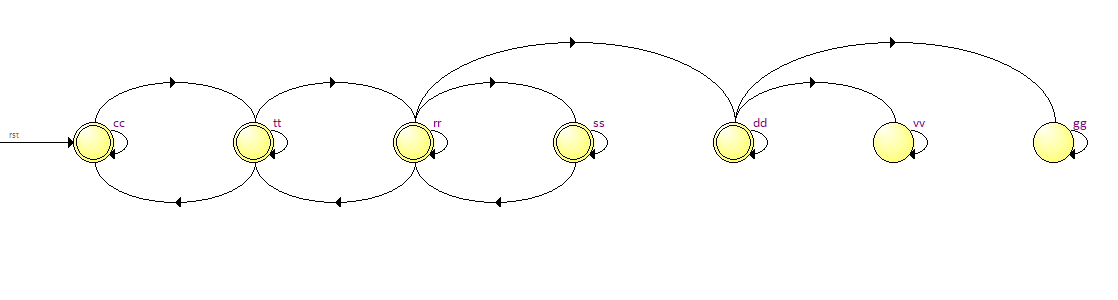
kendalld@pnw.edu

Lab 4 FSM

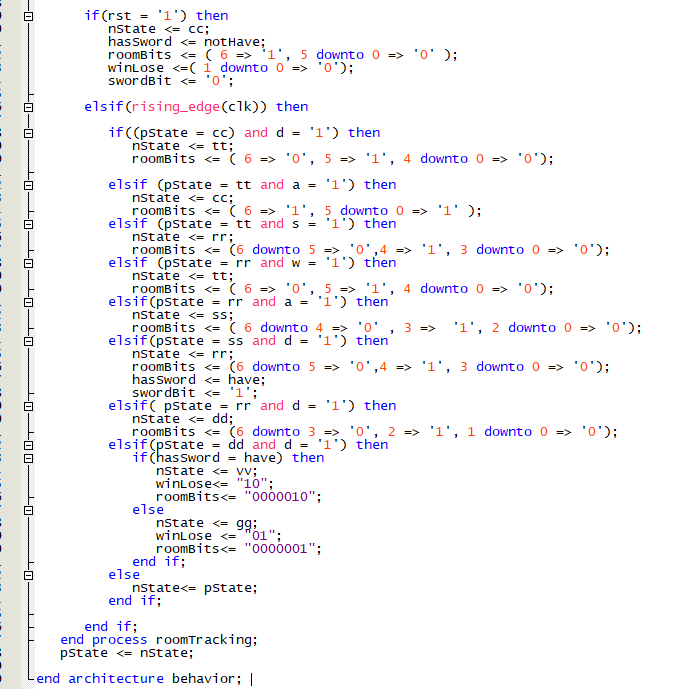
ECE 371 Comp Organization

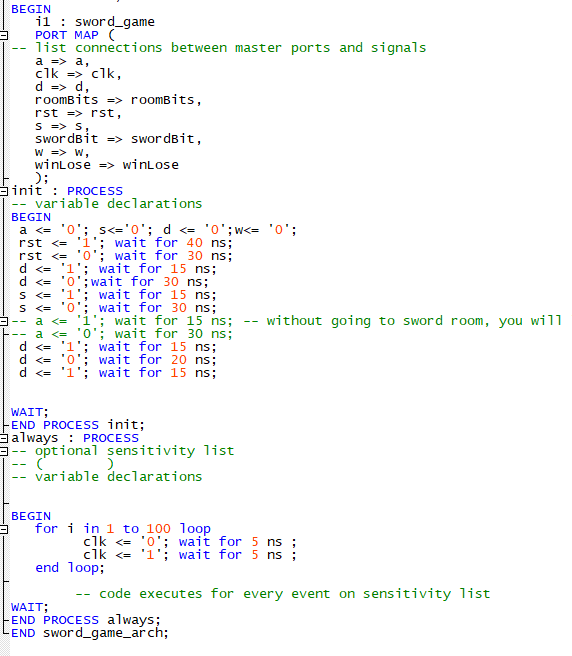
# Part 1

## State Transition Diagrams



## VHDL Code





## Simulation Results

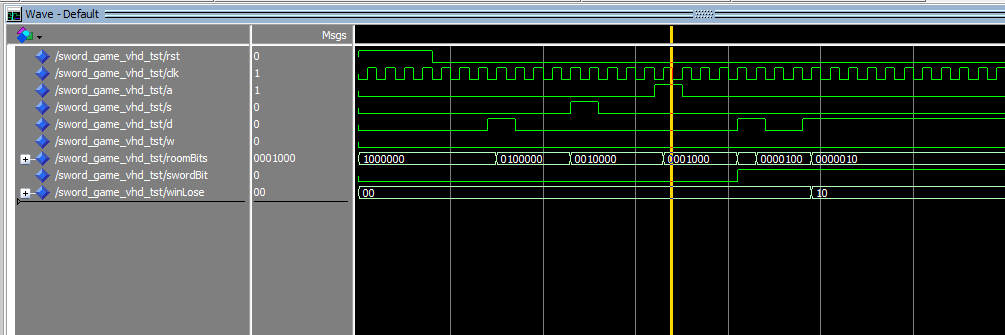


Figure 1 Winning Sim

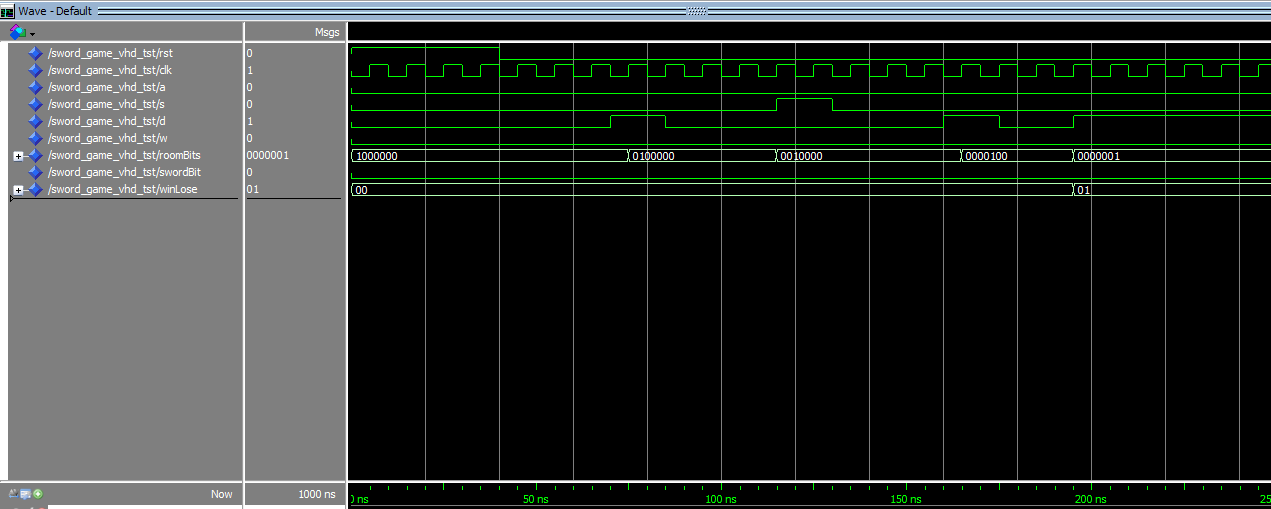
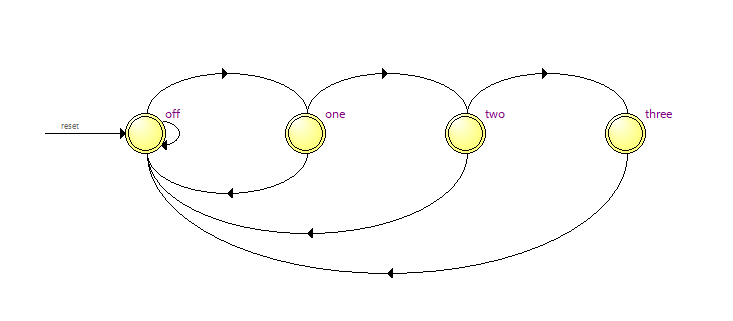
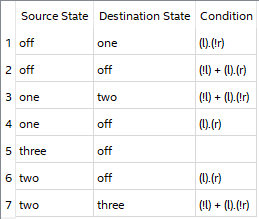


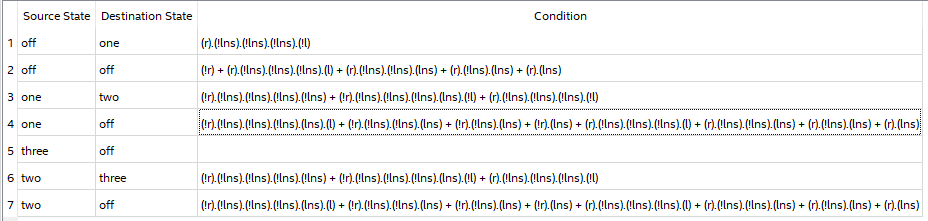
Figure 2 Losing Simulation

# Part 2

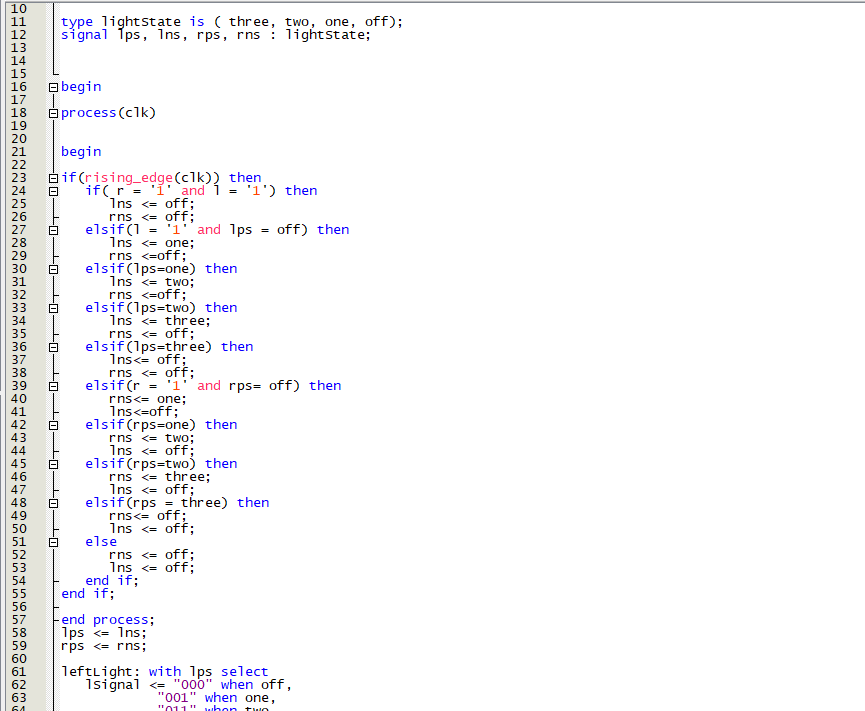
## State Transition Diagrams

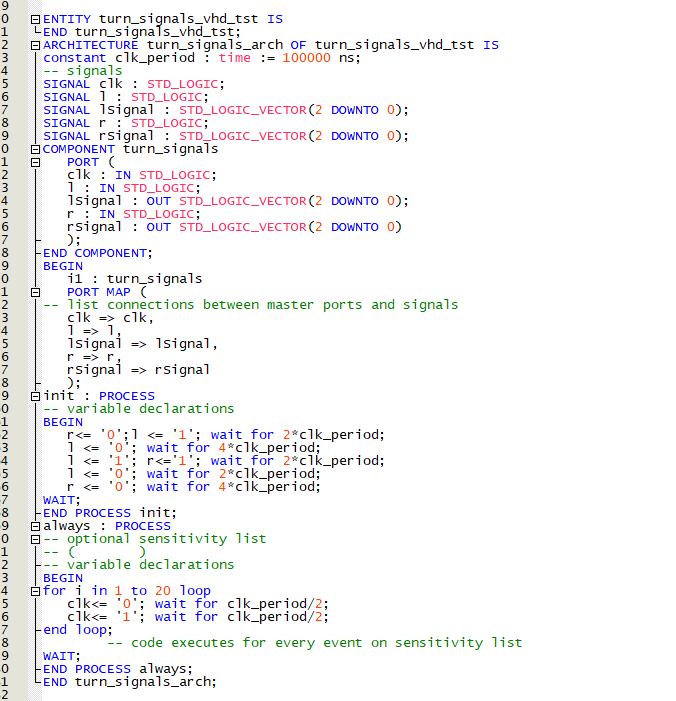






## VHDL Code





## Simulation Results

