LV600 User's Manual

Authors:
Alfred Norman Gifford IV
Daniel Khoury

Project Advisor:
Ken Stevens

University of Utah

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1 Introduction and Motivation

At the University of Utah, students enrolled in Digital VLSI Design (CS/ECE 5710/6710) work in teams to design an integrated circuit (IC) for their final project. Optionally, students may send their chip designs to MOSIS, an IC foundry, for fabrication. As per MOSIS's rules, students who fabricate their chip designs are required to test their received chips and report their results back to MOSIS.

At least one student from any team that chooses to fabricate their chip must enroll in CS/ECE 6712, which teaches students how to test their chips using a device called an application-specific integrated circuit (ASIC) tester. Presently, the University of Utah has two ASIC testers: a Verigy 93000 and a Tektronix LV500. As of this writing, both machines are in troubled states. The Verigy 93000 is no longer operational due to a hard drive failure. The LV500 has many failed sectors, so the system as a whole may prove unreliable when testing a chip.

Simply purchasing a new ASIC tester is not feasible. ASIC testers are extremely expensive machines (millions to billions of dollars) – partly because of a niche market, but mainly because they are incredibly difficult systems to engineer, construct, and maintain.

Our project, which we term the LV600, is an ASIC tester based largely upon the LV500. The project's intention is to provide an ASIC tester that is good enough for most student-designed VLSI chips. This document serves as both the final report for our project and the user's manual for the system that we hope to ultimately provide to the University.

In this document, we also include ideas for how to build upon our project, and we strongly encourage students to consider building an ASIC tester for their senior project if they have any interest in such machines. The project provides so many learning experiences – it's conceptually simple, but the devil lies in the details.

2 Overview of ASIC Testers

All ASIC testers build upon the same simple idea:

1. The user specifies what outputs to expect from their chip in response to what inputs.
2. The system applies the user-specified inputs to the device under test (DUT) and later samples the outputs of the DUT.
3. The machine reports how the sampled outputs compare to the outputs expected by the user.

In this section, we provide an abstracted overview of how the Tektronix LV500 implements the above steps. Although we are not familiar with the implementation of other ASIC testers, like the Verigy 93000, we believe that an understanding the LV500's implementation does well to sprout relatable ideas.

NOTE: More detailed information about the LV500's physical implementation can be found here. We chose to abstract away some of the details in these slides that we deemed irrelevant for this section.

2.1 Step 1: User Specifications

TODO: Norm, Daniel

2.2 Step 2: Testing

TODO: Norm, Daniel

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TODO: Norm, Daniel

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TODO: Norm, Daniel

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TODO: Norm

4.2 Numato Saturn FPGA Development Board

TODO: Daniel

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TODO: Norm, Daniel

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TODO: Norm, Daniel

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TODO: Norm (web server code), Daniel (C code)

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TODO: Daniel

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TODO: Norm, Daniel

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TODO: Norm, Daniel

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TODO: Norm, Daniel

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TODO: Norm, Daniel

9 Special Thanks

We are sincerely grateful to the following people:

- Ken Stevens, our Master's project advisor, for providing us with proper guidance throughout this project.
- Erik Brunvand, our senior project advisor, for providing us with FPGA boards for prototyping and the ZIF socket we used for our DUT board.
- Michelle Gifford, Norm's wife, for helping to create the housing for our project.
- Advanced Circuits, our go-to PCB manufacturer, for offering student prices that cannot be found anywhere else.
- Our families, who put up with our absences and will need to get to know us again.

10 Contact Information

Feel free to email us any questions/comments regarding our project, ASIC testers in general, or your own ASIC tester project.

Alfred "Norm" Gifford: agiffiv@gmail.com
Daniel Khoury: d.khoury@outlook.com

11 References