**DUT Board Schematic**

**I/O PINS:**

* **128** for the ZIF socket (bidirectional)
* **2** for the counter ICs (inputs to ICs, outputs from FPGA)
* **1** for the voltage translator ICs (inputs to ICs, output from FPGA)
* **3** for the SRAM ICs (inputs to ICs, outputs from FPGA)
* **5** for the output buffers (4 inputs to IC, 1 output from IC, 4 outputs from FPGA, 1 input to FPGA)
* **3** for power pins
  + Ground (global)
  + 3.3V volts powers the four counter ICs, the eight SRAM ICs, the 16 output buffer ICs, and the VL input to the 16 voltage translator ICs
  + A configurable VCC pin is needed for the VCC input to the 16 voltage translator ICs
* Total number of pins: **142**
* Pins provided by FPGA for DUT board: **139** 
  + Pins provided by FPGA for main board: **7**
    - **2** needed for RX/TX signals
    - **5** for template registers
* Note that the BeagleBone Black, not the FPGA board, will be controlling the power circuitry

**COMPONENTS (BOTTOM OF THE BOARD):**

* **BOTTOM HEADER BANK**
  + Components:
    - Eight of Adafruit’s extra tall, SMD 2x20 female headers
      * https://www.adafruit.com/products/2714
  + Placement:
    - Each side of the board will house two headers
      * Any unused pins tied to ground
      * Total of 160 pins
  + Connectivity:
    - Outputs are connected directly to the top header bank (see below)
  + Purpose:
    - These headers connect to the main PCB on one end and the other header bank on top of the DUT board
* OUTPUT BUFFER BANK
  + Components:
    - Eight parallel-in, serial-out shift registers (daisy-chained)
  + Placement:
    - Two on each side of the board (arranged within the bottom header bank)
  + Connectivity:
    - Four control pins are provided by the FPGA via the bottom header bank
    - One output pin (serial output) is routed to the FPGA via the bottom header bank
    - The data pins are tied to the output of the voltage translators and the SRAM data lines
      * Note that the shift register is opaque except when reading from the SRAM blocks
  + Purpose:
    - After the test vectors have all been launched, the output vectors are split amongst eight SRAM blocks. In order to read data from the SRAM blocks into the FPGA, the FPGA will reset the counter, disable the voltage translators, set the SRAM to read mode, and fetch the SRAM contents into these output buffers so that the FPGA can read in the data serially and transmit it to the BeagleBone Black
* SRAM BANK
  + Components:
    - Eight 16-channel parallel SRAM blocks
  + Placement:
    - Two on each side of the board (near the edge)
  + Connectivity:
    - ~CS, ~OE, and ~WE lines provided by FPGA via bottom header bank
    - Data lines are outputs of voltage translators, inputs into output buffers
    - Address lines are provided by counter ICs
  + Purpose:
    - The SRAM blocks store DUT outputs that can be read later
* VOLTAGE TRANSLATOR BANK
  + Components:
    - 16 high-to-low voltage translators
  + Placement:
    - Two next to each SRAM IC
  + Connectivity:
    - Inputs tied to DUT
    - Outputs tied to both output buffer and SRAM ICs
  + Purpose:
    - Translates any high-voltage DUT outputs into 3.3V for the output buffer and SRAM blocks
  + **IMPORTANT:** These must be disabled when reading from SRAM

**COMPONENTS (TOP OF THE BOARD):**

* TOP HEADER BANK
  + Components:
    - 16 headers (same headers as the bottom header bank)
    - Unlike the bottom header bank, two header positions are required for each pin; 1 Ohm resistors are used to bridge two header positions
  + Placement:
    - Four headers on each side
  + Connectivity:
    - On one side is the DUT, on the other side is the input to the voltage translators
  + Purpose:
    - Used to bridge connections between the DUT and the rest of the circuit board
* COUNTER BANK
  + Components:
    - Four counter ICs, all of them configured to operate identically
      * Rationale: Having four ICs splits the load capacitance of the SRAM blocks
  + Placement:
    - One in each corner
  + Connectivity:
    - Two pins tied directly to the FPGA via the bottom header bank
    - Each counter IC controls the address pins of two SRAM blocks on the other side of the board
  + Purpose:
    - These counters are used when writing to and reading from the SRAM blocks

**PROTOCOL**

[TODO, e.g. what is the state when the board is first connected and the system is powered up, how do things go; be specific!]