PROGRAMMABLE GAIN AMPLIFIER DESIGN

Design of a High-Impedance Microphone Pre-Amplifier using Sky130A Technology

Dr. Phillip Allen
Prof. Emeritus, ECE, Georgia Tech

Version 240809

Specifications

High-Impedance Microphone Pre-Amplifier Specifications

Description

Instrumentation amplifier, especially for use as a microphone pre-amplifier.

Parameter	Min	Typical	Max	Unit	Notes
Operating Temperature	-40	25	85	°C	
Input Impedance		10		MΩ	High-Z for microphone sensitivity
Open loop Gain	18		78	dB	Adjustable for different use cases
Frequency Response	20		50000	Hz	Audible range and machine monitoring
Equivalent Input Noise		10	20	nV/√Hz	At 1kHz
Total Harmonic Distortion		0.05	0.1	%	At 1kHz and nominal level
Output Voltage Swing	350		avdd - 350	mV	At 1 kOhms load
Output Voltage Swing	150		avdd - 150	mV	At 10 kOhms load
Current Consumption (Enabled)		25	60	uA	Minimize for battery-powered devices
Current Consumption (Disabled)		1	10	nA	
CMRR (Common Mode Rejection Ratio)	65	75		dB	Important for differential inputs
PSRR (Power Supply Rejection Ratio)	65	75		dB	Ensures stability with power supply fluctuations
Input common-mode range	(avdd / 2) - 0.5	avdd / 2	(avdd / 2) + 0.5	V	Set by internal bias circuit
Input range	1		1000	uV	No clipping/distortion at min and max gain
Input-referred offset	-1		1	mV	
Output load resistance	1			kOhms	
Slew rate		±1		V/us	

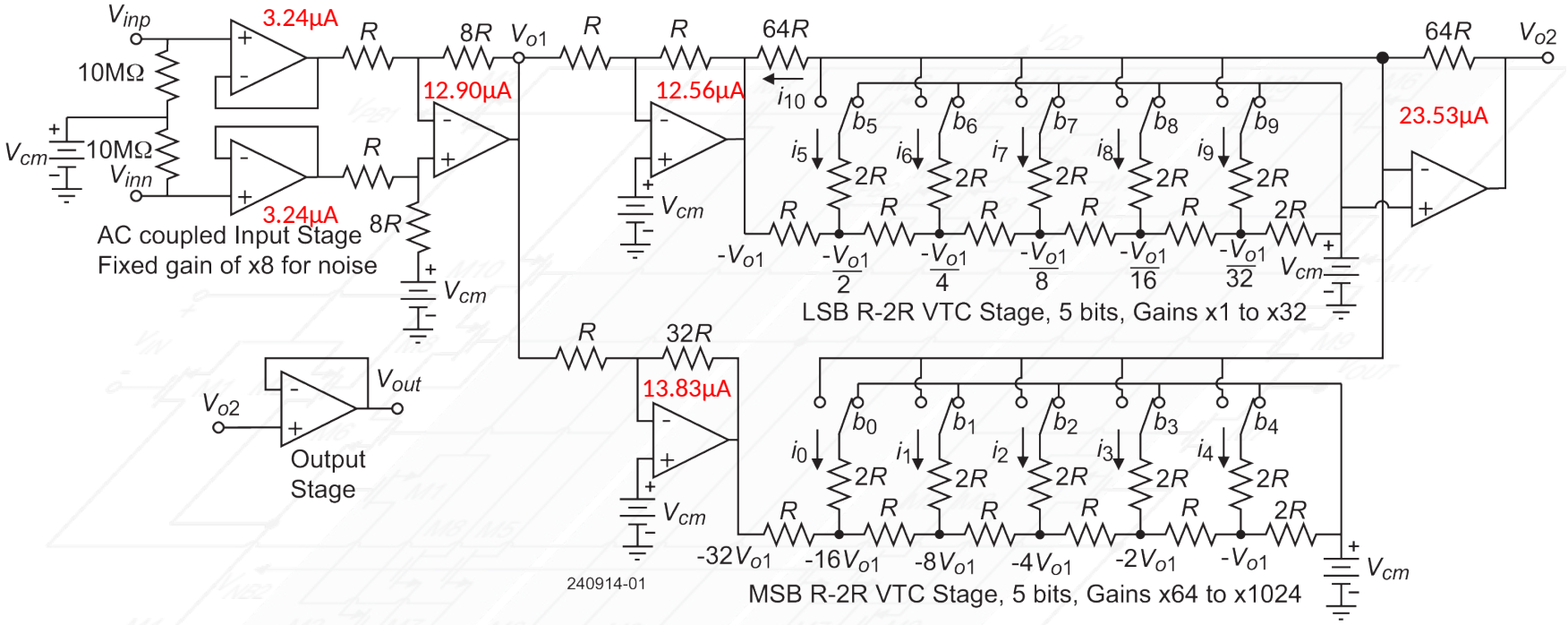
Input is AC coupled with the coupling capacitor off-chip. The biasing for the common-mode voltage is part of the amplifier circuit.

Note: 78dB is ~8192x gain; this implies a two-stage architecture. This should be implemented as two programmable gain stages, the first one gain 4 to 128 (5 bits selection) and the second one gain 2 to 64 (5 bits selection).

Overview of R-2R PGA Architecture

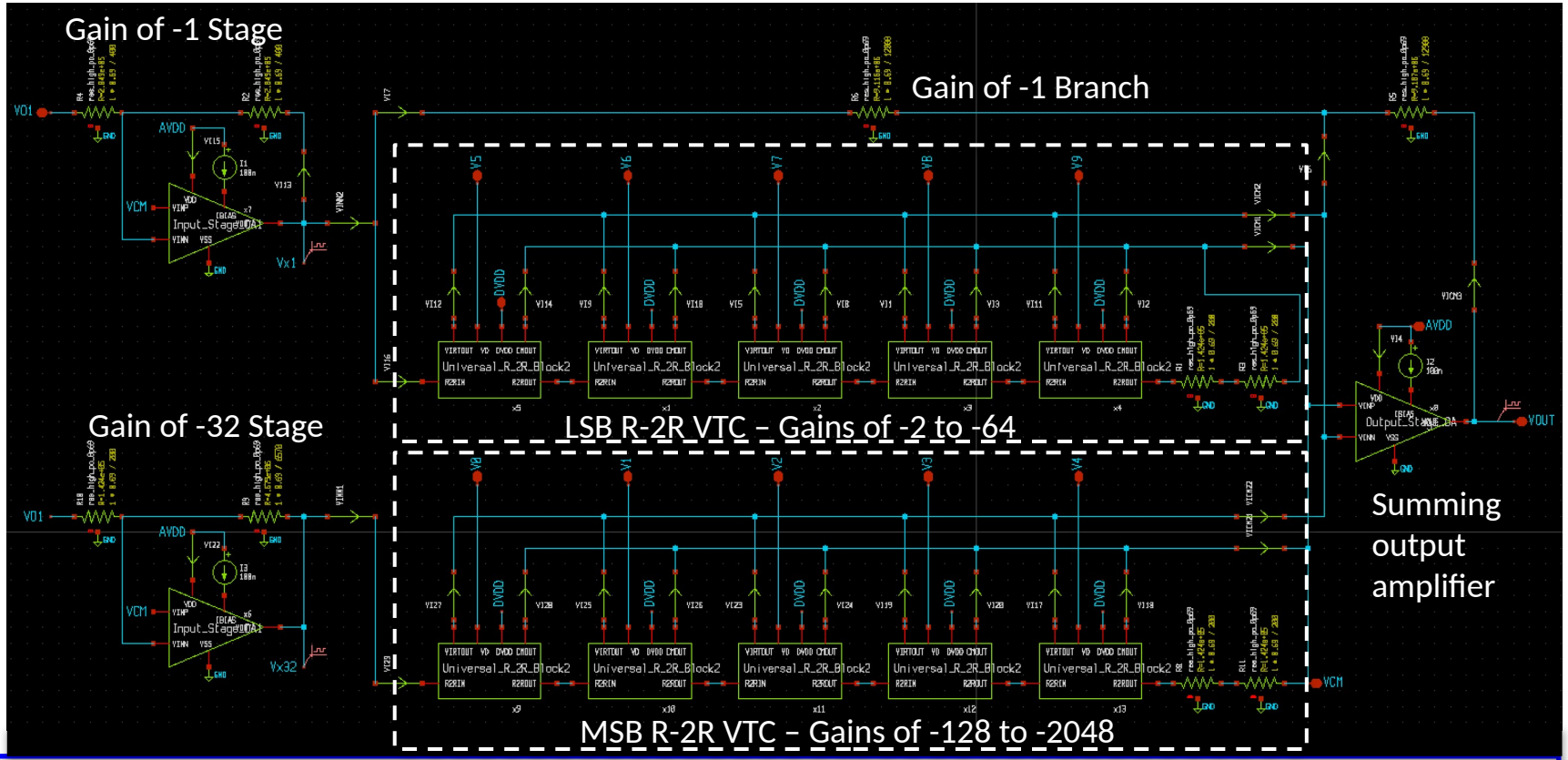
- The PGA uses two 5-bit R-2R voltage to current converters to achieve a 10-bit PGA block with gains from 1 to 1024
- A differential input stage with a fixed gain of 8 to help meet the noise specification
- Bias current requirements is 40μA for the 10-bit PGA block and 40μA for the differential input stage
- 10-bit PGA block requires thirty-seven 100kΩ, one 3.2MΩ, and two 6.4MΩ resistors

Overview of R-2R PGA Parallel Architecture



Total bias current not including the output stage is approximately 70µA. Output loaded with 100kΩ.

10-Bit PGA Block Schematic

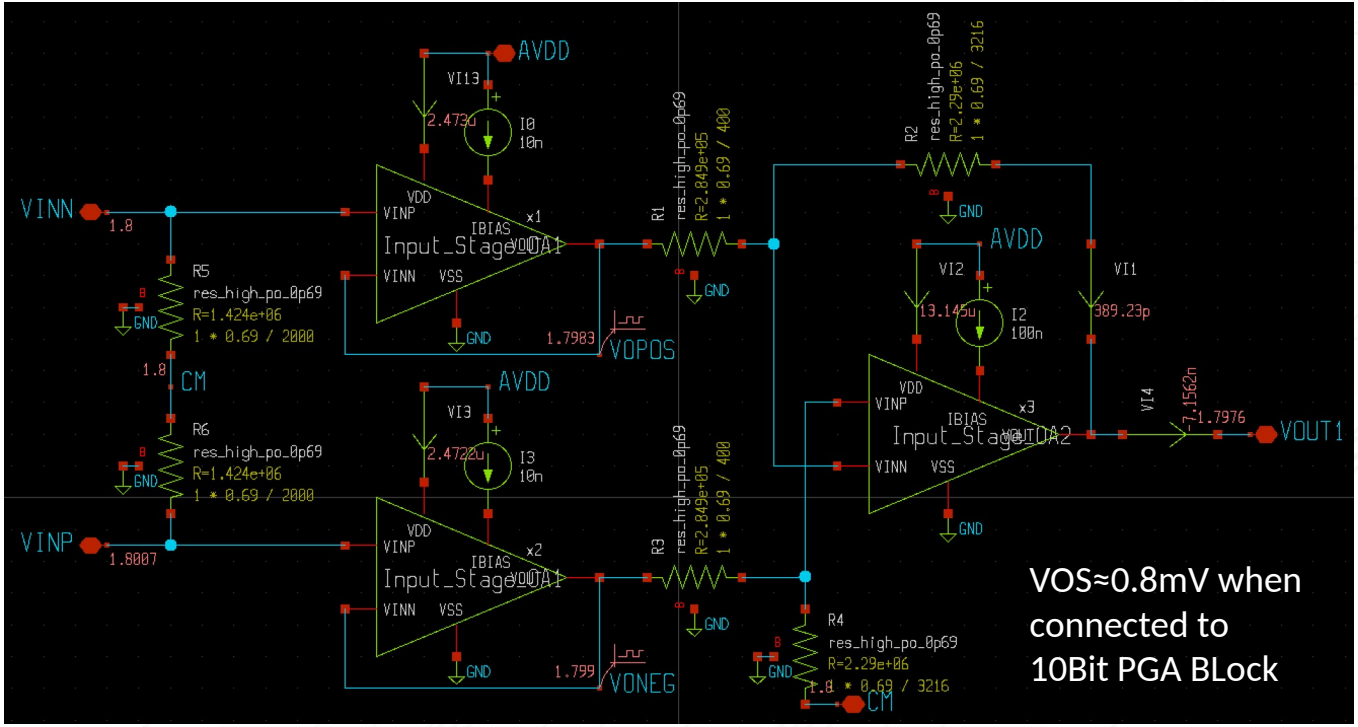


Considerations on Architecture Choice

- The x-1 and x-32 stages could be replaced by making the resistor difference in the R-2R network of the LSB VTC stage 32 times larger than the resistors in the R-2R network of the MSB VTC stage.
- The problem with this is the smaller resistors of the MSB VTC stage require too much current drive. If the LSB resistors are 1MΩ, then the MSB resistors are 31.25kΩ. To get a 1.5V change requires 1.5V/31.25kΩ = 48μA.
- For the architecture of the last slide, the output op amp must drive 100kΩ and the output op amp of the input amplifier must drive 50kΩ (two 100kΩ resistances in parallel). This could be increased to approximately 100kΩ by increasing the resistances of the x-1 stage from 100kΩ to 1MΩ.
- The basic architecture tradeoff for the 10-Bit PGA block is resistance size versus bias current.

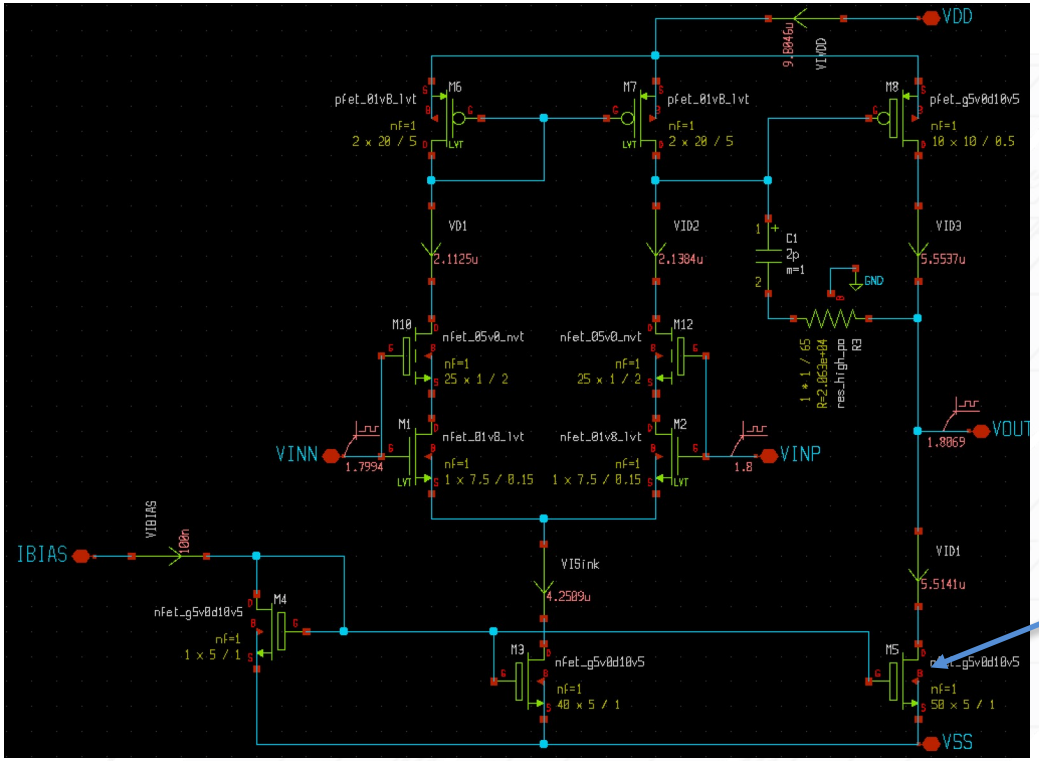
Input Stage Schematic

Total quiescent current ≈ 19.68µA



Op amps are Miller compensated two-stage. Need the lower output resistance to be able to drive 200kΩ loads.

Two-Stage Op Amp

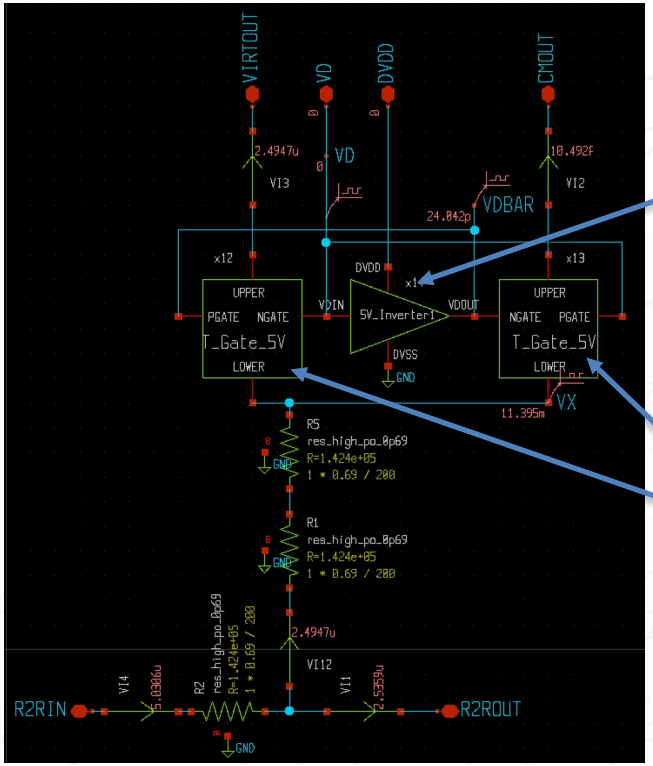


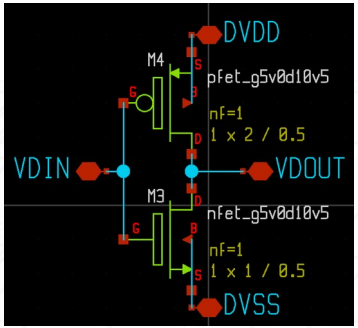
Gain = 88dB
GB = 8MHz (3pF load)
PM = 75° (3pF load)
Bias current = 10µA
Rout ≈ 50kohm

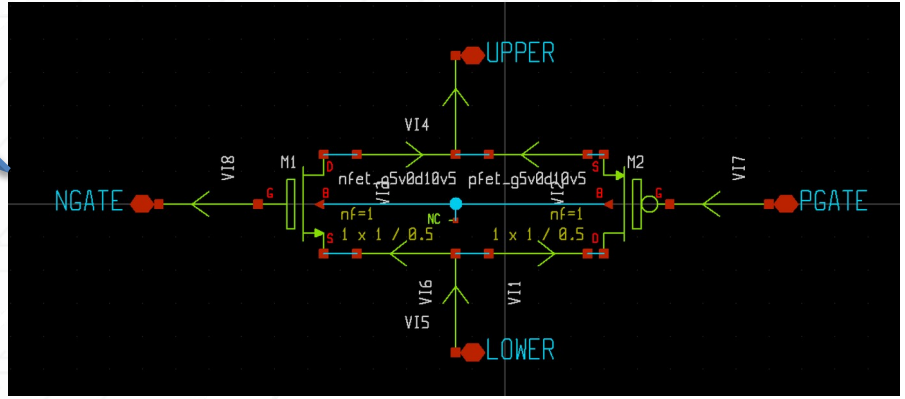
The Class A current sink must be large enough to pull the output to its lower voltage specification. Increase this *W* to satisfy the equation below.

$$I_{Sink} \approx \frac{1.5V}{R_{Load}}$$

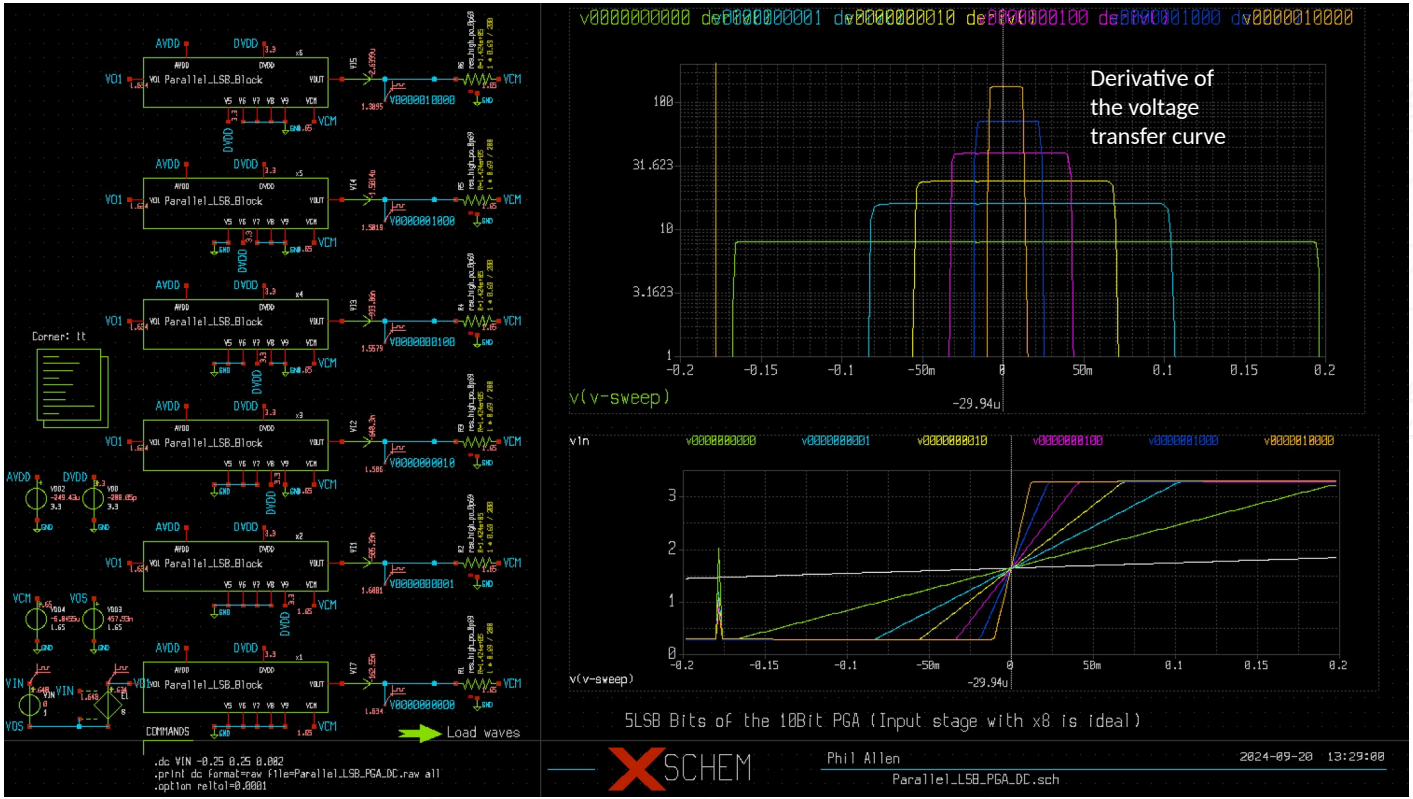
R-2R Schematic





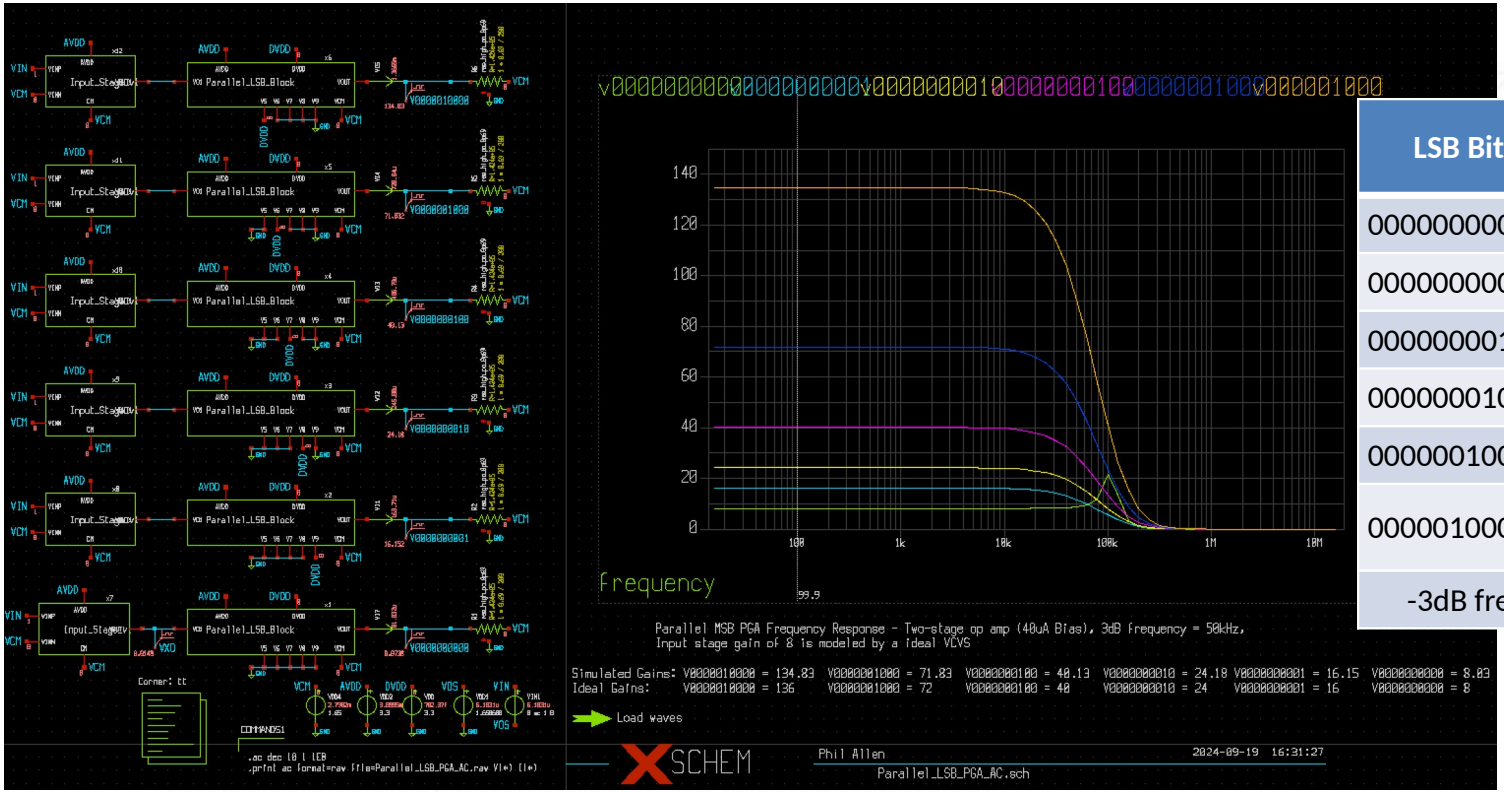


DC Sweep of LSB Bits of 10Bit PGA



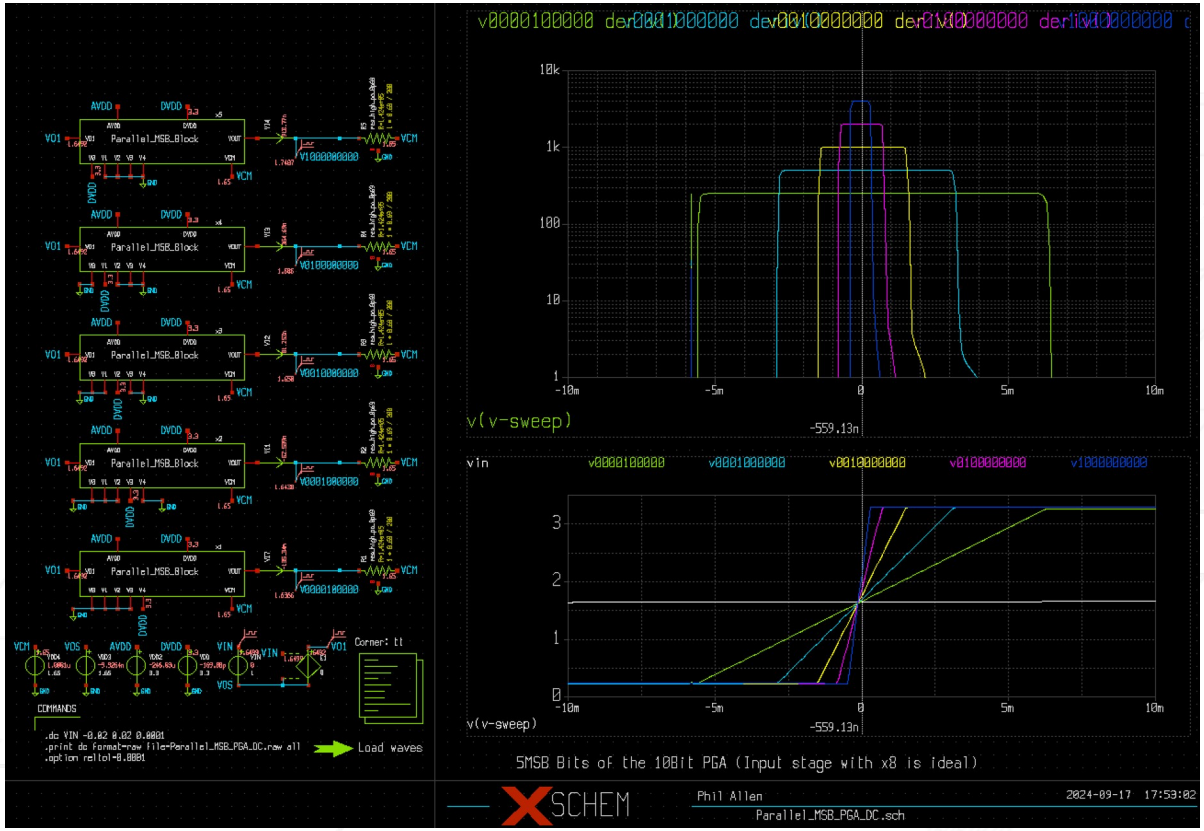
Ideal input stage with gain of 8 was used to simplify the simulation. The actual input stage has an offset of about 0.6mV that does not affect this data.

Frequency Response of LSB Bits of 10Bit PGA



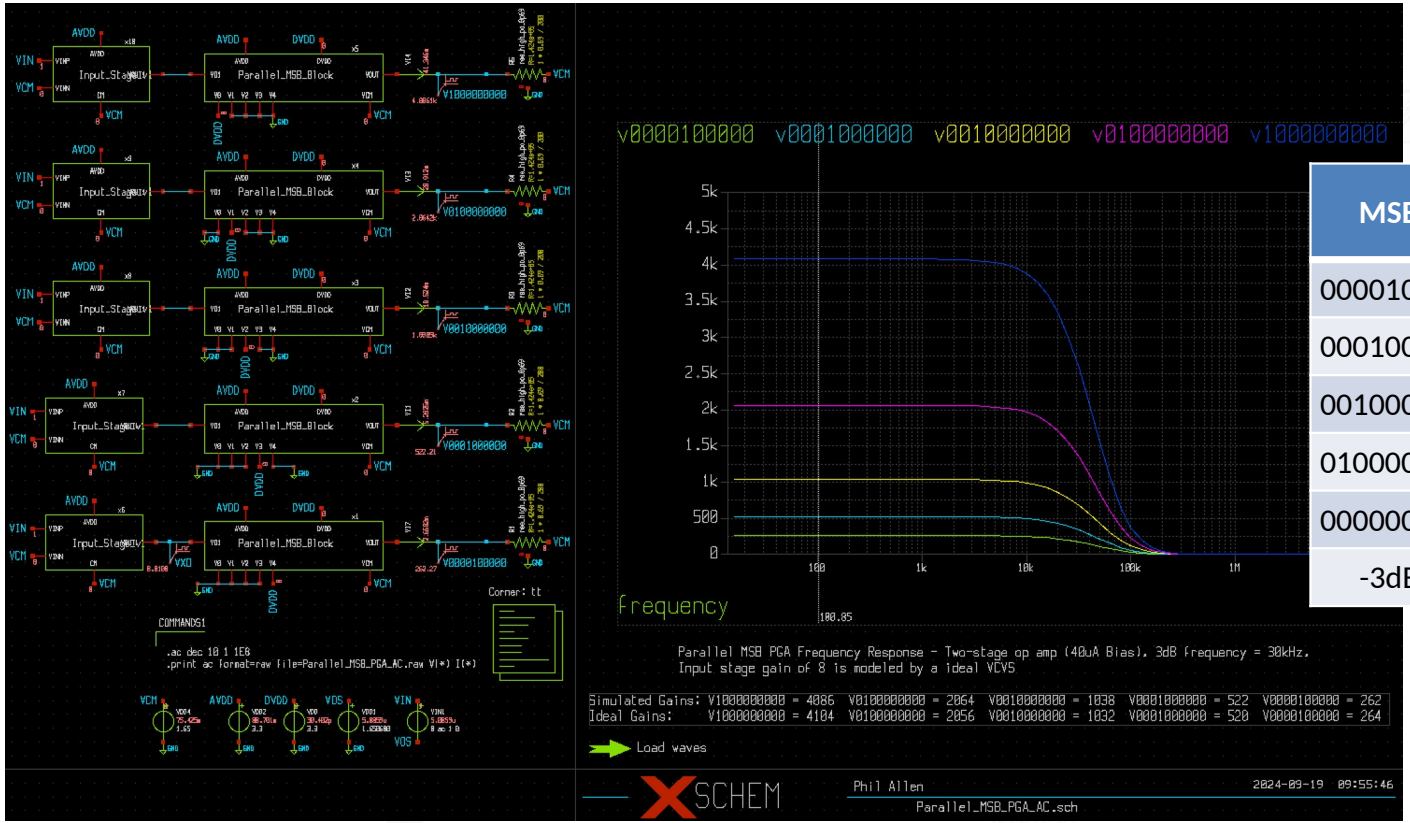
LSB Bit	Ideal Gain	Actual Gain
0000000000	8	8.03
0000000001	16	16.15
0000000010	24	24.18
0000000100	40	40.13
0000001000	72	71.83
0000010000	136	134.83
-3dB frequency ≤ 50kHz		

DC Sweep of MSB Bits of 10Bit PGA



Ideal input stage with gain of 8 was used to simplify the simulation. The actual input stage has an offset of about 0.6mV that must be included to allow the high gains to operate in the correct dc region.

Frequency Response of MSB Bits of 10Bit PGA



MSB Bit	Ideal Gain	Actual Gain
0000100000	264	262
0001000000	520	522
0010000000	1032	1038
0100000000	2056	2064
0000000000	4104	4086
-3dB frequency ≤ 30kHz		

Resistor Summary

Stage/Block	Resistor Count
5Bit LSB VCT	Seventeen 100kΩ resistors
5Bit MSB VCT	Seventeen 100kΩ resistors
Output Summer	Two 6.4MΩ resistors
x1 Inverter for LSB VCT	Two 200kΩ resistors
x32 Inverter for MSB VCT	One 100KΩ and one 3.2MΩ resistors
Input Amplifier	Two 5MΩ, two 200kΩ, and two 1.6MΩ resistors

To Do

- Noise and distortion simulations

Summary

- PGA uses two R-2R voltage-to-current converters (VTC) in parallel along with a gain of 1 to achieve the gains from 1 to 1024.
- The input differential to single-ended amplifier has a fixed gain of 8 which gives the PGA gains of 8 to 8192.
- The programmable gain is determined by identical resistors which should give maximum accuracy
- The feedback resistor of the output summer (6.4MΩ) could be used to tune the gains for best match
- The x1 and x32 inverters could be eliminated by making the resistor ratio of the LSB VTC to the MSB VTC 32:1. This will require more current to drive the smaller resistors.
- An adjustment for VOS will be required to keep the high gains in the linear region of the voltage transfer curve