

Schwap CPU Design Documentation

Charlie Fenoglio, Alexander Hirschfeld, mckeeaj, and Wesley Van Pelt

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1 Registers

There are a total of 76 16-bit registers; 12 are fixed and 64 (spilt into 16 groups of 4) "schwapable" registers.

1.1 Register Names and Descriptions

Name	Number	Description	Saved Across Call?
\$0	0	The Value 0	-
\$pc	1	Program Counter	Yes
\$sp	2	Stack Pointer	Yes
\$ra	3	Return Address	Yes
\$s0 - \$s3	4 - 7	User Temporary Saved	Yes
\$t0 - \$t3	8 - 11	User Temporaries	No
\$h0 - \$h3	12 - 15	Schwap	-

1.2 Schwap Registers

The "schwap" registers are registers that appear to be swapped using a command. There is no data movement when schwapping, it only changes which registers the \$h0 - \$h3 refer to. There are 8 groups the user can switch between and 8 reserved groups. Using "rsh 16" will return to the previous used group.

1.2.1 Schwap Group Numbers, Descriptions, and Uses

Group Number	ID	Uses	Saved Across Call?
0 - 7	0 - 3	User Temporaries	No
8	0 - 3	I/O for devices 0 - 3	-
9	0 - 3	Arguments 0 - 3	No
10	0 - 3	Return Values 0 - 3	No
11	0 - 3	System Call Values 0 - 3	No
12	0 - 3	Kernel Reserved	No
13	0 - 3	Temporary Restore	No
14	0	Exception Cause	No
	1	Exception Status	No
	2	EPC	No
	3	Exception Temporary	No
15	0 - 3	Assembler Temporaries	No
16	-	Go to the last used group	-

2 Instructions

All instructions are 16-bits. The destination register is also used as a source unless otherwise noted. All offsets are bit shifted left by 1 since all instructions are 2 bytes long.

2.1 Instruction Types and Bit Layouts

Instructions can be manually translated by putting the bits for each of the components of the instructions in the places listed by the diagrams for each type. The OP codes, function codes, and types can be found on the "Core Instructions" (2.2) table. The destination and source are register numbers, which can be found under the "Register Names and Descriptions" (1.1) table. Schwap group numbers can be found under the "Schwap Group Numbers, Descriptions, and Uses" (1.2.1) table.

2.1.1 A-Type

Used for all ALU operations. It consists of a 4-bit OP code, 4-bit destination, 4-bit source, and a 4-bit function code.

OP Code		Destination		Source		Func. Code	
15	12	11	8	7	4	3	0

2.1.2 B-Type

Used for branching. It consists of a 4-bit OP code, 4-bit 1st source, 4-bit 2nd source, and a (signed) 4-bit offset.

OP Code		Source 0		Source 1		Offset	
15	12	11	8	7	4	3	0

2.1.3 H-Type

Used for schwapping. It consists of a 4-bit OP code, 8 unused bits, and a 5-bit schwap group number.

OP Code						Group	
15	12					4	0

2.1.4 J-Type

Used for jumping. It consists of a 4-bit OP code, 4-bit source, and an 8-bit (signed) offset.

OP Code		Source		Offset			
15	12	11	8	7			0

2.1.5 R-Type

Used for reading and writing memory. It consists of a 4-bit OP code, 4-bit destination (not used as a source), 4-bit source, and a 4-bit (unsigned) offset.

OP Code		Destination		Source		Offset	
15	12	11	8	7	4	3	0

2.1.6 S-Type

Used for sudo. Only has a 4-bit OP code.

OP Code							
15	12						

2.2 Core Instructions

OP Code	Function Code	Name	Type	Syntax	Meaning	Description
0x0 and 0x1 [†]	0x0	add	A	add [dest], [src] add [dest], [immediate]	dest += src dest += immediate	Adds 2 Integers
	0x1	adu	A	adu [dest], [src] adu [dest], [immediate]	dest += src dest += immediate	Adds 2 Unsigned Integers
	0x2	sub	A	sub [dest], [src] sub [dest], [immediate]	dest -= src dest -= immediate	Subtracts 2 Integers
	0x3	sbu	A	sbu [dest], [src] sbu [dest], [immediate]	dest -= src dest -= immediate	Subtracts 2 Unsigned Integers
	0x4	sll	A	sll [dest], [immediate]	dest <<= immediate	Left Logical Bit shift
	0x5	srl	A	srl [dest], [immediate]	dest >>= immediate	Right Logical Bit shift
	0x6	sra	A	sra [dest], [immediate]	dest >>>= immediate	Right Arithmetic Bit shift
	0x7	and	A	and [dest], [src] and [dest], [immediate]	dest &= src dest &= immediate	Ands 2 Values
	0x8	orr	A	orr [dest], [src] orr [dest], [immediate]	dest = src dest = immediate	Ors 2 Values
	0x9	xor	A	xor [dest], [src] xor [dest], [immediate]	dest ^ = src dest ^ = immediate	Xors 2 Values
	0xA	not	A	not [dest], [src] not [dest], [immediate]	dest = ~src dest = ~immediate	Bitwise Nots 2 Values
	0xB	tsc	A	tsc [dest], [src] tsc [dest], [immediate]	dest = ~src + 1 dest = ~immediate + 1	Converts a number to 2's compliment
	0xF	cpy	A	cpy [dest], [src] cpy [dest], [immediate]	dest = src dest = immediate	Copies a value
0x2	-	jr	J	jr [regNumber]	PC = regNumber	Sets the PC to the value in the register
0x3	-	rsh	H	rsh [groupNumber]	-	Sets the schwappable registers to use
0x4	-	beq	B	beq [src0], [src1], label	-	Branches to the label if src0 == src1
0x5	-	bnq	B	bnq [src0], [src1], label	-	Branches to the label if src0 != src1
0x6	-	bgt	B	bgt [src0], [src1], label	-	Branches to the label if src0 > src1
0x7	-	r	R	r [dest], [src]	-	Moves the value in memory at the address in src into dest
0x8	-	w	R	w [dest], [src]	-	Moves the value in dest to the address in src in memory
0xF	-	sud	S	sud	-	Same as "syscall" in MIPS

[†]0x0 is used for instructions which do not use an immediate, 0x1 is used if the instruction does use an immediate

2.3 Pseudo Instructions

Name	Syntax	Actual Code	Description
j	j label	jr [instructionNumber]	Jumps to the instruction at the label by using jr and the instruction number
jal	jal label	cpy \$ra, \$pc j [label]	Stores the return address and then jumps to the label
beq	beq [src0], [src1], label	bnq [src0], [src1], Next j label Next:	Branches to the label if src0 == src1 [†]
bnq	bnq [src0], [src1], label	beq [src0], [src1], Next j label Next:	Branches to the label if src0 != src1 [†]
bgt	bgt [src0], [src1], label	bgt [src0], [src1], Next1 j Next2 Next1: j label Next2:	Branches to the label if src0 > src1 [†]

[†]Will become pseudo instruction iff the branch is more than 7 instructions down and 8 instructions up.

3 Examples

3.1 Basic Use Examples

3.1.1 Loading an immediate into a register

```
ldi $t0, 32      #Loads 32 into t0
```

3.1.2 Iteration and Conditionals

This is an example of which will iterate over 4 array elements in memory and add 32 to each of them. It will stop repeating after the 4 elements using beq.

```
# There is a base memory address for an array in memory at s0
ldi $t0, 8
cpy $t1, $0
loop:
    r    $t2, 0($s0)
    add $t2, 32
    w    0($s0), $t2
    add $t1, 2
    beq $t0, $t1, loop
```

3.1.3 I/O

To get input:

```
rsh 8          # Switch to the IO schwap
cpy $t0, $h0    # Copy the input from device 0 into t0
```

To give output:

```
rsh 8          # Switch to the IO schwap
cpy $h0, $t0    # Copy the output for device 0 from t0
```

3.2 relPrime and gcd Implementation

3.2.1 Assembly

RelPrime:			
	rsh	9	<i>#set schwap</i>
	cpy	\$s2, \$ra	<i>#save \$ra</i>
	cpy	\$s0, \$h0	<i>#copy n out of schwap</i>
	li	\$s1, 0x2	<i>#load 2 to m</i>
	rsh	9	<i>#set schwap to args</i>
While:			
	cpy	\$h0, \$s0	<i>#set a0 to n</i>
	cpy	\$h1, \$s1	<i>#set a1 to m</i>
	jl	GCD	<i>#call GCD</i>
	rsh	10	<i>#set schwap</i>
	li	\$t0, 0x1	<i>#load immediate 0x1 to t0</i>
	bne	\$h0, \$t0, Done	<i>#branch to done if r0 != 1</i>
	add	\$s1, 0x1	<i>#add 1 to m</i>
	j	While	<i>#jump to the start of the loop</i>
Done:			
	rsh	10	<i>#load return registers</i>
	cpy	\$h0, \$s1	<i>#set r0 to m</i>
	jr	\$s2, 0	<i>#return to the previous function</i>

GCD:			
	rsh	9	<i>#schwap to argument register</i>
Base:			
	bne	\$h0, \$z0, GMain	<i>#a!=0 go to GMain</i>
	cpy	\$t0, \$h1	<i>#copy h1 to t0 for RSH</i>
	rsh	10	<i>#schwap to return registers</i>
	cpy	\$h0, \$t0	<i>#load t0 to r1</i>
	jr	\$ra, 0	<i>#return</i>
GMain:			
	beq	\$h1, \$z0, Exit	<i>#jump to exit if b is zero</i>
	bgt	\$h0, \$h1, If	<i>#jump to If if a>b</i>
Else:			
	sub	\$h1, \$h0	<i>#else: b=b-a</i>
	j	GMain	<i>#loop</i>
If:			
	sub	\$h0, \$h1	<i>#if: a=a-b</i>
	j	GMain	<i>#loop</i>
Exit:			
	cpy	\$t0, \$h0	<i>#copy h0 to t0 for rsh schwap</i>
	rsh	10	<i>#make sure we're in the right spot</i>
	cpy	\$h0, \$t0	<i>#copy t0 to h0</i>
	jr	\$ra	<i>#return</i>

3.2.2 Machine Code

RelPrime		GCD	
PC	Hex	PC	Hex
00	3009	42	3009
02	063F	44	5C05
04	04CF	46	085F
06	050E	48	300A
08	0002	4A	0A8F
0A	3009	4C	2300
0C	0C4F	4E	4B05
0E	0D5F	50	0C0F
10	031F	52	0072
12	300F	54	2C00
14	0C0F	56	301F
16	0042	58	6CD7
18	2C00	5A	0DC2
1A	301F	5C	300F
1C	300A	5E	0C0F
1E	080E	60	004E
20	0001	62	2C00
22	4C85	64	301F
24	0C0F	66	0CD2
26	000A	68	300F
28	2C00	6A	0C0F
2A	301F	6C	004E
2C	0500	6E	2C00
2E	0001	70	301F
30	300F	72	08CF
34	0C0F	74	300A
36	000C	76	0C8F
38	2C00	78	2300
3A	301F		
3C	300A		
3E	0C5F		
40	2600		