ELEC 401 Analog CMOS Integrated Circuit Design
Opamp Design

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Introduction

This report will cover the design steps for a two-stage operational amplifier using 0.35-µm CMOS technology, which meets the required design specifications and is based on the topology provided in class.

Initial Considerations

Since the device can consume no more than 1 mW of energy, the maximum current of the device is as follows:

$$3.3\,V \times I_{max} = 1\,mW$$
$$I_{max} = 303.03\,\mu A \quad (1)$$

In order to maximize the unity gain frequency, a large current is allotted to the differential-input stage. Table 1 shows the expected current in each component.

Transistor	Current (µA)
M11	25
M12	25
M5	200
M7	35

Table 1: Expected currents in each component.

The total does not add up to the maximum current in case more current is unexpectedly required in a certain stage.

Amplifier Design

In order to have a large output voltage swing, V_{bias2} is chosen to be 2.4 V. Using DC analysis, V_{th} of M6 and M7 are found to be near -0.7 V. V_{eff} of these two transistors can be calculated using this equation:

$$V_{eff} = V_{SG} - |V_{th}| \quad (2)$$

The V_{eff} of M6 and M7 is approximately 0.2 V.

The current of a transistor in the saturation region is:

$$I_d = \frac{1}{2} k \frac{W}{L} v_{eff}^2$$

(3)

The k values are derived based on current and v_{eff} values obtained from the simulation (with arbitrary width and length values):

- $k_p = 5.132 \times 10^{-5}$
- $k_n = 1.204 \times 10^{-4}$

For now, let us assume that every transistor in the differential-input and common-source stages have a length of 0.35μm. Using Eq. (3), the widths of M5 and M7 are found to be 68 μm and 11.9 μm respectively.

For the other transistors (not part of the biasing circuitry), it is impossible to know the overdrive voltages. Thus, the next calculations will assume voltages that will provide the desired specifications of the op-amp. However, after running the simulation, it is likely that these values will be very different and that adjustments will need to be made.

The unity gain frequency is given in the following equation:

$$\omega_{ta} = \frac{g_{m1}}{C_c} \tag{4}$$

Since it is standard for Cc to be near 1pF, we will assume that this is the value. For a unity gain frequency of 250 MHz a transconductance of at least 1.57 mA/V is required. Assuming that M1 is in saturation, this can be calculated as:

$$g_m = \sqrt{2k\frac{W}{L}I_D} \tag{5}$$

With current being constant, it would be favorable to have a low overdrive voltage (based on Eq. (3)) to be able to increase the width. A width of 100 μm will result in a unity gain frequency of approximately 272.6 MHz and an overdrive voltage of 0.12 V. M2 should have the same dimensions as M1.

The slew rate can be found using this equation:

$$SR = V_{eff\,1}\omega_{ta} \tag{6}$$

The estimated slew rate for this device is therefore 200.0 V/μs.

The low frequency gain of this device is characterized by the equation:

$$A_v = g_{m1}¿$$

(6)

$$r_0 = \frac{1}{\lambda I_D}$$

(7)

Changing the voltage will have no effect on the gain since it is proportional to the transconductance but inversely proportional to r_o. Therefore the only way to increase the gain would be by decreasing the overdrive voltage of M6. If this value is 0.12 V, the low frequency gain will be 77.0 dB (using an estimated lambda value of 0.1 V^{-1}) and the width of M6 is 14.1 μm.

By knowing the overdrive voltages of M6 and M7, the peak-to-peak voltage swing can be estimated as well:

$$V_{PP} = V_{DD} - V_{eff\,6} - V_{eff\,7}$$

(8)

This value is found to be 2.98 V, which is well beyond the required value.

To avoid systematic voltage offset, this relationship must hold:

$$\left(\frac{W}{L}\right)_4 = \frac{\left(\frac{W}{L}\right)_6 \left(\frac{W}{L}\right)_5}{2\left(\frac{W}{L}\right)_7}$$

(9)

Therefore, the width of M4 should be 39.95 μm.

R_C would most likely be required to achieve a phase margin of 60º. As a starting point, R_C is chosen according to this equation:

$$R_c = \frac{1}{1.2\,\omega_t C_c}$$

(10)

Although the unity gain frequency is not yet known, if it is assumed that it is 250 MHz, then R_C is 530.5Ω.

Table 2 summarizes the calculated values of each component and Table 3 outlines the performance of this device.

Transistor	Width (μm)	Length (μm)
M1	100	0.35
M2	100	0.35
M3	39.95	0.35
M4	39.95	0.35
M5	68	0.35
M6	14.1	0.35
M7	11.9	0.35
Resistor	Resistance (Ω)	
R_C	530.5	
Capacitor	Capacitance (pF)	
C_C	1	
C_L	0.5	

Table 2: Calculated values for components in the differential-input and common-source stage.

V_{DD}	3.3 V
V_{bias2}	2.4 V
Bias current of M12	25 μA
Nominal input common-mode	1.65 V
Overall power consumption	0.9405 mW
Output peak-to-peak Swing	2.98 V
Low-frequency differential to single-ended gain	60.85 dB
Small-signal unity gain frequency	272.6 MHz
Slew rate	200 V/μs

Table 3: Calculated performance values.

Simulation Results

Using the values calculated above, the Bode plots for the open-loop gain were obtained and are shown in Figure 1 and Figure 2.

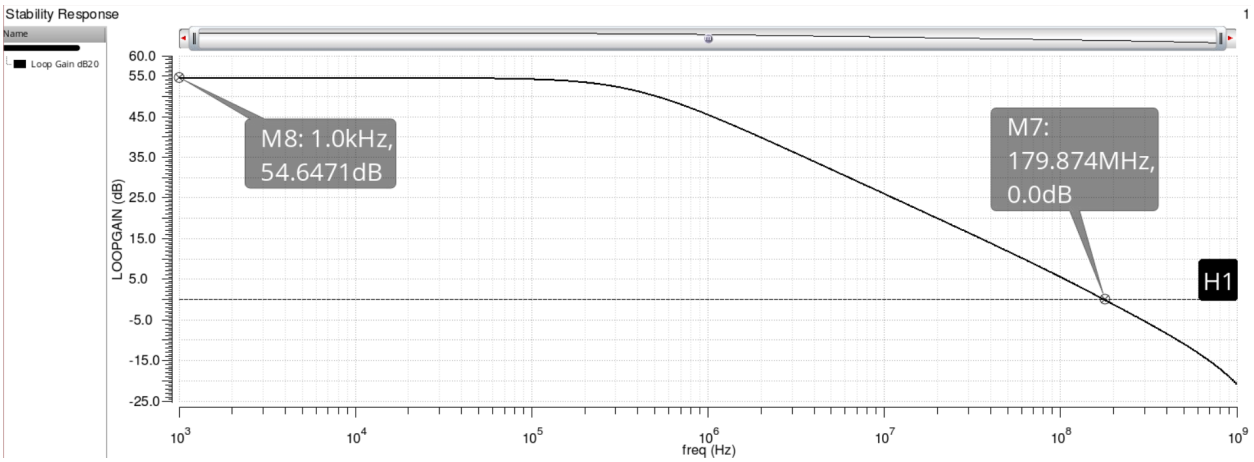

Figure 1: The open-loop gain (magnitude) of the device using calculated values.

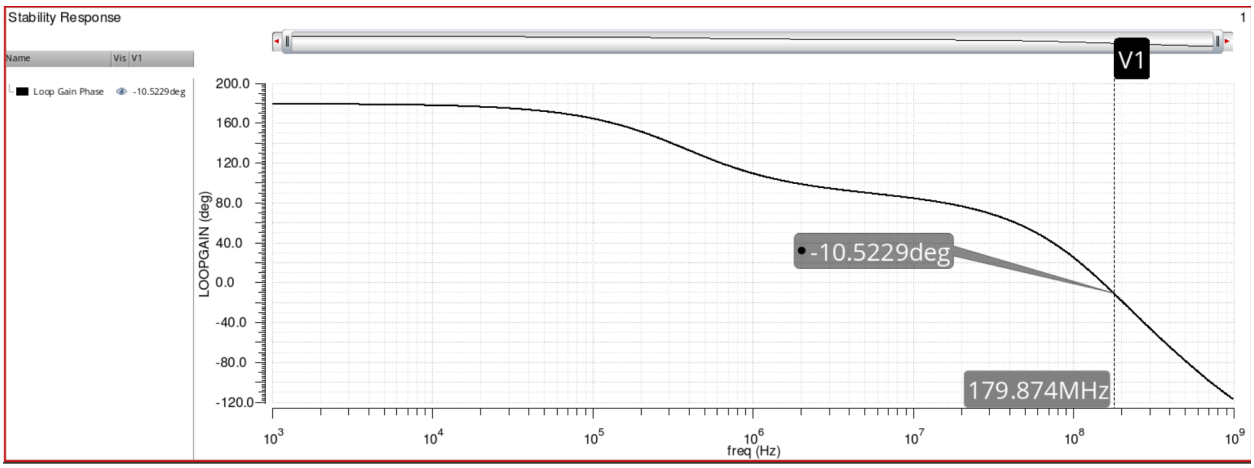

Figure 2: The open-loop gain (phase) of the device using calculating values.

Based on these plots, the low frequency gain is 54.6 dB, the unity gain frequency is 179.9 MHz, and the phase margin is -10.5 degrees. All three of these values do not meet the requirements.

Correcting the Discrepancies

It was discovered that changing the widths and lengths of each transistor can affect the low frequency gain, phase margin and unity frequency gain. Since V_{eff} of M1, M2, and M6 were chosen arbitrarily, changing the ratio between the widths and lengths is permitted (as long as the transistors remain in the saturation region). For M5 and M7, as long as this ratio is constant, the dimensions can be swept within permitted values (this is achieved by using variables in Cadence Virtuoso).

Thus, several parameter sweeps were done to achieve the required specifications.

For example, adjusting the width of M1 (with M2 having identical width) changes the open-loop gain as shown in Figure 3.

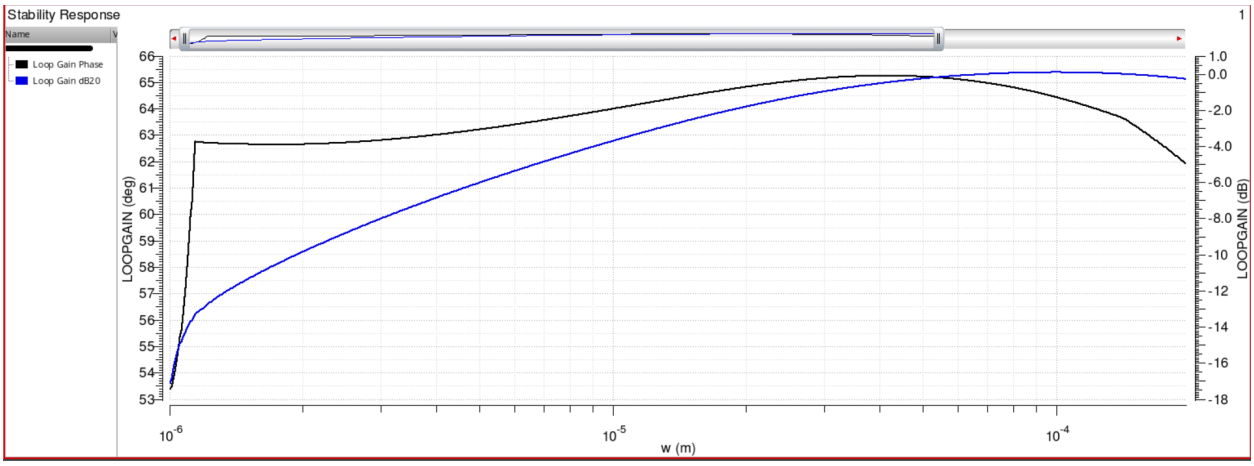

Figure 3: The open-loop gain of this device at 250MHz as a function of the width of M1.

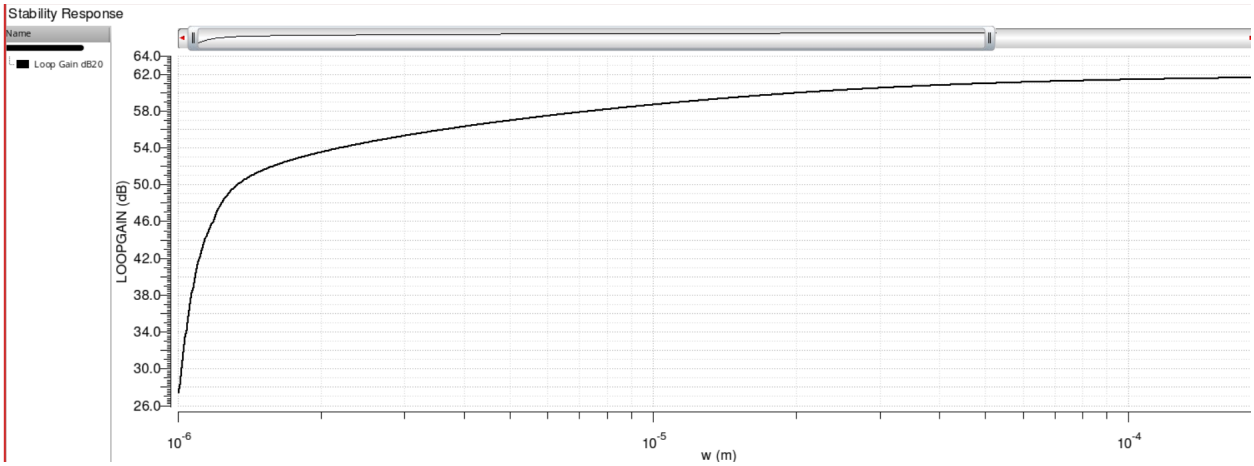

Figure 4: The low-frequency (1 kHz) open-loop gain of this device as a function of the width of M1.

These graphs imply that a large width for M1 is desirable. The final dimensions of each transistor and the performance of the device are presented in a later section of this paper.

Current Mirror Design

Based on the simulation, in order to obtain the desired results, a V_{bias2} of 2.4 V is required. Knowing that the overdrive voltage for M11 and M12 is 0.2 V and calculating for the currents to be 25 µA, the saturation current equation (Eq. (3)) is used. This is with all of the widths of the transistors in the biasing circuit set to 0.35 µm.

The widths for M11 and M12 are found to be 8.52 µm.

R is arbitrarily chosen to be 4kΩ. Using Ohm's law, the voltage drop across the resistor is 0.1 V. Therefore, V_{GS9} is 0.1 V higher than V_{GS10}. Since it is known that the width of M10 is four times the width of M9, Eq. (3) can be used to calculate the dimensions of these two transistors as follows:

$$I_D = \frac{1}{2} k_n \left(\frac{4\,W9}{L} \right) \left(V_{eff\,10} \right)^2 = \frac{1}{2} k_n \left(\frac{W9}{L} \right) \left(V_{eff\,10} + 0.1 \right)^2$$

$$4\,V_{eff\,10}^2 = \left(V_{eff\,10} + 0.1 \right)^2$$

$$V_{eff\,10} = 0.1\,V$$

$$W_{10} = 34.1\,\mu m$$

$$W_9 = 8.52\,\mu m$$

Table 4 summarizes the calculated values of each component.

Transistor	Width (μm)	Length (μm)
M9	8.52	0.35
M10	34.1	0.35
M11	8.52	0.35
M12	8.52	0.35
Resistor	Resistance (kΩ)	
R	4	

Table 4: Calculated values for components in the biasing circuitry.

Simulation Results

Based on results from DC analysis, V_{bias2} and the current in M12 were found to be 2.43 V and 20.17 μA respectively.

Correcting the Discrepancies

Since the simulated current and V_{bias2} does not match the calculated value, parameter sweeps were applied for the bias circuitry in order to obtain the correct current in M12 and a V_{bias2} of 2.4 V.

For example, Figure 5 shows I_{12} as a function of the width of M9 (with W10 always being four times W9).

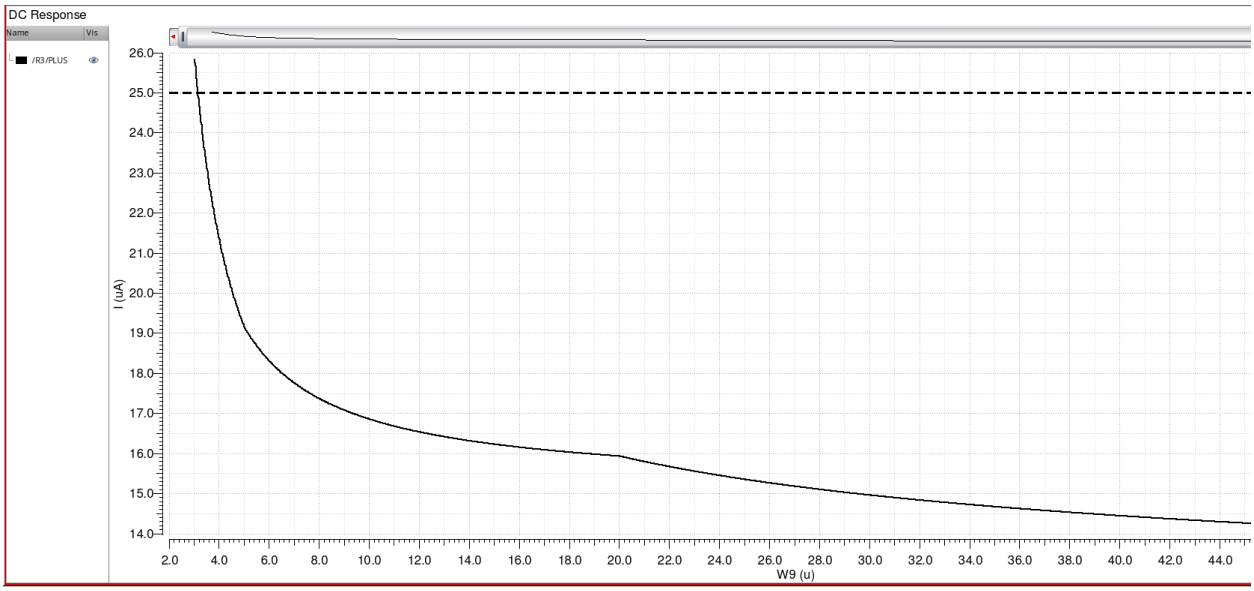

Figure 5: The current in M12 as a function of the width of M9.

After completing various parameter sweeps, I_{12} was successfully set to 25 µA. The final dimensions are presented in the following section.

Final Design

Table 5 shows the parameters of each component and Table 6 outlines the performance of this device. Figure 6 is the schematic of the design and Figures 6-14 show the results of various simulated tests.

Transistor	Width (µm)	Length (µm)
M1	70.0	0.35
M2	70.0	0.35
M3	21.19	0.35
M4	21.19	0.35
M5	61.0	0.35
M6	15.8	0.7
M7	23.04	0.7
M9	3.115	0.35
M10	12.46	0.35
M11	8.0	0.35
M12	8.0	0.35
Resistor	Resistance (kΩ)	
R	4.52	
R_C	4.5	
Capacitor	Capacitance (pF)	
C_C	50	
C_L	0.5	

Table 5: The specifications for each component.

V_{DD}	3.3 V
V_{bias2}	2.401 V
Bias current of M12	25.08 µA
Nominal input common-mode	1.65 V
Input common-mode range	> 0.5 V
Overall power consumption	0.995 mW
Output peak-to-peak Swing	3.017 V
Low-frequency differential to single-ended gain	60.85 dB
Small-signal unity gain frequency	251.228 MHz
Phase margin	64.81°
Slew rate	≈ 7000 V/µs
10 to 90% Settling time	≈ 150 ns

Table 6: The performance of this device.

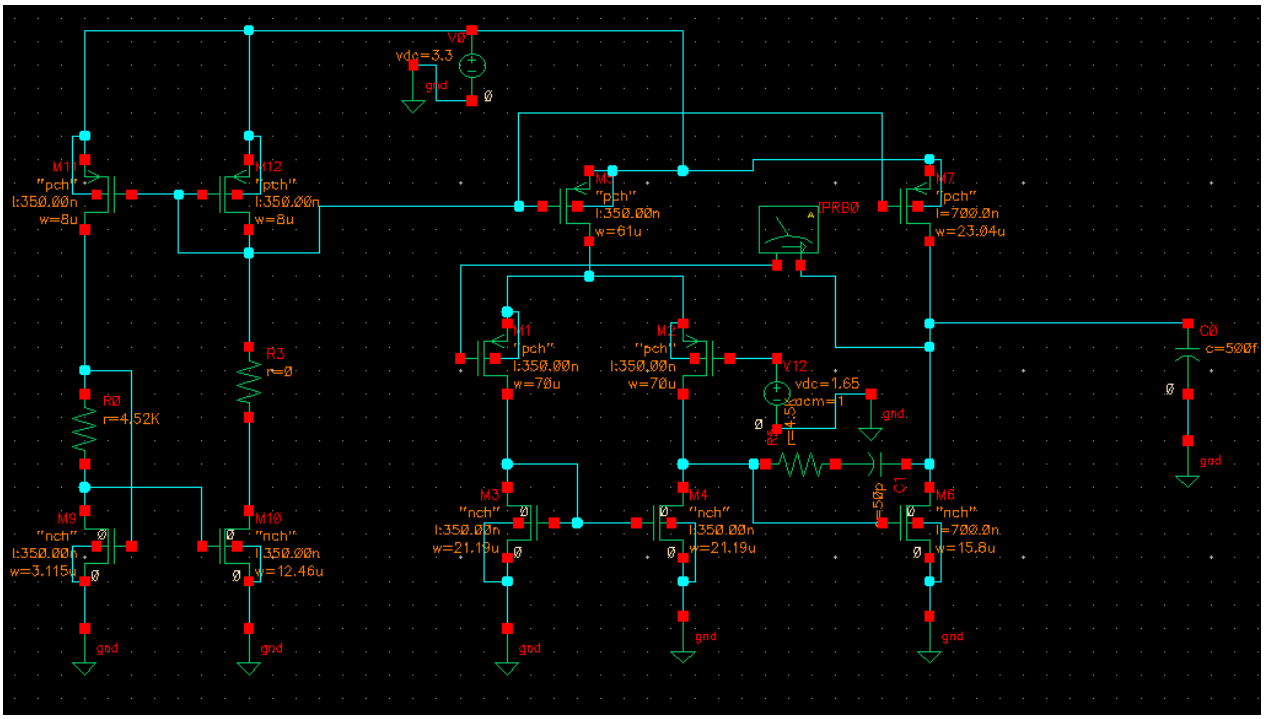

Figure 6: The schematic of this design with transistor dimensions and component values.

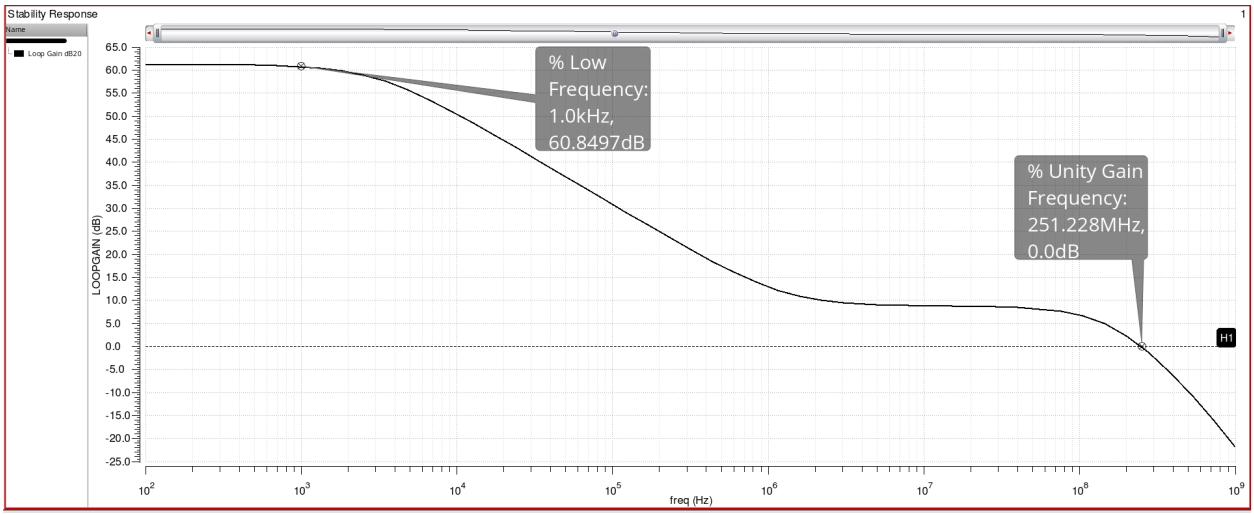

Figure 7: The Bode plot of the magnitude of the open-loop gain. The low and unity gain frequencies are labeled.

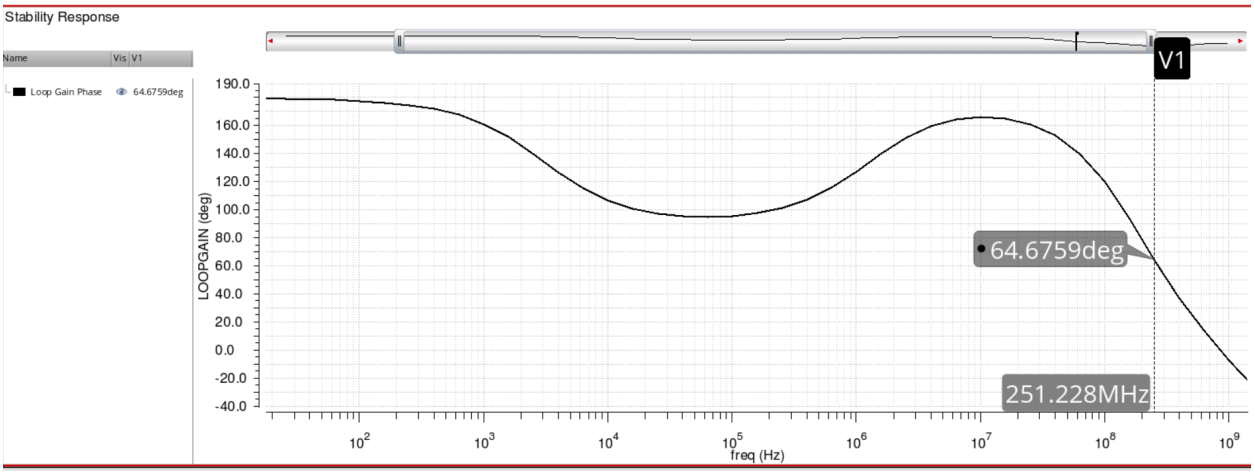

Figure 8: The Bode plot of the phase of the open-loop gain. The phase margin is labeled.

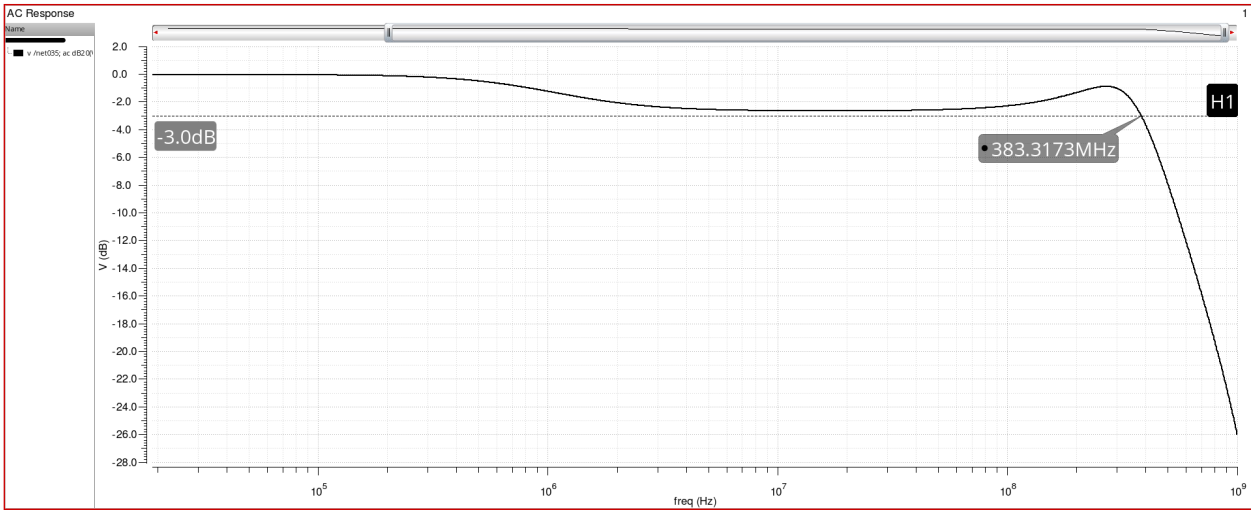

Figure 9: The Bode plot of the closed-loop gain with the -3dB frequency labeled.

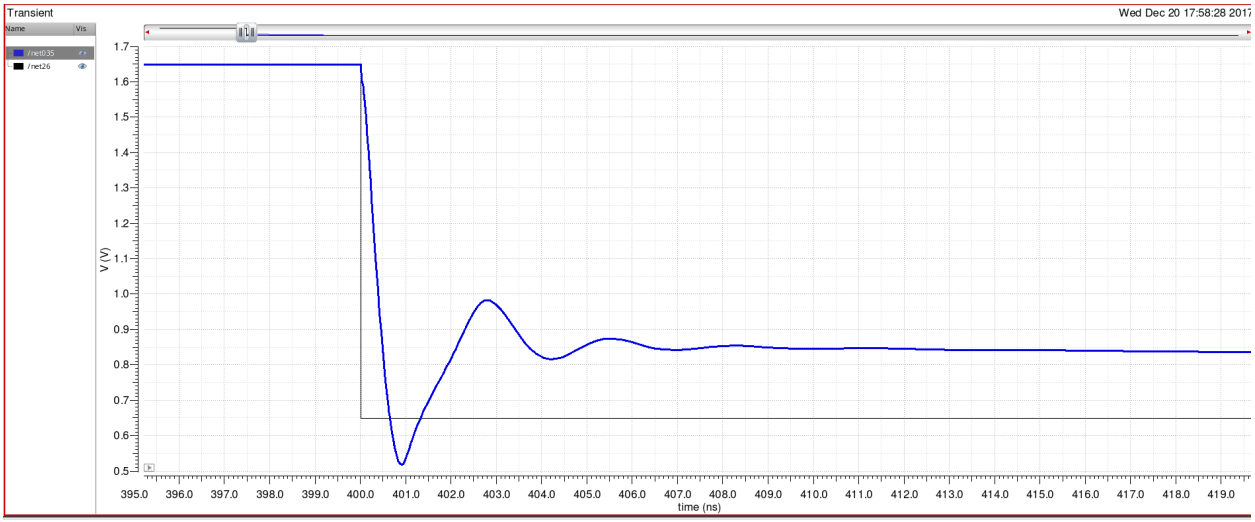

Figure 10: The chart that was used to find the slew rate and the 10-90% settling time of the op-amp. In black is the input voltage (2.65V – 1.65V step) and in blue is the output signal.

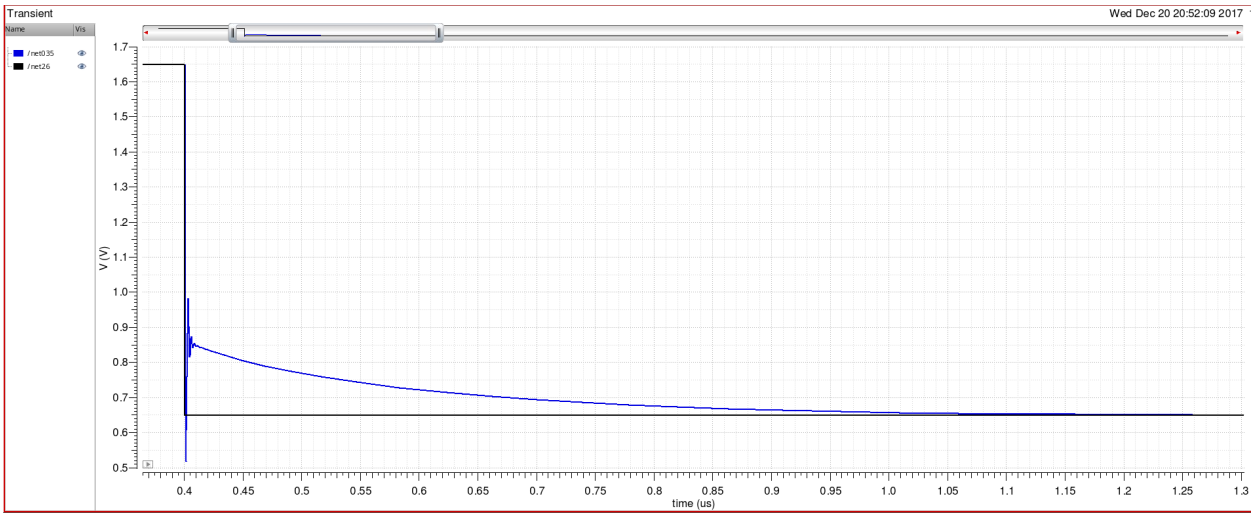

Figure 11: The transient response of a step voltage of -1V.

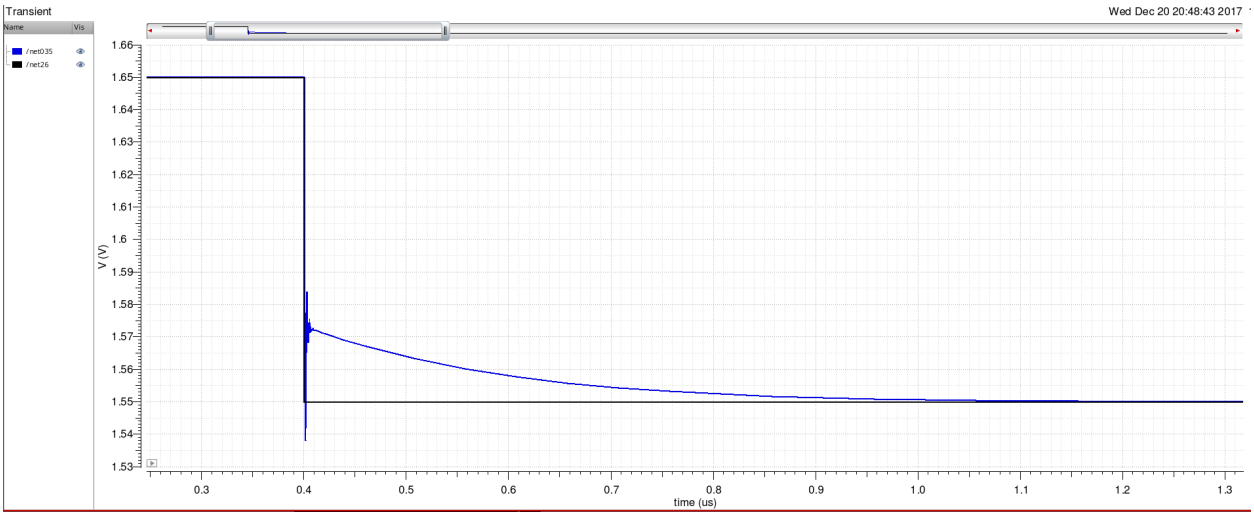

Figure 12: The transient response of a step voltage of -0.1V.

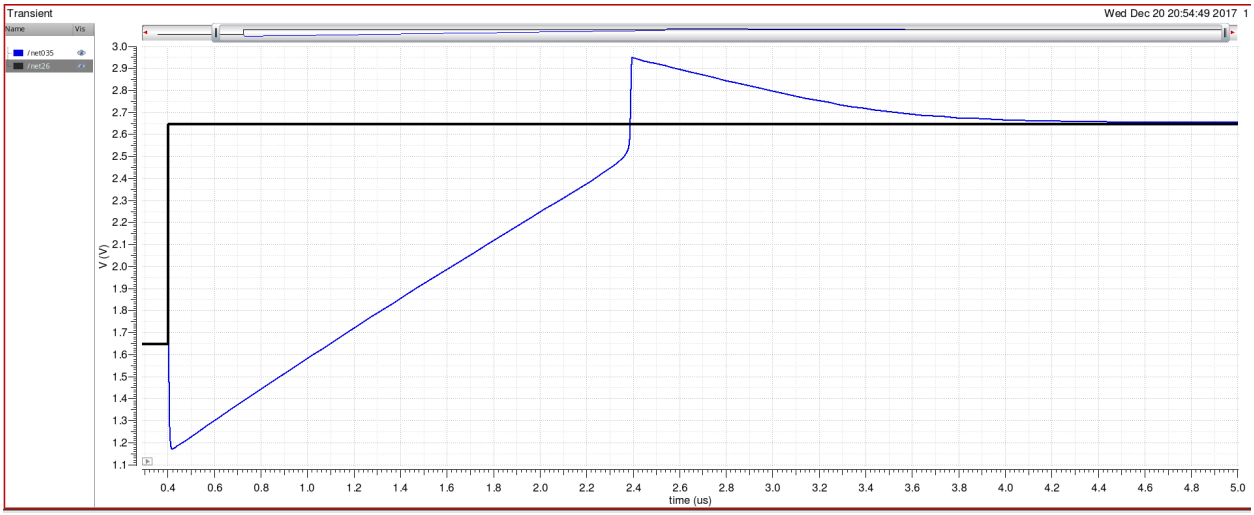

Figure 13: The transient response of a step voltage of 1V.

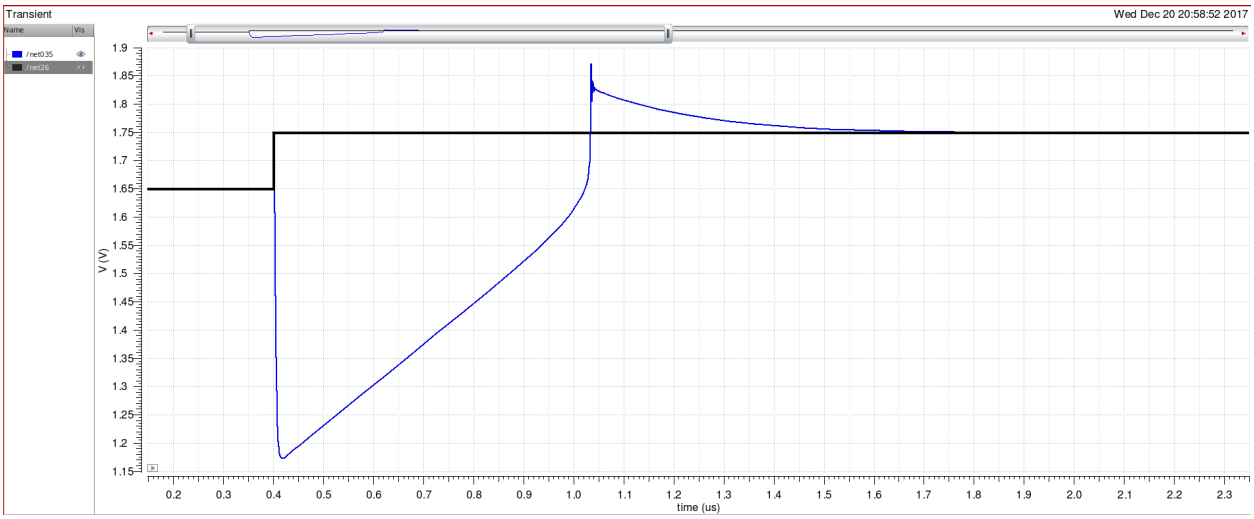

Figure 14: The transient response of a step voltage of 0.1V.

Discussion

The Bode plots presented above show values that are expected. However, the transient response of the system indicates that this op-amp has a slew rate that is considerably higher than what is expected. Furthermore, when a positive input step is applied, the output voltage drops to approximately 1.2V at the slew rate. However, the output reaches a steady-state voltage that is the same as the input after 4.6μs (in the case for a 1V step input). This behavior is very unexpected but does not undermine the main function of this device. Potential causes of this phenomena include erroneous calculations done by the simulation software or other factors that were not considered in the analysis. Because of this, it is unknown how the device will perform if manufactured.

In summary, this device meets all specifications but suffers from unexpected behavior in certain conditions.