2.1GHz Inductor Degenerated Common Source Low-Noise Amplifier Design

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***Abstract* – This report outlines the design process and results of an inductor degenerated common source low-noise amplifier (CSLNA) with a center frequency of 2.1GHz. This device is designed to be fabricated using the 45nm CMOS process. The design met all specifications (except for the noise factor) and power consumption was optimized.**

I. Introduction

IN an increasingly interconnected world, it is becoming more important to ensure that data is sent wirelessly across large distances with very little noise. The purpose of an LNA is to amplify weak signals that are supplied by an antenna without altering them. This is achieved by having a large enough S21 value (gain), and an acceptable IIP3 and noise factor.

II. CALCULATION PROCESS

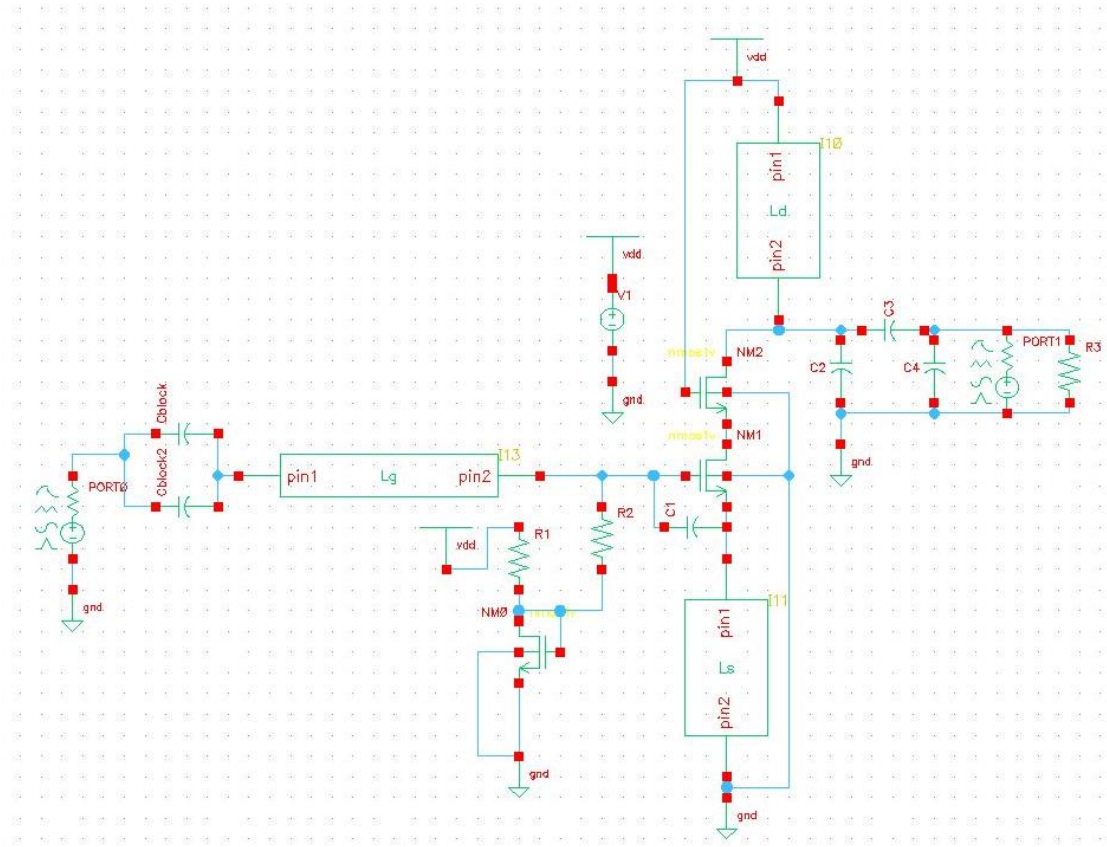


Fig. 1. The Cadence schematic of the LNA.

Hand calculations were done to calculate first pass values of the components shown in Fig. 1. The first step was to find an inductor with the largest quality factor at 2.1GHZ. This was done using parametric sweeps and was found to be L_d = 14.52 nH with R_p =

814.1Ω. Fig. 2. shows the π-model of this inductor and Fig. 3. shows the voltage of the input of the non-ideal inductor as a function of frequency when a current of 1mA is applied (used to find R_p of the inductor).

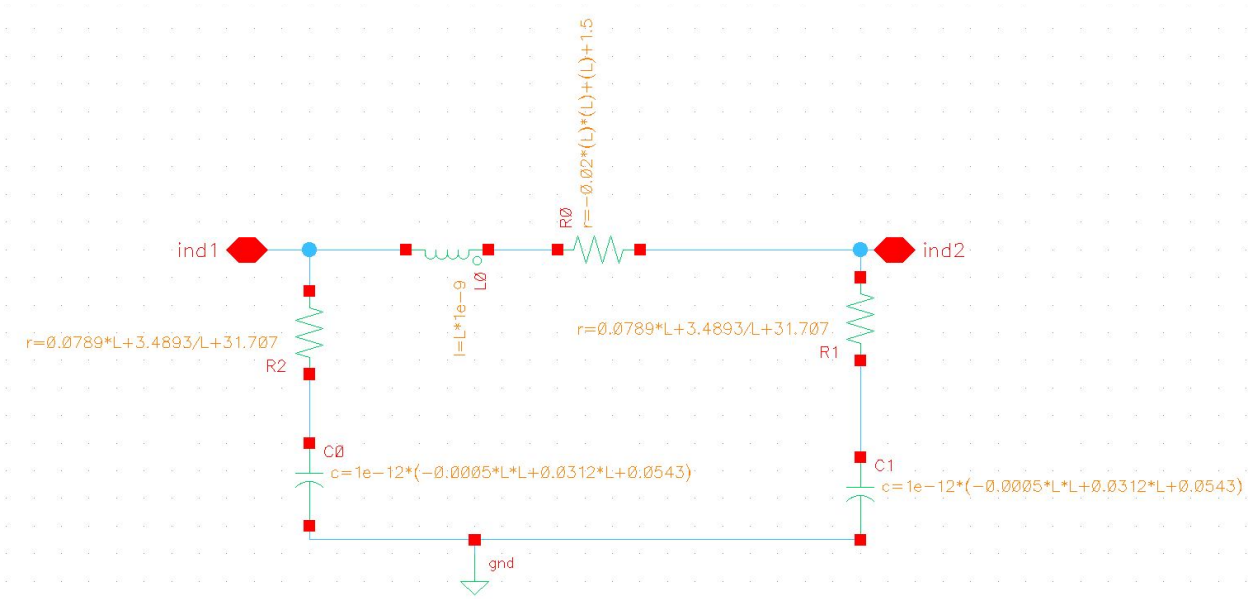


Fig. 2. The π-model of the inductors used in the LNA. This is abstracted as rectangular symbols labelled: 'Lg,' 'Ls,' and 'Ld.'

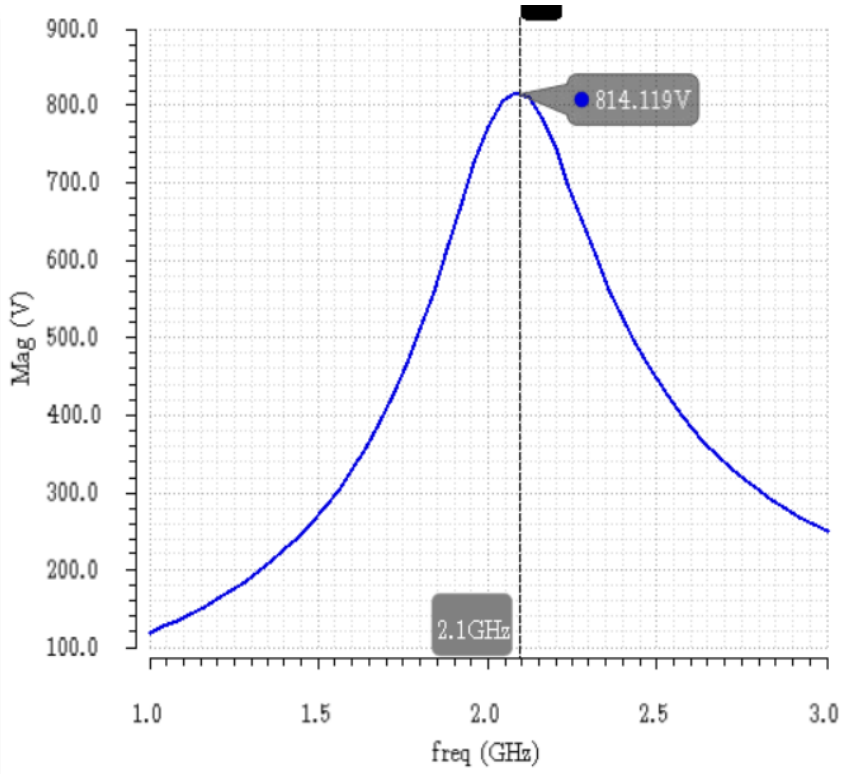


Fig. 3. The voltage of the input of the inductor as a function of frequency when a current of 1mA is applied.

From this information, the other parameters of the circuit were calculated as shown in the appendix. Table 1 contains the first pass values.

Parameter	Values
C2	C = 31.65fF
C3	C = 6.8pF
L_s	L = 0.2nH
L_g	L = 14.2nH
C1	C = 368fF
NM1, NM2	L = 45nm, W = 200μm
Cblock	C = 20pF
R2	R = 20kΩ

Table 1. First pass values.

III. SIMULATION RESULTS

In order to achieve the best performance possible, multiple iterations of parameter sweeps were done. The final values vary substantially from the calculated ones. Table 2 and Table 3 contain the overview and DC operating points of each component respectively.

Components	Values
NM0	L = 45nm, W = 722nm
NM1, NM2	L = 45nm, W = 192μm
Cblock, Cblock2	C = 20pF
C1	C = 10fF
C2	C = 18.7fF
C3	C = 10pF
C4 (C_L)	C = 50fF
L_g	L = 11.8nH
L_s	L = 700pH
L_d	L = 11.8nH
R1	R = 2kΩ
R2	R = 10kΩ
R3	R = 120Ω

Table 2. The values of each component used.

Components	Characteristics	Values
NM0	gm	629.9μS
	V_{ds}	799.2mV
	V_{dsat}	175.0mV
	I_d	100.4μA
NM1	gm	121.8mS
	V_{ds}	224.3mV
	V_{dsat}	154.4mV
	I_d	16.8mA
NM2	gm	140.7mS
	V_{ds}	562.0mV
	V_{dsat}	135.2mV

Table 3. The DC operating points of the transistors.

Fig. 4-9 are performance plots of the device when operating at 2.1GHz. The results are tabulated in Table 4.

Specification	Value
S11	-16.028dB
S12	-46.09dB
S21	15.051dB
S22	-10.48dB
Noise Factor	3.527dB
IIP3	-4.72dBm

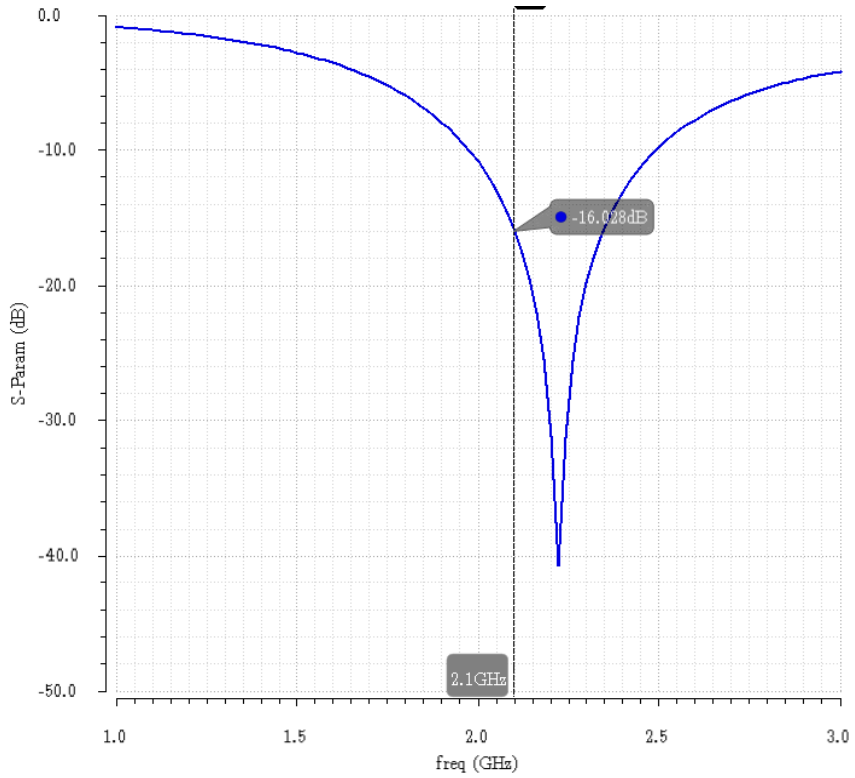


Fig. 4. A plot of S11 between 1GHz and 3GHz.

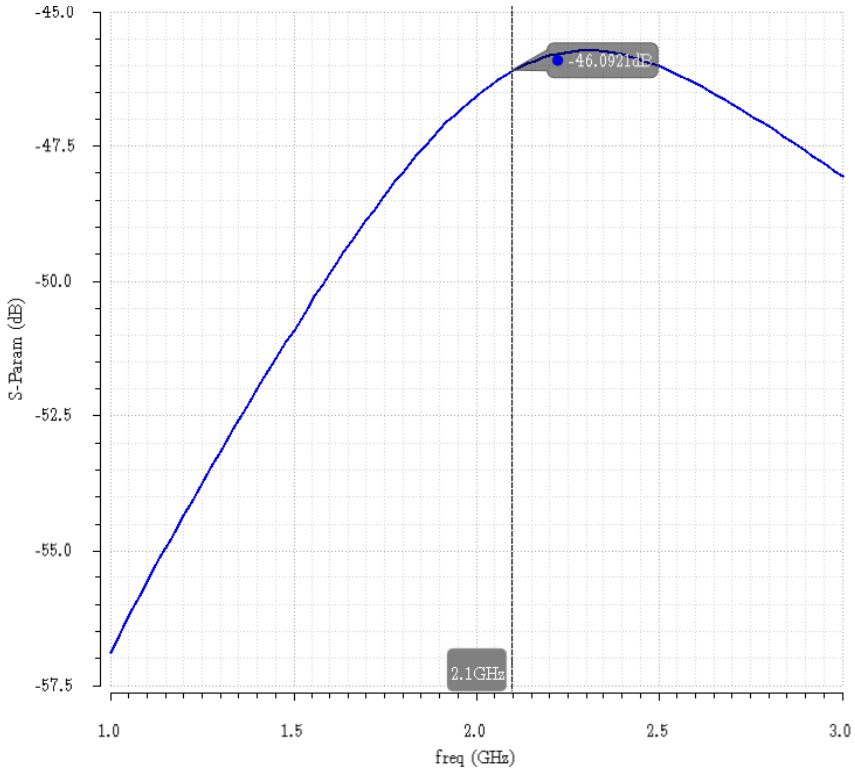


Fig. 5. A plot of S12 between 1GHz and 3GHz.

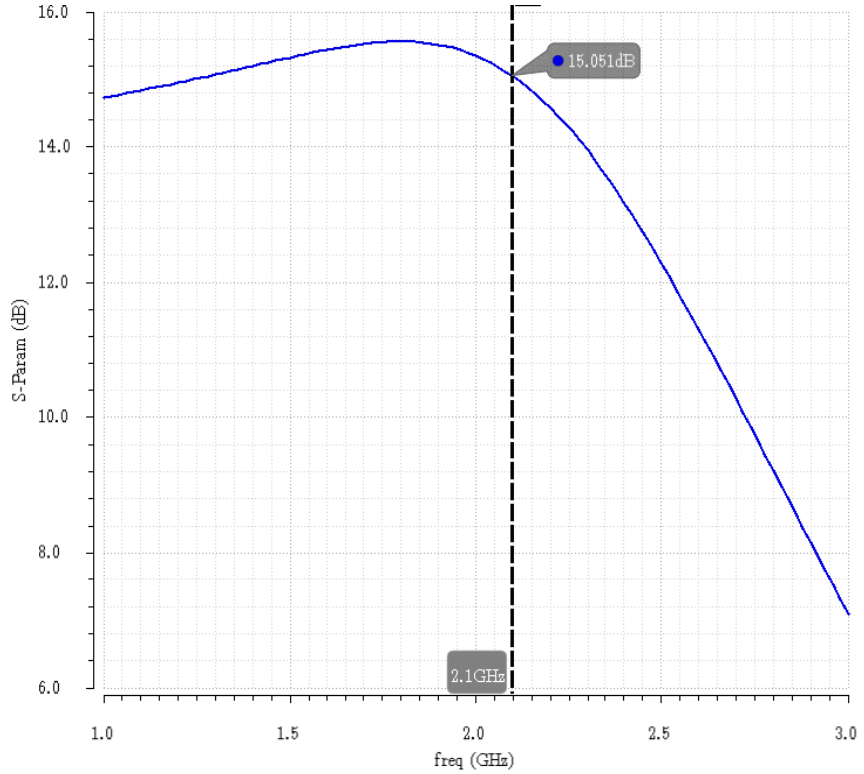


Fig. 6. A plot of S21 between 1GHz and 3GHz.

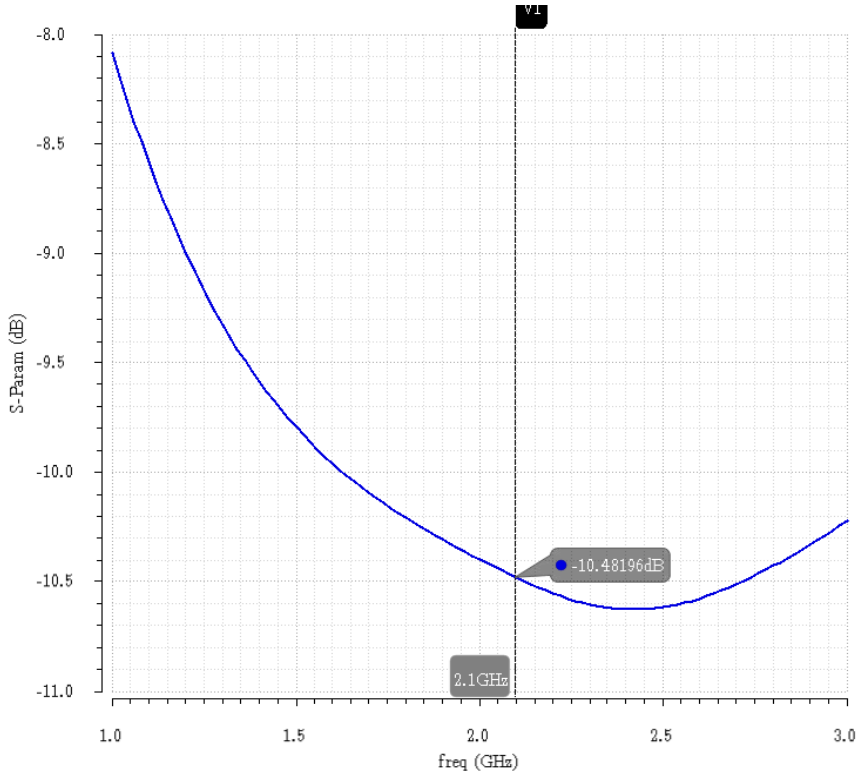


Fig. 7. A plot of S22 between 1GHz and 3GHz.

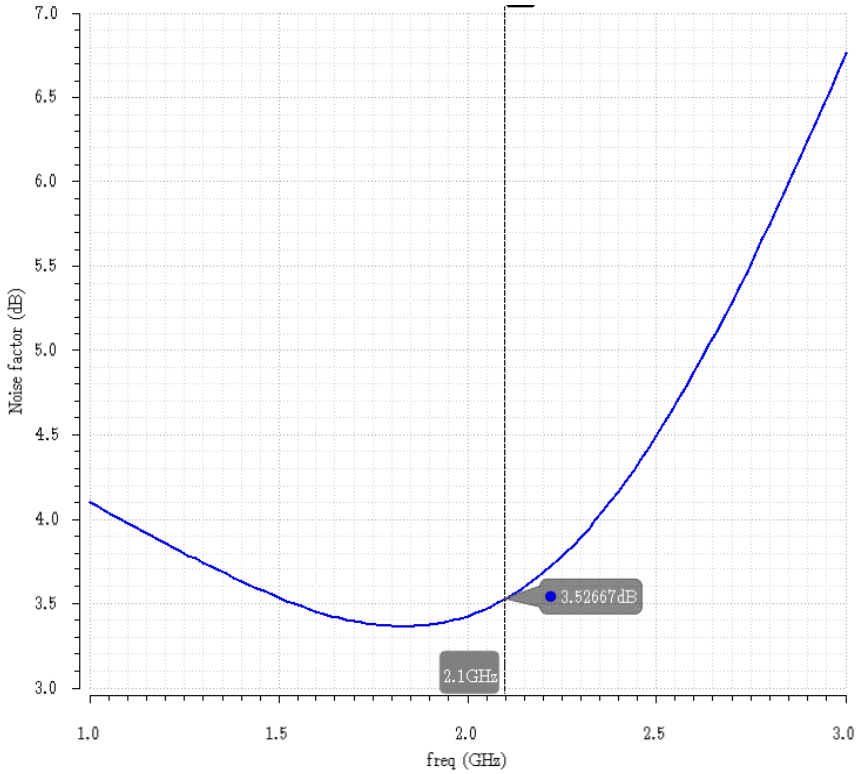


Fig. 8. A plot of the noise factor between 1GHz and 3GHz.

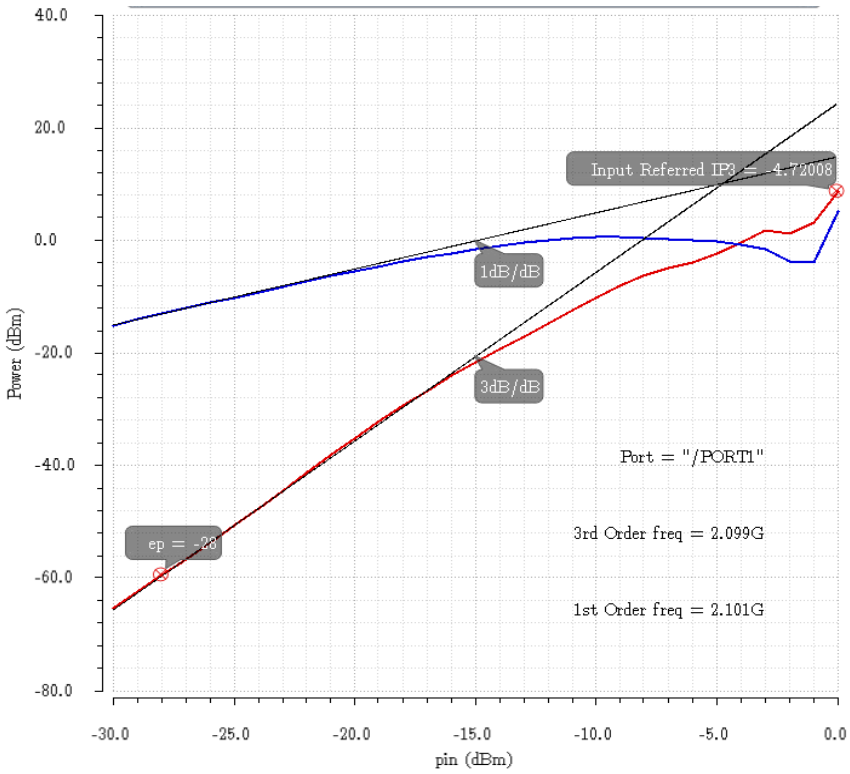


Fig. 9. A plot showing the PIIP3 performance.

This circuit draws 16.8mA of current and thus consumes 16.8mW. The gain (S21) is proportional to the width of NM1 and NM2. Unfortunately, the same is true for the current, as shown in Fig. 10. The gain was also found to be inversely proportional to L_s while the IIP3 value is proportional to that value. In order to optimize power, the size of L_s was decreased until the IIP3 was near -5dBm. This increased the gain and allowed the width of the transistor to be decreased. Although the power consumption is large, this was the best value possible.

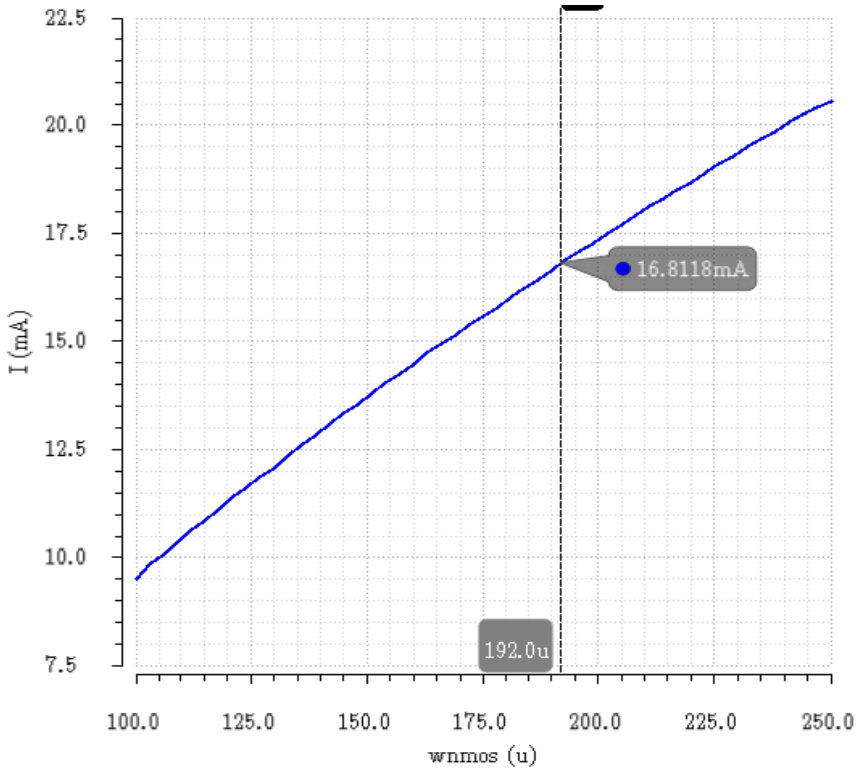


Fig. 10. A plot showing the current through the cascaded NMOS as a function of the transistor width.

IV. DISCUSSION

Every requirement was met except for the noise factor. Using this topology, it was found that reducing the noise will cause the other specifications to no longer be met.

V. ACKNOWLEDGEMENT

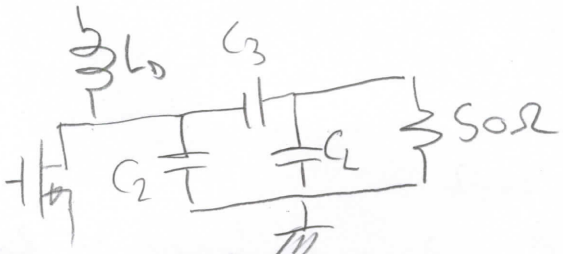
I would like to acknowledge Sam Lightbody for helping me overcome several challenges while working on this project. Without his support, it would not have been possible to achieve these results.

REFERENCES

[1] B. Razavi, *RF microelectronics*. Pearson Education, Inc., 2012.

Hand Calculations

- Top segment of circuit:

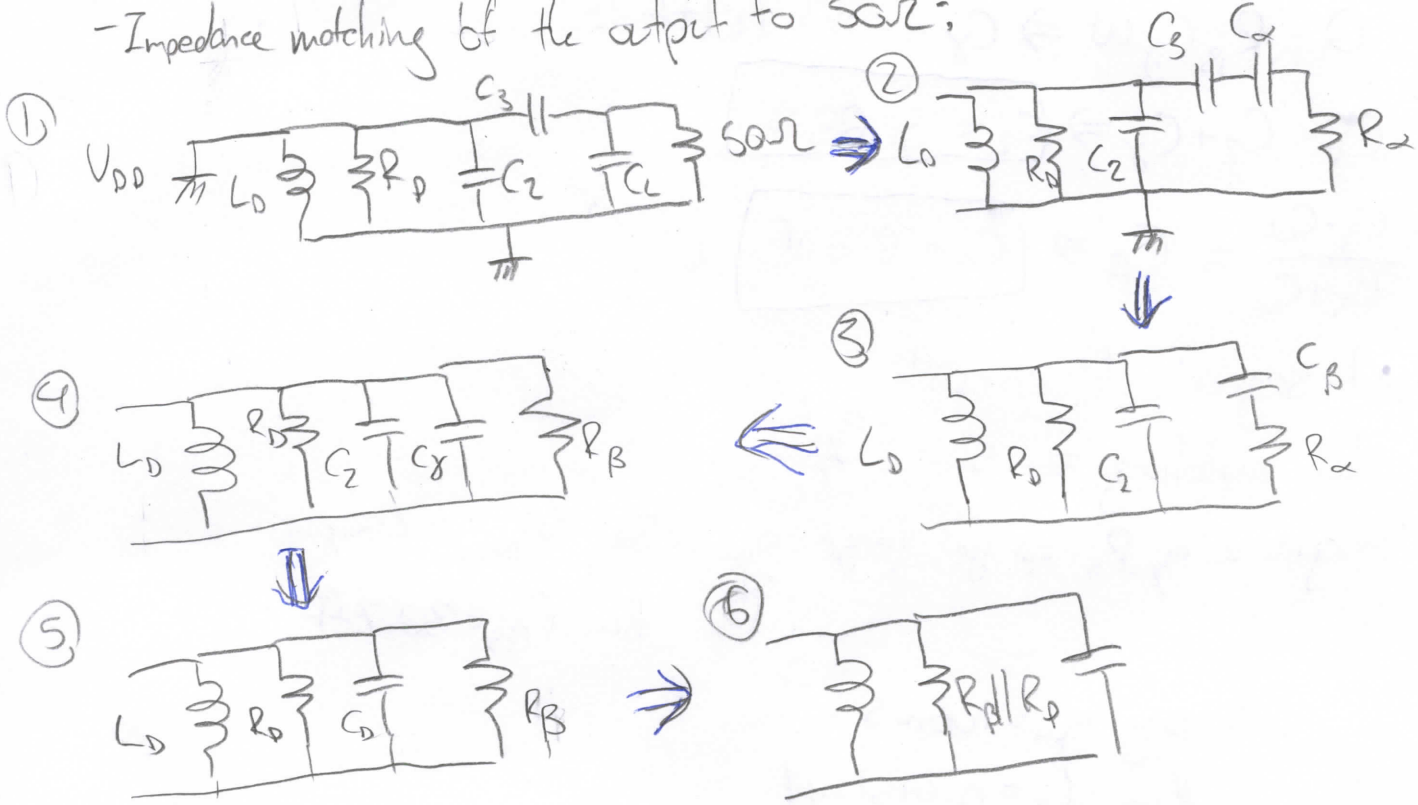


- from simulation we know:

$L = 14.52\,nH$

$R_p = 814.1\,\Omega$

- Impedance matching of the output to 50Ω:



$R_p \| R_\beta = 50$

$\frac{R_p R_\beta}{R_p + R_\beta} = 50 \Rightarrow R_\beta = 53.2723\,\Omega$

$C_D = \frac{1}{\sqrt{LC}} \Rightarrow C_D = 395.6\,fF$

$C_L = 50fF \quad R = 50\Omega$

$Q = R_p C\omega = 0.032987$

$C_2 = 46pF$

$R_2 = 50\Omega$

$R_\beta = 53.2773$ and $R_2 = 50\Omega$

(R_2 is in series with C_β and is transformed to R_β)

$R_\beta = (Q^2+1)R_S \Rightarrow Q = 0.0255824 = \frac{1}{C_\beta R_2 \omega} \Rightarrow C_\beta = 5.925pF$

$Q = R_\beta C_\gamma \omega \Rightarrow C_\gamma = 363.949fF$

$C_D = C_2 + C_\gamma \Rightarrow C_2 = 31.65fF$

$\frac{C_3 \cdot C_2}{C_3 + C_2} = C_\beta \Rightarrow C_3 = 6.8pF$

- Input segment of circuit

for matching $\Rightarrow 50 = \frac{g_m L_S}{C_{GS}}$

gain $= g_m R_S \Rightarrow$ get large g_m. Say $W_{nmos} = 260\mu m$

then $C_{GS} = 30.2fF$

say $g_m = 100mS$

then $L_S = 0.0151nH$

↳ too small → use minimum size: 0.2nH

and iterate in simulation to satisfy $50 = \frac{g_m L_S}{C_{GS}}$

$\omega_o = \frac{1}{\sqrt{(L_g + L_S)C_{GS}}} \Rightarrow L_g = 190nH \leftarrow$ too big must iterate

increase C_{GS} by adding capacitor (also helps with 50Ω matching)

So using $50 = \frac{g_m L_s}{C_{GS}} \Rightarrow$ the additional capacitance is 368fF

total $C_{GS} = 400fF$

thus $L_g = 14.2nH$

Noise Factor:

$$NF = 1 + g_{m1} R_S \gamma \left(\frac{\omega_0}{\omega_T}\right)^2 \quad \in ([1] B. Razavi)$$

and $$R_S = \left(\frac{C_{GS1}}{C_{GS1} + C_{pad}}\right)^2 L_S \omega_T$$

$$\omega_T = \frac{g_m}{C_{GS}}$$

reduce noise by reducing L_S (already done - L_S at minimum)

IIP3: gets better as L_S is increased. Will most likely increase L_S to meet all specs.

C_{block}: make as large as possible (20pF)

R_2: also make large (20kΩ)

Current mirror: sweep values to know optimal gate voltage