Voltage-Controlled Oscillator Design

Dante St. Prix 37764157

***Abstract* – This report outlines the design process of a voltage-controlled oscillator (VCO) with a center frequency of 13GHz and its performance. The tuning range and power consumption were optimized to be 40% and 4.2mW respectively at the expense of phase noise.**

I. Introduction

IT is crucial to design high-performance VCOs as they output signals that are mixed with the input RF signal. A good design with low phase noise will allow the receiver to provide a relatively unaltered signal to the ADC for further processing. Having a large tuning range increases the versatility of the oscillator.

II. CALCULATION PROCESS

The NMOS CCVCO topology with capacitor banks was chosen. This design allows for a large tuning range without increasing phase noise by an excessive amount. The design is shown in Fig. 1.

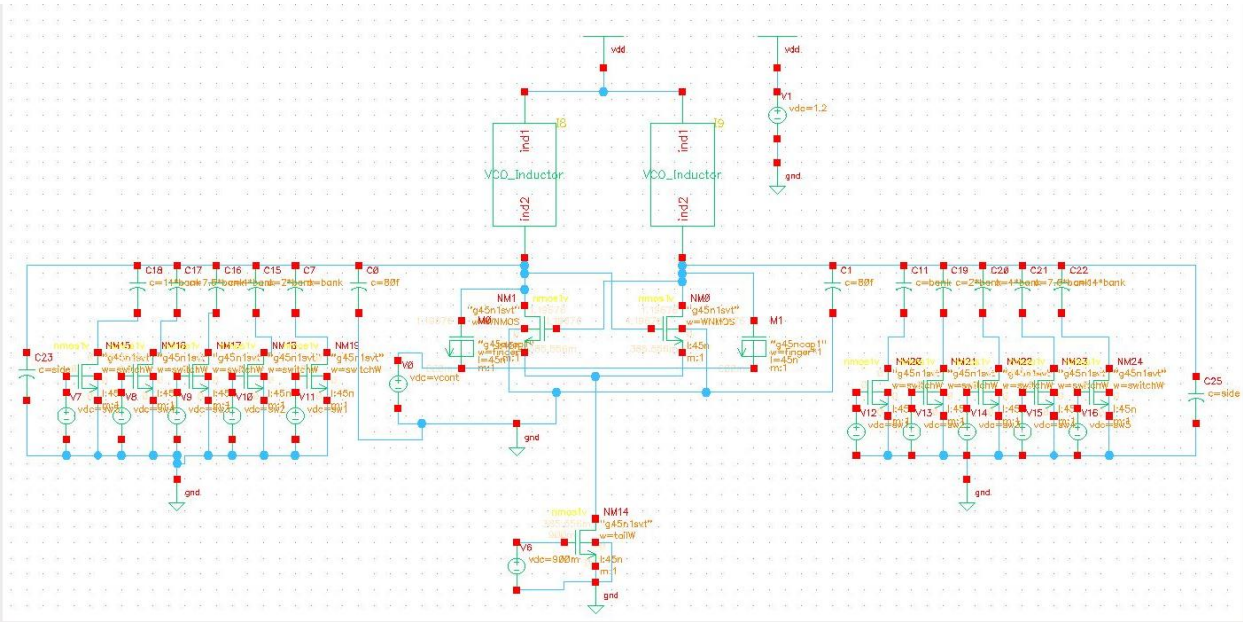

Fig. 1. The Cadence schematic of the VCO.

The first step was to find an inductor with the largest quality factor at 13GHZ possible. This was done using parametric sweeps and was found to be L = 350pH. Fig. 2. shows the π-model of this inductor.

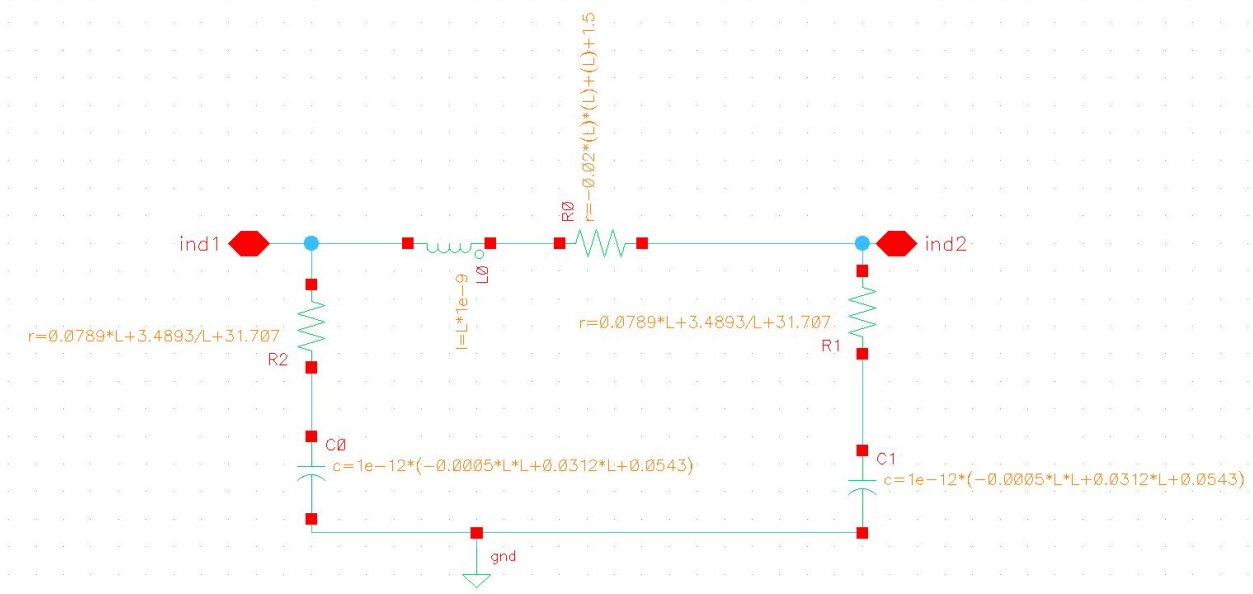

Fig. 2. The π-model of the inductors used in the VCO. This is abstracted as a rectangular symbol below VDD in the schematic in Fig. 1.

From this information, the other parameters of the circuit were calculated as shown in the appendix. Table 1 contains the calculated values. The widths of the transistors are not contained here as they require current sweeps to be known.

Parameter	Values
I_{ss}	>1.325mA
Varactor Capacitance	>184.88fF
Bank Capacitance	11.99fF

Table 1. First pass calculated values.

III. SIMULATION RESULTS

In order to achieve the best performance possible, multiple iterations of parameter sweeps were done. The final values vary substantially from the calculated ones. Table 2 and Table 3 contain the overview and DC operating point of each component respectively.

Components	Function	Values
NM0, NM1	Center NMOS	L = 45nm, W = 15µm
NM2	Tail Current Source	L = 45nm, W = 19.4µm
NM3, NM4, NM5, NM6, NM7, NM8, NM9, NM10, NM11, NM12	Capacitor Bank Switches	L = 45nm, W = 22.56µm
C0, C1	Capacitor Bank 1	C = 13fF
C2, C3	Capacitor Bank 2	C = 26fF
C4, C5	Capacitor Bank 3	C = 52fF
C6, C7	Capacitor Bank 4	C = 97.5fF
C8, C9	Capacitor Bank 5	C = 182fF
Var1, Var2	Varactor	L = 45nm, W = 55µm
L1	Inductor at V_{dd}	L = 350pH

Table 2. The function and values for each circuit component used.

Components	Characteristics	Values
M1, M2	gm	12.1mS
	V_{ds}	811.207mV

	V_{dsat}	164.806mV
NM2	gm	15.2mS
	V_{ds}	385.556mV
	V_{dsat}	228.877mV
	I_d	3.5049mA
Differential Output Waveform	Amplitude	712mV
Total Power Consumption	Power	4.2mW

Table 3. The DC operating point of the circuit when every switch of the capacitor bank is closed.

Fig. 3. shows that the phase noise at 1MHz offset from the center frequency is -92.5dBc/Hz. Table 4. Shows that much of the phase noise originates from the flicker noise of the tail current source.

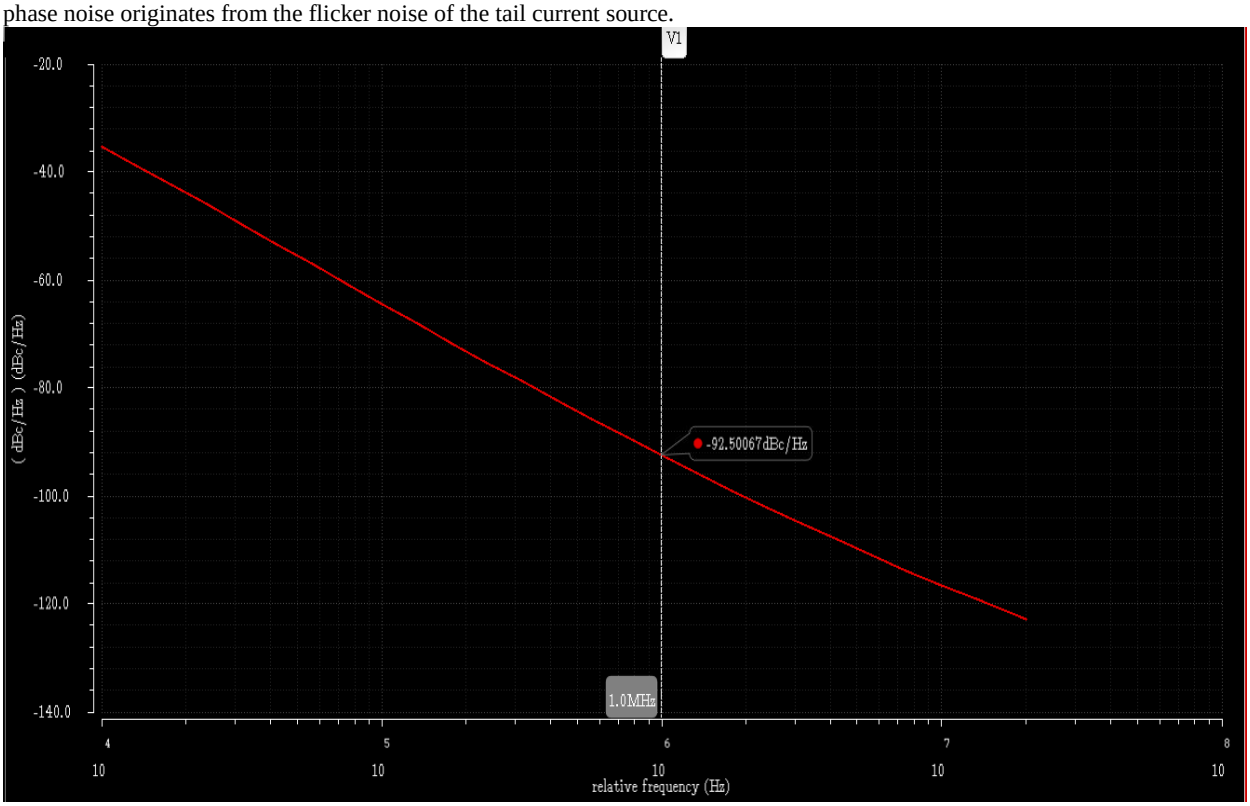

Fig. 3. A plot of the phase noise at 1MHz offset from the center frequency of 13GHz.

Device	Param	Noise Contribution	% Of Total
/NM14	fn	3.29725e-11	23.01
/NM0	fn	3.25956e-11	22.75
/NM1	fn	3.25953e-11	22.75
NM0.xrg.r1	thermal_noise	1.49674e-11	10.45
NM1.xrg.r1	thermal_noise	1.49672e-11	10.45
NM14.xrg.r1	thermal_noise	4.04622e-12	2.82
/NM0	id	2.46262e-12	1.72
/NM1	id	2.46246e-12	1.72
/NM14	id	1.49765e-12	1.05
/I9/R0	rn	9.33697e-13	0.65

Spot Noise Summary (in V^2/Hz) at 1M Hz Sorted By Noise Contributors

Table 4. The PSS analysis noise summary. NM14 is the tail current source and NM0 and NM1 are the central NMOS's.

Fig. 4, 5 and 6 show the phase noise at a spot frequency of 1MHz offset at three capacitor bank combinations (with vcont being swept).

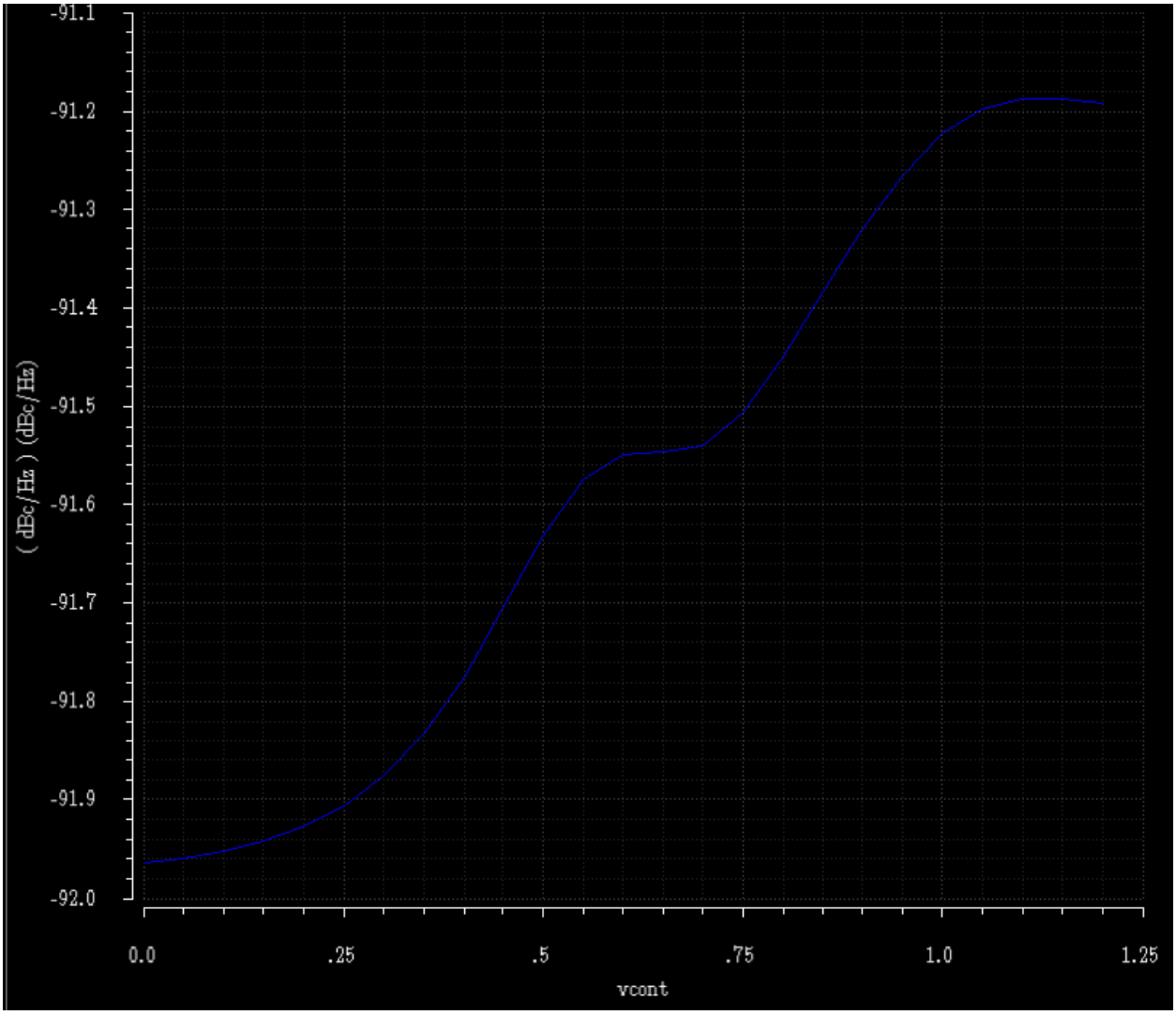

Fig. 4. The spot phase noise near 10.4GHz as a function of vcont.

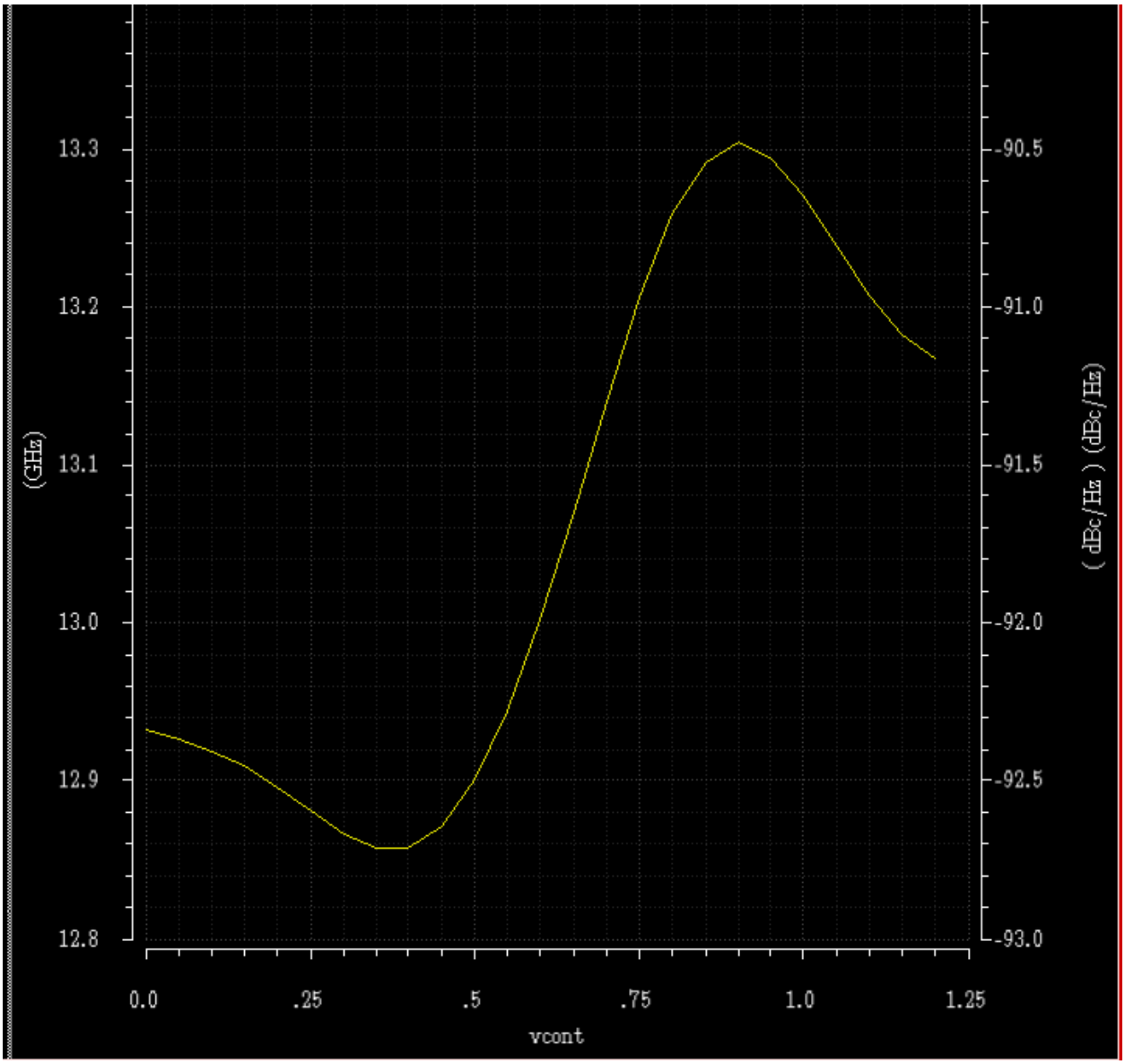

Fig. 5. The spot phase noise near 13GHz as a function of vcont.

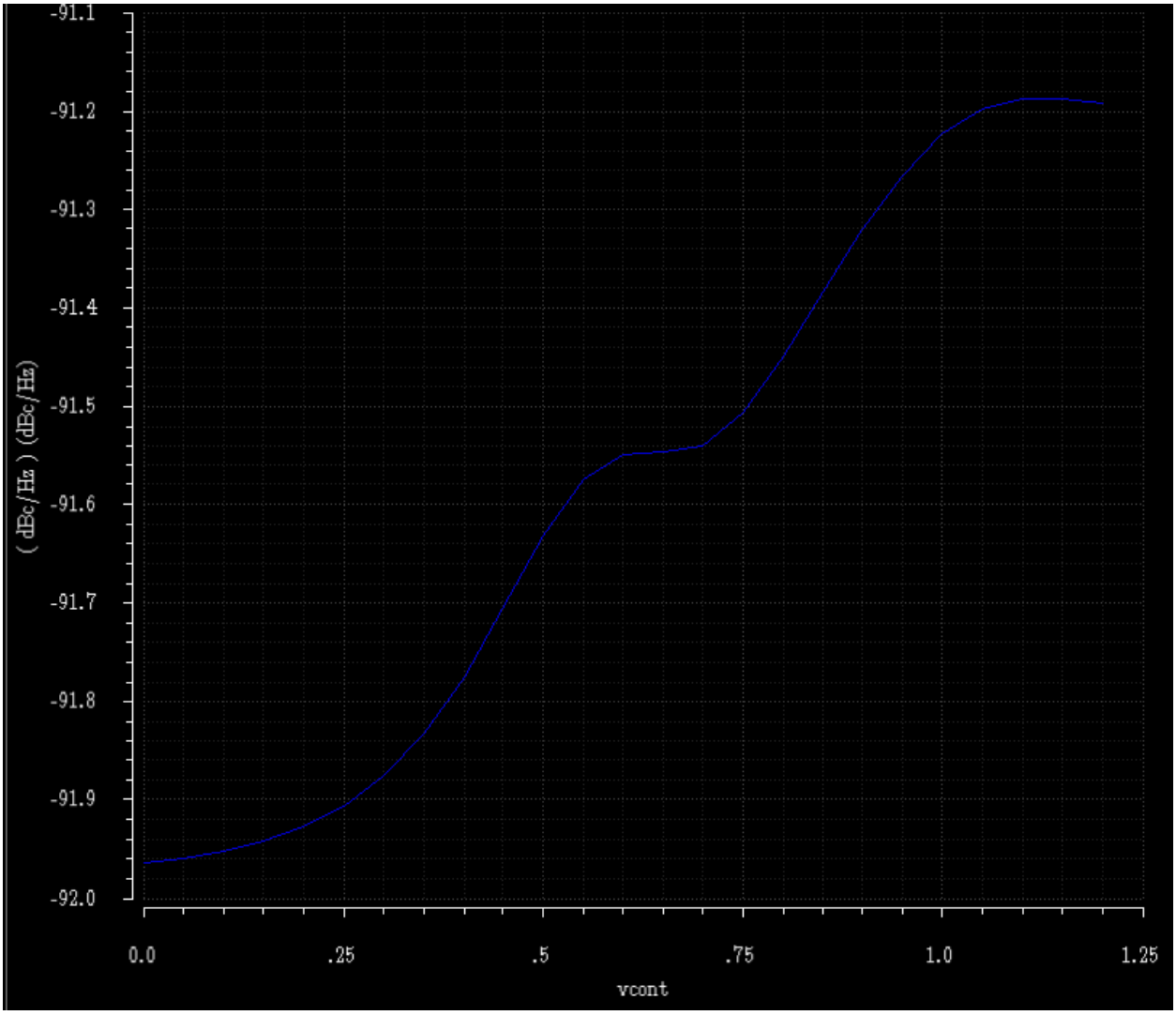

Fig. 6. The spot phase noise near 15.4GHz as a function of vcont.

Fig.7. shows the frequency of oscillation as a function of vcont (x-axis) with every toggle combination of the capacitor bank switches. There are no blind spots between 10.4GHz and 15.6GHz. The VCO gain near 13GHz is 642MHz/V. This gain becomes greater at higher frequencies and smaller at lower frequencies.

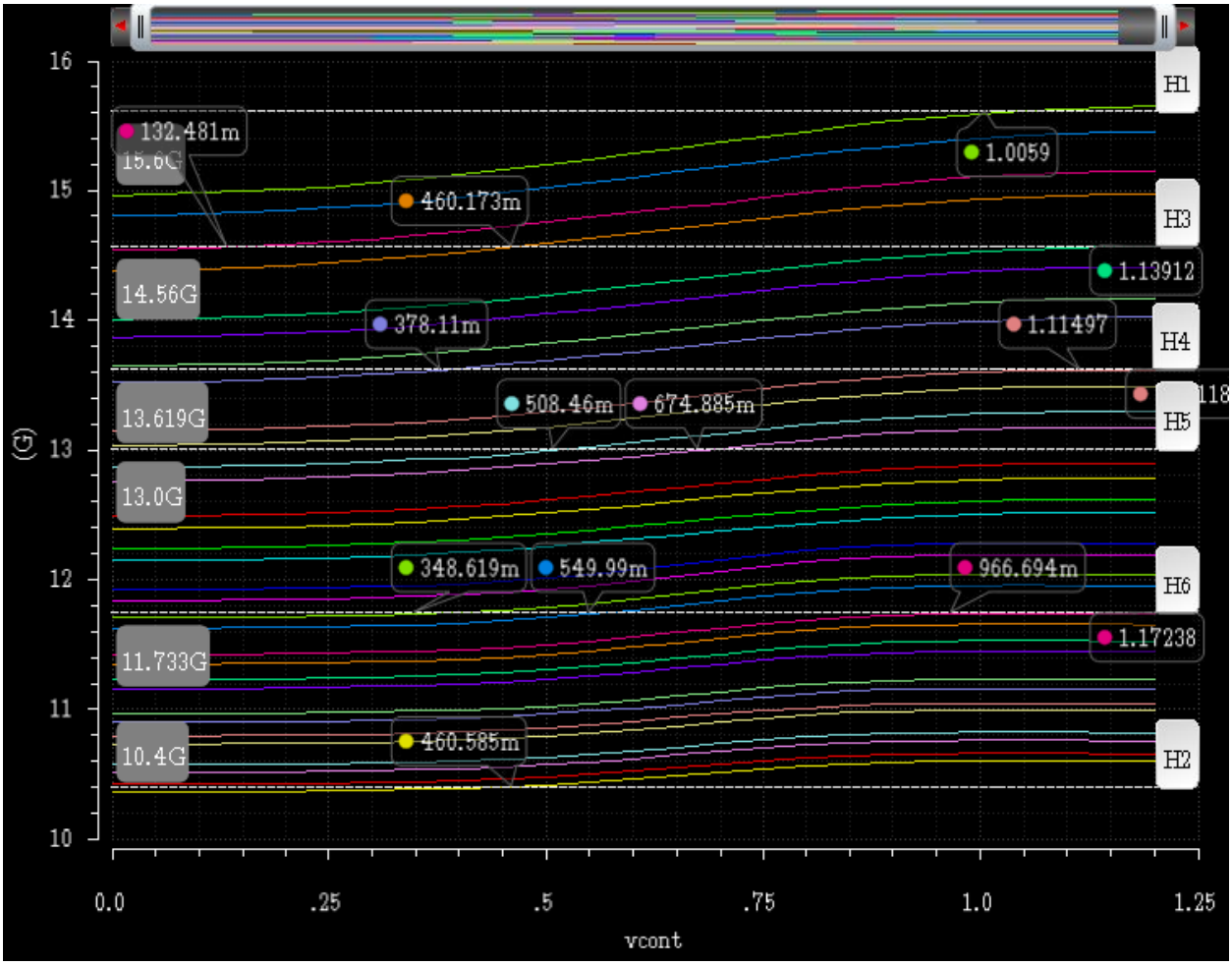

Fig. 7. The frequency of oscillation as a function of vcont. Each curve represents a combination of switch states in the capacitor bank.

Fig. 8 and Fig. 9 show the singled-ended and differential output waveforms at 13GHz respectively.

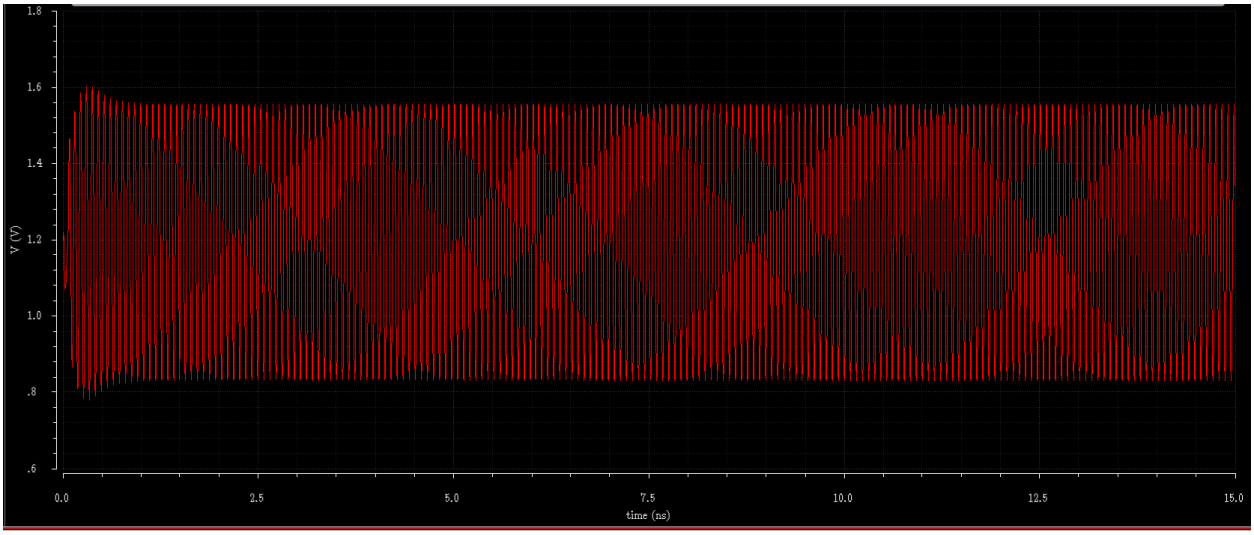

Fig. 8. The single-ended output at 13GHz.

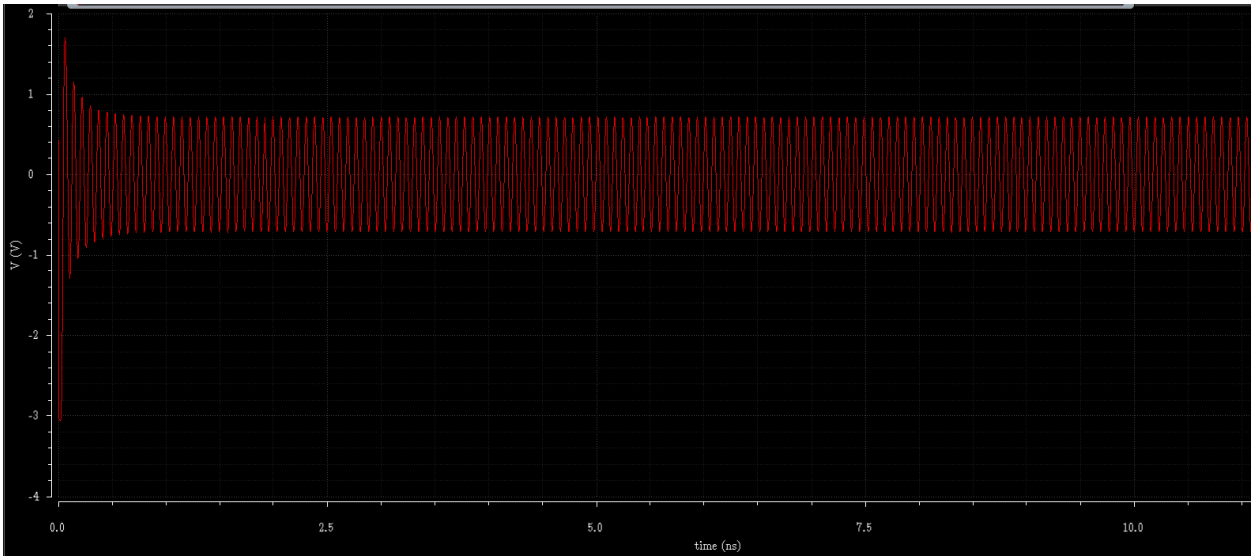

Fig. 9. The differential output at 13GHz.

IV. DISCUSSION

It was not possible to meet every specification with this topology. This is because of the limitations of the 45-nm process, which reduced the quality factor. In this design, tuning range and power consumption were optimized at the expensive of phase noise. If phase noise were to be improved, then the width of the tail current source should be increased. This would increase the current and consume more power.

During analysis, it was discovered that the greatest source of phase noise is the tail current source. One conceivable way to improve the phase noise may be to place an inductor at the drain of the tail current source and a capacitor between that point and ground that will resonate at 26GHz. This, however will most likely reduce the tuning range.

Voltage-Controlled Oscillator
Hand Calculations.

- From parametric sweeps

$L = 350\,pH$

$R_s = 1.84755\,\Omega$

$R_{sub} = 41.704\,\Omega$

$C_{sub} = 65fF$

1) Find R_p

$Q_s = \frac{L\omega}{R_s}$

$R_{P1} = (Q^2+1)R_s = 444.218\,\Omega$

$C_s = 3.25\times10^{-14}\,F$

$Q_{cap} = \frac{1}{2C_sR_{sub}\omega} = 4.516$

$R_{P2} = (Q^2+1)R_s = 1784.7\,\Omega$

$\frac{C_{sub}\cdot C_{sub}}{C_{sub}+C_{sub}} = C_s$

$\Rightarrow$

$R_p = 355.686\,\Omega$

overall $Q \approx 8$ for circuit

2) $g_m R_p \geq 1$ (for startup condition)

thus

$g_m > 2.811\,mS$

3) To maintain the transistors in saturation

$V_{DS} > V_{GS} - V_{TH}$

$A = \text{amplitude} = \frac{2}{\pi} I_{bias} \times R_p$

$V_{DS} + A > V_{DD} - A - V_{TH}$

$2A < V_{TH}$

thus $A < \frac{1}{2} V_{TH}$

$I_{SS} = I_{bias} < 1.325mA$ (assuming $V_{TH} \approx 0.6V$)

4) Noise

$$\frac{\pi^2}{R_p} \frac{kT}{I_{SS}} \left(\frac{3}{8}\gamma + 1\right) \frac{\omega_o^2}{4Q^2 \Delta\omega^2}$$

$\Delta\omega = 6.28 \times 10^6$ rad/s

$\omega_o = 81.68 \times 10^9$ rad/s

$\gamma = 2$

$T = 298.25K$

$k = 1.3866 \times 10^{-23}$

$Q \approx 8$

noise < -112 dBc

within 1.325mA

5) Varactor size

$$\omega_o = \frac{1}{\sqrt{LC}} = \frac{1}{\sqrt{L(C_{GS} + 4C_{GD} + C_{DB} + nC_u + C_L + C_{var}}}$$

C_u = bank capacitor

neglect C_{GS}, C_{GD}, C_{DB}

use C_L, C_{var}, C_{bank}

calculate for 15.6GHz and 10.4GHz

15.6GHz: $C_{total} = 2.9738 \times 10^{-13}$ F

10.4GHz: $C_{total} = 6.6912 \times 10^{-13}$ F

$C_L = 80$fF (fixed)

Used capacitance: $C_L + C_s = 80\text{fF} + 32.5\text{fF} = 112.5\text{fF}$

15.6GHz leftover = 184.88fF

10.4GHz leftover = 556.62fF

thus $C_{var} <$ less than 184.88fF since neglecting some parasitic capacitances

5 bank capacitors

go up to 556.62fF − 184.88 = 371.74fF

$31C_u = 371.74$fF (using binary logic)

$11111_b \times C_u = 31C_u$

thus $C_u = 11.99$fF

*This uses default varactor capacitances, not considering changes due to Vcont.

6) Use current vs g_m plot to determine widths of transistors

-increasing W of switches for increased g_{on} (helps with Q) but also increases C_{SD} & C_{DB}.