Dante St. Prix
37764157

Design, Analysis and Simulation of a CMOS Double-Balanced Mixer
EECE 571F

I. Design and Results

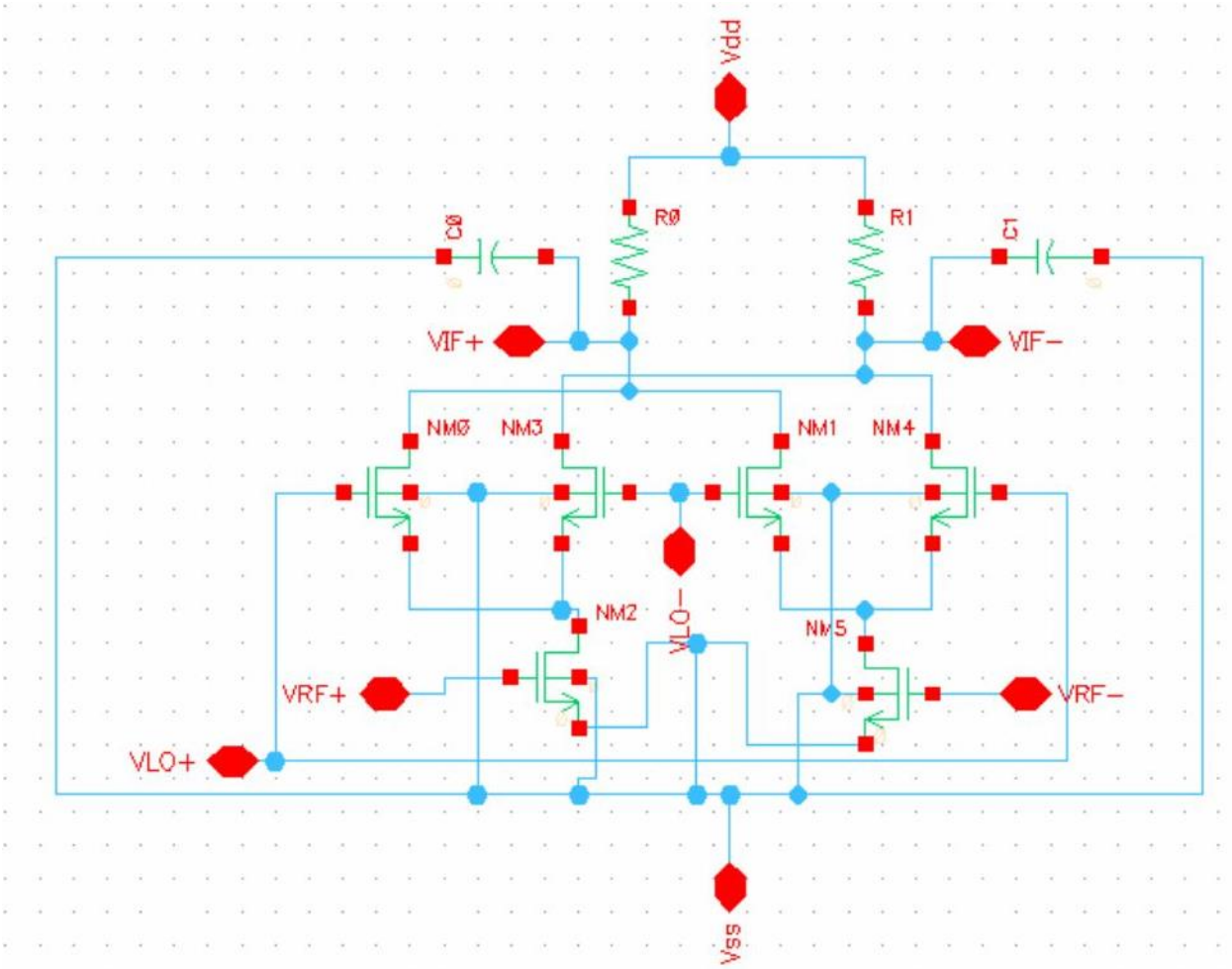


Fig. 1. The schematic of the mixer.

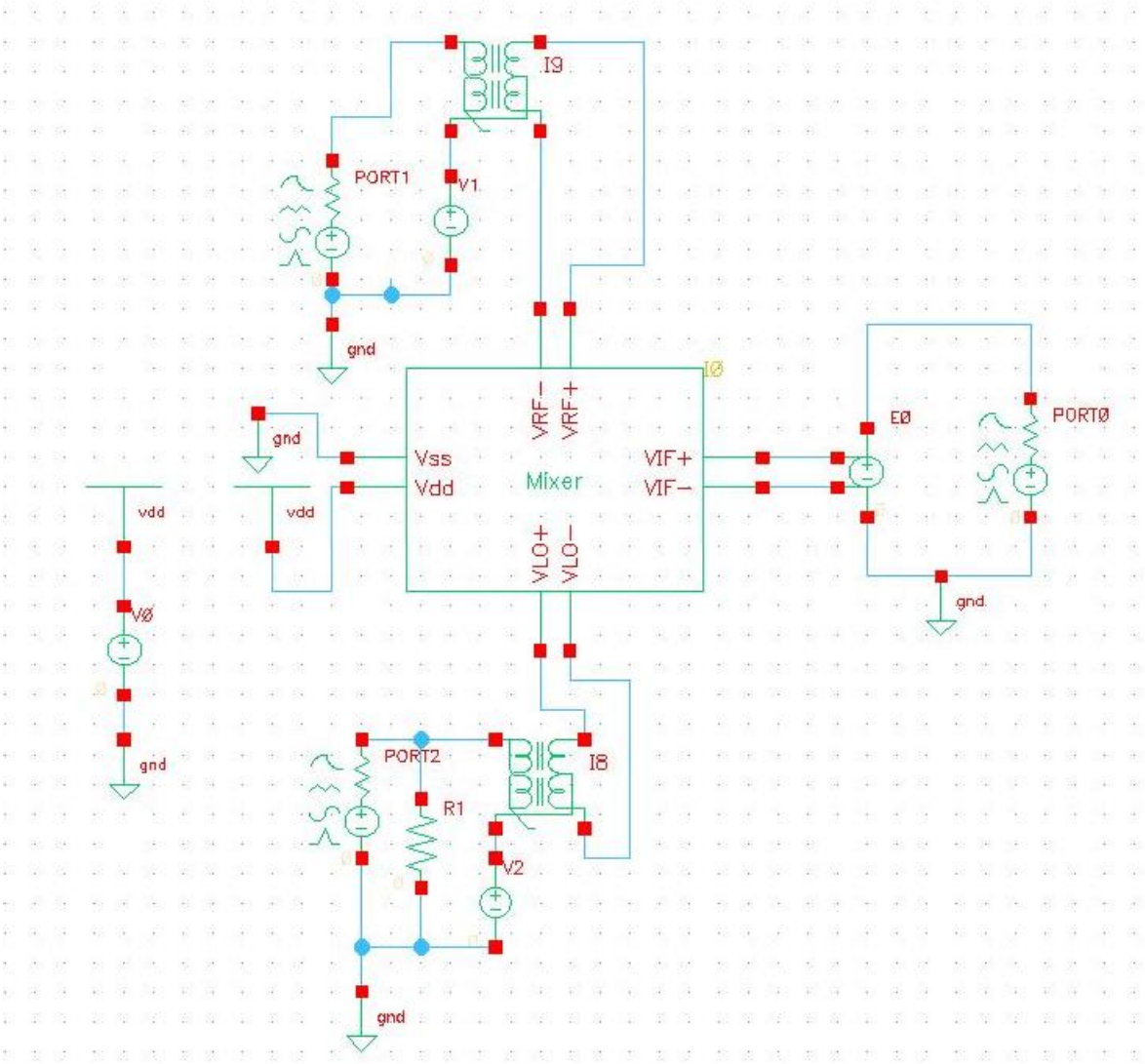


Fig 2. The schematic of the inputs and outputs to the mixers (abstracted as a symbol in Cadence).

Table 1 – The component Parameters

Components	Function	Values
R0, R1	Drain Resistor	R = 44.14Ω
NM0, NM1, NM3, NM4	LO Transistor	L = 45nm, W = 160µm
NM2, NM5	RF Transistor	L = 45nm, W = 271µm
C0, C1	Load Capacitor	C = 50fF

Table 2 – The DC Operating Points

Components	Characteristics	Values
NM0, NM1, NM3, NM4	gm	120.1mS
	V_{ds}	330.7mV
	V_{dsat}	165.4mV
NM2, NM5	gm	40.8mS
	V_{ds}	66.1mV
	V_{dsat}	341.4mV
	I_d	36.4mA

Local Oscillator	Amplitude	500mV
RF Input	Amplitude	10mV

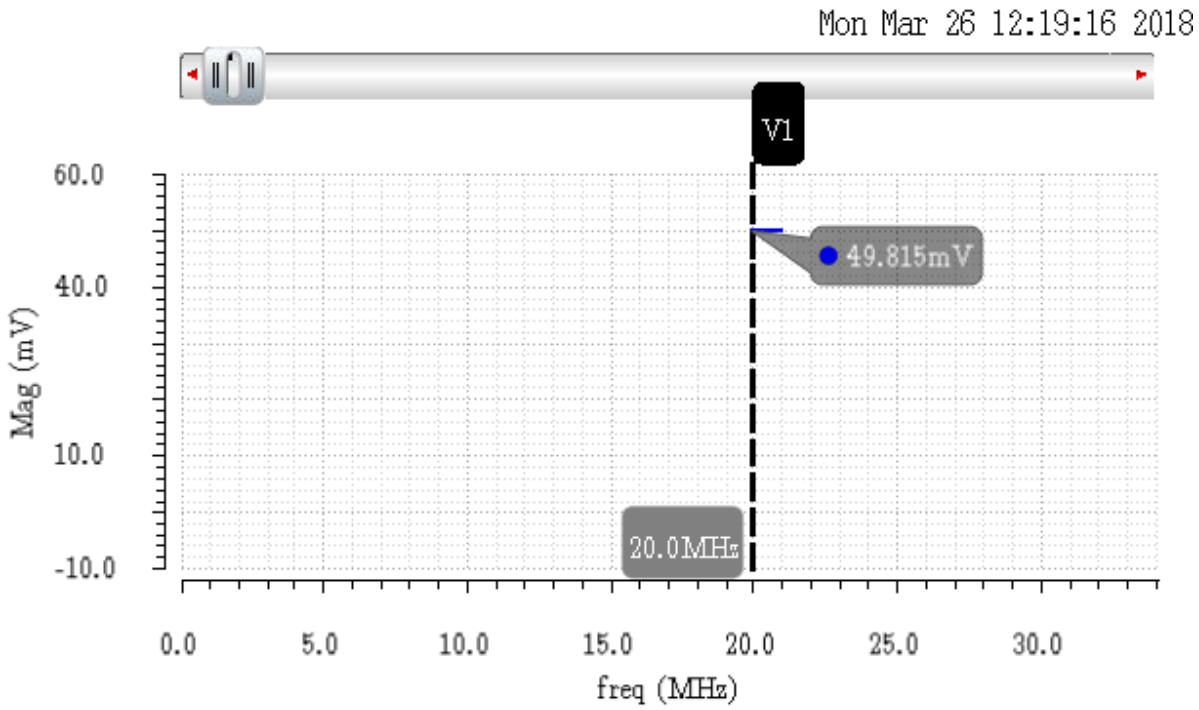


Fig. 3. The graph of the magnitude of the IF signal when the input RF signal has a magnitude of 10mV.

Based on Fig. 3. the conversion gain is determined to be 4.9815 (13.948dB).

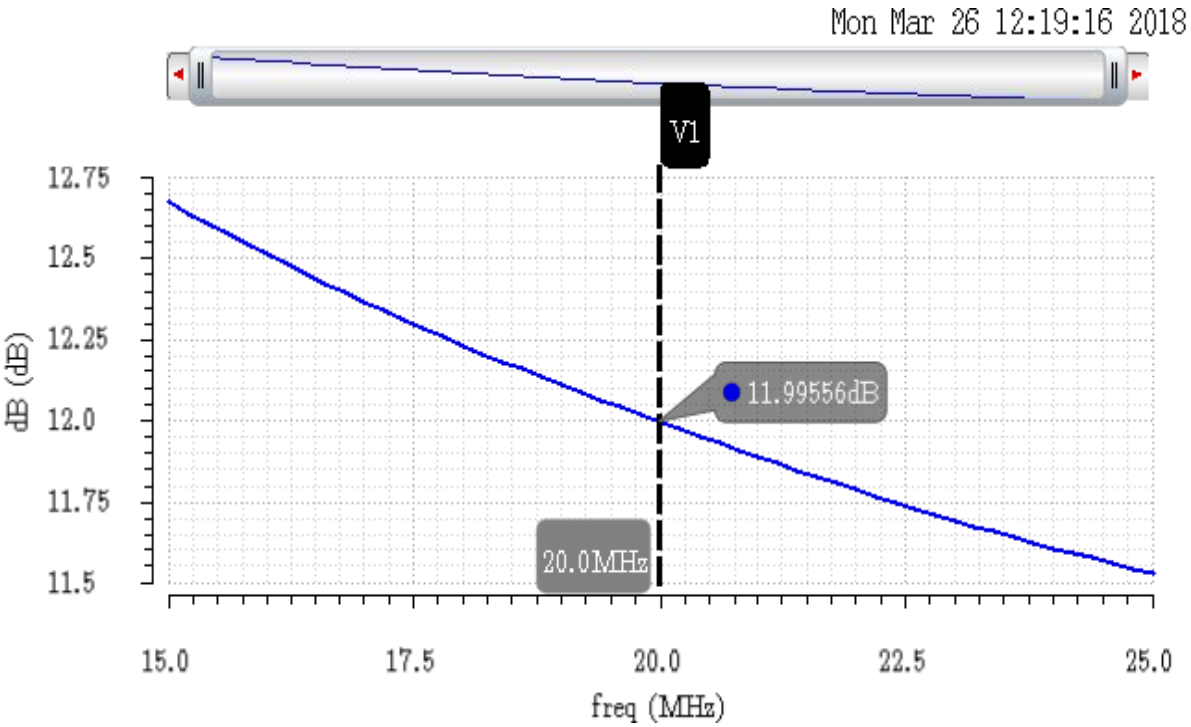


Fig. 4. The noise figure of the device near 20MHz.

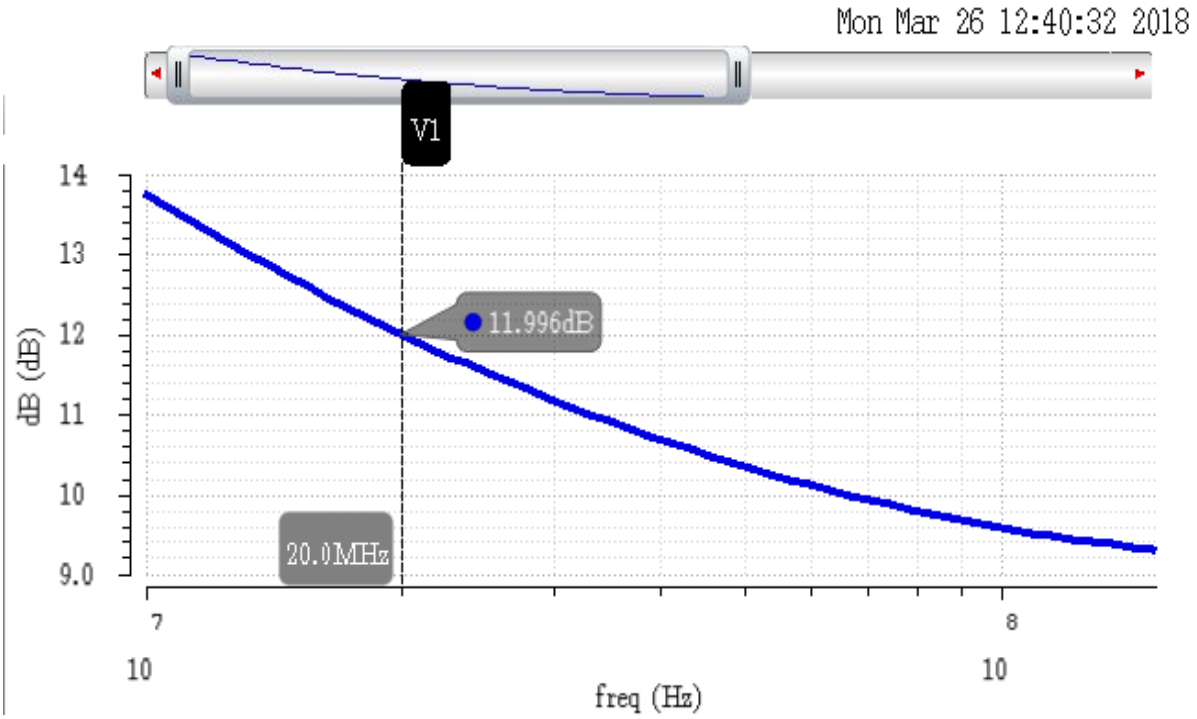


Fig. 5. The noise figure of the device between 10MHz and 150MHz.

The mixer was designed to have a noise figure of 11.995dB at 20MHz.

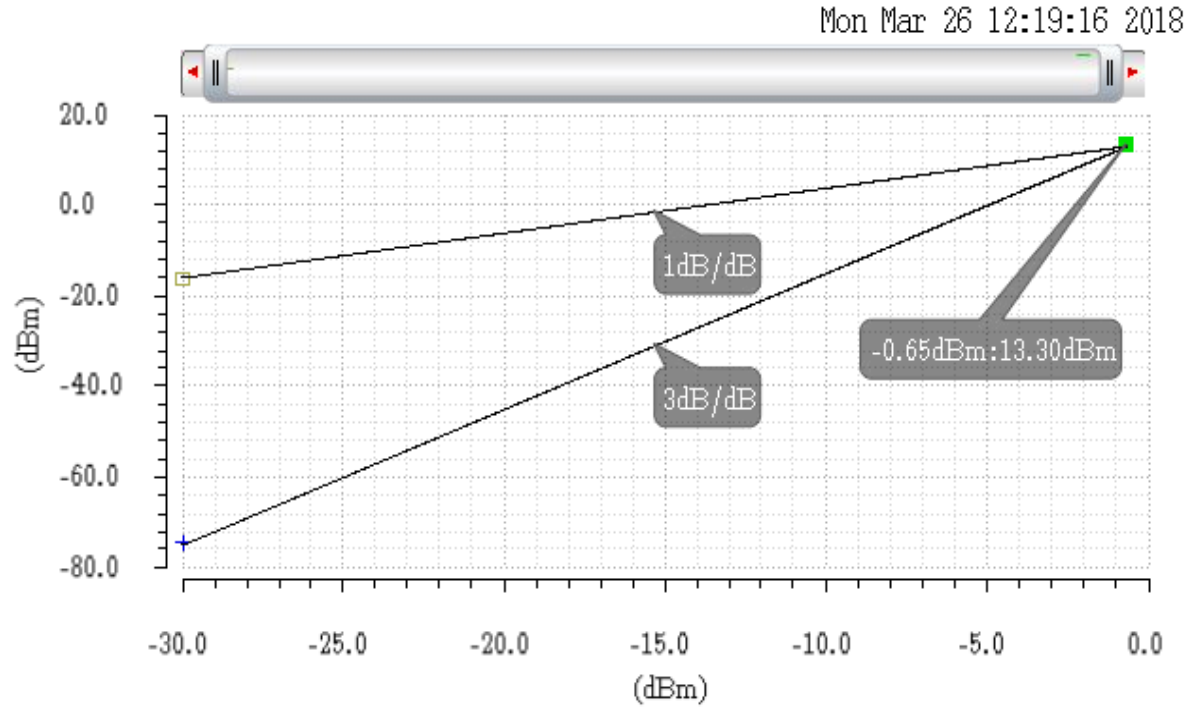


Fig. 6. The results of the IP3 analysis.

Based on Fig. 6, the PIIP3 is -0.65dBm.

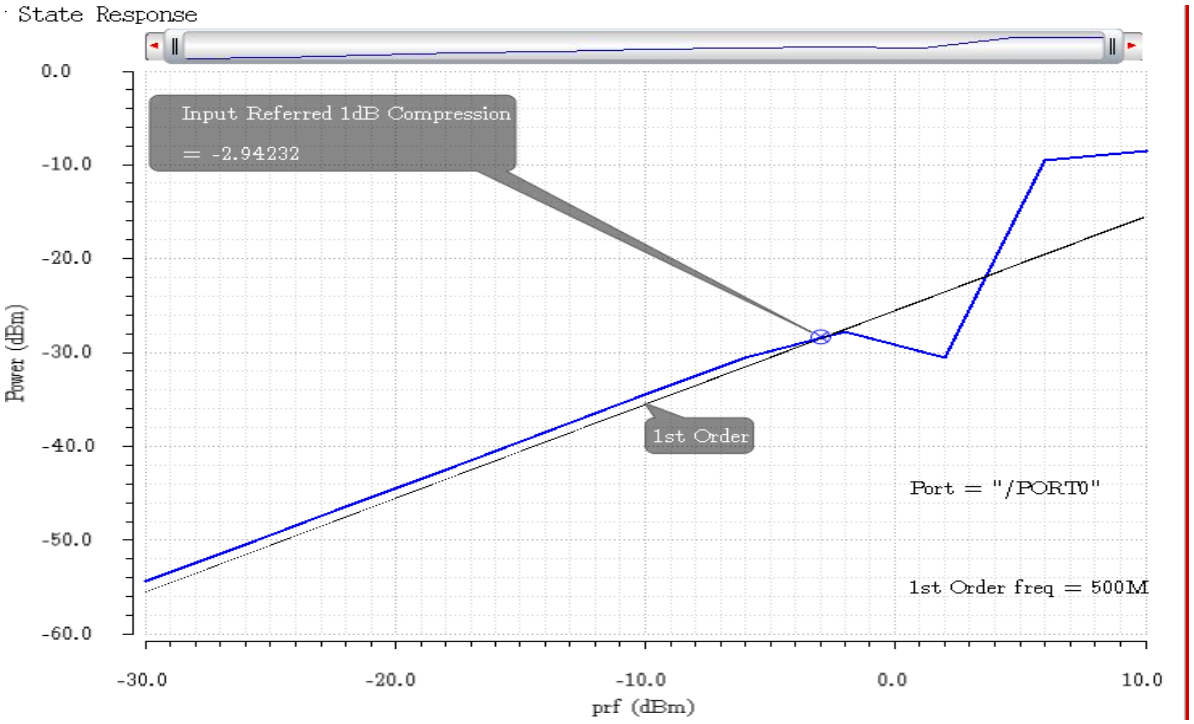


Fig. 7. A plot for the 1dB compression point.

Based on Fig. 7. the 1dB compression point is -2.94232, which meets the design specifications.

II. Discussion

An attempt was made to satisfy the PIIP3 requirement, however this was not possible. This is because the noise figure is inversely proportional to the PIIP3 as shown in the following relation:

$$IIP3 \propto V_{GS} - V_{TH}$$

$$\overline{V_{n}^{2}}_{n,in} \propto \frac{1}{g_m} \propto \frac{1}{V_{GS} - V_{TH}}$$

Satisfying the linearity requirement will cause the noise figure to become too high. I decided to minimally meet the noise requirement in order to increase the PIIP3 as much as possible nonetheless.

One strategy to reduce the noise without affecting the linearity was to scale the width and resistance values. The widths of all transistors were multiplied by an integer value α and the resistances were multiplied by the reciprocal of α. Unfortunately, I was still not able to achieve the PIIP3 specifications and the power consumption became very high. However, since linearity is a more important parameter than power consumption in this design, I sacrificed efficiency for a slightly higher PIIP3 value.

It is likely that a different mixer topology is required to meet both the noise and linearity specifications. A simple solution may be to add a PMOS transistor with its source at VDD and its drain at the source of the RF transistor.

Dante St. Prix
37764157

Acknowledgements: These results were found in collaboration with Mario Liverant and Jyot Kiran Kaur.

EECE 571F - Mixer Project
Hand Calculations

Dante St.Prix
37764157

Methodology:
- Calculate values for an SBM with all the same specifications except a conversion gain of 3dB higher (15dB instead of 12dB)

Initial assumptions:

$I_{bias} = 2mA$

$V_{DD} = 1.2V$

$V_{OD,RF} = 300mV$

$V_{OD,LO} = 150mV$

Apply Equations:

$$V_{R,max} = V_{DD} - \left[V_{OD,RF} + \left(1 + \frac{1}{\sqrt{2}}\right)V_{OD,LO}\right]$$

$$= 644mV$$

$$R_D = \frac{V_{R,max}}{I_D} = \frac{644mV}{1mA} = 644\Omega$$

- choose a smaller resistor to provide more voltage headroom

$\Rightarrow R_D \approx 500\Omega$

$$A_v = \frac{2}{\pi} g_{m,RD} R_D$$

$A_V = 15dB = 5.623$

$g_{m,RD} = 17.67mS$

Using a test bench:

the required M_{RF} width is: 17.2μm
(assuming $L = 45nm$)

$$\overline{V_{n,in}^2} = \pi^2 kT\left(\frac{\gamma}{g_{m,RF}} + \frac{2}{g_{m,RF}^2 R_D}\right)$$

$\gamma = 2$

$T = 298.15\,K$

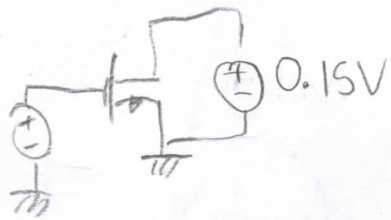
$k = 1.3806\times10^{-23}\ \frac{m^2 kg}{s^2 K}$

$\overline{V_{n,in}^2} = 5.1188\times10^{-18}\ V^2/Hz$

$$F = 1 + \frac{\pi^2}{4R_S g_{m,RF}}\left(\gamma + \frac{2}{g_{m,RF} R_D}\right) = 7.21772$$

$NF = 8.580\,dB$ ✓

Using testbench for M_{LO} width with proper V_{DD}



Requires $W = 14.6$ for $I_D = 1mA$
(assuming $L = 45nm$)

- This design did not work! The V_{DS} of M_{LO} was excessively high, forcing M_{RF} into triode. The widths for the transistors in the final report is based on using trial and error to find a combination of widths that allow both transistors to be in saturation.
- To convert this design to a DBM, the resistance of R_D is divided by two.
- The PIIP3 and compression point cannot be calculated by hand.