

We felt that the design of the ALU was well designed but a little more complicated than it needed to be but was overall well designed and partitioned into sub-modules. The use of full adders within the ripple carry adder was helpful but the full adders could have been implemented without the use of half adder modules. The ALU also used a bit more wires than needed and the c_in input into the ALU became useless and wasted power with different ALU modes such as with the AND and XOR operations. Despite these drawbacks, the circuit is fast, and performs its designed functions with precision and speed.