BOSTON UNIVERSITY

College of Engineering

Photonic Chips for Machine Learning

Compare with hardware accelerator on FPGA

Zhaohan Song (jimmy95@bu.edu) & Geye Lin (gylin@bu.edu)

Github

Introduction

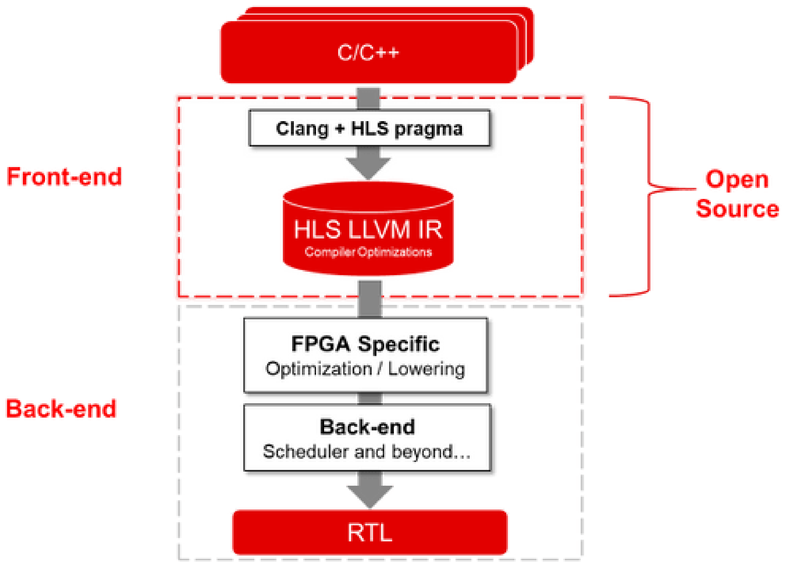
Compare two sets of simulated data – Matrix Multiplication, to prove photonic chips have following advantages:

a. Faster speed
b. Less energy consumption

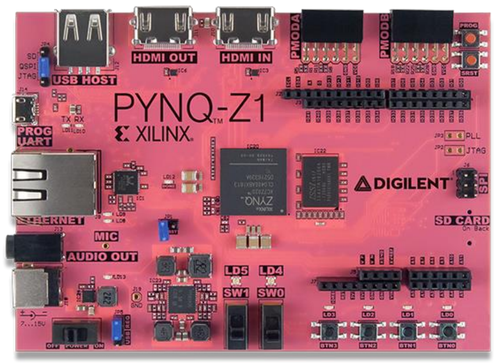
Materials and Methods

Software:

a. Vivado (2022.1)
b. Vitis HLS (2022.1)

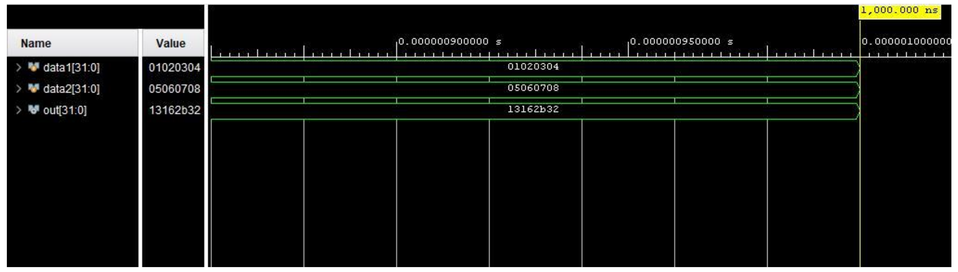


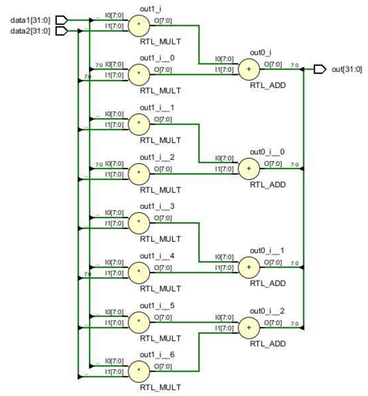
Hardware: PYNQ-Z1 (Zynq-7000)



Goals and results

a. Implement a simple matrix multiplexer on FPGA.





b. Using pipelining method to accelerate the speed of matrix multiplication.

All Compared Solutions

solution2: xc7z020clg484-1
solution1: xc7z020clg484-1

Performance Estimates

Timing

Clock		solution2	solution1
ap_clk	Target	10.00 ns	10.00 ns
	Estimated	6.499 ns	6.499 ns

Latency

		solution2	solution1
Latency (cycles)	min	37	16
	max	37	16
Latency (absolute)	min	0.370 us	0.160 us
	max	0.370 us	0.160 us
Interval (cycles)	min	38	17
	max	38	17

Utilization Estimates

	solution2	solution1
BRAM_18K	0	0
DSP	2	8
FF	105	486
LUT	458	706
URAM	0	0

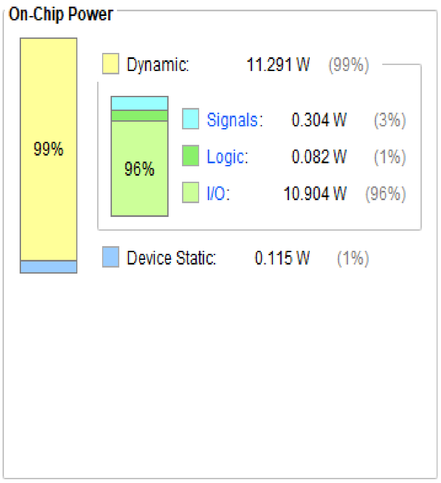
c. Using Vivado tools to simulate the running speed and power consumption.

Summary

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	**11.405 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**46.5°C**
Thermal Margin:	38.5°C (20.3 W)
Effective ϑJA:	1.9°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity



Improvements

a. Try More complex matrix multiplication
b. Build whole system including ram, I/O, etc.

Next Goals

Combining two teams' simulation works and prove the advantages of photonic chips for machine learning