J3 – FPGA JTAG
J4 – CPU dbug port
J5 – control UART

J4
1 SWCLK
2 SWD
3 GND

J5
1 UART_TX
2 UART_RX
3 GND

J3
1 TMS
2 TCK
3 TDI
4 GND
5 TDO
6 VDD33

J6 1 GND

J7 1 GND

VDD33 C11 100n GND
C10 100n
C9 100n
C8 100n
C16 100n

VDD33
C5 100n
C6 100n
C2 100n
C4 100n
C1 100n
C3 100n
GND
C7 +1V1
2.2uF

GND
LEDK1 330 R12
LEDK2 330 R13
LEDK3 330 R14
LEDK4 330 R15
LEDK5 330 R16
LEDK6 330 R17

14 GND
13 PW_5V
12 SYS_A0
11 PW_LED
10 SYS_WRn
9 SYS_RDn
8 SYS_D0
7 SYS_D1
6 SYS_D2
5 SYS_D3
4 SYS_D4
3 SYS_D5
2 SYS_D6
1 SYS_D7

R1 3.9K SYS_A0_lv
R2 3.9K SYS_WRn_lv
R3 3.9K SYS_RDn_lv
R4 0 PW_5V
R5 0 VDD33
C11 100n GND

U5
SN74LXC8T245QPWRQ1

SYS_D7 3	VCCA	VCCB	24 VDD33
SYS_D6 4	A1	VCCB	23
SYS_D5 5	A2	*OE	22 GND
SYS_D4 6	A3	B1	21 SYS_D7_lv
SYS_D3 7	A4	B2	20 SYS_D6_lv
SYS_D2 8	A5	B3	19 SYS_D5_lv
SYS_D1 9	A6	B4	18 SYS_D4_lv
SYS_D0 10	A7	B5	17 SYS_D3_lv
GND 11	A8	B6	16 SYS_D2_lv
GND 12	GND	B7	15 SYS_D1_lv
	GND	B8	14 SYS_D0_lv
	GND	GND	13 GND

CONTROL INPUTS (1)		PORT STATUS	
OE	DIR	A PORT	B PORT
L	L	Output (Enabled)	Input (Hi-Z)
L	H	Input (Hi-Z)	Output (Enabled)
H	X	Input (Hi-Z)	Input (Hi-Z)

U2
LCMXO2-1200HC-4SG32C

TDO 1	PT10C	PAD	33 GND
VDD33 2	VCC	PT10D	32 TDI
GND 3	GND	VCCIO0	31 VDD33
SYS_D6_lv 4	PL9A	PT11C	30 TCK
SYS_D7_lv 5	PL9B	PT11D	29 TMS
VDD33 6	VCCIO3	PT12C	28 SYS_A0_lv
VDD33 7	VCCIO2	PT12D	27 FPGA_S0
SYS_D5_lv 8	PB4C	PT15C	26 FPGA_S1
SYS_D4_lv 9	PB6C	PT15D	25 FPGA_S2
SYS_D3_lv 10	PB6D	VCCIO0	24 VDD33
SYS_D2_lv 11	PB9A	PT17D	23 FPGA_S3
SYS_D1_lv 12	PB9B	GND	22 GND
SYS_D0_lv 13	PB11A	PR5C	21 FPGA_S4
SYS_RDn_lv 14	PB11B	PR5D	20 FPGA_S5
VDD33 15	VCCIO2	VCCIO1	19 VDD33
SYS_WRn_lv 16	PB20C	VCC	18 VDD33
		PB20D	17 FPGA_S6

U3
MX25V1635FZUI

QSPI_SS 1	CS#	GND	9 GND
QSPI_SD1 2	SO/SIO1	VCC	8 VDD33
QSPI_SD2 3	WP#/SIO2	HOLD#/SIO3	7 QSPI_SD3
GND 4	GND	SCLK	6 QSPI_SCLK
		SI/SIO0	5 QSPI_SD0

VDD33
R18 10K
GND
C15 100n

U1
RP2040

	RUN	GPIO0	2 DSP_D0
		GPIO1	3 DSP_D1
		GPIO2	4 DSP_D2
		GPIO3	5 DSP_D3
		GPIO4	6 DSP_D4
		GPIO5	7 DSP_D5
		GPIO6	8 DSP_D6
		GPIO7	9 DSP_D7
		GPIO8	11 DSP_D8
		GPIO9	12 DSP_D9
		GPIO10	13 DSP_D10
		GPIO11	14 DSP_D11
		GPIO12	15 UART_TX
		GPIO13	16 UART_RX
		GPIO14	17 DSP_D12
		GPIO15	18 DSP_D13
		GPIO16	27 DSP_D14
		GPIO17	28 DSP_D15
		GPIO18	29 DSP_CSn
		GPIO19	30 DSP_WR
		GPIO20	31 DSP_RS
		GPIO21	32 DSP_RD
		GPIO22	34 DSP_RST
		GPIO23	35 FPGA_S0
		GPIO24	36 FPGA_S1
		GPIO25	37 FPGA_S2
		GPIO26_ADC0	38 FPGA_S3
		GPIO27_ADC1	39 FPGA_S4
		GPIO28_ADC2	40 FPGA_S5
		GPIO29_ADC3	41 FPGA_S6
47 USB_DP			
46 USB_DM			
QSPI_SS 56	QSPI_SS		
QSPI_SD0 53	QSPI_SD0		
QSPI_SD1 55	QSPI_SD1		
QSPI_SD2 54	QSPI_SD2		
QSPI_SD3 51	QSPI_SD3		
QSPI_SCLK 52	QSPI_SCLK		
	XIN 20		
	XOUT 21		
SWCLK 24	SWCLK		
SWD 25	SWD		
19	TESTEN		
	GND 57		
45	VREG_VOUT		
23	DVDD		
1	IOVDD		
48	USB_VDD		
43	ADC_AVDD		
44	VREG_IN		

C13 15pf
Y1 ABM8G-12.000MHZ-4Y-T3
C14 15pf
GND
GND__1

J1
Conn_2Rows-45Pins

LEDK1	1	2	LEDK2
LEDK3	3	4	LEDK4
LEDK5	5	6	LEDK6
PW_LED	7	8	GND
VDD33	9	10	VDD33
DSP_TE	11	12	DSP_CSn
DSP_RS	13	14	DSP_WR
DSP_RD	15	16	DSP_SDA
DSP_SDO	17	18	DSP_D0
DSP_D1	19	20	DSP_D2
DSP_D3	21	22	DSP_D4
DSP_D5	23	24	DSP_D6
DSP_D7	25	26	DSP_D8
DSP_D9	27	28	DSP_D10
DSP_D11	29	30	DSP_D12
DSP_D13	31	32	DSP_D14
DSP_D15	33	34	DSP_D16
DSP_D17	35	36	DSP_DE
DCLK	37	38	DSP_HSYNC
GND	39	40	DSP_VSYNC
DSP_RST	41	42	VDD33
GND	43	44	VDD33
GND	45		

NO.	DESCRIPTION	NO.	DESCRIPTION
1	LEDK1	24	D6
2	LEDK2	25	D7
3	LEDK3	26	D8
4	LEDK4	27	D9
5	LEDK5	28	D10
6	LEDK6	29	D11
7	LED_A	30	D12
8	GND	31	D13
9	VCI	32	D14
10	IOVCC	33	D15
11	TE	34	D16
12	CS	35	D17
13	RS	36	DE
14	WR	37	DCLK
15	RD	38	HSYNC
16	SDA	39	GND
17	SDO	40	VSYNC
18	D0	41	RESET
19	D1	42	IM2
20	D2	43	IM1
21	D3	44	IM0
22	D4	45	GND
23	D5		

J2
J8
1 GND
2
3
4
5
6
7
8
9
10
11
12
13
14

J8 – Spare

U4
GND 1 GND
VOUT 3 VDD33
VIN 2 PW_5V
C12 100n
GND

TP1 DSP_D0
TP2 DSP_D1
TP3 DSP_D2
TP4 DSP_D3
TP5 DSP_D4
TP6 DSP_D5
TP7 DSP_D6
TP8 DSP_D7
TP9 DSP_CSn
TP10 DSP_WR
TP11 DSP_RS
TP12 DSP_RD
TP13 DSP_RST

TP14 FPGA_S0
TP15 FPGA_S1
TP16 FPGA_S2
TP17 FPGA_S3
TP18 FPGA_S4
TP19 FPGA_S5
TP20 FPGA_S6

D1 LED
FPGA_S6
R19 10K
GND

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