

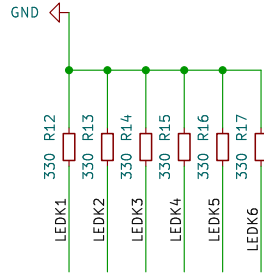
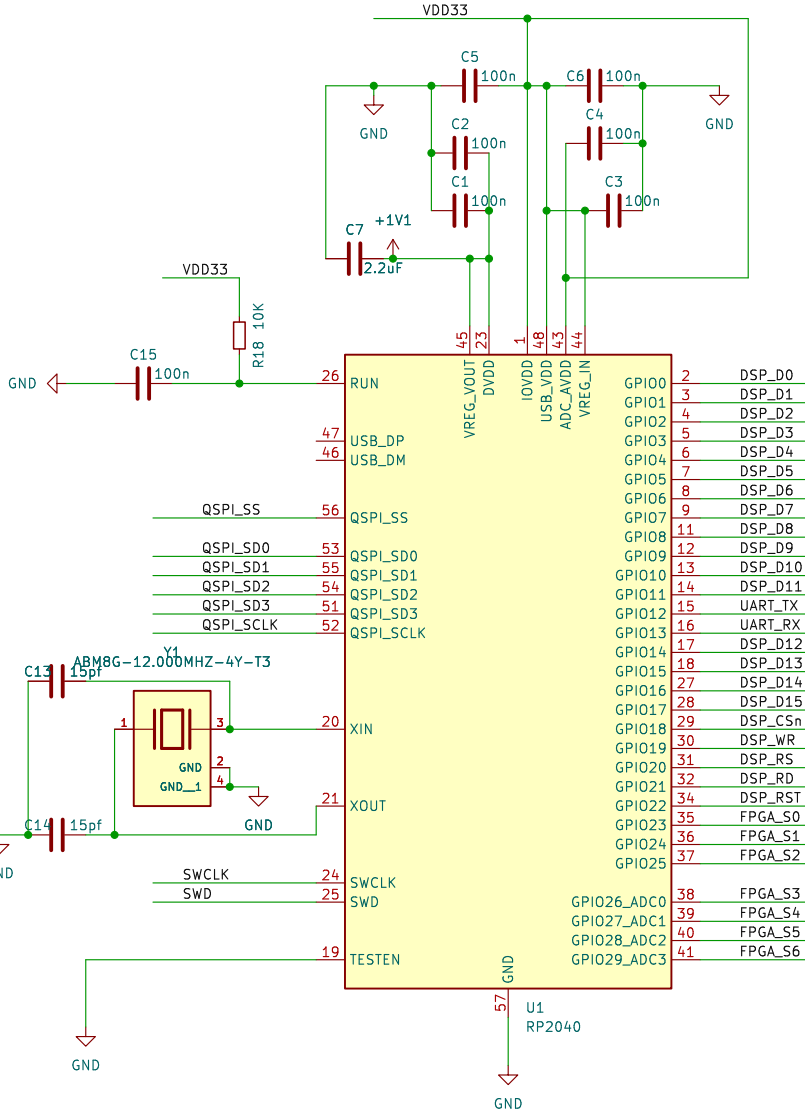
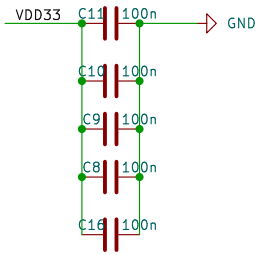
J3 - FPGA JTAG  
J4 - CPU debug port  
J5 - control UART

J4 1 SWCLK  
2 SWD  
3 GND

J3 1 TMS  
2 TCK  
3 TDI  
4 GND  
5 TDO  
6 VDD33

J5 1 UART\_TX  
2 UART\_RX  
3 GND

J6 1 GND  
J7 1 GND



Conn\_2Rows-45Pins

LEDK1	1	2	LEDK2
LEDK3	3	4	LEDK4
LEDK5	5	6	LEDK6
PW_LED	7	8	GND
VDD33	9	10	VDD33
DSP_TE	11	12	DSP_CS
DSP_RS	13	14	DSP_WR
DSP_RD	15	16	DSP_SDA
DSP_SDO	17	18	DSP_D0
DSP_D1	19	20	DSP_D2
DSP_D3	21	22	DSP_D4
DSP_D5	23	24	DSP_D6
DSP_D7	25	26	DSP_D8
DSP_D9	27	28	DSP_D10
DSP_D11	29	30	DSP_D12
DSP_D13	31	32	DSP_D14
DSP_D15	33	34	DSP_D16
DSP_D17	35	36	DSP_DE
DCLK	37	38	DSP_HSYNC
DSP_D18	39	40	DSP_VSYNC
DSP_RST	41	42	VDD33
GND	43	44	VDD33
GND	45		

NO.	DESCRIPTION	NO.	DESCRIPTION
1	LEDK1	24	D6
2	LEDK2	25	D7
3	LEDK3	26	D8
4	LEDK4	27	D9
5	LEDK5	28	D10
6	LEDK6	29	D11
7	LED_A	30	D12
8	GND	31	D13
9	VCI	32	D14
10	IOVCC	33	D15
11	TE	34	D16
12	CS	35	D17
13	RS	36	DE
14	WR	37	DCLK
15	RD	38	HSYNC
16	SDA	39	GND
17	SDO	40	VSYNC
18	D0	41	RESET
19	D1	42	IM2
20	D2	43	IM1
21	D3	44	IM0
22	D4	45	GND
23	D5		

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Title:

Size: A3  
KiCad E.D.A. kicad 7.0.9

Date:

Rev:

Id: 1/1