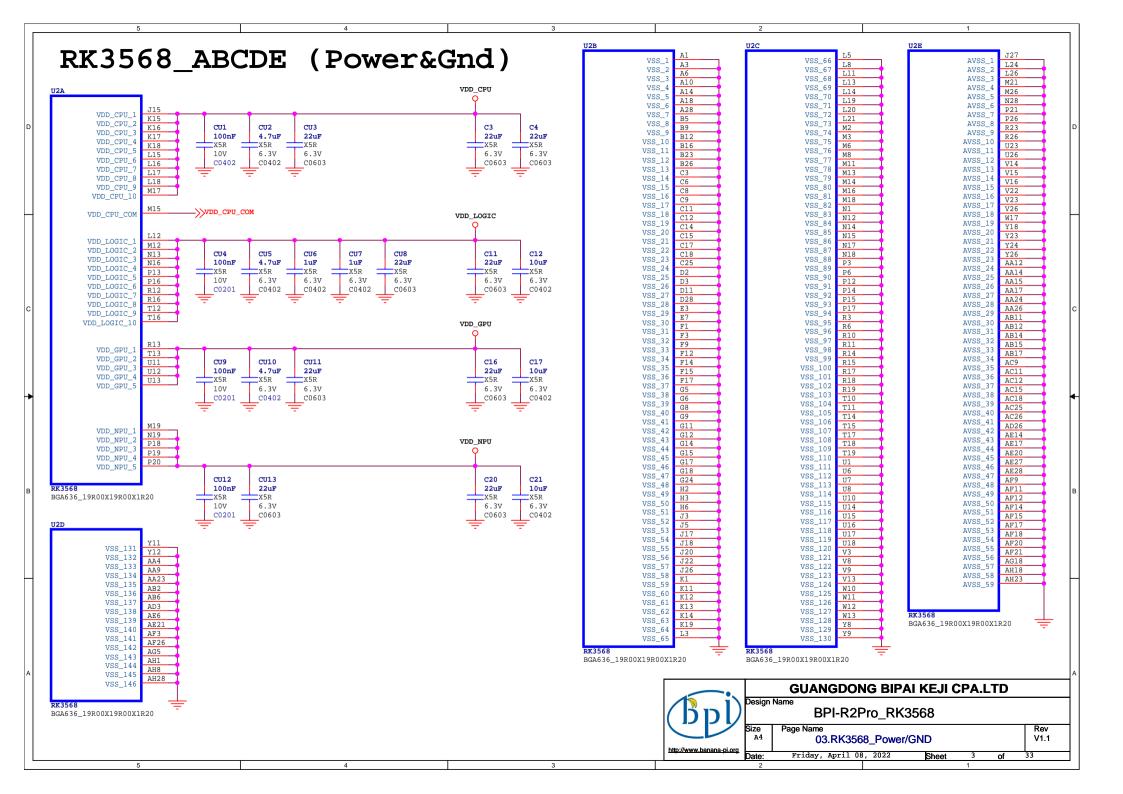


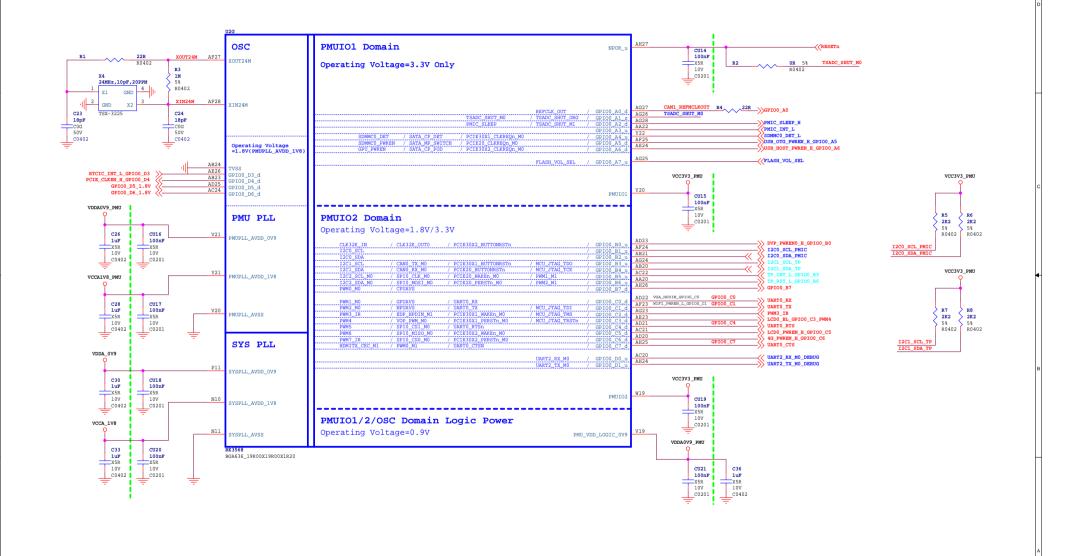
### LPDDR4/4x DQ

**************************************	\\ DDR_DQ0_A
LPDDR4_DQ0_A	DDR_DQ1_A
LPDDR4_DQ1_A	DDR_DQ2_A
LPDDR4_DQ2_A	DDR_DQ3_A
LPDDR4_DQ3_A	DDR_DQ4_A
LPDDR4_DQ4_A	DDR_DQ5_A
LPDDR4_DQ5_A	DDR_DQ6_A
LPDDR4_DQ6_A	DDR_DQ7_A
LPDDR4_DQ7_A	<i>&gt;&gt;</i>
TRANSA DMO A //	DDR_DM0_A
LPDDR4_DM0_A <<-	
TRADA DOGOD A //	\\ DDR_DQSOP_A
LPDDR4_DQS0P_A  LPDDR4_DQS0N_A	C DDR_DQSON_A
	//
	\\ DDR_DQ8_A
LPDDR4_DQ8_A <<	DDR_DQ9_A
LPDDR4_DQ9_A </td <td>DDR_DQ10_A</td>	DDR_DQ10_A
LPDDR4_DQ10_A </td <td>DDR_DQ10_A</td>	DDR_DQ10_A
LPDDR4_DQ11_A </td <td>DDR_DQ11_A</td>	DDR_DQ11_A
LPDDR4_DQ12_A <	DDR_DQ12_A  DDR_DQ13_A
LPDDR4_DQ13_A </td <td>DDR_DQ13_A  DDR_DQ14_A</td>	DDR_DQ13_A  DDR_DQ14_A
LPDDR4_DQ14_A </td <td></td>	
LPDDR4_DQ15_A	S DDR_DQ15_A
LPDDR4_DM1_A <<=	DDR_DM1_A
**	
LPDDR4_DQS1P_A </td <td>&gt;&gt; DDR_DQS1P_A</td>	>> DDR_DQS1P_A
LPDDR4_DQS1P_A  LPDDR4_DQS1N_A	DDR_DQS1N_A
**	<i>"</i>
LPDDR4_DQ0_B </td <td>\\ DDR_DQ0_B</td>	\\ DDR_DQ0_B
LPDDR4_DQ1_B	DDR_DQ1_B
LPDDR4 DQ2 B	<pre>Company DDR_DQ2_B</pre>
LPDDR4_DQ3_B	CDDR_DQ3_B
LPDDR4_DQ4_B	DDR_DQ4_B
LPDDR4_DQ5_B	CDDR_DQ5_B
LPDDR4_DQ6_B	DDR_DQ6_B
LPDDR4_DQ7_B	CDDR_DQ7_B
TEDDICA_DEL_B ((	<i>&gt;&gt;</i>
LPDDR4_DM0_B <<-	DDR_DM0_B
TRADANA BOGGA = //	\\ DDR_DQSOP_B
LPDDR4_DQS0P_B LPDDR4_DQS0N_B	DDR_DQS0N_B
THUNK#_DÖRON_B <<	<i>"</i>
	\\ DDR_DQ8_B
LPDDR4_DQ8_B <<	DDR_DQ9_B
LPDDR4_DQ9_B <<	DDR_DQ10_B
LPDDR4_DQ10_B <<	DDR_DQ11_B
LPDDR4_DQ11_B	DDR_DQ12_B
LPDDR4_DQ12_B </td <td>DDR_DQ12_B DDR_DQ13_B</td>	DDR_DQ12_B DDR_DQ13_B
LPDDR4_DQ13_B </td <td>DDR_DQ14_B</td>	DDR_DQ14_B
LPDDR4_DQ14_B <<	
LPDDR4_DQ15_B	S DDR_DQ15_B
LPDDR4_DM1_B -</td <td>DDR_DM1_B</td>	DDR_DM1_B
**	nnp nosip R
LPDDR4_DQS1P_B \\ LPDDR4_DQS1N_B	DDR_DQS1P_B DDR_DQS1N_B

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(Bpl)	Design I	Name BPI-R2Pro_RK3568				
http://www.banana-oi.org	Size A3	Page Name 02.RK3568_DDR P	HY			Rev V1.1
IND.//www.banana-bi.org	Date:	Friday, April 08, 2022	Sheet	2	of	33



### RK3568\_G(OSC/PLL/PMUIO1/2)



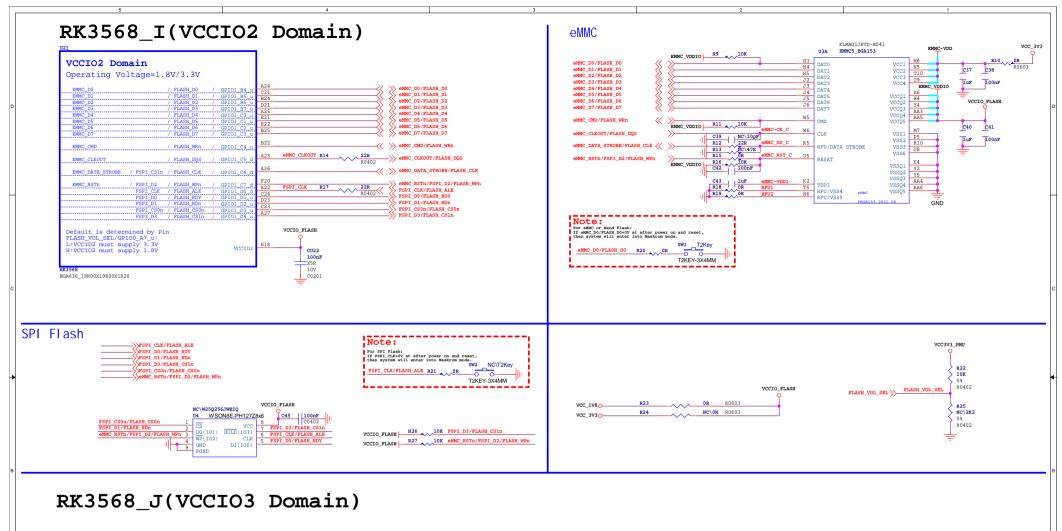
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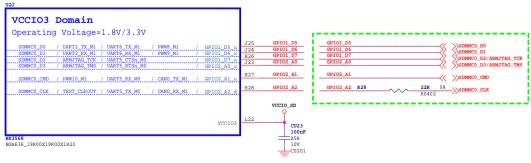
BPI-R2Pro\_RK3568

04.RK3568\_OSC/PLL/PMUIO

Friday, April 08, 2022

Rev V1.1

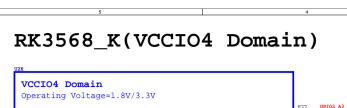




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http://www.banana-pi.org	Size A3	Page Name 05.RK3568_Flash/	SD(IO2_3)			Rev V1.1
IIID://www.ballaria-bi.bid	Date:	Friday, April 08, 2022	Sheet	5	of	33

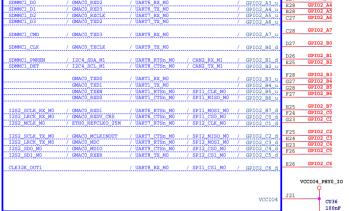
### RK3568 V(USB2.0 HOST) RK3568 U(USB3.0/SATA/OSGMII/PCIe2.0 x1) USB3.0 USB2.0 HOST USB3 OTG0 D OTGO\_HS/FS/LS USB3\_OTG0\_VBUSDE //USB3 OTG0 VBUSDET SUSB2\_HOST2\_DM (USB Download) C47 //tises orgo to 100nF Diff 90 Ohm +10% X5R USB2\_HOST3\_DP USB2\_HOST3\_DM Diff 90 Ohm +10% USB3.0 C0402 USB3\_HOST1\_DP USB3\_HOST1\_DM USB3 HOST1 I HOST1 HS/FS/LS USB3\_HOST1\_DM USB AVDD 0V9 USB3.0 HSB3 AVDD OV R8 5mA, < 25mV USB2\_AVDD\_0V9 USB AVDD 1V8 OTG0/HOST1 30mA.<50mV HS/FS/LS USB3\_AVDD\_1V8 Power p9 30mA.<50mV USB2\_AVDD\_1V8 M23 10mA,<200mV USB3 AVDD 3V 100nF 100nF 100nF P10 10mA, < 200mV USB2\_AVDD\_3V MULTI\_PHY0/1/2 C0201 C0201 100nF 100nF 100nF BGA636\_19R00X19R00X1R20 USB3.0 OTG0 SS and SATAO Mux C0201 C0201 C0201 USB3\_OTG0\_SSTXP/SATA0\_TXI USB3\_OTG0\_SSTXN/SATA0\_TXI USB3 OTG0 RK3568 W(PCIe3.0 $\times$ 2) USB3.0 HOST1 SS and SATA1 and OSGMII MO Mux USB3\_HOST1\_SSTXP/SATA1\_TXP USB3\_HOST1\_SSTXN/SATA1\_TXN USB3\_HOST1\_SSTXN/SATA1\_TXN USB3\_HOST1\_SSTXN USB3\_HOST1\_SSTXP/SATA1\_TXP/QSGMII\_TXP\_M HSB3 HOST1 SSTXN/SATA1 TXN/OSGMIT TXN M USB3 HOST1 SSRXP/SATA1 RXP 3\_HOST1\_SSRXP/SATA1\_RXP 3\_HOST1\_SSRXN/SATA1\_RXN USB3\_HOST1\_SSRXN USB3\_HOST1\_SSRXN Fault Diff 90 Ohm ±10% USB3\_HOST1\_SSRXP/SATA1\_RXP/QSGMII\_RXP\_MG $PCIe3.0 \times 2$ HISB3 HOST1 SSRXN/SATA1 RXN/OSGMIT RXN M Default piff 85 Ohm ±10% >>PCIE30\_TX0P PCIE30\_TX0E USB3 HOST1 PCIE30\_TXON PCIE30\_TXON Diff 85 Ohm ±10% >>>PCIE30\_TX1P PCIe2.0 and SATA2 PCIE30 TX11 and OSGMII M1 Mux PCIE20\_TXP/SATA2\_TXP Diff 85 Ohm ±10% (PCIE30\_RX0E PCIE20 TXP/SATA2 TXP/OSGMII TXP M DOTEST PYNI PCIE20 TXN/SATA2 TXN PCIE20\_TXN/SATA2\_TXN/QSGMII\_TXN\_M SATA2TXN PCIE30 RXON Diff 85 Ohm ±10% (PCIE30\_RX1P PCIE20\_RXP/SATA2\_RXP/QSGMII\_RXP\_M DCTE30 PY1 DCTE20 DYN/SATA2 DY PCIE20 RXN/SATA2 RX PCIE30 RX1N PCIE20 RXN/SATA2 RXN/QSGMII RXN M PCIE30\_RX11 Diff 85 Ohm ±10% Diff 100 Ohm ±10% Diff 100 Ohm ±10% //PCIE30\_REFCLEP\_IN PCIE30\_REFCLKP\_I PCIE20\_REFCLKN PCIE20\_REFCLK PCIE30 REFCLKN I Diff 100 Ohm ±10% Default SATA3.0 Port2 MULTI PHY U19 PCIE30\_RESREF R29 PCIE30\_RESREE REFCLK MULTI PHYO REFCLKN VDDA\_0V9 PCIE30\_AVDD\_0V9\_1 MULTI PHY0/PHY1有两对REFCLK, 暂时没启用, 悬空即可 PCIE30 AVDD 0V9 VDDA\_0V9 R20 150mA,<20mV R21 VCCA\_1V8 MULTI\_PHY\_AVDD\_0V9\_1 MILTT PHY AVDD 0V9 : VCCA\_1V8 U22 60mA, <50mV PCIE30\_AVDD\_1V8 MULTI\_PHY\_AVDD\_1V8 C57 BGA636 19R00X19R00X1R20 C61 4.7uF 100nF 100nF \_4.7uF 100nF 100nF 4.7uF BGA636 19R00X19R00X1R20 X5R 10V X5R 10V X5R 6.3V C0402 C0201 C0201 C0402 C0402 **GUANGDONG BIPAI KEJI CPA.LTD BPi-R2 Pro** 06.RK3568 USB/PCIe/SATA PHY

Rev V1.1













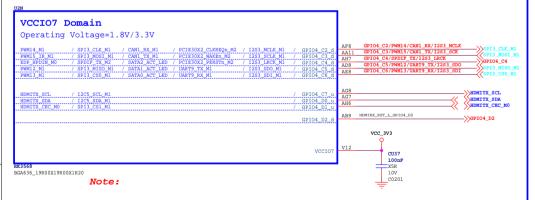
### VCCIO4: Default 3.3V

X5R 10V C0201

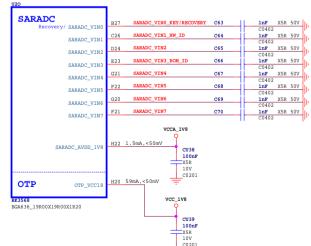


## RK3568\_N(VCCIO7 Domain)

BGA636\_19R00X19R00X1R20



## RK3568\_O(SARADC/OTP)



# SARADC\_VINO\_KEY/RECOVERY SARADC\_VINL\_HM\_ID SARADC\_VINL\_BOM\_ID SARADC\_VINL\_BOM\_ID SARADC\_VINLS SARADC\_VINLS SARADC\_VINLS SARADC\_VINLS SARADC\_VINLS SARADC\_VINLS SARADC\_VINLS

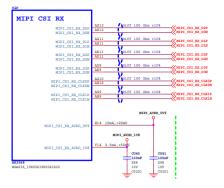
### Note:

Caps of between dashed green lines and U1000 should be placed under the U1000 package  $\,$ 

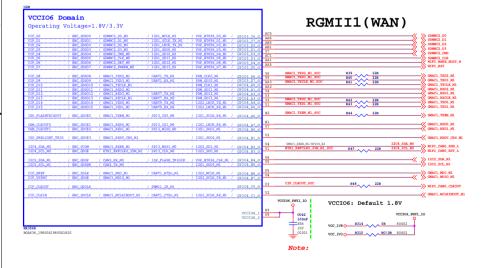
# http://www.banana-pl.org

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### RK3568\_P(MIPI\_CSI\_RX)

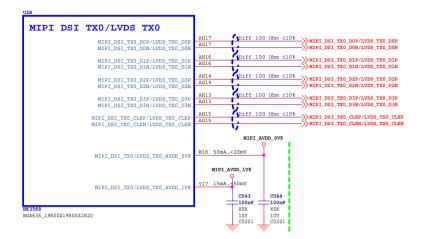


### RK3568\_M(VCCIO6 Domain)

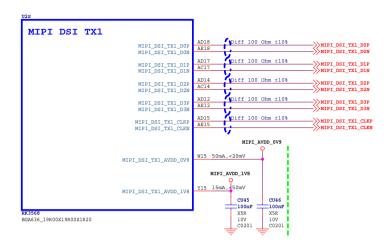




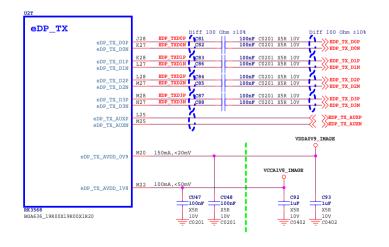
### RK3568\_R(MIPI\_DSI\_TX0/LVDS\_TX0)



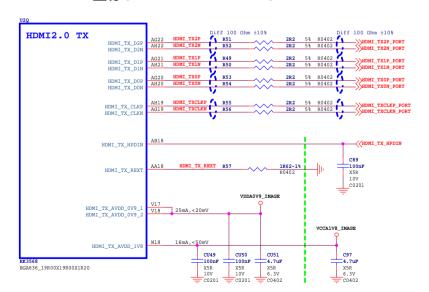
### RK3568\_S(MIPI\_DSI\_TX1)



### RK3568\_T(eDP TX)

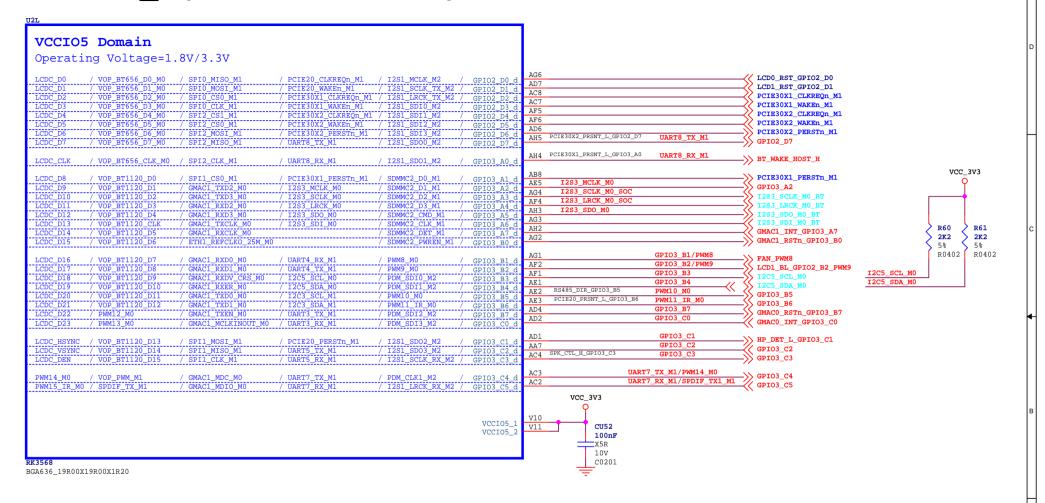


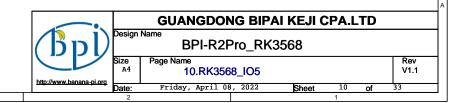
### RK3568\_Q(HDMI2.0 TX)



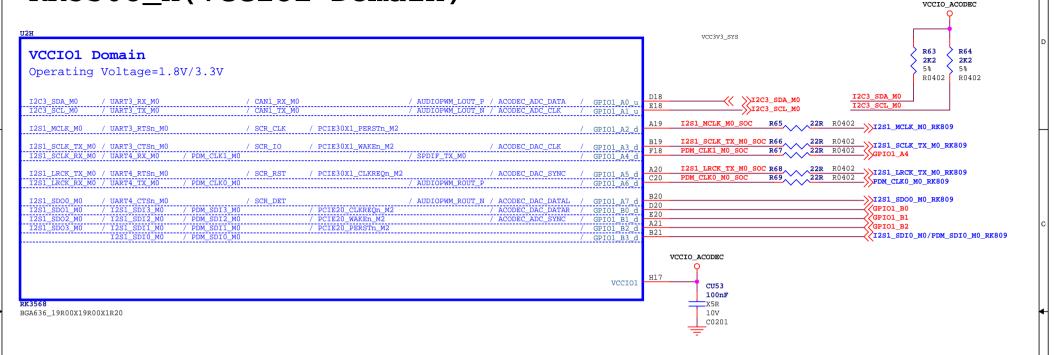
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(Bpl)	Design I	BPI-R2Pro_RK	3568			
http://www.banana-pi.org	Size A3	Page Name 09.RK3568_DSI/HI	DMI/eDP			Rev V1.1
IIID://www.ballaria-bi.bid	Date:	Friday, April 08, 2022	Sheet	9	of	33

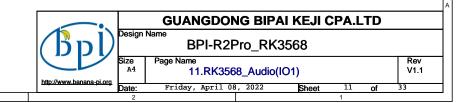
# RK3568\_L(VCCIO5 Domain)



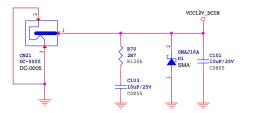


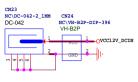
# RK3568\_H(VCCIO1 Domain)





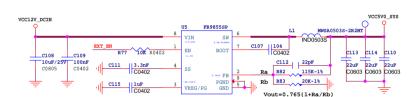
### **12V/3A DCIN**



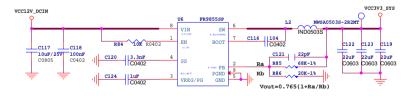


### VCC5VO\_SYS

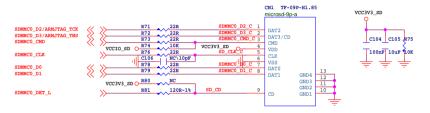
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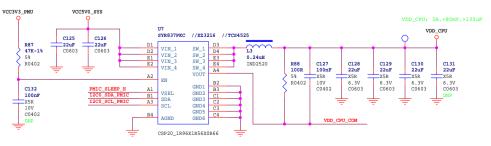
### VCC3V3\_SYS



### SD Card

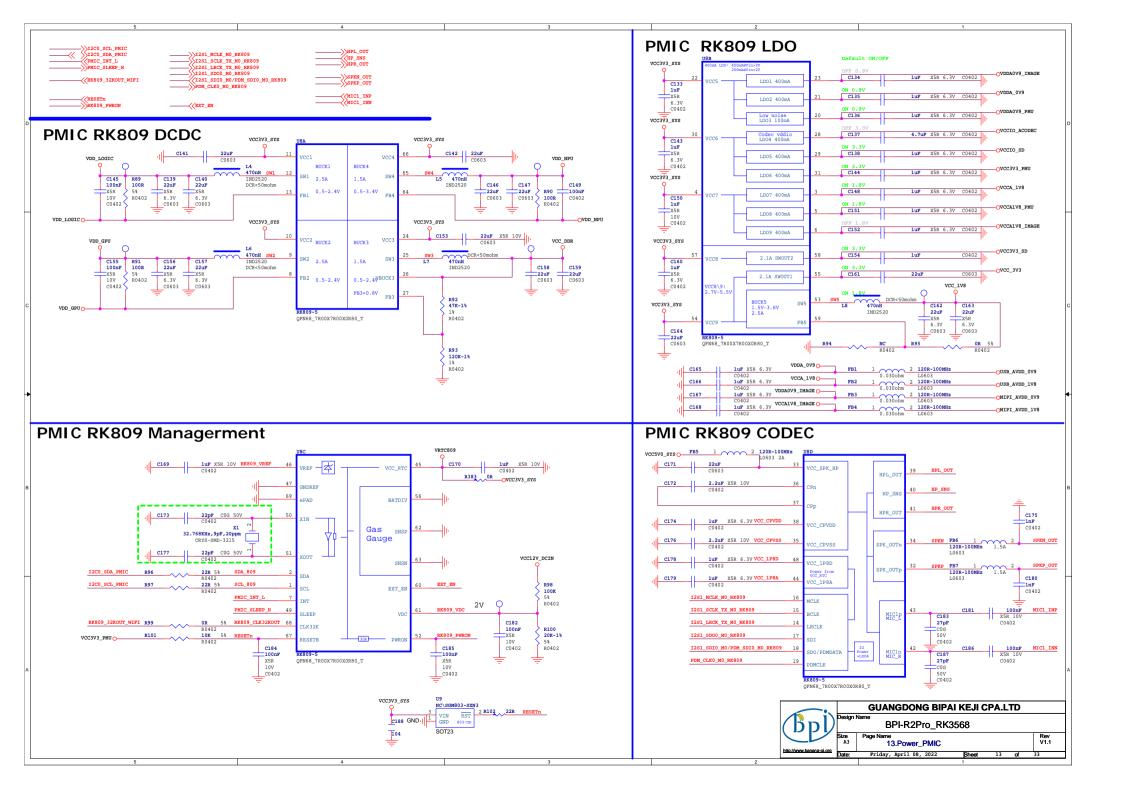


### VDD\_CPU

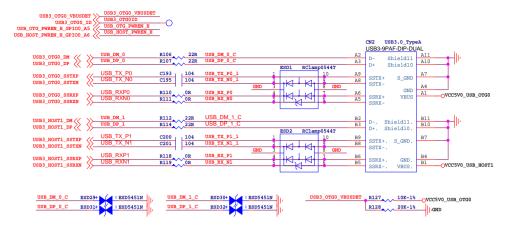


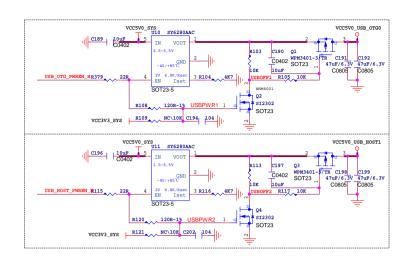
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BPI-R2Pro_RK3568						
http://www.banana-pi.org	Size A3	Page Name 12.Power_DC IN /S	DMMC0			Rev V1.1
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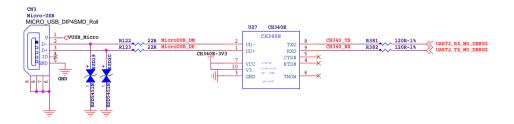


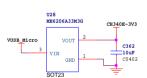




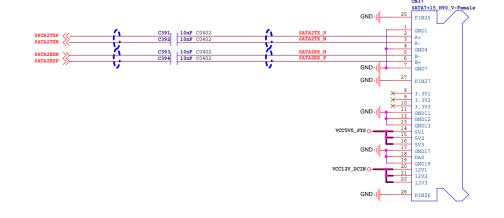


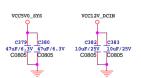
### MicroUSB Debug



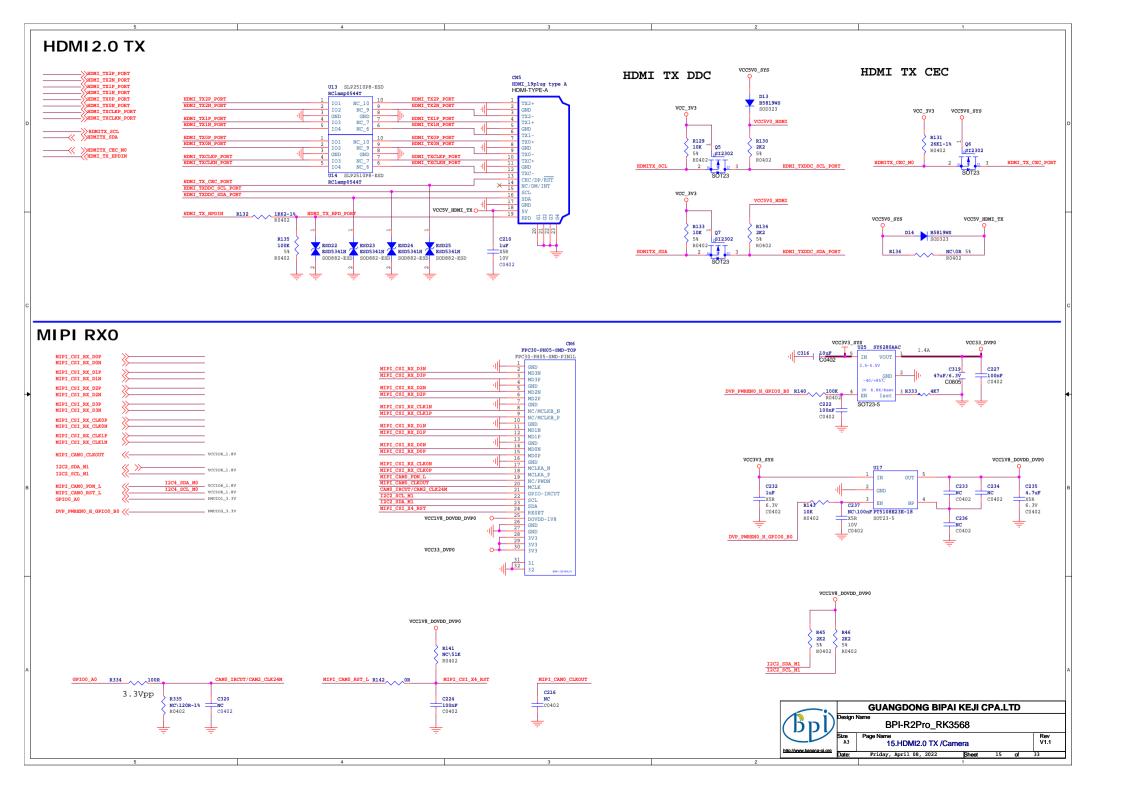


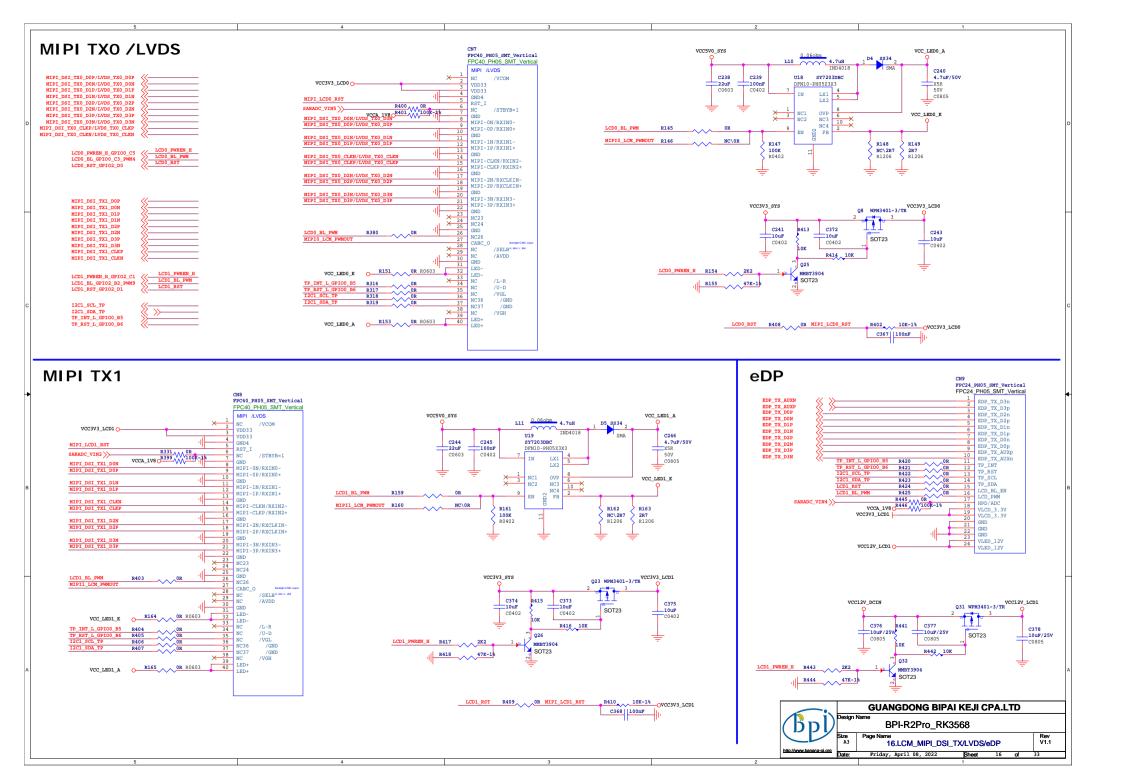
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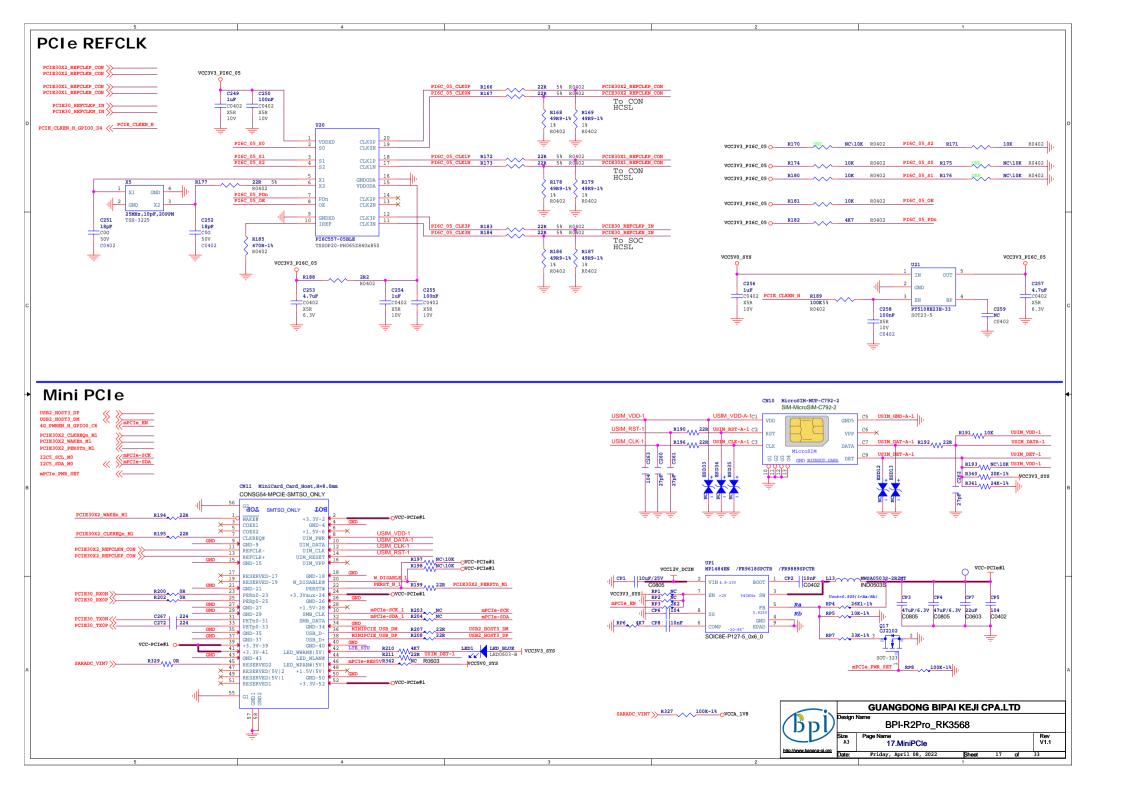




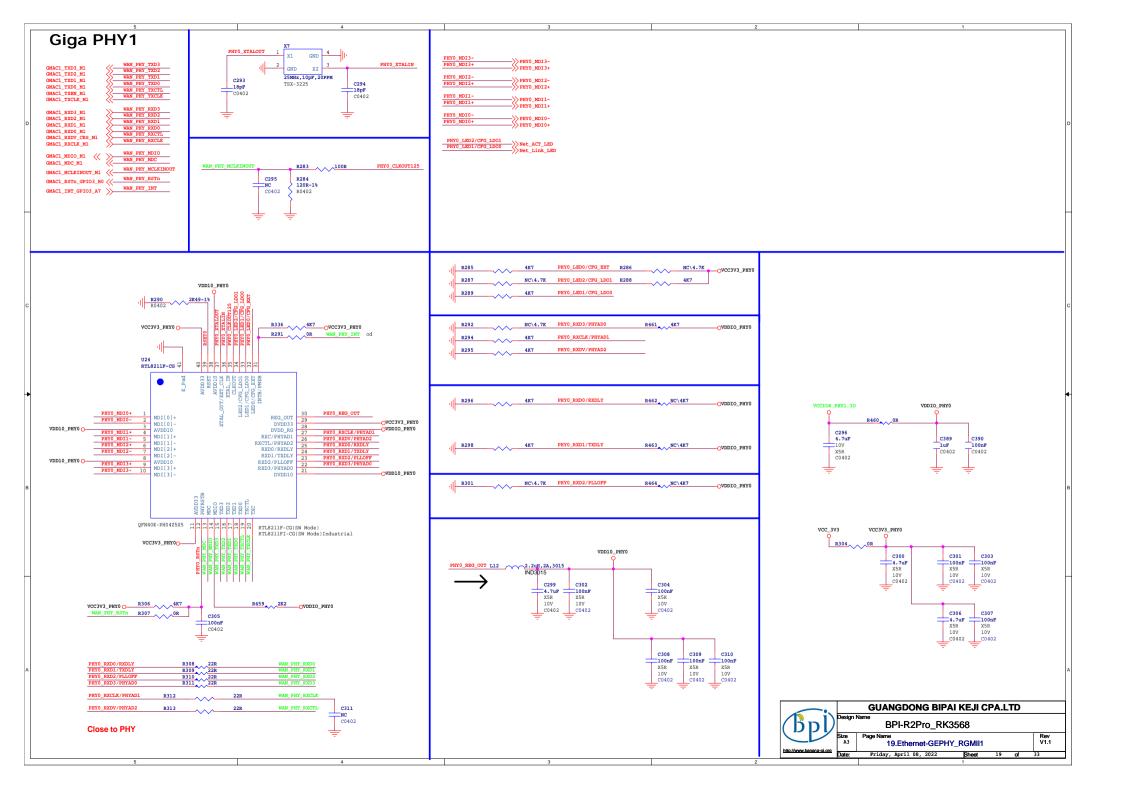
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(Bpl)	Design I	BPI-R2Pro_RK3	568			
http://www.banana-pi.org	Size A3	Page Name 14.USB3 Port /SATA	1			Rev V1.1
IIIID.//www.baliana-bi.bid	Date:	Friday, April 08, 2022	Sheet	14	of	33

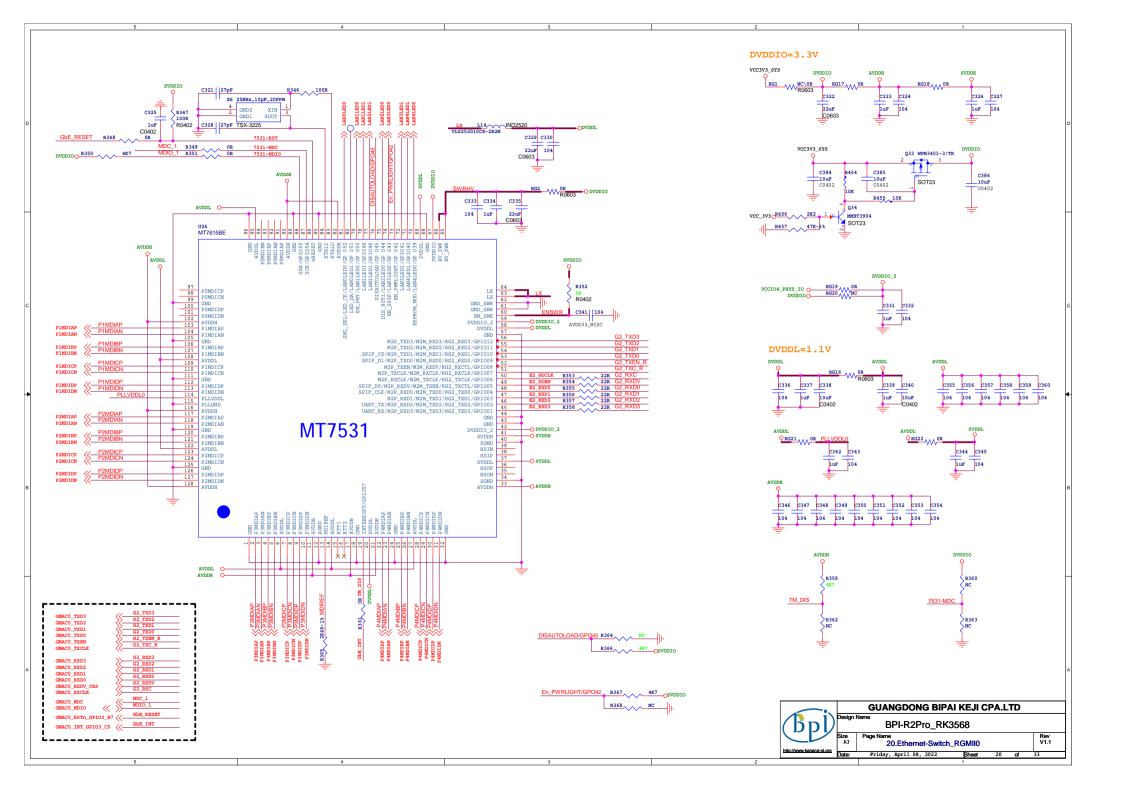


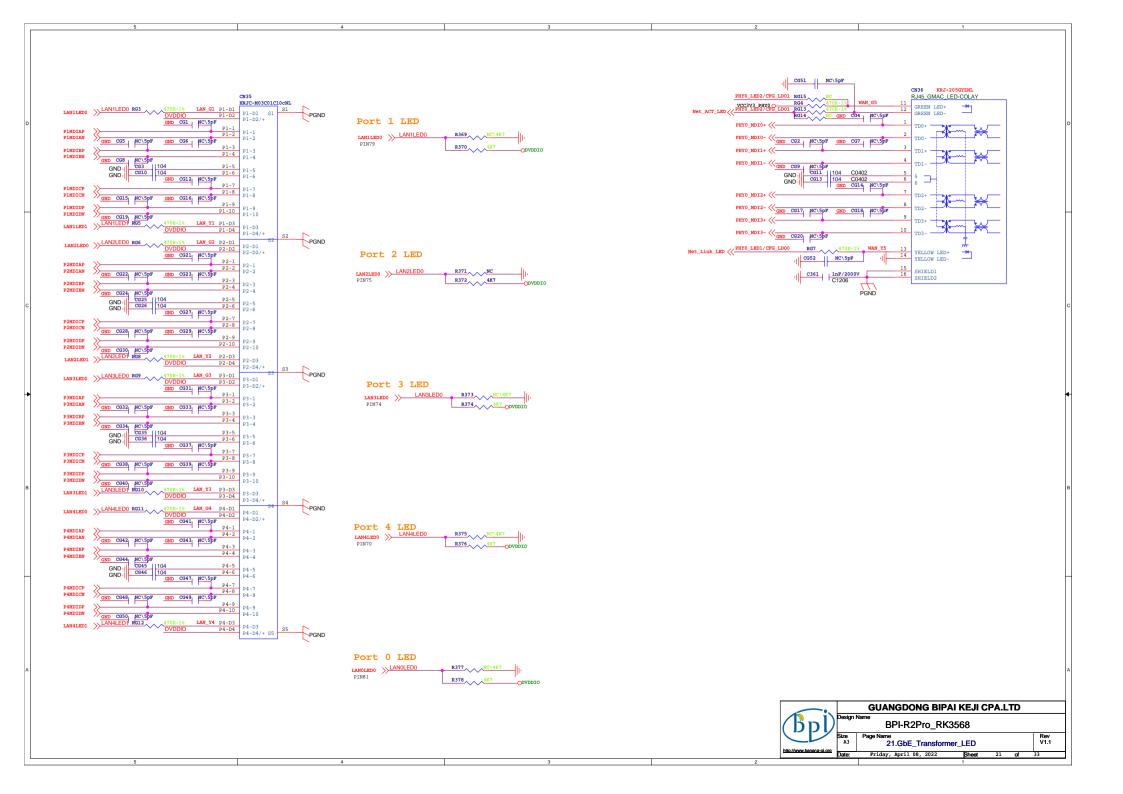


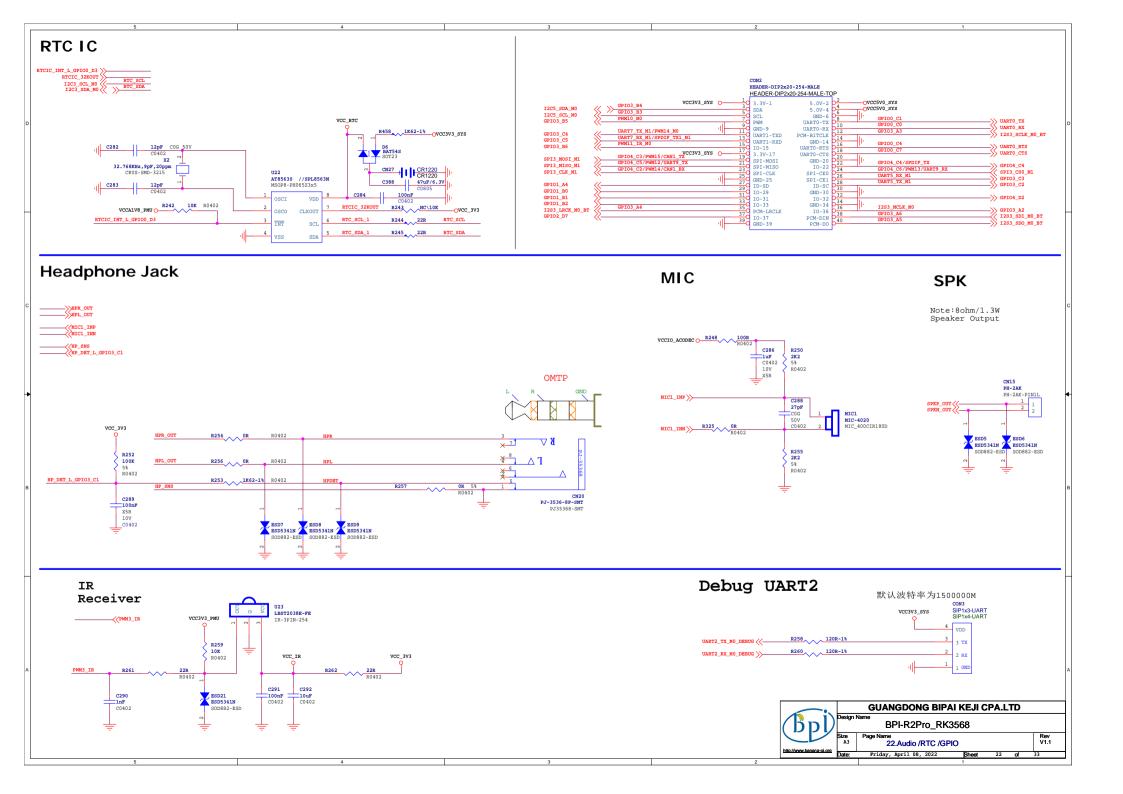


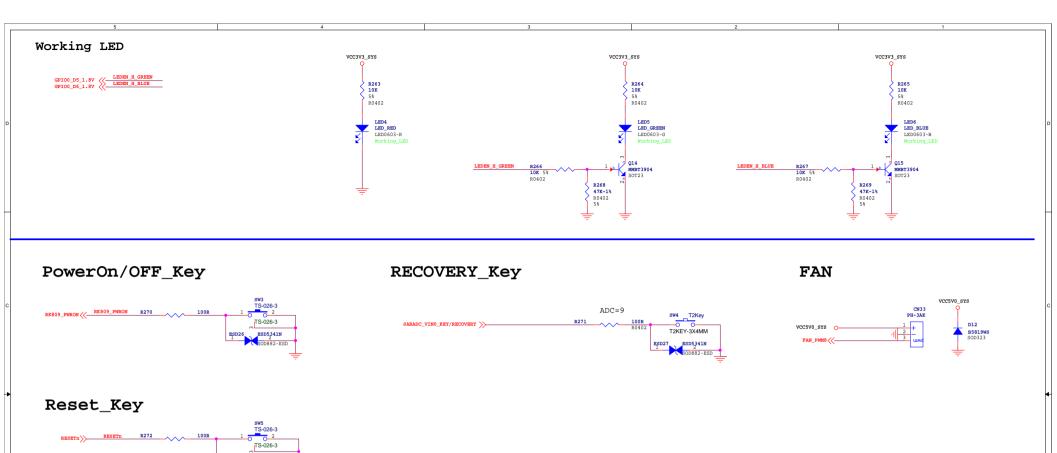
### M.2 KET-E CN13 NGFF2230-KEYE-42H M. 2 KEY E Socket (Platform Side HOST) USB2\_HOST2\_DP R214 M22R NGFF\_DP LED\_BLUE R219 W 4K7 OVCC-NGFF USB2\_HOST2\_DM R215 22R NGFF\_DM LED#1\_WiFi(I,OD) PCM\_CLK/I2S SCK(1.8V) C R216 NGFF\_SDCLK 9 SDMMC2\_CLK SDIO CLK(1.8V) PCM SYNC/I2S WS (1.8V) R224 \( \sqrt{22R NGFF\_SDCMD} 11 \) SDMMC2 CMD SDIO CMD(1.8V) PCM\_IN/I2S SD\_IN (I,1.8V) SDMMC2 DO SDIO DATAO(1.8V) PCM\_OUT/I2S SD\_OUT(0,1.8V) LED\_BLUE R439 WCC-NGFF R226 MA 22R NGFF\_SDD1 15 SDMMC2 D1 SDIO DATA1(1.8V) LED#2\_BT(I,OD) R228 W 22R NGFF\_SDD2 17 SDMMC2\_D2 SDTO DATA2(1.8V) CMD19 R449 /// 22R R217 W 22R NGFF\_SDD3 19 SDMMC2\_D3 SDIO DATA3(1.8V) UART WAKE HOST(I.3.3V SDIO WAKE HOST(I.1.8V) UART RX(I,1.8V) VCCIO6\_PHY1\_IO VCC3V3\_SYS WIFT RST NOTCH26 027 NOTCH27 NOTCH28 CJ2102 SOT-323 NOTCH29 NOTCH30 UART TX(0,1.8V √⟨BT UART CTS VCCIO6\_PHY1\_IO VCC3V3\_SYS C277 224 PCIE30\_TX1P PETp0 (O. Host) HART RTS(0.1.8V BT\_REG\_ON R434 AAA 4K7 C281 224 PCIE30\_TX1N PRTn0(0.Host) RESERVEDS HOST\_MAKE\_BT R435 VVCCIO6\_PHY1\_IO GND39 RESERVED40 CJ2102 R232 OR BT\_HOST\_WAKE R436 ANA 4K7 OVCCIO6\_PHY1\_IO SOT-323 PCIE30 RX1P PERp0(I,Host) RESERVED42 GPIO2\_C5 >>> UART8\_TX\_M0\_BT R234 OR 44 PCTE30 RX1N PERnO(I,Host) COEX3(1.8V) 45 CND45 COEX\_RXD(I,1.8V) VCCIO6 PHY1 IO VCC3V3 SYS R419 OVCC3V3\_SYS PCIE30X1\_REFCLKP\_CON >>-REFCLEP(Host) COEX TXD(0.1.8V) R235 OR R0402 RK809\_32KOUT\_WIFI R236 NC\OR R0402 RK809\_32KOUT\_WIFI PCIE30X1\_REFCLKN\_CON >>-REFCLKN(Host) SUSCLK (O. 32kHz. 3.3V 029 R237 22R PERSTO#(0,3.3V) PCIE30X1 PERSTn M1 CJ2102 SOT-323 PCIE30X1\_CLKREQn\_M1 >> R238 22R R437 10K VCC3V3\_SYS CLKREQ0(3.3V) W\_DISABLE\_BT#2(0,3.3V) PCIE30X1\_WAKEn\_M1 >> R239 22R R438 10K OVCC3V3\_SYS PEWake0(3.3V) W\_DISABLE-WiFi#1(0,3.3V) 57 I2C\_DATA\_NFC(1.8V) GND57 VCCIO6\_PHY1\_IO VCC3V3\_SYS X 59 2nd Lane PETpl I2C\_CLK\_NFC(0,1.8V) 2nd Lane PETnl I2C\_ALERT\_NFC(I,1.8V) 64 NGFF\_Moule\_ID1 R328 W OR SARADC\_VIN6 63 CJ2102 SOT-323 GND63 RESERVED6 66 X BT\_UART\_CTS ( × 65 PERSTI 2nd Lane PRRp1 × 67 2nd Lane PERn1 CLKRROT 69 PEWake1 PCIE20\_REFCLKP <<-----71 2nd Lane REFCLKpl 73 PCIE20\_REFCLKN </---2nd Lane REFCLKnl NGFF\_SDCLK R384 \_\_\_\_\_\_ 4K7 fixl CND75 fix2 R385 \_\_\_\_\_\_4K7 NGFF\_SDD0 R386 AAA 4K7 NGFF2230-KEYE-S1 NGFF\_SDD1 R387 W 4K7 NGFF\_SDD2 NGFF\_SDD3 R389 /// 4K7 WiFi\_WAKE VCC3V3\_SYS VCC-NGFF WPM3401-3/TR WiFi\_REG R392 4K7 R393 \_\_\_\_\_\_4K7 C279 C280 47uF/6.3V C0805 C0805 C314 10uF C0402 R231 10K SOT23 NC\10K **GUANGDONG BIPAI KEJI CPA.LTD** Q13 BPI-R2Pro\_RK3568 SOT23 Rev V1.1 18.M.2-KEYE Friday, April 08, 2022

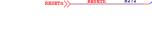












SARADC\_VIN1\_HW\_ID >>--SARADC\_VIN3\_BOM\_ID >>-----



### HW\_ID



SARADC_VIN1	Up Resistance	Down Resistance
HW_ID0	10K	DNP
HW_ID1	10K	110K
HW_ID2	20K	100K
HW_ID3	33K	100K
HW_ID4	18K	36K
HW_ID5	36K	51K
HW_ID6	51K	51K
HW_ID7	51K	36K
HW_ID8	36K	18K
HW_ID9	100K	33K
HW_ID10	100K	20K
HW_ID11	110K	10K
HW ID12	DNP	10K



### BOM\_ID

SARADC_VIN3	Up Resistance	Down Resistance
BOM_ID0	10K	DNP
BOM_ID1	10K	110K
BOM_ID2	20K	100K
BOM_ID3	33K	100K
BOM_ID4	18K	36K
BOM_ID5	36K	51K
BOM_ID6	51K	51K
BOM_ID7	51K	36K
BOM_ID8	36K	18K
BOM_ID9	100K	33K
BOM_ID10	100K	20K
BOM_ID11	110K	10K
BOM_ID12	DNP	10K

(BPI)	Desi Size A:

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